JPhys Energy

PURPOSE-LED PUBLISHING™

PAPER • OPEN ACCESS

Improved V_{oc} using Ce-alloyed ZnO buffer layers in thin film CdSeTe/CdTe solar cells

To cite this article: Luksa Kujovic *et al* 2026 *J. Phys. Energy* **8** 025017

Journal of Physics: Energy

PAPER

Improved V_{oc} using Ce-alloyed ZnO buffer layers in thin film CdSeTe/CdTe solar cells

Luksa Kujovic[1,*], Xiaolei Liu[1], Zhaoxia Zhou[1], Stuart Robertson[1], Ali Abbas[1], Mustafa Togay[1], Samuel E Machin[1], Jacques Kenyon[1], Zeyad Elsayed[1], Kieran M Curson[1], Ciaran Llewelyn[2], Dan A Lamb[2], Stuart J C Irvine[2], Wei Zhang[3], Chungho Lee[3], Timothy Nagle[3], Dingyuan Lu[3], Gang Xiong[3], Jake W Bowers[1] and John M Walls[1]

[1] Loughborough University, Loughborough LE11 3TU, United Kingdom
[2] Faculty of Science & Engineering, Swansea University, Swansea SA1 8EN, United Kingdom
[3] California Technology Center, First Solar, Inc., 1035 Walsh Ave, Santa Clara, CA 95050, United States of America
[*] Author to whom any correspondence should be addressed.

E-mail: l.kujovic@lboro.ac.uk

OPEN ACCESS

RECEIVED
24 February 2026

REVISED
28 May 2026

ACCEPTED FOR PUBLICATION
3 June 2026

PUBLISHED
29 June 2026

Keywords: CeO_2, ZnO, CeZnO, buffer layer, CdSeTe/CdTe solar cell, band alignment

Supplementary material for this article is available online

Abstract

Incorporating ZnO as a buffer layer in thin film CdSeTe/CdTe solar cells leads to high conversion efficiencies. However, the sub-optimal band alignment at the ZnO/CdSeTe interface limits the V_{oc}. In this study, Ce is used to alloy the ZnO buffer layer to widen the band gap and improve band alignment, leading to an increase in J_{sc} and V_{oc}. The 50 nm and 100 nm thick ZnO and CeZnO buffer layers are deposited on SnO_2:F coated soda-lime glass using radio frequency sputtering. To study the effect of Ce alloying, the Ce atomic percent is varied from 3% to 9%. The buffer layers are fabricated into As-doped CdSeTe/CdTe devices using First Solar's process. The device incorporating the 3% CeZnO buffer layer leads to the highest efficiency and V_{oc}. However, the saturation current density and ideality factor are observed to increase as the Ce content increases, suggesting that Ce alloying degrades the quality of the front p–n junction. The interface defect density is estimated using *C*–*V* and DLCP profiling, the interface defect density is observed to increase significantly when incorporating more than 3% Ce. There is an apparent trade-off between front interface passivation and band alignment.

1. Introduction

Cadmium telluride is a direct band gap material which fully absorbs light within a few microns, this is due to its absorption coefficient being greater than 10^4 cm^{-1} [1]. As a result, thin film CdTe solar cells benefit from requiring less semiconductor material than silicon-based solar cells. Furthermore, CdTe modules can be manufactured in under 3 h, making them a commercially successful technology, with the current worldwide installed capacity exceeding 30 GWp [2]. Thin film CdTe solar cells have a low temperature coefficient ($-0.21\%\,°C^{-1}$) [3], making them a suitable technology for warm climates. The embodied energy and carbon from manufacturing CdTe modules is 2–3 times lower than that of Si modules [4], this is largely due to CdTe modules requiring 98%–99% less semiconductor material and requiring less energy during manufacturing [5]. Thin film CdTe-based solar cells suffer from a relatively large open-circuit voltage (V_{oc}) deficit to the Shockley–Queisser (SQ) limit. Assuming an absorber band gap of 1.40 eV ($V_{oc,SQ}$: 1.138 V [6]) for the record CdSeTe/CdTe solar cell (V_{oc}: 0.905 V [7]), the V_{oc} deficit is 0.233 V. Recombination at the front n-type/p-type interface is one of the key factors limiting the V_{oc} [8], as a result, interface engineering is a critical research goal for the further development of thin film CdTe solar cells [9].

The front n-type buffer layer is placed between the transparent conducting oxide (TCO) and absorber, which together form the p–n junction. Buffer layers are a critical component which help

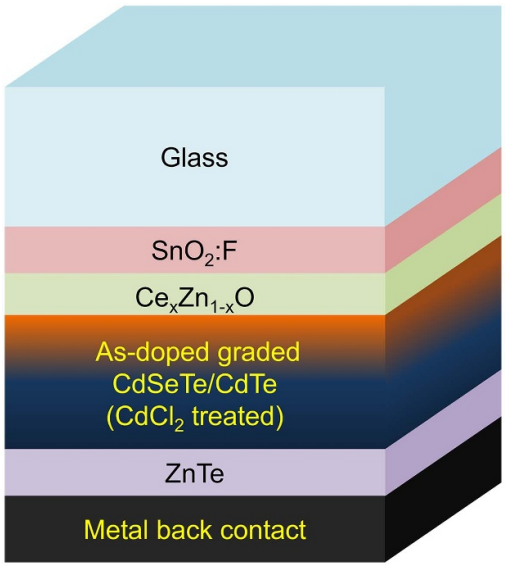


Figure 1. The device structure incorporating the $Ce_xZn_{1-x}O$ buffer layers (not to scale).

improve the performance of CdSeTe/CdTe solar cells by improving charge transport, reducing recombination and improving contact quality [10, 11]. Cerium oxide (CeO_2) is a wide band gap material with high thermal and chemical stability [12–14], making it a promising material for photovoltaic applications [15–17]. Researchers have alloyed ZnO with CeO_x to increase the conduction band minimum, facilitating the charge injection and transfer from a perovskite absorber to the electron transporting material [18]. This has led to an improvement in device performance, increasing the efficiency from 16% to 19.5% after incorporating CeO_x. Furthermore, reported environmental tests show that CeO_x alloying improves the moisture, ultraviolet, and thermal stability of perovskite solar cells [18]. The Ce alloying effect on the band gap has been studied, the band gap increased from 3.19 eV to 3.29 eV after alloying ZnO with Ce [19]. Photoluminescence (PL) and Raman measurements indicate that Ce alloying retains the high quality of the films and shows good PL behaviour [20]. The slight shift of the A_{1L} and E_{1L} peaks in the Raman spectra increased with Ce alloying, indicating that Ce alloying can change the free carrier concentration in ZnO nanorods [20]. However, the Ce alloying effect on the carrier concentration needs to be further investigated.

Previously, we co-sputtered CeZnO buffer layers using CeO_2 and ZnO targets, resulting in an increased buffer layer band gap, improved V_{oc} and short-circuit current density (J_{sc}) [21]. The improvement in J_{sc} was attributed to the band gap widening. The temperature dependent J–V measurements showed an increase in activation energy, suggesting that front interface recombination decreases with Ce alloying, resulting in an increase in V_{oc}. However, co-sputtering can lead to inconsistent film compositions due to voltage fluctuations at the highly resistive CeO_2 sputtering target.

In this work, we report on the use of $Ce_xZn_{1-x}O$ front buffer layers for thin film CdSeTe/CdTe solar cells, prepared using alloyed targets. The effect of varying the Ce content from 0 to 9 At% on device performance is studied.

Figure 1 shows the device structure which incorporates the $Ce_xZn_{1-x}O$ buffer layers, where x varies from 0 to 0.09.

Following device fabrication, the solar cells are characterized using current density–voltage (J–V), external quantum efficiency (EQE), capacitance–voltage (C–V), drive-level capacitance profiling (DLCP), cross-sectional scanning transmission electron microscopy (STEM) and energy dispersive x-ray spectroscopy (EDX). Thicker copies of the ZnO and $Ce_xZn_{1-x}O$ films are characterized using UV–Vis–NIR spectrophotometry and x-ray diffraction (XRD).

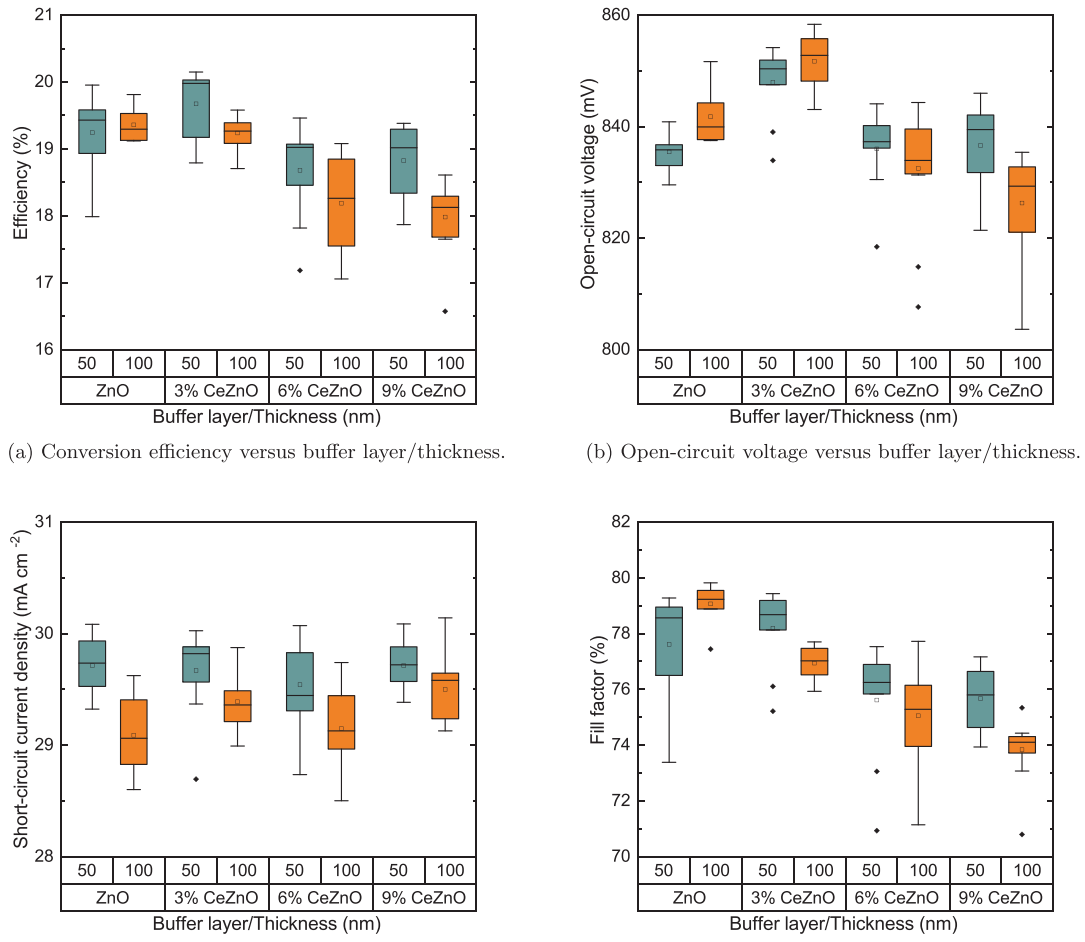
2. Results and discussion

2.1. Band gap tuning

The direct band gap values of the ~500 nm thick ZnO and $Ce_xZn_{1-x}O$ films were extrapolated using Tauc plots obtained from transmittance and reflectance data. The Tauc plots, transmittance, and

Table 1. Band gap of ZnO and $Ce_xZn_{1-x}O$ films.

Sample	Band gap (eV)
ZnO	3.26
$Ce_{0.03}Zn_{0.97}O$	3.30
$Ce_{0.06}Zn_{0.94}O$	3.33
$Ce_{0.09}Zn_{0.91}O$	3.35



(a) Conversion efficiency versus buffer layer/thickness.

(b) Open-circuit voltage versus buffer layer/thickness.

(c) Short-circuit current density versus buffer layer/thickness.

(d) Fill factor versus buffer layer/thickness.

Figure 2. Device performance for varying Ce content in 50 and 100 nm thick buffer layers. Each plot consists of 8 devices which have 12 cells each. The 8 devices were fabricated in the same batch.

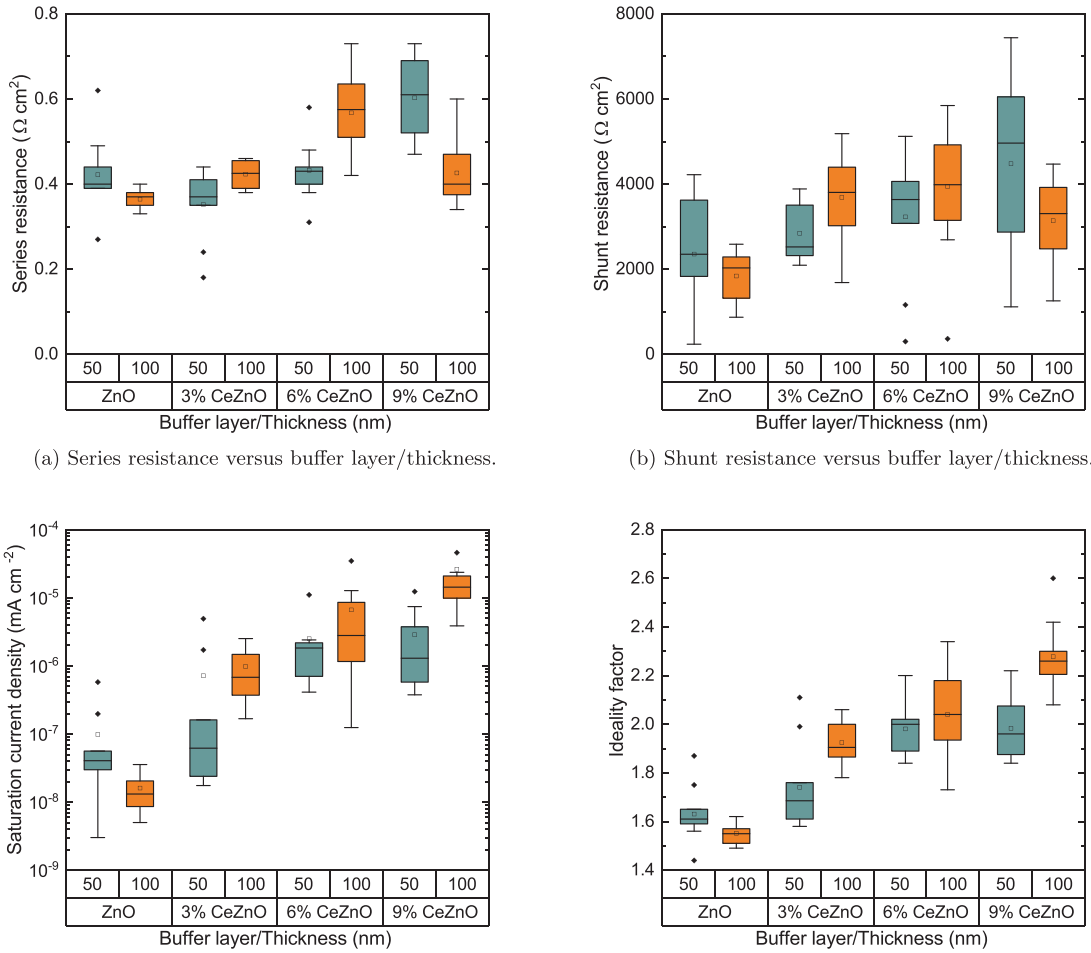
reflectance spectra are presented in Supplementary figure 1. The band gap values of the ZnO and $Ce_xZn_{1-x}O$ buffer layers are presented in table 1.

The band gap of ZnO can be tuned from 3.26 to 3.35 eV with Ce (9 At%) alloying. The ZnO band gap widening effect has previously been demonstrated with Ce alloying [19, 21].

2.2. Electrical measurements

The performance parameters from *J–V* measurements are presented for devices incorporating 50 and 100 nm thick ZnO and $Ce_xZn_{1-x}O$ buffer layers in figure 2. Note that the $Ce_xZn_{1-x}O$ samples are presented as 100(x)% CeZnO.

As shown in figure 2(a), the highest conversion efficiency is achieved using the 50 nm thick $Ce_{0.03}Zn_{0.97}O$ buffer layer. Increasing the Ce content beyond 3 At% leads to a decrease in efficiency. Furthermore, figure 2(b) shows that the mean and median V_{oc} is highest when incorporating the 50 and 100 nm thick $Ce_{0.03}Zn_{0.97}O$ buffer layers. This suggests that alloying with 3 At% Ce provides a more favorable band alignment with CdSeTe, consistent with reduced interface recombination. The 100 nm buffer gives slightly higher V_{oc}, but the 50 nm buffer provides the best overall device performance because it combines high V_{oc} with higher J_{sc} and fill factor, leading to the highest efficiency. This



(a) Series resistance versus buffer layer/thickness.

(b) Shunt resistance versus buffer layer/thickness.

(c) Saturation current density versus buffer layer/thickness.

(d) Ideality factor versus buffer layer/thickness.

Figure 3. Extracted parameters from *J–V* measurements for varying Ce content in 50 and 100 nm thick buffer layers. Each plot consists of 8 devices which have 12 cells each. The 8 devices were fabricated in the same batch.

reflects the classic buffer thickness trade-off between optical transparency and shunt prevention [22]. Similar to efficiency, the V_{oc} decreases when incorporating more than 3 At% Ce. Figure 2(c) shows that the J_{sc} is higher when using the thinner buffer layer, due to the reduction in parasitic absorption losses. The effect of the band gap widening is not clearly evident in the J_{sc} values, further indicating that the main benefit of the 3% CeZnO device is the improvement in V_{oc}. The fill factor is observed to decrease with Ce alloying.

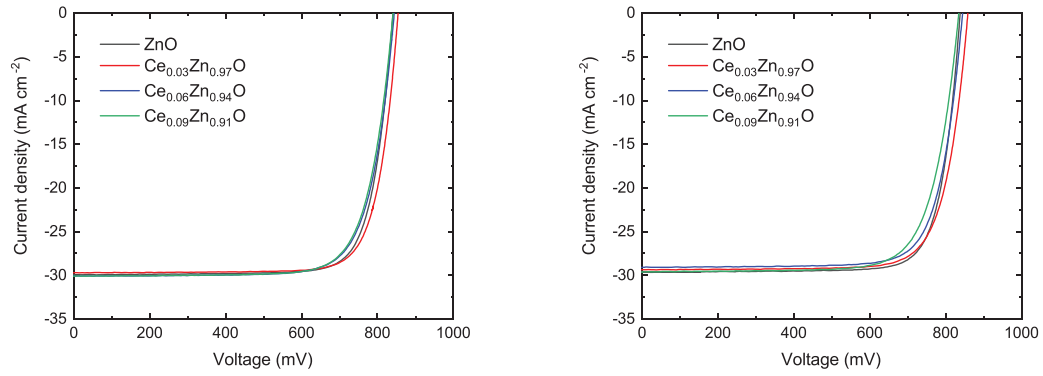
The extracted series resistance (R_s), shunt resistance (R_{sh}), saturation current density (J_0), and ideality factor (n) values are presented in figure 3.

The R_s shown in figure 3(a) does not vary significantly with Ce content or buffer layer thickness, suggesting that the buffer itself is not introducing major resistive voltage losses. In contrast, figure 3(b) shows that CeZnO-based devices generally exhibit higher R_{sh}. Furthermore, the 3% CeZnO 100 nm sample has a slightly higher R_{sh} than the 50 nm sample, which likely contributes to the marginally higher V_{oc} by suppressing leakage/recombination through shunt pathways. Figures 3(c) and (d) show a clearer dependence on Ce content, both J_0 and n increase with Ce, indicating stronger recombination at higher Ce concentrations. These trends suggest that the best performing 3% CeZnO device benefits from a balance between improved interface energetics and acceptable junction quality, whereas higher Ce concentrations degrade the junction through increased defect-assisted recombination.

The illuminated *J–V* curves of the highest efficiency cells are presented in figure 4. Figures 4(a) and (b) show the devices incorporating the 50 and 100 nm thick buffer layers, respectively.

When comparing the *J–V* curves, it is clear that the devices incorporating the $Ce_{0.03}Zn_{0.97}O$ buffer layer benefit from having a higher V_{oc}, this confirms the statistical trends in figure 2. The *J–V* parameters of the highest efficiency cells are summarized in table 2.

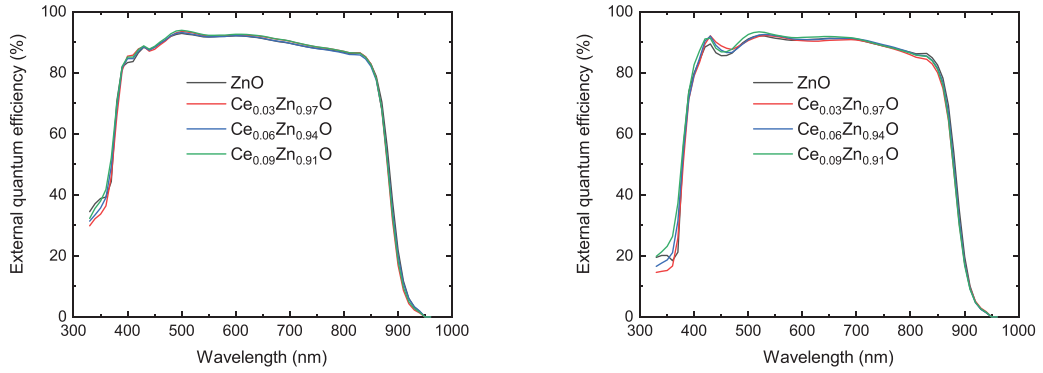
While individual champion cell changes in J_{sc} and V_{oc} are modest, the 50 nm 3% CeZnO device shows a clear improvement over the ZnO baseline (20.15% vs. 19.95% efficiency, 854.2 vs. 840.9 mV



(a) Current density-voltage curves of the cells incorporating the 50 nm thick buffer layers.

(b) Current density-voltage curves of the cells incorporating the 100 nm thick buffer layers.

Figure 4. Current density–voltage characteristics of the highest efficiency cells incorporating buffer layers with varying Ce content.



(a) External quantum efficiency of the devices incorporating the 50 nm thick buffer layers.

(b) External quantum efficiency of the devices incorporating the 100 nm thick buffer layers.

Figure 5. External quantum efficiency for devices incorporating buffer layers with varying Ce content.

V_{oc}). More importantly, the statistical box plots in figure 2 demonstrate that 3 At% Ce gives the highest median and mean V_{oc} across both thicknesses, with the 50 nm sample yielding the highest efficiency.

Figure 5 presents the EQE of the devices incorporating 50 nm (figure 5(a)) and 100 nm (figure 5(b)) thick buffer layers.

The EQE in the short wavelength region increases with Ce content. At 370 nm (buffer layer absorption region), the EQE increases (relative increase vs ZnO) by 3.6% (3 At% Ce), 11.0% (6 At% Ce), and 17.3% (9 At% Ce) for the 50 nm samples, and even more dramatically for the 100 nm samples (up to +75.5%). This is due to the buffer layer band gap increasing with Ce alloying, as seen in table 1.

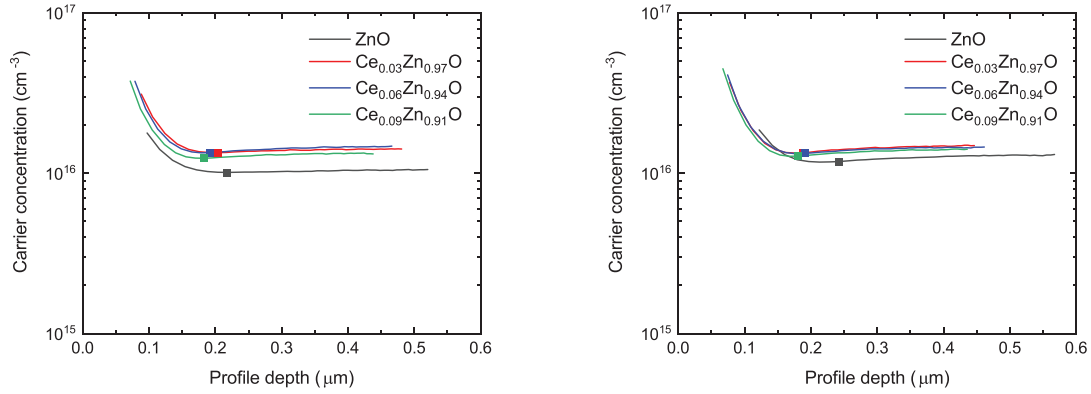
The carrier concentration obtained from *C–V* measurements is presented as a function of profile depth in figure 6.

The absorber carrier concentration is extracted at the zero-voltage bias point. Table 3 presents the absorber carrier concentration for cells incorporating 50 and 100 nm thick buffer layers with varying Ce content. The hole density is between 1.0×10^{16} and 1.4×10^{16} cm^{-3} for all buffer conditions, confirming that the observed device performance differences arise from front interface modifications rather than absorber doping variations.

The *C–V* profiles can be affected by the presence of deep defects or interface defects, whereas DLCP is insensitive to the response from the interface defects due to an improved signal-to-noise ratio. The interface defect density can be estimated by calculating the difference between the carrier concentrations obtained from *C–V* and DLCP measurements [23]. Figure 7 presents the interface defect density versus the buffer layer used in the device.

Table 2. The *J–V* characteristics and extracted parameters of the best performing cells.

Buffer layer	Thickness (nm)	Eff. (%)	V_{oc} (mV)	J_{sc} (mA cm^{-2})	FF (%)	R_s (Ω cm^2)	R_{sh} (Ω cm^2)	J_0 (mA cm^{-2})	n
ZnO	50	19.95	840.9	29.93	79.27	0.49	3799	1.54×10^{-8}	1.56
	100	19.81	837.8	29.62	79.82	0.38	2585	8.58×10^{-9}	1.51
$Ce_{0.03}Zn_{0.97}O$	50	20.15	854.2	29.70	79.43	0.41	3258	2.25×10^{-8}	1.61
	100	19.58	858.3	29.36	77.70	0.38	4271	3.52×10^{-7}	1.86
$Ce_{0.06}Zn_{0.94}O$	50	19.46	844.1	30.07	76.68	0.38	3114	1.21×10^{-6}	1.96
	100	19.08	844.3	29.07	77.72	0.55	2690	1.25×10^{-7}	1.73
$Ce_{0.09}Zn_{0.91}O$	50	19.38	841.0	30.09	76.59	0.47	6094	1.21×10^{-6}	1.95
	100	18.61	834.4	29.60	75.34	0.48	2984	3.87×10^{-6}	2.08



(a) Devices incorporating the 50 nm thick buffer layers. (b) Devices incorporating the 100 nm thick buffer layers.

Figure 6. Carrier concentration versus profile depth, the squares indicate the zero-voltage bias point.

Table 3. Absorber carrier concentration for cells incorporating buffer layers with varying Ce content.

Buffer layer	Thickness (nm)	Absorber carrier concentration (cm^{-3})
ZnO	50	1.01×10^{16}
	100	1.18×10^{16}
$Ce_{0.03}Zn_{0.97}O$	50	1.35×10^{16}
	100	1.34×10^{16}
$Ce_{0.06}Zn_{0.94}O$	50	1.34×10^{16}
	100	1.33×10^{16}
$Ce_{0.09}Zn_{0.91}O$	50	1.24×10^{16}
	100	1.28×10^{16}

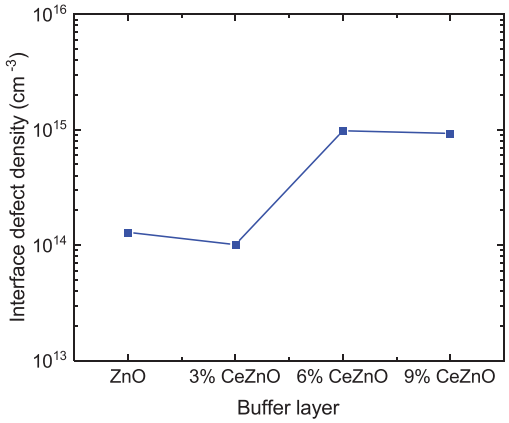


Figure 7. Interface defect density for varying Ce content in the 50 nm thick buffer layer.

The interface defect density is the lowest for the 3% CeZnO buffer and increases significantly at ⩾6% Ce. This trend correlates with the V_{oc} results (figure 2(b)), where 3% Ce gives the highest median/mean values and higher Ce contents show degradation. The increased defect density at higher Ce enhances interface recombination.

2.3. Materials Characterization

The cross-sectional STEM images of the FTO/ZnO/CdSeTe and FTO/$Ce_xZn_{1-x}O$/CdSeTe interfaces are presented in figure 8.

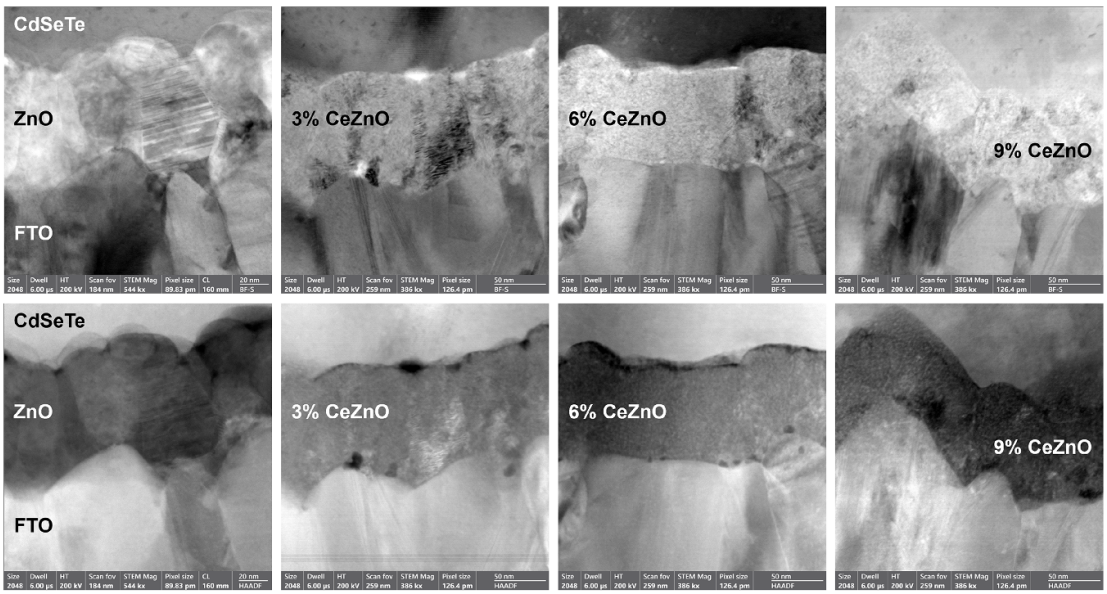
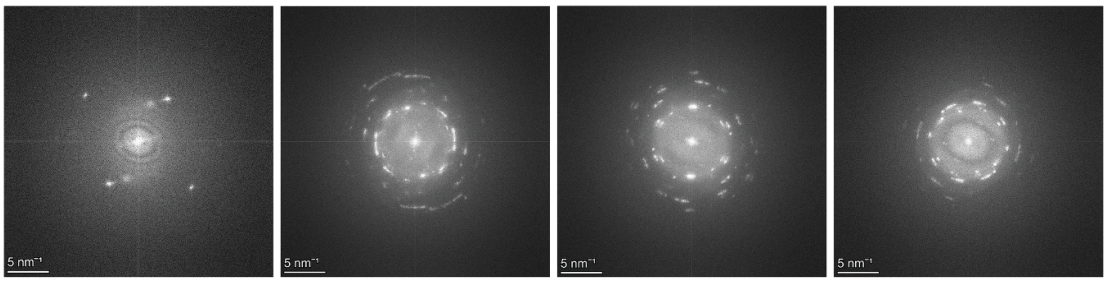


Figure 8. Cross-sectional STEM images (top: BF, bottom: HAADF) of the FTO/ZnO/CdSeTe and FTO/$Ce_xZn_{1-x}O$/CdSeTe interfaces, note that the buffer layers are 80–100 nm thick.



(a) ZnO. (b) 3% CeZnO. (c) 6% CeZnO. (d) 9% CeZnO.

Figure 9. FFT images of the ZnO and CeZnO buffer layers presented in figure 8.

The ZnO film appears to be more crystalline than the CeZnO films after device processing. Also, some small voids are observed at the front interface when using the 3% CeZnO and 6% CeZnO layers. The fast Fourier transform (FFT) patterns of the buffer layers from figure 8 are presented in figure 9.

The ZnO buffer is made up of columnar grains that are ∼45 nm wide. The FFT pattern in figure 9(a) is obtained from the middle of a grain and it shows that the ZnO grain is fully crystallized. However, each grain in the CeZnO layers is composed of randomly oriented nano-crystallites of ∼3-10 nm, the corresponding FFT patterns in figures 9(b)–(d) support this observation. Furthermore, the ∼500 nm thick ZnO and CeZnO films on Eagle glass were analyzed using XRD, the XRD peaks show that the CeZnO films are less crystalline than the ZnO film (Supplementary figure 2 and Supplementary table 1). As shown in Supplementary table 1, the dominant (002) peak position shifts to lower 2θ values with Ce alloying, indicating lattice expansion. This is expected as Ce ions are larger than Zn ions [24]. The lattice mismatch from the larger Ce ions creates local distortions, defects, and disorder. Using the full width at half maximum (FWHM) and Scherrer equation, the crystallite size in the ∼500 nm thick ZnO, 3%, 6%, 9% CeZnO was calculated to be 34.13, 5.50, 6.73 and 6.66 nm, respectively (Supplementary table 1). The XRD analysis corroborates the observations made in figures 8 and 9. The increase in defects beyond 3% Ce (figure 7) correlates with CeZnO structural degradation, as shown by the nanocrystalline disorder (STEM/FFT) and lattice strain from larger Ce ions (XRD). This creates a more defective ZnO/CdSeTe interface.

The cross-sectional STEM images and corresponding EDX elemental maps of the front interface are presented in figure 10.

The ZnO and $Ce_xZn_{1-x}O$ layers uniformly cover the FTO substrate. The Ce maps show that the Ce signal intensity increases as the Ce content is increased from 0 to 9 At%. Typically, Cl decorates the front

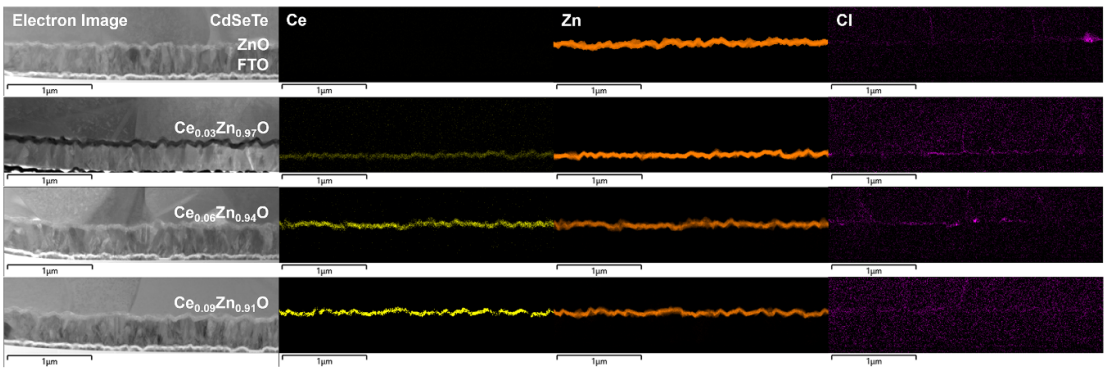


Figure 10. Cross-sectional STEM images and EDX elemental maps showing the front interface of the devices incorporating the 50 nm thick ZnO and $Ce_xZn_{1-x}O$ buffer layers. Background/peak overlap subtraction was not applied to the Cl maps.

interface of CdTe devices [25, 26]. During the $CdCl_2$ heat treatment, Cl diffuses down grain boundaries and accumulates at the front interface, where it participates in passivation [27]. Unusually, Cl was not observed at the front interface of CdSeTe/CdTe devices incorporating ZnO buffer layers deposited at room temperature [28] or 100 °C [29]. However, depositing ZnO at higher temperatures (500 °C) results in Cl segregation at the front interface, suggesting that the quality of the p–n junction is sensitive to the ZnO deposition conditions [29]. The ZnO deposited at 100 °C led to the best performing devices. Figure 10 shows signs of Cl accumulation at the front interface of the ZnO- and CeZnO-based devices. However, it is not as pronounced as in the case of MgZnO- or SnO_2-based devices [25, 30].

3. Conclusions

Cerium alloying has been used to widen the ZnO band gap to 3.35 eV, leading to a reduction in parasitic absorption. Based on conversion efficiency and V_{oc}, the devices incorporating the $Ce_{0.03}Zn_{0.97}O$ buffer layer performed the best, with the highest efficiency being 20.2% (without an anti-reflection coating). Increasing the Ce content beyond 3 At% led to a significant reduction in device performance. The extracted J_0 and n values increase with Ce content, indicating that the p–n junction quality deteriorates after Ce alloying. The estimated interface defect density is also seen to increase with Ce content. In previous work, we have attributed the lack of Cl at the front interface to the high quality of the ZnO/CdSeTe interface. The results in this work show that the ZnO/CdSeTe and CeZnO/CdSeTe interfaces are decorated with Cl. Although the CeZnO/CdSeTe interface has a higher density of defects, the Cl segregation is not observed to increase with Ce alloying. This may be due to the ZnO films being more crystalline than the CeZnO films (as observed with STEM and XRD analysis). These results suggest that Cl segregation at the front interface is dependent on both the crystallinity of the buffer layer and the defect density. Ce alloying increases the interface defect density and is also believed to improve the band alignment between the buffer layer and the absorber. Direct conduction band offset measurements will be needed to quantify this effect. The interface could be further optimized by balancing the defect density and band alignment to achieve a higher efficiency. Overall, the 3% CeZnO buffer layers outperformed intrinsic ZnO for the first time. This discovery opens up new pathways in reducing the V_{oc} deficit and improving the conversion efficiency of thin film CdSeTe/CdTe solar cells. In the future, alloying with lower Ce concentrations (0-5 At%) will be investigated. Future work will also investigate CeZnO deposition at higher temperatures (100 °C–500 °C) as previous ZnO studies have found the optimal deposition temperature to be 100 °C.

4. Methods

4.1. Materials and device synthesis

The glass substrate used for characterizing 500 nm ZnO and CeZnO films was 1.1 mm Corning® Eagle XG® glass supplied by Abrisa Technologies. For device fabrication, commercially available FTO-coated

soda-lime glass substrates (2.65 mm thick) from NSG-Pilkington were used. Prior to cleaning, surface particles were removed from the 5×5 cm substrates using compressed air. The substrates were then wiped with precision wipes soaked in 99.5+% pure isopropanol (IPA) to remove visible contaminants, followed by a second compressed air treatment. Cleaning proceeded with three successive 15 min ultrasonic bath cycles at 40 °C. The first cycle used a detergent solution with deionized (DI) water, while the second and third cycles used >95% pure acetone and 99.5+% pure IPA, respectively. Between cycles, the substrates were rinsed thoroughly with DI water. After the final cleaning step, the glass substrates were stored in a glass beaker containing IPA [31].

The ZnO and CeZnO films were deposited via radio frequency (RF) magnetron sputtering using an AJA International system. RF sputtering was used because the buffer layers are wide band gap semiconductors for which DC sputtering is ineffective due to charge accumulation at the target [31, 32]. RF sputtering overcomes this issue by using an alternating electric field periodically reversing the charge build-up [31, 33] and enabling uniform ion bombardment and material ejection from insulating targets. This results in a stable plasma and high-quality film. When comparing ZnO films prepared by DC and RF sputtering, the RF sputter-deposited films had better quality [31, 34]. Although it is possible to use pulsed-DC for the films in this work, RF sputtering was used as it typically leads to higher quality films [31, 35]. The 4-inch diameter ZnO (99.99% purity), $Ce_{0.03}Zn_{0.97}O$, $Ce_{0.06}Zn_{0.94}O$ and $Ce_{0.09}Zn_{0.91}O$ (99.9% purity) targets were supplied by Plasmaterials, Inc. After loading into the sputtering chamber, the substrate surfaces were subjected to a 5 min plasma treatment for cleaning and activation. The plasma was generated at 100 W at 22 °C, with a working gas pressure of 5 mTorr using a gas mixture of 20% oxygen and 80% argon. Following plasma treatment, ZnO or CeZnO films were deposited at a power density of 1.85 W cm^{-2} and a substrate temperature of 22 °C. The substrates were rotated at 10 rpm and positioned 18.4 cm from the target. The deposition was carried out at a working gas pressure of 1 mTorr with a gas composition of 1% oxygen and 99% argon. Oxygen was introduced during the sputtering process to prevent suboxide formation common in oxide target sputtering. Prior to each deposition, the chamber base pressure was between 2.0×10^{-4} and 4.0×10^{-4} mTorr. Film thicknesses of 50 nm and 100 nm were used for device fabrication, while 500 nm films were prepared for film characterization. These film thicknesses were based on the calculated deposition rate of each target, which was obtained by measuring the thickness of previously deposited films using profilometry.

The CdSeTe/CdTe absorber layer was deposited onto the buffer layers via vapor-transport deposition, yielding an approximate thickness of 3–4 μm [36]. Arsenic was incorporated as a dopant in the absorber. Following deposition, the samples underwent activation through heat treatment in a $CdCl_2$-vapor environment at a temperature between 400 °C–500 °C [36]. The device structure was completed with the deposition of a ZnTe layer and a metal back-contact [37]. Individual cells were then defined by laser scribing, resulting in an active area of 0.445 cm^2 [31].

4.2. Characterization

Profilometry was used to measure the thickness of the sputtered materials, so that the deposition rate could be calculated. The Ambios XP2 stylus profilometer (Ambios Technology, Inc.) was used in this work [31]. To reliably measure the thickness of the samples, after the deposition, polyimide tape was stuck diagonally across the 5×5 cm surface. Hydrochloric acid was used with a cotton swab to etch the sputtered material [31]. After etching, the surface was rinsed using DI water, dried using filtered compressed air, and the tape was removed to reveal a sharp step which could be measured using the profilometer [31].

Transmittance and reflectance spectra were measured using a Varian Cary 5000 UV–Vis–NIR spectrophotometer. The measured transmittance (T_{meas}) and reflectance (R_{meas}) data were used to construct Tauc plots, from which the direct band gap of the $d = 500$ nm thick ZnO and CeZnO films was determined. This was determined by calculation of the absorption coefficient, using the approximation $\alpha \approx -\ln[T_{meas}/(1-R_{meas}^2)]/d$ (such that $R_{meas}^2 exp(-2\alpha d) \ll 1$) [38, 39]. The band gap was then obtained using a $(\alpha h\nu)^\gamma$ vs $h\nu$ Tauc plot for a direct band gap material ($\gamma = 2$), where the linear extrapolation of the absorption edge yields the band gap value at the intercept of the $h\nu$ axis [38, 40].

A Bruker D2 Phaser x-ray diffractometer was used to obtain XRD patterns to analyse the structural properties of the 500 nm thick films. The diffractometer was fitted with a one-dimensional LynxEye detector and a 0.5 mm thick Ni filter to suppress Kβ radiation. Cu Kα radiation (Kα = 1.54184 Å) was run at 30 kV and 10 mA. Diffraction patterns were measured in the 2θ range of 10−80°, with a step size of 0.02°. Sample rotation was set at 15 rpm, with a 1 mm beam slit and a 3 mm anti-scatter plate height [31].

The illuminated J–V characteristics were measured at room temperature under 1 Sun (AM 1.5G) conditions using a class ABB Oriel Sol1A solar simulator [28]. The resulting J–V curves were fitted to the single-diode model using the Lambert W function implemented in MATLAB, enabling extraction of R_s, R_{sh}, J_0 and n [41]. EQE measurements were calibrated using a silicon reference cell with a known, NIST-traceable spectral response. Carrier concentration profiles shown in figure 6 were obtained from C–V measurements performed with an Agilent E4980A LCR meter at a frequency of 40 kHz [37].

Capacitance measurements, including both C–V and DLCP, used to estimate interface defect densities were carried out with a Keysight E4990 impedance analyzer, also at 40 kHz. Depth profiles were obtained from DLCP and C–V measurements conducted in the dark, with carrier concentrations extracted at 0 V bias [31].

For structural analysis, STEM samples were prepared using a standard *in situ* lift-out method [42] with an FEI dual-beam FIB system. Imaging was performed on an FEI Tecnai F20 S/TEM equipped with Gatan bright- and dark-field detectors, a Fischione high-angle annular dark field detector, and an Oxford Instruments X-Max 80 mm^2 windowless EDX spectrometer. Measurements were conducted at an accelerating voltage of 200 kV, with a camera length of 100 mm and a condenser aperture of 70 μm [28].

4.3. Statistical analysis

The box plots presented in figures 2 and 3 show the 25th ($Q1$) and 75th ($Q3$) percentiles, with the interquartile range defined as $IQR = Q3 - Q1$. The minimum and maximum values were taken as $Q1 - 1.5IQR$ and $Q3 + 1.5IQR$, respectively, with data points outside this range classified as outliers. Both mean and median values were included in the plots. Each box represents a sample size of 12 solar cells. Statistical analysis and visualization were carried out using Origin 2020 (OriginLab) [31].

Acknowledgments

The authors acknowledge the use of facilities within the Loughborough Materials Characterisation Centre (LMCC) and First Solar's California Technology Center (CTC). The Loughborough authors are grateful to UKRI and EPSRC for funding the Project through EP/W00092X/1. The Swansea authors were funded through EP/W000555/1. LK is grateful to the EPSRC Supergen SuperSolar Network+ for funding a 3-month secondment to First Solar Inc.

Data availability statement

The data cannot be made publicly available upon publication because they are not available in a format that is sufficiently accessible or reusable by other researchers. The data that support the findings of this study are available upon reasonable request from the authors.

Supplementary Material available at https://doi.org/10.1088/2515-7655/ae7760/data1.

Conflict of interest

W.Z., C.L., T.N., D.L., and G.X. work at First Solar Inc. a publicly traded company which produces CdTe solar panels and develops PV power plants. Apart from this and the funding mentioned in the acknowledgments section, the authors have no other conflict of interest to declare.

Author contributions

Luksa Kujovic 0009-0009-3980-1933
Conceptualization (lead), Data curation (equal), Formal analysis (lead), Investigation (lead), Methodology (equal), Project administration (lead), Validation (lead), Visualization (lead), Writing – original draft (lead)

Xiaolei Liu
Conceptualization (equal), Formal analysis (supporting), Investigation (supporting), Methodology (supporting), Project administration (supporting), Writing – review & editing (equal)

Zhaoxia Zhou
Data curation (equal), Methodology (equal), Writing – review & editing (equal)

Stuart Robertson
Data curation (equal), Methodology (equal), Writing – review & editing (equal)

Ali Abbas
Data curation (equal), Methodology (equal), Writing – review & editing (equal)

Mustafa Togay 0000-0001-5840-2158
Data curation (equal), Formal analysis (equal), Investigation (supporting), Methodology (equal), Writing – review & editing (equal)

Samuel E Machin
Data curation (equal), Writing – review & editing (equal)

Jacques Kenyon
Formal analysis (equal), Software (lead), Writing – review & editing (equal)

Zeyad Elsayed 0000-0002-2797-3043
Data curation (equal), Writing – review & editing (equal)

Kieran M Curson
Writing – review & editing (equal)

Ciaran Llewelyn
Writing – review & editing (equal)

Dan A Lamb 0000-0002-4762-4641
Writing – review & editing (equal)

Stuart J C Irvine
Writing – review & editing (equal)

Wei Zhang
Data curation (equal), Methodology (equal), Resources (equal), Writing – review & editing (equal)

Chungho Lee
Data curation (equal), Methodology (equal), Resources (equal), Writing – review & editing (equal)

Timothy Nagle
Data curation (equal), Methodology (equal), Resources (equal), Writing – review & editing (equal)

Dingyuan Lu
Resources (equal), Writing – review & editing (equal)

Gang Xiong 0000-0002-4601-0277
Resources (equal), Writing – review & editing (equal)

Jake W Bowers 0000-0001-7632-1140
Supervision (supporting), Writing – review & editing (equal)

John M Walls
Conceptualization (equal), Funding acquisition (lead), Project administration (equal), Resources (equal), Supervision (lead), Writing – review & editing (equal)

References

[1] Mathew X and Sebastian P 1999 *Sol. Energy Mater. Sol. Cells* **59** 85–98
[2] Scarpulla M A *et al* 2023 *Sol. Energy Mater. Sol. Cells* **255** 112289
[3] Virtuani A, Pavanello D and Friesen G 2010 *25th European Photovoltaic Solar Energy Conf. and Exhibition/5th World Conf. on Photovoltaic Energy Conversion* vol 3 (EU-PVSEC Valencia) p 83
[4] Wikoff H M, Reese S B and Reese M O 2022 *Joule* **6** 1710–25
[5] Irvine S J C and Rowlands-Jones R L 2016 *IET Renew. Power Gener.* **10** 428–33
[6] Kato Y and Fujiwara H 2021 *Appendix B: Numerical Values of Shockley-Queisser Limit* (Wiley) pp 563–5
[7] NLR, Best research-cell efficiency chart, (available at: www.nlr.gov/pv/cell-efficiency)
[8] Katakumbura N, Phillips A B, Kaluarachchi P N, Abudulimu A, Bastola E, Heben M J and Ellingson R J 2026 *Adv. Theory Simul.* **9** 1e01703
[9] Sartor B E, *et al* 2026 *Joule* **10** 1

[10] Kephart J M, McCamy J W, Ma Z, Ganjoo A, Alamgir F M and Sampath W S 2016 *Sol. Energy Mater. Sol. Cells* **157** 266–75
[11] Song T, Kanevce A and Sites J R 2016 *J. Appl. Phys.* **119** 233104
[12] Wang X *et al* 2017 *J. Mater. Chem.* A **5** 1706–12
[13] Mansilla C 2009 *Solid State Sci.* **11** 1456–64
[14] Luo L, Wu X D, Dye R C, Muenchausen R E, Foltyn S R, Coulter Y, Maggiore C J and Inoue T 1991 *Appl. Phys. Lett.* **59** 2043–5
[15] Corma A, Atienzar P, Garcia H and Chane-Ching J-Y 2004 *Nat. Mater.* **3** 394–7
[16] Jose R, Thavasi V and Ramakrishna S 2009 *J. Am. Ceram. Soc.* **92** 289–301
[17] Tan Z *et al* 2014 *Adv. Mater. Interfaces* **1** 1400197
[18] Meng R, Feng X, Yang Y, Lv X, Cao J and Tang Y 2019 *ACS Appl. Mater. Interfaces* **11** 13273–8
[19] Luo Q, Wang L S, Guo H Z, Lin K Q, Chen Y, Yue G H and Peng D L 2012 *Appl. Phys. A* **108** 239–5
[20] Lang J *et al* 2010 *J. Appl. Phys.* **107** 074302
[21] Kujovic L *et al* 2024 *2024 IEEE 52nd Photovoltaic Specialist Conf.* (Seattle) (IEEE) pp 1068–70
[22] Cantas A, Turkoglu F, Meriç E, Akça F G, Ozdemir M, Tarhan E, Ozyuzer L and Aygun G 2018 *J. Phys. D: Appl. Phys.* **51** 275501
[23] Yin L, Cheng G, Feng Y, Li Z, Yang C and Xiao X 2015 *RSC Adv.* **5** 40369–74
[24] Shannon R D 1976 *Acta Cryst* **32** 751–67
[25] Munshi A H, Kephart J M, Abbas A, Danielson A, Gélinas G, Beaudry J-N, Barth K L, Walls J M and Sampath W S 2018 *Sol. Energy Mater. Sol. Cells* **186** 259–65
[26] Hatton P, Watts M J, Abbas A, Walls J M, Smith R and Goddard P 2021 *Nat. Commun.* **12** 4938
[27] Abbas A *et al* 2013 *IEEE J. Photovolt.* **3** 1361–66
[28] Kujovic L *et al* 2023 *Adv. Funct. Mater.* **34** 2312528
[29] Kujovic L, *et al* 2025 *Adv. Mater. Technol.* **10** 2401364
[30] Infante-Ortega L C *et al* 2024 *2024 IEEE 52nd Photovoltaic Specialist Conf. (PVSC)* (*Seattle*) pp 1387–9 (IEEE)
[31] Kujovic L 2025 *PhD Thesis*, Loughborough University (https://doi.org/10.26174/thesis.lboro.30724235)
[32] Bishop C A 2011 Magnetron sputtering source design and operation *Vacuum Deposition Onto Webs, Films and Foils* 2nd edn, ed C A Bishop (William Andrew Publishing) pp 337–62
[33] Mattox D M 2010 Physical Sputtering and Sputter Deposition (Sputtering) *Handbook of Physical Vapor Deposition (PVD) Processing,* 2nd edn , ed D M Mattox (William Andrew Publishing) pp 237–86
[34] Gao W and Li Z 2004 *Ceram. Int.* **30** 1155–9
[35] Tseng X-L, Chen H-F, Chen Y-S, Chiu S-C, Lo H-H, Fuh Y-K and Li T T 2025 *J. Vac. Sci. Technol. A* **43** 023406
[36] Mallick R *et al* 2023 *IEEE J. Photovolt.* **13** 510–5
[37] Metzger W K *et al* 2019 *Nat. Energy* **4** 837–45
[38] Jubu P R, Obaseki O S, Nathan-Abutu A, Yam F K, Yusof Y and Ochang M B 2022 *Results Opt.* **9** 100273
[39] Look D C and Leach J H 2016 *J. Vac. Sci. Technol. B Nanotechnol. Microelectron.* **34** 04J105
[40] Makuła P, Pacia M and Macyk W 2018 *J. Phys. Chem. Lett.* **9** 6814–7
[41] Zhang C, Zhang J, Hao Y, Lin Z and Zhu C 2011 *J. Appl. Phys.* **110** 064504
[42] Abbas A 2014 *Ph.D. Thesis* (Loughborough University) (available at: https://repository.lboro.ac.uk/articles/thesis/The_microstructure_of_thin_film_cadmium_telluride_photovoltaic_materials/9524558)