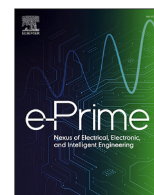
e-Prime - Nexus of Electrical, Electronic, and Intelligent Engineering 17 (2026) 201163

Contents lists available at ScienceDirect

e-Prime - Nexus of Electrical, Electronic, and Intelligent Engineering

journal homepage: www.sciencedirect.com/journal/e-prime-nexus-of-electrical-electronic-and-intelligent-engineering



SiC MOSFET reliability: Review of degradation mechanisms, failures, and enhancement strategies

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A R T I C L E I N F O

Keywords:
Degradation
Failure
Gate oxide
Power MOSFETS
Reliability
Ruggedness
Silicon carbide (SiC)
Wide bandgap

A B S T R A C T

This paper presents a comprehensive review of reliability challenges and degradation mechanisms of silicon carbide (SiC) power MOSFETs, with the objective of clarifying failure phySiCs, test methodologies, and mitigation strategies relevant to high performance power electronic applications. SiC MOSFETs offer superior material properties, including a wide bandgap (3.26 eV), high breakdown electric field (3 MV/cm), and high thermal conductivity (4.9 W/cm·K), enabling operation at high voltage, frequency, and temperature across electric vehicles, renewable energy, aerospace, and industrial systems. However, the rapid adoption of SiC technology has outpaced the development of mature reliability frameworks, leaving critical gaps in understanding long-term degradation under extreme electrical, thermal, and mechanical stresses. This review addresses key reliability concerns, including gate oxide degradation, short-circuit ruggedness, avalanche robustness, thermo-mechanical failure under power cycling, and body diode reliability. Each section explores both fundamental mechanisms and mitigation strategies. Additionally, experimental results from short circuit testing, Unclamped Inductive Switching (UIS) characterization, and body diode evaluation are presented to illustrate practical proofs of some reliability issues. It further incorporates reliability tests reported in standards and the automotive industry, while outlining diagnostic indicators at the device, package, and system levels, emphasizing their sensitivity and applicability. In addition, it examines emerging trends including AI-driven reliability prediction, advanced packaging, novel oxide technologies, and next generation device structures, offering a forward-looking roadmap for improving SiC MOSFET reliability.

1. Introduction

Silicon carbide (SiC) power MOSFETs have emerged as promising candidates for next generation power electronics due to their superior material properties and performance advantages over traditional silicon (Si) devices. 4H-SiC, as the most widely used polytype of silicon carbide for today's commercial power semiconductor devices, exhibits a wide bandgap of approximately 3.26 eV, which enables higher breakdown electric fields (up to 3 MV/cm) and allows the fabrication of devices with much higher blocking voltages, often exceeding 1.2 kV and scalable up to 15 kV [1,2]. In addition, it exhibits significantly higher thermal conductivity (∼4.9 W/cm·K) compared to silicon (∼1.5 W/cm·K), as well as a higher saturation electron velocity (∼2.0×10^7 cm/s vs. ∼1.0×10^7 cm/s in Si). The primary limitation lies in its lower electron mobility (0.95 vs. 1.4×10^3 cm^2/V·s), which can restrict channel conduction. Nevertheless, the superior material properties result in a higher low on-state loss index (2.7 vs. 1.6), [3,4]. The comparison has been highlighted in Fig. 1.

These advantages make SiC MOSFETs particularly well-suited for high efficiency, high frequency, and high power density applications such as electric vehicle (EV) powertrains, renewable energy converters, aerospace systems, and harsh industrial environments. Their ability to operate at elevated junction temperatures, often at up to 175 °C, without

"This research is supported by Swansea University (SUIPRES scholarship) and Vishay Intertechnology, awarded to Ahmed Abdelaleem."
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https://doi.org/10.1016/j.eprime.2026.201163

Available online 4 April 2026
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Nomeclture

V_{gs}	Gate Drive Voltage
$R_{ds(on)}$	Drain-Source on-Resistance
R_g	Gate Resistance
V_{th}	Threshold Voltage
R_{ch}	Channel Resistance
d_{ox}	Oxide Thickness
L	Channel Length
ε_{ox}	Permittivity
μ_{ch}	Channel Mobility
$R_{on,sp}$	Specific on-Resistance
W	Channel Width
V_g	Gate Voltage
D_{it}	Interface Traps Density
E_{ox}	Electric Field
E_a	Activation Energy
β	Typical Weibull Slope
V_{ds}	Drain-Source Voltage
E_{AS}	Avalanche Energy
Q_{rr}	Reverse Recovery Charge
V_F	Forward Voltage Drop
$R_{th,j-c}$	Thermal Resistance from Junction to Case
T_j	Junction Temperature
V_{BR}	Breakdown Voltage
$T_{j,max}$	Maximum Junction Temperature
V_F	Forward Voltage Drop
I_{gss}	Gate Leakage Current
C_{oss}	Output capacitance
g_m	Transconductance
I_{dss}	Drain Leakage Current
V_{sd}	Body Diode Forward Voltage

Acronyms

AGD	Active Gate Drive
ALD	Atomic Layer Deposition
BD	Body Diode
BTI	Bias Temperature Instability
BJT	Bipolar Junction Transistor
CTE	Coefficient of Thermal Expansion
DGS	Dynamic Gate Stress
DMOS	Double-Diffused MOSFET
DRB	Dynamic reverse bias
DSC	Double-Sided Cooled
EMI	Electromagnetic Interference
EV	Electric Vehicle
PCBs	Printed Circuit Boards
FLR	Field Limiting Ring
F-N	Fowler-Nordheim
H^3TRB	High Humidity High Temperature Reverse Bias
HV-H^3TRB	High Voltage High Humidity High Temperature Reverse Bias
HTGB	High Temperature Gate Bias
HTRB	High Temperature Reverse Bias
HTS	High Temperature Storage
IMC	Intermetallic Compound
JBS	Junction Barrier Schottky
JTE	Junction Termination Extension
LSTM	Long Short-Term Memory
LTS	Low Temperature Storage
MIS	Metal Insulator Semiconductor
ML	Machine Learning
NBTI	Negative BTI
PBTI	Positive BTI
PC	Power Cycling
RNNs	Recurrent Neural Networks
RUL	Remaining Useful Life
SAM	Scanning Acoustic Microscopy
SBD	Schottky Barrier Diode
SC	Short Circuit
SCWT	Short Circuit Withstand Time
SEM	Scanning Electron Microscopy
Si	Silicon
SiC	Silicon Carbide
SJ	Superjunction
SSC	Single-Sided Cooled
SVM	Support Vector Machines
TAT	Trap-Assisted Tunnelling
TC	Thermal Cycling
TST	Thermal Shock Test
TDDB	Time-Dependent Dielectric Breakdown
UIS	Unclamped Inductive Switching
WBG	Wide Bandgap

significant leakage current degradation or thermal runaway further expands their usability in automotive, and military grade systems [5,6].

The majority functions of SiC power MOSFETs are in converters [7, 8]. The survey summarised in Fig. 2 demonstrates the major failures in these power electronic systems. As shown in Fig. 2(a), thermal stresses (steady-state and cyclic temperature variations) account for 55% of failures. Vibration and mechanical shock contribute to 20%, followed by humidity and moisture effects at 19%, while contaminants and dust cause about 6% of failures [9]. Fig. 2(b) illustrates how these stresses translate into failures among converter components. Capacitors are responsible for 30% of failures. printed circuit boards (PCBs) follow closely with 26%. Power devices, which include MOSFETs and IGBTs, contribute to 21% of failures, reflecting the impact of high electrical and thermal stress. Solder joints represent another critical weak point with 15%, as they are prone to cracking under thermal and mechanical cycling. Connectors and other minor components contribute 3% and 7%, respectively [9]. These findings emphasize that managing thermal, mechanical, and environmental stresses is essential for improving the long-term reliability of converters, while power devices remain a crucial focus due to their direct impact on system efficiency and performance [10,11].

Reliability, commonly defined as the ability of a device or system to perform its intended function over a specified period under given conditions, is typically described using failure-rate metrics [12]. For power semiconductor devices, the time dependent evolution of failure rate follows a characteristic trend known as the bathtub curve, as illustrated in Fig. 3. This curve can be divided into three distinct phases: Early Failures (infant mortality), Random Failures (useful life), and Wear-out Failures [13]. While this framework is general, its interpretation is important for SiC MOSFETs due to their operation under higher electric fields, higher junction temperatures, and more aggressive thermal cycling compared to Si devices.

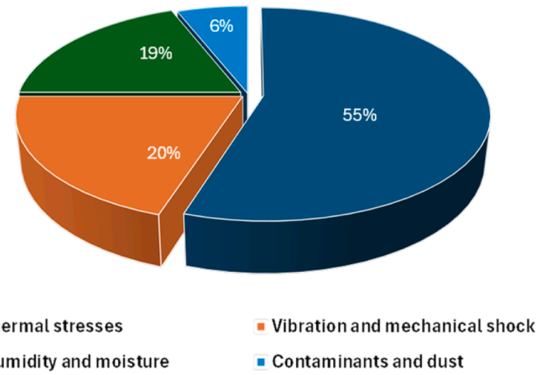
In the early failure phase, a relatively high failure rate is observed due to latent manufacturing and process defects, resulting in premature failure of a small fraction of devices. As these units are eliminated, the failure rate stabilizes during the useful-life phase, where devices operate with near constant reliability and wear-out mechanisms remain inactive [14]. Over extended operation, long-term aging and degradation processes lead to a sharp increase in failure rate, marking the wear-out phase. The duration of the useful-life phase defines the practical

lifetime of the device, which manufacturers aim to fully encompass within the rated service conditions.

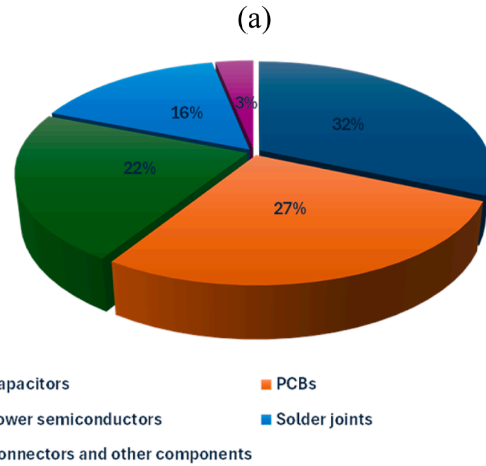
Despite their benefits, SiC MOSFETs are still a relatively recent technological development. Their exposure to combined electrical, thermal, and mechanical stresses under extreme operating conditions raises significant concerns about long-term reliability. Typical stress factors include high dv/dt and di/dt rates, repetitive avalanche events, and high temperature biasing, all of which may accelerate degradation in gate oxide integrity, threshold voltage stability, and package reliability [15,16]. Unlike silicon devices, where decades of field experience support robust design practices, SiC adoption has outpaced the development of comparable reliability frameworks [17,18]. Compounding this challenge, many qualification procedures such as High Temperature Reverse Bias (HTRB), High Temperature Gate Bias (HTGB), and power cycling are directly inherited from Si technology, yet may not adequately reflect the unique degradation behaviours of WBG materials [19]. For instance, recent studies show that SiC MOSFETs experience distinctive reliability threats, such as gate oxide degradation due to high electric fields [20], threshold voltage drift [21], and body diode wear-out under surge and reverse conduction stress [22].

Failure modes in SiC MOSFETs can be broadly classified into chip-level (intrinsic) and package-level (extrinSiC, including interconnects and packaging) mechanisms. At the chip level, Fig. 4, the most critical degradation typically arises in the gate oxide and the body diode, the latter often affected by stacking faults during reverse conduction. At the package level, Fig. 5, reliability issues mainly originate from bond wires and solder layers, which are prone to thermo-mechanical fatigue. A typical package consists of the semiconductor die, bond wires, substrate, baseplate, and heat sink. Here, the solder layers provide mechanical and thermal connections between the chip, substrate, and baseplate, but the solder film between the ceramic substrate and the baseplate is particularly vulnerable to cracking and delamination under thermal cycling stress.

This review provides a concise evaluation of key reliability challenges in SiC power MOSFETs, focusing on dominant failure mechanisms, degradation under electrical and thermal stress, and recent advances in ruggedness and design. It draws on current experimental data and industry trends to highlight factors affecting long-term performance. The paper is structured as follows: Section 2 explores gate oxide reliability issues, including threshold voltage instability and time



(a)



(b)

Fig. 2. *Survey of stress factors and failure contributors in power electronic converters: (a) sources of stress, and (b) component level failures.*

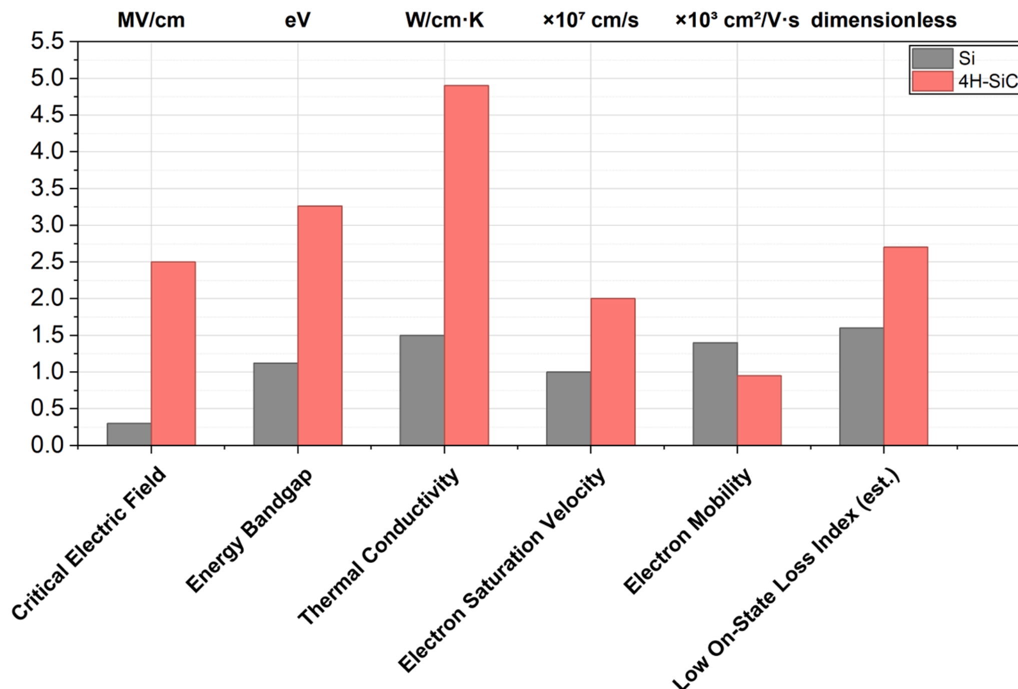


Fig. 1. *Key characteristics of 4H-SiC versus Si.*

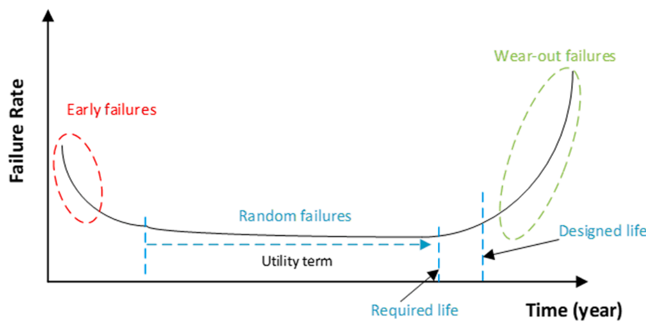


Fig. 3. *Failure rate progression of semiconductor devices across their lifetime (bathtub curve).*

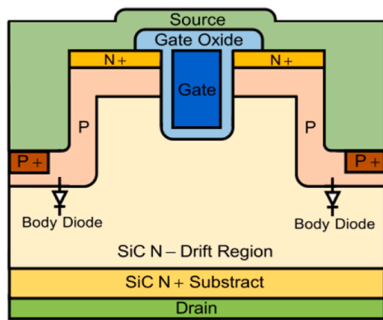


Fig. 4. *Chip-level architecture of SiC MOSFET (trench structure)* [23].

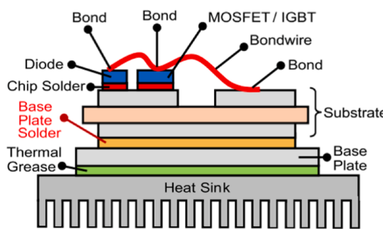


Fig. 5. *General package-level architecture of SiC MOSFET* [23].

dependent dielectric breakdown. Section 3 addresses SC ruggedness, clarifying failure phenomena during fault conditions and highlights results for short circuit withstand time (SCWT), while Section 4 focuses on avalanche ruggedness and degradation mechanisms, particularly under repetitive or unclamped switching transients including experimental demonstrations. Section 5 reviews reliability under power cycling stress, emphasising the impact of thermo-mechanical fatigue on packaging and interconnects. Section 6 discusses the reliability of the body diode and its susceptibility to degradation and surge current stress, while considering some experimental results. Section 7 integrates reliability tests and related standards, highlighting their methodologies and applicability. Section 8 summarizes the diagnostic indicators associated with each failure site, comparing their sensitivity and linearity as reliability metrics. Section 9 outlines solutions and future trends, including novel oxide technologies, advanced packaging, AI-assisted prediction, and new device architectures. Section 10 concludes with key insights and future research directions. Fig. 6 illustrates the structural organisation of the review.

2. GATE oxide degradation and reliability

2.1. Gate oxide structure

Although both Si and SiC MOSFETs employ similar planar and trench gate structures, the key differences between the two technologies arise from the material properties of SiC, particularly at the SiC/SiO_2 interface, rather than structural design. In Si devices, the Si/SiO_2 interface is mature and well-optimized, whereas in SiC, the same oxide growth process introduces carbon-related defects, such as carbon clusters and C–O complexes, which significantly degrade the oxide quality. These defects lead to higher interface trap densities, charge trapping, and threshold voltage instability. Furthermore, the band alignment between

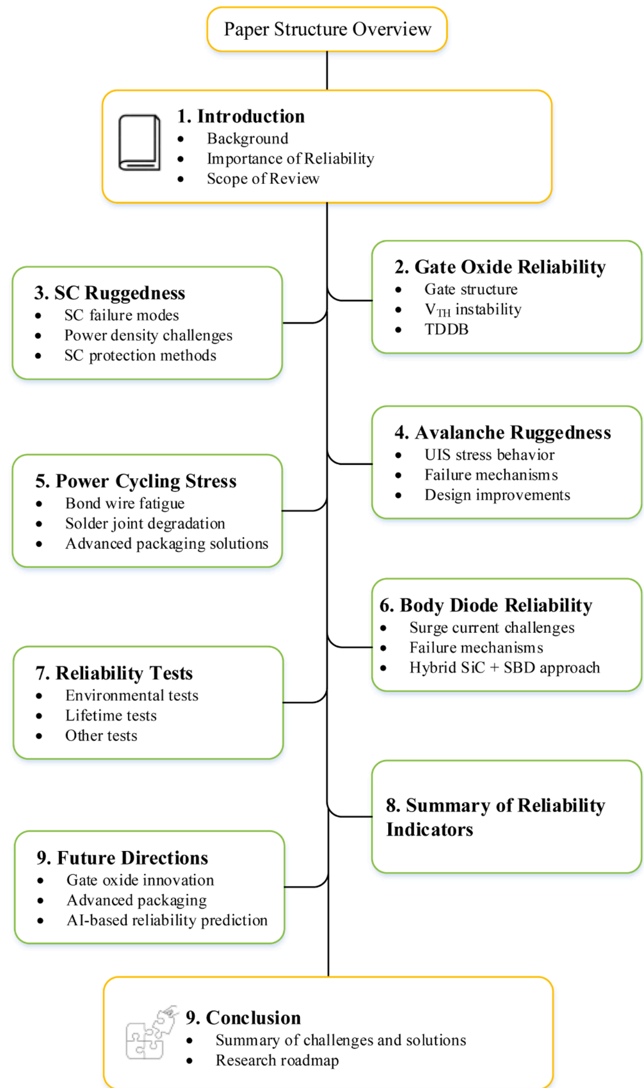


Fig. 6. *Structural overview of the paper illustrates the main content of each section.*

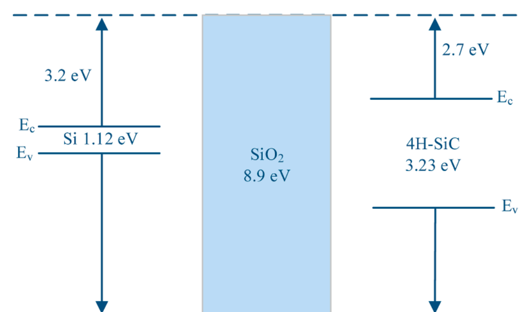


Fig. 7. *Energy band offsets for Si/SiO_2 and 4H-SiC/SiO_2 interfaces* (**E_c** *is conduction band edge,* **E_v** *is valance band edge)* [24].

SiC and SiO_2 differs from that in Si MOSFETs as shown in Fig. 7. Specifically, SiC has a lower conduction and valence band offset with respect to SiO_2, which reduces the energy barrier for carrier injection and increases the likelihood of tunnelling and gate leakage [24]. SiC MOSFETs may use either planar (DMOS) or trench architectures, as shown in Fig. 8 [25]. The planar design forms the channel through diffused regions at the device surface, while trench devices etch vertical gate channels into the SiC substrate to better manage electric fields and reduce on-resistance. These design choices in SiC are aimed at improving performance under high voltage and high temperature conditions [26,27]. Table I summarizes the key differences between them. Each design represents a step forward in improving channel mobility, reducing on-resistance, and enhancing reliability. While planar MOSFETs are simple and widely used, they suffer from poor interface quality and higher conduction losses. Double trench devices address these limitations by forming channels along trench sidewalls and shielding the gate oxide, though non-uniform channel properties remain a concern. The asymmetric trench structure further optimizes device performance by aligning the channel to the most favourable crystal orientation, achieving the lowest on-resistance, improved switching behaviour, and robust oxide reliability. However, the SiC/SiO_2 interface remains a critical reliability challenge due to the defect mechanisms [28]. To compensate, SiC MOSFETs require a higher gate drive voltage ($V_{gs} \approx$ 15–20 V) compared to Si MOSFETs ($V_{gs} \approx$ 10–15 V) to achieve low on-resistance ($R_{ds(on)}$). Additionally, the internal gate resistance (R_g) in SiC MOSFETs is inherently higher due to smaller chip sizes for equivalent ratings, necessitating lower external gate resistances (≈0–5 Ω) for fast switching, though this must be balanced against surge protection [29]. The Miller effect is more pronounced in SiC MOSFETs due to their faster dv/dt, demanding robust gate drivers. Furthermore, the body diode in SiC MOSFETs while fast, has a high reverse recovery charge (Q_{rr}) and forward voltage, leading to increased switching losses. This often necessitates the use of an external SiC Schottky diode in parallel [30]. Table II summarises the key differences between the gate structures of Si and SiC MOSFETs for clearer understanding.

2.2. Threshold voltage instability

Threshold voltage, V_{th}, represents a critical reliability challenge in SiC power MOSFETs, directly influencing device controllability, switching accuracy, and long-term system reliability. In contrast to their silicon counterparts, SiC MOSFETs exhibit more noticeable and complex V_{th} shifts, primarily due to extensive charge trapping at the SiC/SiO_2 interface and within the gate oxide layer. These instabilities can result in significant deviations from expected gate drive performance, compromising efficiency, control accuracy, and fault tolerance [31,32].

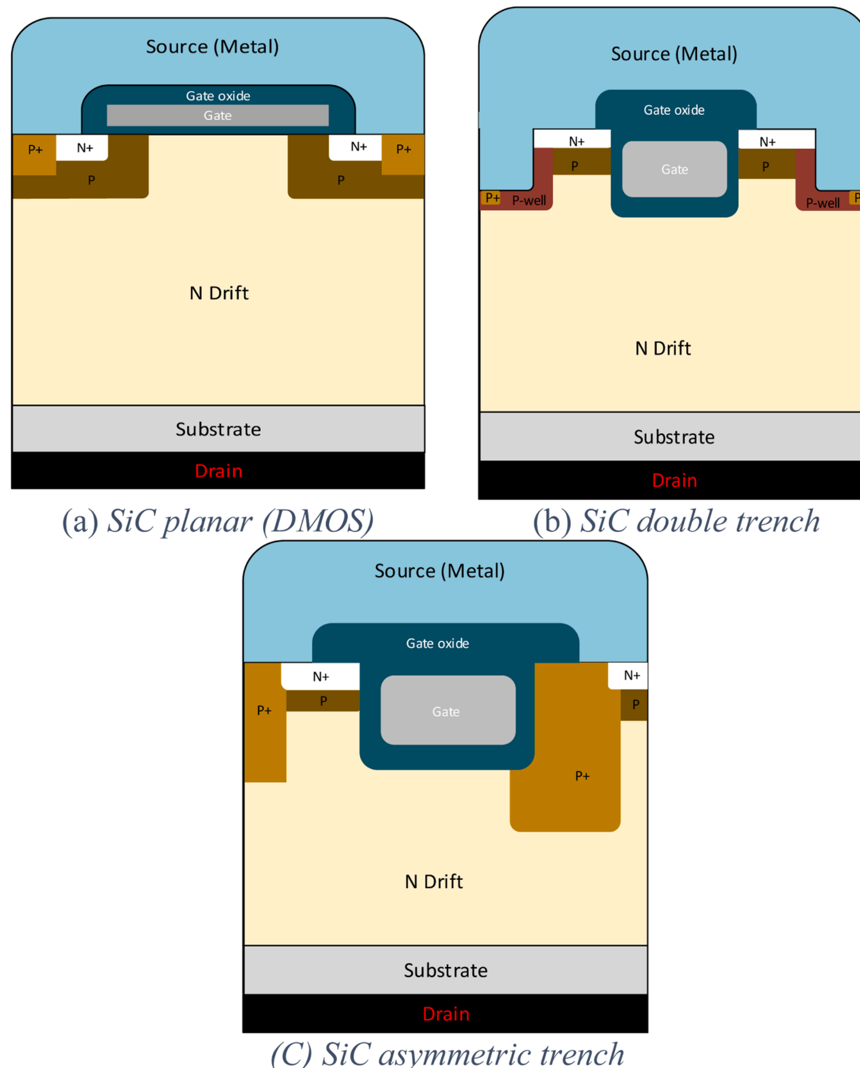


Fig. 8. *Schematic of the structure of SiC power MOSFET.*

Table I
Comparison of SiC MOSFET Gate Structures.

Feature	Planar Gate (DMOS)	Double Trench	Asymmetric Trench
Channel Orientation	Lateral, surface channel	Vertical trench sidewalls (different planes)	Channel aligned to a-plane <11−0> (optimal orientation)
Channel Mobility	Low (poor SiC/SiO_2 interface, high trap density)	Higher than planar (but varies by sidewall orientation)	Highest, due to optimal orientation and reduced trap density
$\mathbf{R_{DS(on)}}$	High (limited scalability)	Reduced vs. planar (wider effective channel)	Lowest, ≈ 50% of planar
Interface Trap Density	High	Moderate, but varies across sidewalls	Lowest (best interface quality)
Cell Pitch / Scalability	Limited scalability	Larger pitch due to second trench (reduces channel density)	Compact design, high channel density
Gate Oxide Reliability	Stressed at higher fields, some shielding from parasitic JFET	Deep p-well shields oxide, reducing field stress	Deep p-well shields oxide, reducing field stress
Body Diode	Present but not optimized, higher conduction loss	Second trench adds significant body diode conduction area	P-wells act as body diode emitters, well-optimized
Drive Voltage	Requires higher V_{GS} for full conduction	Moderate, device dependent	Standard +15 V drive, easy gate control
Switching Performance	Moderate, higher Q_{GD}	Improved, but sidewall differences complicate behavior	Excellent, low Q_{GD}/Q_{GS} ratio, controlled switching, low dynamic losses
Maturity of Technology	Most mature (commercially widespread, simpler process)	Mature but more complex fabrication	Latest commercial trend (e.g., Infineon CoolSiC™)
Advantages	Simple, established, robust	Lower $R_{DS(on)}$, oxide shielding, proven structure	Best trade-off: low $R_{DS(on)}$, high mobility, good switching & reliability
Disadvantages	High $R_{DS(on)}$, poor mobility, limited scaling	Uneven sidewall properties, larger pitch	More complex design, orientation-sensitive fabrication

2.2.1. *Mechanisms of V_{th} instability*

- *Interface Traps Effects*

The 4H-SiC/SiO_2 interface typically exhibits a high density of interface traps D_{it}, higher than $10^{12}cm^{-2}.eV^{-1}$, primarily due to the presence of residual carbon and bond imperfections introduced during oxidation [33]. While the structural nature of these defects is introduced in the previous section, their dynamic behaviour under high electric fields becomes especially critical here. These traps interact with carriers during device operation, especially under high electric fields which is leading to charge capture and emission dynamics that cause transient and long-term variations in V_{th}.

- *Bulk Oxide Charge Trapping*

Charge trapping also occurs within the bulk of the gate oxide, particularly in the presence of near-interfacial oxide traps such as oxygen vacancies and hydrogen related defects. These bulk traps contribute to gradual V_{th} drift during prolonged electrical stress, especially in devices with ultra-thin gate oxides (<50 nm) and high gate electric fields (>5 MV/cm) [34]. This drift typically exhibits logarithmic time dependence, with activation energy ≈ 0.1–0.3 eV and worsens at elevated temperatures [35].

Table II
Key Differences Between Si and SiC MOSFET Gate Structures.

Aspect	Si MOSFETs	SiC MOSFETs
Gate Oxide Interface Quality	Excellent (Si/SiO_2 interface is nearly ideal)	Poorer (SiC/SiO_2 has high interface trap density)
Electric Field in Gate Region	Lower (Si has lower critical field ~0.3 MV/cm)	Much higher (SiC critical field ~2.5–6 MV/cm) Requires design mitigation
Gate Drive Voltage	±10–15 V	Often +15–20 V (on) / –5 V (off)
Gate Oxide Thickness	Can be thin (~10–30 nm)	Typically, thicker (e.g., 40–80 nm), although recent devices use thinner oxides with passivation techniques to mitigate breakdown.
Trench Structures	Used to reduce cell pitch and on-resistance	Used but require careful field-plate and JFET region design to avoid field crowding
Gate Resistance (R_g)	Lower internal R_g	Higher internal R_g due to small die size and higher sheet resistance
Planar Structure	Mature, highly optimised DMOS with hexagonal, square or stripe cellular arrangements	Similar DMOS structure, but with shorter channels due to poor channel field effect mobility
Interface Degradation Over Time	Minimal	Significant; reliability concern (bias temperature instability, threshold voltage drift)

2.2.2. *Impact on circuit behaviour*

- *Gate Drive Maloperation*

Threshold voltage shifts during regular operation (in-situ) can lead to significant gate drive misbehaviour. Positive V_{th} shifts, often caused by electron trapping under continuous gate bias, increase the channel resistance, thereby raising $R_{DS(on)}$ and contributing to higher conduction losses. Conversely, negative V_{th} shifts may reduce turn-off robustness and increase off-state leakage current, potentially leading to thermal runaway or degraded efficiency in power converters [36,37].

- *Timing Errors*

In high frequency switching applications (e.g., EV traction inverters), delayed turn on/off due to V_{th} hysteresis can cause shoot-through currents [38].

2.2.3. *Bias temperature instability (BTI) effects*

BTI originates from charge trapping and detrapping processes within the gate oxide and at the SiO_2/SiC interface, leading to parametric drift, hysteresis, and potential degradation of switching margins. It represents a progressive and often partially reversible degradation mechanism, making its interpretation strongly dependent on stress conditions, and recovery behaviour. In SiC MOSFETs, both positive and negative gate bias conditions contribute to BTI through distinct physiCal mechanisms.

- *Positive BTI (PBTI)*

Under positive gate bias (ON-state condition), electrons tunnel into oxide traps, increasing V_{th}. This effect worsens at high temperatures (>150 °C) [39].

- *Negative BTI (NBTI)*

Negative gate stress (OFF-state condition) leads to hole trapping, reducing V_{th} and increasing leakage. NBTI is less severe in SiC than Si but remains a concern during prolonged OFF-state biasing at elevated temperatures [40].

Studies also show partial V_{th} recovery upon removal of stress bias, indicating reversible trap dynamics, which must be considered when interpreting stress test results [41].

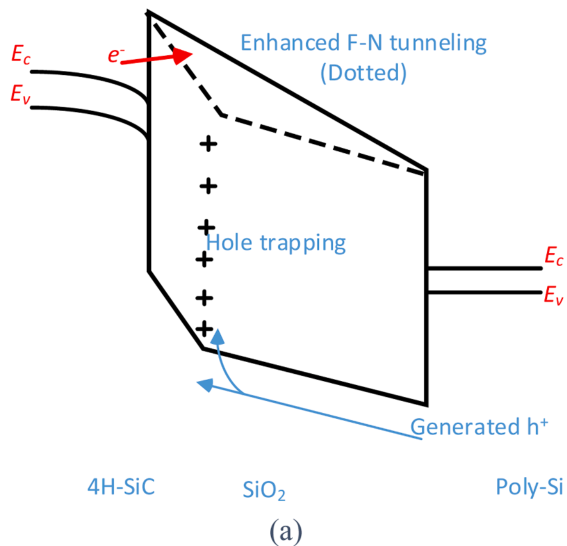
Table III compares the effect of PBTI and NBTI on the change value of

Table III
Bias Temperature Effect on V_{th} Shifts.

Stress Condition	Mechanism
PBTI $V_{gs} > 0$	Electron trapping in oxide
NBTI $V_{gs} < 0$	Hole trapping at interface

the V_{th}.

Fig. 9 illustrates the energy band diagrams depicting the two primary trapping phenomena: (a) hole trapping and (b) electron trapping. Under NBTI, generated holes (h^+) from impact ionisation or gate injection accumulate near the Poly-Si/SiO_2 interface, leading to a negative ΔV_{th} due to positive charge screening of the gate field. Conversely, during PBTI, electrons tunnel into oxide traps via Fowler-Nordheim (F-N) tunnelling from the Poly-Si gate, becoming trapped near the SiO_2/4H-SiC interface (Fig. 9b), which increases V_{th}. The figure highlights how these processes alter the local electric field, modulating the effective barrier width for F-N tunnelling: Hole trapping alters the local electric field, effectively modulating the barrier shape and enhancing carrier injection under certain conditions, while electron trapping partially restores it. These dynamics, exacerbated by temperature, contribute to hysteresis and long-term V_{th} drift, critically impacting SiC MOSFET reliability in high-temperature applications [42].



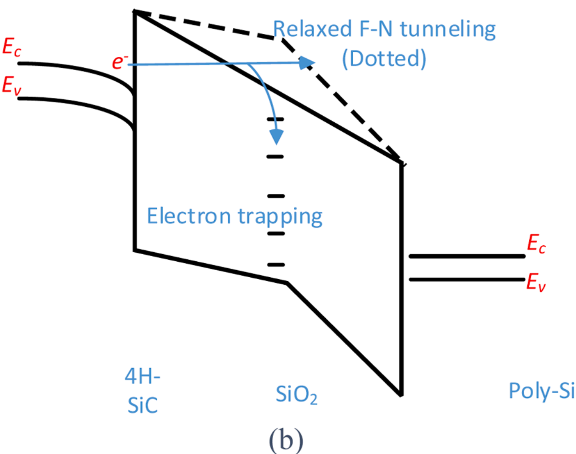


Fig. 9. Energy band diagrams illustrating how (a) hole trapping and (b) electron trapping influence the tunnelling barrier widths and Fowler–Nordheim (F–N) tunnelling currents at the charge injection interface.

2.3. Mitigation strategies

The inherent vulnerability of SiC/SiO_2 interfaces to defects has driven the development of targeted mitigation approaches, with recent advancements focusing on three key areas:

2.3.1. Thermal nitridation of gate oxide

Post-oxidation annealing in NO or N_2O environments introduces nitrogen at the SiC/SiO_2 interface, passivating carbon related traps and significantly reducing D_{it} [43].

2.3.2. Gate stack engineering

An effective approach is gate stack engineering using alternative high-k dielectric materials. Fig. 10 illustrates the simulated variation in V_{th} for 4H-SiC Metal Insulator Semiconductor (MIS) structures as a function of dielectric thickness across several dielectric materials, including SiO_2, Y_2O_3, AlN, Al_2O_3, and HfO_2. Among these, SiO_2 exhibits the highest threshold voltages, with V_{th} exceeding 7 V at 50 nm thickness. In contrast, high-k dielectrics such as HfO_2 and Al_2O_3 demonstrate significantly lower V_{th} values for the same thickness range, indicating improved gate control and reduced effective oxide field stress. The use of these materials can help suppress charge trapping and interface state density, both of which are critical contributors to V_{th} drift under prolonged operation. These findings support the ongoing research into high-k dielectrics as promising candidates for enhancing long-term reliability and stability in SiC power devices [44]. However, despite their benefits, high-k dielectrics face challenges such as poor interface quality with SiC, increased trap densities, thermal instability, and long-term reliability concerns, limiting their full replacement of SiO_2 in commercial devices.

2.3.3. Dynamic gate voltage control

Advanced gate driver techniques, such as adaptive V_{gs} regulation or active feedback can compensate for V_{th} shifts in real time, improving system stability and reliability under varying thermal and electrical stress [45].

2.3.4. Channel mobility engineering

In addition to gate oxide and voltage control techniques, improving channel mobility through interface defect reduction has emerged as a crucial strategy for enhancing SiC MOSFET reliability. As described by [46], channel resistance R_{ch} is inversely proportional to the channel mobility μ_{ch}, and can be expressed as:

$$R_{ch} = \frac{d_{ox}L}{\varepsilon_{ox}\mu_{ch}W(V_g - V_{th})} \quad (1)$$

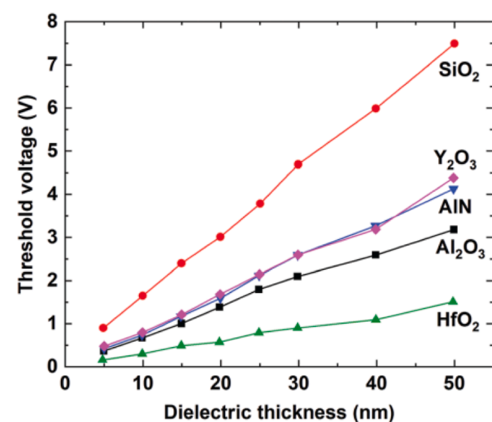


Fig. 10. *Modelled dependence of threshold voltage on dielectric thickness in 4H-SiC MIS structures using various dielectric materials* [44].

where $d_{ox}, L, \varepsilon_{ox}, W, V_g, V_{th}$ are the oxide thickness, channel length, permittivity, width, gate voltage, and threshold voltage respectively. The study highlighted several reliability benefits associated with increasing μ_{ch} as shown in Fig. 11.

- Lower Specific On-Resistance: Higher channel mobility reduces the specific on-resistance $R_{on,sp}$, which allows for smaller chip areas for the same current rating. This improves cost efficiency and thermal management.
- Thicker Gate Oxides Allowed: With higher μ_{ch}, a thicker gate oxide can be used without degrading on-state conduction. This lowers the electric field in the oxide, thus reducing gate oxide stress, charge trapping, and threshold voltage instability.
- Improved Short-Channel Behaviour: Higher mobility also permits longer channel lengths, helping suppress short-channel effects. This improves saturation characteristics, reduces leakage current, and enhances short-circuit ruggedness.

Overall, mobility engineering, through advanced interface treatment techniques such as nitridation, post-oxidation annealing, and alternative dielectrics, offers a compelling route for simultaneous performance enhancement and long-term gate reliability.

2.4. Gate oxide degradation mechanisms

The long-term reliability of the gate oxide in SiC MOSFETs is governed by progressive degradation mechanisms, with time-dependent dielectric breakdown (TDDB) being the most critical. This stress-induced process determines the intrinsic lifetime of the gate dielectric under both operational and accelerated test conditions and has emerged as a dominant failure mechanism [47].

2.4.1. Experimental evaluation of TDDB

TDDB refers to the progressive accumulation of defects in the gate oxide under continuous electrical stress, ultimately resulting in dielectric failure. In 4H-SiC MOSFETs, TDDB is influenced by native defects such as oxygen vacancies, carbon clusters, and dangling bonds near the SiC/SiO_2 interface, which act as precursors for trap-assisted tunnelling (TAT) and local field enhancement [31,48]. The degradation mechanism involves the formation of percolation paths, leading to either soft or hard oxide breakdown. These failures may occur even at gate voltages significantly below the intrinsic breakdown field of SiO_2 (approximately 8–10 MV/cm). Studies have shown that TDDB lifetime (T^b) in SiC exhibits a Weibull slope (β) between 2 and 4, indicative of defect-driven breakdown [49].

2.4.2. Influence of electric field and temperature

The TDDB lifetime is typically modelled using empirical acceleration laws. Field-driven models include the E-model, 1/E model, the combined E + 1/E model, each reflecting different assumptions about how the oxide field accelerates bond breakage or carrier-induced defect generation [47,48]. TAT or percolation model provides a more phySiCal picture, describing breakdown as a progressive buildup of localized defects until a conductive path forms. In contrast, temperature acceleration is described by the Arrhenius model, where defect activity increases exponentially with thermal energy. Collectively, these relationships can be expressed as [50,51]:

$$T^b = \begin{cases} Ae^{\gamma/E_{ox}}; \ E - model \\ Ae^{B/E_{ox}}; \ 1/E \ model \\ Ae^{\alpha/E_{ox} - BE_{ox}}; \ E + 1/E \ model \\ Ae^{E_a/K_B T}; \ Arrhenius \ model \end{cases} \quad (2)$$

where E_{OX} is the oxide electric field, T is temperature, E_a is activation energy, K_B is Boltzmann constant and γ, A, α, B are fitting parameters. Experimental data report activation energies ranging from 0.7 to 0.9 eV for SiC MOSFETs under moderate electric fields (3–6 MV/cm) [52], notably lower than Si's typical range of 1.1–1.3 eV. However, lower E_a values (0.2–0.6 eV) may occur in SiC under high-field (>7.5 MV/cm) or high-temperature (>175 °C) conditions [53]. Table IV Summarizes the differences between these acceleration models.

2.4.3. Comparison with Si devices

In comparison to Si MOSFETs, while thermal SiO_2 exhibits similar intrinsic breakdown fields in both materials, the TDDB lifetimes in SiC devices are often significantly shorter. Si MOSFETs benefit from decades of process refinement and typically achieve TDDB lifetimes exceeding 10^6 hours under nominal conditions. In contrast, SiC devices require advancements such as post-oxidation annealing, alternative dielectric stacks, and interface passivation to achieve comparable reliability [54]. Table V summarizes the comparison gate oxide degradation mechanisms in SiC and Si MOSFETs.

2.4.4. Material and process defects

Beyond intrinsic oxide limitations, process induced imperfections during oxidation and interface formation critically impact reliability. Non-uniform oxidation, contamination, and insufficient passivation can lead to increased trap densities, enhance charge trapping, and accelerate early oxide failure. Therefore, improving fabrication control, including oxidation temperature, ambient chemistry, and annealing conditions, is essential for ensuring consistent oxide quality and extending device lifetime [55].

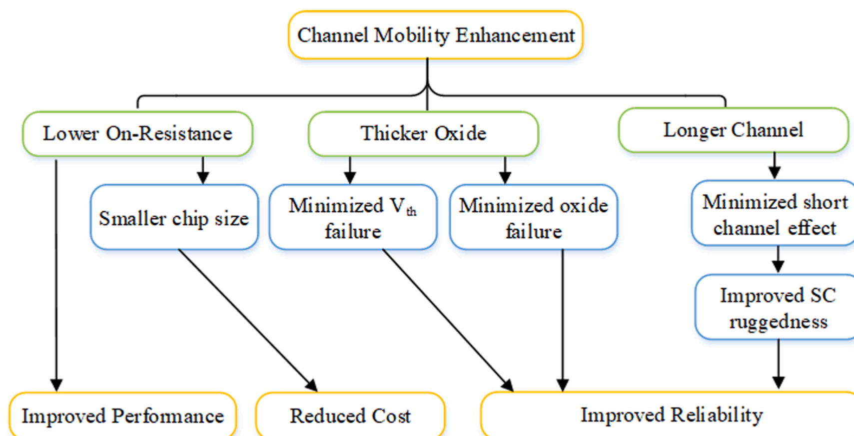


Fig. 11. *Enhancement techniques in channel mobility of SiC MOSFETs* [46].

Table IV
Comparison of TDDB Acceleration Models for SiC MOSFET Gate Oxides [31].

Model	Mechanism	Conduction Path	Driving Factor	Field Dependence	Temperature Dependence	Polarity Dependence
E-model	Thermochemical bond breaking	Trap generation	Electric field	Strong	Strong	No
1/E model	Carrier-induced defect generation	Fowler–Nordheim tunnelling	Field + energy	Strong	Weak	Yes
E + 1/E model	Combined field + carrier	Mix of FN + trap growth	Field + energy	Strong	Moderate	Yes
TAT/Percolation model	Defect buildup & percolation	Trap-assisted tunnelling	Electric field	Strong	Strong	Partial
Arrhenius model	Thermally activated bond breaking	Not field-specific	Temperature	None	Strong (activation energy)	No

Table V
Summary of Gate Oxide Degradation Mechanisms in SiC vs. Si MOSFETs.

Aspect	SiC MOSFETs	Si MOSFETs
Breakdown Field of SiO_2	~8–10 MV/cm	~8–10 MV/cm
TDDB Failure Features	Defect generation, trap-assisted tunnelling, local field enhancement, soft/hard breakdown	Mainly trap generation and oxide wear-out
Defect Sources	Carbon clusters, Si dangling bonds, oxygen vacancies near SiC/SiO_2 interface	Interface traps and oxide charges (fewer native defects)
Activation Energy (E_a) for TDDB	~0.2–0.6 eV	~0.7–1.2 eV
Typical Weibull Slope (β)	2–4 (field-driven defect accumulation)	Often >4 (indicates more consistent breakdown behaviour)
TDDB Lifetime Under Stress	Shorter due to poor interface quality and higher field operation	Longer, especially with optimised oxide processes
Mitigation Needs	Post-oxidation annealing, nitridation, high-κ dielectric integration	Mature process – fewer reliability enhancements required

3. SHORT circuit (SC) ruggedness

SiC MOSFETs performance under short-circuit conditions remains a key challenge. Compared to traditional silicon devices, SiC MOSFETs have a much shorter withstand time during faults, requiring advanced protection strategies to ensure system reliability. This section examines their failure mechanisms, thermal limitations, and key protection methods to enhance ruggedness in high power applications.

3.1. SC failure modes

SiC MOSFETs exhibit distinct SC failure modes compared to their Si IGBT counterparts. One of the primary challenges is their inherently lower short circuit withstand time (SCWT), which is a critical parameter in motor drives and fault-prone environments. For instance, 1.2 kV SiC MOSFETs typically endure SC conditions for approximately 2–12 μs [56, 57], whereas similarly rated Si IGBTs can withstand up to 30–40 μs [56] under comparable stress conditions. This reduced SCWT in SiC devices is attributed to their higher current densities and lower thermal mass, leading to rapid temperature escalation during fault events.

The dominant failure mechanisms in SiC MOSFETs under SC conditions are thermal runaway and gate oxide degradation. During a short circuit event, the device experiences a surge in power dissipation, causing localised heating. This rapid temperature rise can lead to the melting of metal contacts and degradation of the gate oxide layer, ultimately resulting in device failure. Additionally, the high electric fields present during SC events can exacerbate gate oxide stress, leading to increased leakage currents and potential breakdown.

Furthermore, the device architecture of SiC MOSFETs, characterised by thinner gate oxides and shorter channel lengths to achieve low on-resistance, inherently compromises their SC ruggedness. These design choices, while beneficial for performance, make the devices more susceptible to damage under fault conditions. Therefore, understanding these failure modes is crucial not only for real-time protection design but also for setting derating guidelines and establishing test protocols for device qualification [56-58].

3.2. Impact of high power density

SiC MOSFETs are renowned for their high power density, which, while advantageous for efficiency, can exacerbate short circuit vulnerabilities. During SC events, the rapid energy deposition leads to intense localised heating, particularly in the drift region, resulting in swift temperature rises that can exceed the thermal limits of the device. This rapid thermal buildup can lead to thermal runaway and device failure if not promptly mitigated [59].

3.3. SC protection methods

To address these challenges, advanced SC protection strategies have been developed. Active gate driving techniques, such as dynamic gate voltage clamping, have been shown to effectively reduce peak SC currents. For instance, an active gate drive (AGD) approach achieved up to a 46% reduction in SC current and a 51% reduction in SC loss compared to conventional gate drives in 1.2 kV SiC MOSFETs [60].

Complementing AGD, desaturation detection circuits monitor V_{ds} during operation. If V_{ds} exceeds a predefined threshold, indicating a potential SC event, the circuit rapidly turns off the MOSFET, typically within 1–2 μs, to prevent thermal runaway. A comprehensive review highlighted that desaturation detection is among the most widely adopted short-circuit protection methods for SiC MOSFETs, owing to its simplicity and effectiveness. However, it also noted that the response speed of desaturation detection can be limited by the blanking time, which is the intentional delay introduced to prevent false triggering during normal switching transients [56].

To validate the short-circuit protection concepts discussed above, representative SCWT experimental results are presented as an illustrative case study within the review framework. Fig. 12 shows experimental results of the SCWT response of a latest fourth-generation trench SiC MOSFET. The gate voltage (yellow) is initially held at –5 V and then driven high to initiate the short circuit pulse. Immediately after the fault is applied, the drain current (green) rises rapidly to a peak of approximately 297 A, followed by a slight current droop characteristic of channel mobility degradation and self-heating during SC conduction. During the event, the drain-source voltage (blue) remains clamped near the DC bus value of ≈400 V, with a small overshoot up to ≈534 V at SC clearance.

The gate source voltage experiences mild negative ringing between +20 V and –5 V, and the gate current (pink) remains relatively low with a peak of ±(8–15) μA, indicating that the gate oxide remains intact throughout the fault duration. This behaviour is consistent with the improved SC robustness of trench-structure SiC MOSFETs, where optimized channel design and reduced electric field crowding help limit

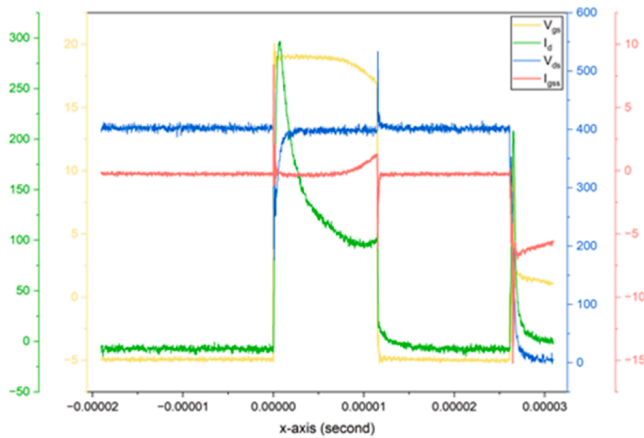


Fig. 12. *Experimental SCWT waveforms of a fourth-generation trench SiC MOSFET.*

thermal runaway and mitigate gate-oxide degradation during high energy short circuit events. Despite these improvements, the achievable SCWT of SiC MOSFETs remains significantly shorter than that of conventional Si IGBTs, which continue to offer superior short circuit endurance due to their current saturated behaviour and inherently robust bipolar conduction.

Table VI highlights the discussed details of SiC MOSFETS under SC conditions and compares them with their corresponding in Si IGBTs.

4. Avalanche ruggedness

This section explores the behaviour of SiC devices under UIS, identifies critical failure mechanisms, and reviews design strategies aimed at improving avalanche ruggedness and long-term reliability.

4.1. Unclamped inductive switching (UIS)

UIS events represent a critical stress condition in power devices, particularly in motor drives, power supply systems, and inductive load switching. The standard UIS setup, shown in Fig. 13, applies a high drain current and allows the device to absorb the inductor's stored energy in avalanche mode. As shown in Fig. 14, the drain source voltage surges during turn-off while the current decays exponentially, resulting in significant energy dissipation across the device. In such scenarios, avalanche capability becomes a key indicator of device ruggedness. Unlike Si IGBTs that inherently avoid avalanche operation due to latch-up risks, SiC MOSFETs can enter avalanche mode, allowing them to sustain energy from inductive overshoot through impact ionisation and

Table VI
Key Differences between SiC MOSFETs and Si IGBTs Under Short-Circuit (SC) Conditions.

Parameter	SiC MOSFETs	Si IGBTs
Short-Circuit Withstand Time (SCWT)	~2–12 µs	≥30 µs
Power Density	Higher (leads to rapid thermal rise)	Lower (slower thermal buildup)
Thermal Management	Challenging due to localised heating in drift region, thermal bottlenecks	Easier due to lower heat flux
Dominant SC Failure Mechanisms	Thermal runaway, gate oxide degradation, defect activation	Latch-up, junction failure
Device Design Focus	Low on-resistance, fast switching	High SC ruggedness
Short-Circuit Protection Techniques	Active Gate Drive (AGD), desaturation detection, dynamic clamping, soft shutdown	Desaturation detection, soft shutdown

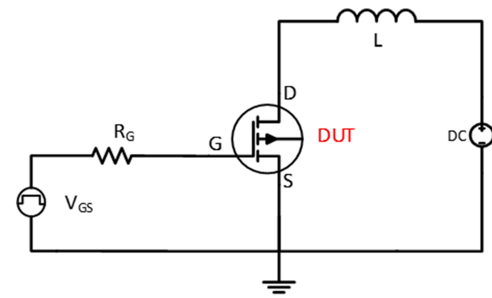


Fig. 13. *Standard unclamped inductive switching (UIS) test circuit for evaluating avalanche ruggedness in SiC MOSFETs.*

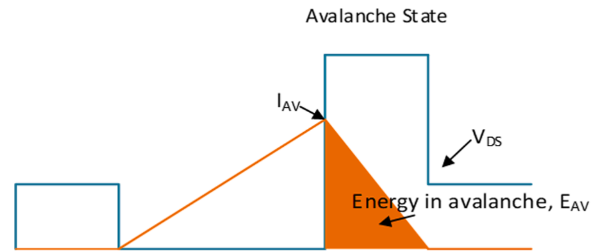


Fig. 14. *Typical drain current and voltage waveforms during UIS, showing avalanche phase and energy dissipation.*

hole generation in the drift region. However, due to the wide bandgap and low intrinsic carrier concentration of SiC, the onset of avalanche conditions leads to extremely high electric fields and significant energy dissipation within a small active area, risking localised thermal and structural damage if not managed [61,62].

Studies report that SiC MOSFETs withstand avalanche energy in the low mJ/mm^2 range, with failure often precipitated by localized thermal hotspots or oxide degradation near the termination edge during UIS events [63]. As such, understanding the failure mechanisms and improving avalanche tolerance through termination engineering, cell design, and robust passivation remains an active research area [64].

To illustrate the avalanche stress mechanisms and reliability implications discussed above, representative UIS experimental results are presented as an illustrative case study within the review framework. Fig. 15 presents UIS test results conducted on a planar SiC MOSFET. The yellow, blue, green and pink waveforms are the gate–source voltage V_{gs}, the drain–source voltage V_{ds}, the avalanche current I_d, and the gate current I_{gss}, respectively. When the device is forced off under inductive load, the drain current cannot change abruptly, forcing the MOSFET into

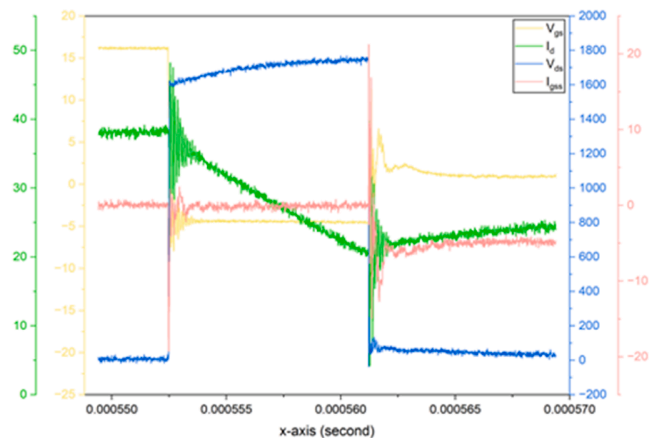


Fig. 15. *Experimental UIS test waveforms of a planar SiC MOSFET.*

avalanche. This is evident from the rise in V_{ds}, which peaks at approximately 1.77 kV, significantly above the nominal blocking rating, indicating avalanche breakdown of the drift region. Simultaneously, the avalanche current exhibits a plateau around 30–35 A, with a peak overshoot of 48 A, reflecting the inductive current being commutated through the body diode and drift region.

During the avalanche event, the device experiences substantial electrical stress. The gate source voltage exhibits a pronounced negative ringing, reaching –21 V, driven by high di/dt and parasitic inductances in the gate loop. Additionally, the gate current increases sharply, with I_{gss} peaking at ±20 μA, indicating hot-carrier injection and localized electric-field stress at the gate oxide interface. These UIS degradation mechanisms in planar SiC MOSFETs can be explained as impact ionization, hole generation in the JFET region, and oxide electric-field crowding can accelerate gate oxide wear-out and elevate leakage levels. The measured waveforms therefore clearly illustrate the intrinsic UIS vulnerability of planar SiC MOSFET structures and the associated reliability risks under high energy avalanche conditions.

4.2. Avalanche failure mechanisms

During avalanche operation in SiC MOSFETs, several intrinsic failure mechanisms can be activated depending on the device structure and stress conditions. A critical failure pathway involves parasitic bipolar junction transistor (BJT) latch-up, which is triggered by impact ionisation in the JFET region. Under high avalanche current, generated electron-hole pairs can forward-bias the body source junction, inadvertently activating the parasitic BJT formed by the n⁺ source, p-body, and n-drift regions. Once turned on, this BJT sustains current independent of the gate bias, leading to thermal runaway and permanent damage. Some investigations showed that latch-up thresholds are highly sensitive to cell pitch and base resistance, particularly under repetitive UIS stress [65].

Another dominant degradation route arises from localised thermal damage due to intense power dissipation during avalanche. Power densities can exceed 10^5 W/cm^2 within microseconds, particularly near the gate oxide and termination region, resulting in bond wire lift-off, metallization melting, or gate oxide rupture [66]. Studies confirmed that thermally induced delamination and micro-cracking in the passivation layers often act as precursors to catastrophic failure, especially during repetitive avalanche events. These mechanisms highlight the need for careful electrothermal design and termination engineering in high reliability SiC power systems [64].

4.3. Design improvements for better UIS performance

Improving avalanche ruggedness in SiC MOSFETs under UIS stress requires structural enhancements targeting key failure mechanisms such as field crowding, thermal localization, oxide breakdown, and parasitic BJT activation. Effective strategies include junction termination optimization, buffer layer engineering, and channel structure design (e.g., trench vs. planar), each contributing to better electric field management, thermal handling, and oxide protection.

4.3.1. Optimised junction termination structures

The termination region plays a critical role in determining the electric field distribution at the device periphery during UIS events. Poor termination design leads to field peaking, which significantly increases the risk of gate oxide rupture and early avalanche failure. To counter this, Field Limiting Rings (FLRs), Junction Termination Extensions (JTEs), and deep trench terminations have been widely adopted. These structures distribute the depletion region more uniformly and reduce electric field concentration near the gate and edge termination. The study [67] demonstrated that grading the JTE region using multi-zone doping not only improved the breakdown voltage uniformity but also enhanced avalanche energy tolerance in 1.2 kV SiC MOSFETs.

4.3.2. Enhanced buffer layers for high energy transients

The buffer layer, typically located between the n-drift region and the SiC substrate, serves as a key energy absorbing layer during avalanche conditions. A well-engineered buffer moderates the high energy impact ionisation front, disperses heat, and reduces the likelihood of parasitic BJT activation by lowering the base resistance. Studies showed that step-graded n-type buffer layers in 4H-SiC effectively extended avalanche survivability by smoothing the electric field transition at the drift-buffer interface [68]. Meanwhile, [69] demonstrated through failure analysis that buffer doping profiles significantly influenced avalanche robustness by affecting hole extraction and thermal distribution in the device.

4.3.3. Impact of trench and planar structures on UIS ruggedness

Beyond termination and buffer engineering, gate/channel geometry significantly affects avalanche tolerance. A recent investigation [70] compared the UIS performance of planar, symmetrical double-trench, and asymmetrical trench 1.2 kV SiC MOSFETs using a novel high energy avalanche method based on incremental source voltage stress. Planar devices showed the lowest avalanche energy density and early oxide breakdown due to electric field crowding near the gate oxide. Symmetric trench devices, with deep P-well shielding, improved field management and energy absorption but became vulnerable under elevated temperatures due to oxide fatigue. In contrast, the asymmetric trench design, featuring a field-shielded trench and channel aligned to the (11–20) crystal plane, exhibited the highest avalanche energy tolerance, especially at 175 °C. This geometry effectively suppressed electric field peaks and improved mobility without triggering parasitic BJT conduction. These findings underscore the importance of channel orientation, oxide protection, and trench asymmetry in enhancing avalanche ruggedness across SiC MOSFET designs.

Key mechanisms, stress responses, and structural improvements related to avalanche ruggedness in SiC MOSFETs during UIS operation have been summarized in Table VII.

Table VII
Summary of Avalanche Ruggedness and Design Considerations for SiC MOSFETs.

Aspect	Description / Observation	References
Unclamped Inductive Switching (UIS)	UIS events are common in motor drives, traction systems, and power supplies, UIS forces SiC MOSFETs into avalanche mode to absorb inductor energy, stressing the drain and gate oxide.	[61,62]
Energy Levels	Typical avalanche energy ratings low mJ/mm^2 range in commercial 1.2 kV SiC MOSFETs.	[63]
Failure Trigger Locations	Failures commonly initiate at termination edges, gate oxide, or localised hotspots.	[63,64]
Parasitic BJT Latch-up	Caused by impact ionisation; turns on n⁺/p/n structure, leading to thermal runaway and uncontrolled current.	[65]
Thermal Failure Modes	$>10^5$ W/cm^2 power densities can cause bond wire lift-off, oxide rupture, and passivation cracks.	[66]
Termination Optimization	FLRs, JTEs, and trench terminations reduce field crowding; multi-zone JTE doping enhances E_{AV}.	[67]
Buffer Layer Engineering	Step-graded or doped buffer layers absorb energy, suppress latch-up, and enhance thermal stability.	[68,69]
Gate and Channel Structure	Avalanche ruggedness is influenced by gate geometry. Planar devices show earlier oxide breakdown due to field crowding, while asymmetrical trench designs improve energy tolerance and thermal handling.	[70]

5. Reliability under power cycling stress

Power cycling reliability is a critical factor in the long-term performance of SiC MOSFETs, especially in applications involving frequent thermal transitions caused by periodic power dissipation during operation. Repeated junction temperature fluctuations can induce mechanical fatigue in various packaging elements, potentially leading to device degradation or failure. This section addresses the primary reliability challenges under power cycling conditions, including thermal stress-induced bond wire lift-off, degradation of die attach and solder joints, and explores emerging relevant solutions.

5.1. Thermal stress and bond wire lift-off

One of the primary failure mechanisms in power semiconductor modules subjected to power cycling stress is the degradation and eventual lift-off of bond wires, which provide both the main electrical connection and a path for heat dissipation between the semiconductor die and the package terminals. In SiC MOSFETs, the higher permissible junction temperatures ($T_{j,\max}$ of 175–200 °C) and faster switching speeds lead to more aggressive thermal gradients compared to silicon counterparts, making them more susceptible to thermo-mechanical fatigue. Repetitive heating and cooling during on-off cycles induce cyclic mechanical strain at the wire–pad interface, particularly in aluminium bond wires, due to the mismatch in coefficient of thermal expansion (CTE) between the bond wire and the underlying metallization layer. Over time, this strain leads to crack initiation and propagation at the heel of the bond, eventually causing partial or complete lift-off, increased contact resistance, and localised hot spots [71,72].

Experimental studies using accelerated power cycling tests have demonstrated that bond wire degradation remains a dominant failure mode in SiC modules even under moderate current and temperature swing conditions. For instance, some studies revealed that bond wire lift-off typically occurs after 10^4–10^6 cycles [73,74], depending on the thermal swing (ΔT_j) and current amplitude.

Additionally, techniques such as scanning acoustic microscopy (SAM) and X-ray imaging have confirmed that early-stage delamination or void formation at the wire interface can significantly accelerate the degradation process [75]. The PC test is fully described later in the paper in reliability tests section. As such, improving wire material selection (e.g., AlCu, Ag) and adopting wire-less packaging methods (e.g., sintered die attaches or planar interconnects) are active research areas aimed at mitigating this reliability bottleneck in SiC-based power modules.

5.2. Die attach and solder joint degradation

While bond wire fatigue is primarily driven by mechanical stress at the wire pad interface, the die attaches and solder joints in SiC power modules are subject to creep-driven degradation under prolonged power cycling. These joints experience plastic deformation and void formation due to repeated thermal expansion and contraction, particularly at elevated junction temperatures enabled by SiC's wide bandgap. The mismatch in CTE between the SiC die, solder layer, and copper baseplate causes shear stress across the die attach region, which gradually initiates micro voids and cracks, particularly near the die edges and corners.

Unlike wire bond degradation, which results in open circuit failures, solder degradation leads to progressive delamination, reduced thermal conductivity, and rising junction to case thermal resistance ($R_{th,jc}$), ultimately resulting in overheating and system-level failure. Studies demonstrated that significant void growth and intermetallic compound (IMC) formation were observed in the solder layer after 61,000–220,000 thermal cycles (ΔT_j=120 K) and 830,000–1430,000 cycles (ΔT_j=90 K), while no degradation occurred even after 3000,000 cycles at ΔT_j=60 K [76,64], directly correlating with device performance degradation. Advanced diagnostics like X-ray microtomography, SAM, and cross-sectional Scanning Electron Microscopy (SEM) imaging are commonly used to monitor void propagation and delamination depth, making them essential tools for assessing long-term solder joint reliability [77].

For clarity, Table VIII summarises the dominant packaging failure sites in SiC MOSFETs under power cycling stress, together with their primary stress drivers, and characteristic degradation mechanisms.

5.3. Improving thermo-mechanical reliability

To address the limitations of conventional solder joints and bond wires under power cycling conditions, advanced packaging technologies such as silver (Ag) sintering and copper (Cu) clip bonding have emerged as effective solutions for improving the thermo-mechanical reliability of SiC power modules. Unlike traditional solder, Ag sintering offers superior thermal conductivity (~250 W/m·K) and mechanical robustness at high temperatures. It forms a porous, interlocked microstructure that resists creep and void growth under thermal stress, significantly extending the lifetime of the die attach layer. Experimental results have shown that Ag sintered joints can endure over 10^6 power cycles with minimal degradation [78], making them especially suitable for automotive and high frequency switching applications.

In parallel, Cu clip bonding is increasingly replacing aluminium wire bonding due to its enhanced current-carrying capability, lower parasitic inductance, and better heat spreading. By forming a direct metal connection between the SiC die and the lead frame, Cu clips eliminate the heel-crack vulnerability associated with wire bonds and reduce the thermal resistance path. Studies have reported that Cu clip bonded SiC MOSFETs exhibit lower junction temperatures and improved power cycling endurance, particularly under high current density conditions [79]. Furthermore, the integration of sintered Ag die attach with Cu clip interconnects has proven effective in achieving highly reliable, compact, and low-inductance packaging designs [80].

Table IX summarises the key differences between traditional and advanced packaging approaches discussed in this subsection. In SiC MOSFETs, the intrinsic body diode provides a freewheeling current path during reverse conduction.

6. BODY diode reliability AND surge current stress

In SiC MOSFETs, the intrinsic body diode provides a freewheeling current path during reverse conduction. However, unlike external fast recovery diodes, the SiC MOSFET body diode faces unique reliability challenges under repetitive reverse conduction and surge current stress. This section explores the limitations of using the intrinsic body diode, examines the failure mechanisms triggered by high current pulses, and highlights recent strategies aimed at improving its ruggedness and reliability

6.1. Challenges of using intrinsic body diode

The intrinsic body diode of SiC MOSFETs, formed by the P-N junction between the p-body and the n-drift region, presents significant limitations when used in reverse conduction. As shown in Fig. 16, this diode is embedded in the vertical structure of the MOSFET and conducts current when the device is reverse-biased. One of the primary drawbacks is its relatively high forward voltage drop (V_F), typically ranging from 2.5 V to 3.5 V, compared to ~0.7–1 V in silicon PiN diodes. This elevated V_F results from SiC's wide bandgap (~3.26 eV), which inherently raises the built-in potential across the junction. As a consequence, using the intrinsic body diode in continuous conduction, such as in the freewheeling path of motor drives or inverters, leads to increased conduction losses and reduced overall system efficiency [81,82]. This makes the body diode less suitable for applications requiring frequent reverse conduction or soft switching unless specific mitigation strategies, such as synchronous rectification or external Schottky diodes, are employed.

Table VIII
Summary of Dominant Packaging Failure Mechanisms in SiC MOSFETs under Power Cycling Stress.

Failure Spot	Dominant Stress Drivers	Primary Failure Mechanisms	Key Degradation Indicators
Bond Wires	Junction temperature swing (ΔT_j), current density, CTE mismatch	Heel cracking, wire lift-off, increased contact resistance	Rise in $R_{ds(on)}$, local hot spots, intermittent open-circuit behavior
Die Attach / Solder Joints	Repetitive thermal cycling, high operating temperature, CTE mismatch (SiC–substrate)	Creep, void growth, delamination, IMC formation	Increase in $R_{th(j-c)}$, reduced heat dissipation, thermal runaway
Package-Level Interconnects	Mechanical fatigue, thermo-mechanical stress	Cracking, delamination, loss of mechanical integrity	Degraded thermal impedance, mechanical failure

Table IX
Comparison of Packaging Techniques to Enhance SiC MOSFET Reliability Under Power Cycling.

Aspect	Conventional Technology	Advanced Solution
Die Attach Material	Tin-based solder (e.g., SAC alloys)	Sintered silver paste
Wire Interconnect	Aluminium bond wires	Copper clip bonding
Thermal Conductivity	~50–60 W/m·K	~250 W/m·K (Ag sinter), superior heat dissipation
Mechanical Degradation	Creep, void formation, IMC growth	Minimal creep, robust microstructure
Power Cycling Lifetime	~10^4–10^5 cycles (moderate ΔTj)	>10^6 cycles under similar or harsher conditions
Failure Mechanisms	Bond wire heel cracking, solder delamination	Significantly reduced fatigue and delamination
Current Carrying Capability	Limited (Al wire)	High (Cu clip, wider contact area)
Inductance	High (loop inductance from wire bonds)	Low (shorter current path, lower ESL)
Integration Complexity	Mature and low-cost	Higher cost, but increasingly adopted in industry
Application Suitability	Low/medium stress environments	Automotive, industrial, and high-reliability systems

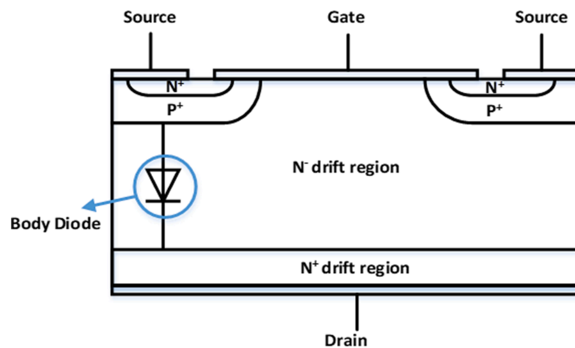


Fig. 16. *Cross-sectional structure of a typical SiC MOSFET, highlighting the intrinsic body diode formed between the p-body and n-drift region.*

Moreover, while SiC diodes generally exhibit negligible Q_{rr}, the body diode in a MOSFET can still experience minor reverse recovery effects due to the presence of interface traps and carrier injection, further complicating its use in high-speed switching applications [83].

6.2. Failure mechanisms under high surge currents

When a SiC MOSFET's intrinsic body diode is subjected to high surge current events, such as inrushes, fault transients, or freewheeling during inductive turn-off, it can experience rapid internal degradation that significantly impacts device reliability. Although the body diode does not directly involve the gate terminal, the associated self-heating and carrier injection during high surge conduction may indirectly induce charge trapping near the gate oxide, contributing to a shift in V_{th}. Simultaneously, $R_{ds(on)}$ tends to increase due to carrier mobility degradation and contact damage within the source metallization or drift region. These changes lead to reduced current-handling efficiency and elevated conduction losses in subsequent operation cycles [84].

Additionally, repeated or excessive surge currents can cause non-uniform current spreading across the die, resulting in localised hot-spots and possible activation of the parasitic BJT structure under extreme conditions. This can initiate soft breakdown of the gate oxide or even thermal runaway if adequate protection is not in place. Failure analysis in literature has revealed that prolonged exposure to surge pulses not only causes deformation in bond wires and metallization layers but also contributes to die cracking or delamination in extreme cases [85]. Therefore, understanding the thermal-electrical interaction during high-current conduction is essential for designing robust SiC power modules, particularly in applications with frequent surge stress such as EV inverters and industrial drives.

6.3. Solutions to improve body diode reliability

To overcome the reliability and efficiency limitations of the intrinsic body diode in SiC MOSFETs, a widely adopted solution is the integration of an external Schottky barrier diode (SBD) in a hybrid configuration. Unlike the body diode, which has a high forward voltage and exhibits bipolar degradation under surge current stress, the SiC SBD is a majority carrier device with lower V_F (typically <1.5 V) and negligible Q_{rr}. When connected in antiparallel with the MOSFET, the SBD naturally conducts during reverse current flow, thereby bypassing the intrinsic body diode and significantly reducing conduction losses and thermal stress in free-wheeling and reverse conduction applications [86].

This approach not only improves energy efficiency but also enhances surge current ruggedness, as the SBD can be designed with optimised chip area and layout to better manage current spreading and heat dissipation. Commercial implementations, such as hybrid modules that co-package a SiC MOSFET and an SBD, have demonstrated improved reverse conduction performance and extended device lifetime in motor drives, onboard chargers, and power factor correction circuits [87]. Moreover, recent advancements in integrated SBD within the MOSFET structure show promise in further minimising parasitic elements and packaging complexity while maintaining high reliability under repetitive stress [88].

To illustrate the practical impact of body diode reliability challenges and the effectiveness of mitigation strategies discussed above, representative experimental case studies are briefly discussed. The performance of 1.2 kV SiC planar MOSFETs has been thoroughly investigated under three operating scenarios in [89]. The first scenario, the device is paired with SiC SBD, ensuring that the body diode (BD) does not conduct. In the second, the SiC SBD is removed, forcing the device to rely solely on its body diode. The third scenario uses both SiC SBD and the BD connected in parallel (SBD+BD). For the first case, an auxiliary diode must be placed in series with the switch to block BD conduction in the third quadrant, which introduces extra conduction losses and affects switching losses differently for each device technology. A hard-switched converter model is simulated to evaluate and compare the losses of these diode configurations against those achieved with synchronous rectification as shown in Fig. 17. The SiC MOSFET were tested using several gate resistance values (10 Ω, 15 Ω, 30 Ω, and 68 Ω) and at a junction temperature 150 °C. All the tests are conducted with an 800 V DC link

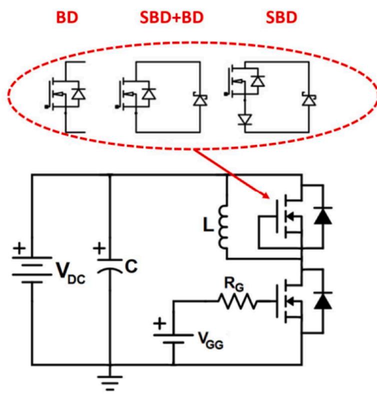


Fig. 17. *Test setup of clamped inductive switching illustrates the various high-side diode configurations* [89].

and a load current of 30 A. The switching tests are carried out under three different high side diode configurations. Fig. 18 presents the turn-on and turn-off energies versus gate resistance for three scenarios. As illustrated, the turn-off energy does not vary with the body diode configuration. This is expected because turning the transistor off effectively turns the diode on, and the diode's turn-on behaviour remains the same whether the conduction path is through the BD, SBD, or the SBD+BD combination. In contrast, the measured turn-on energies exhibit clear differences. The lowest turn-on energy occurs with the SBD configuration, followed by the SBD+BD arrangement, and then the BD alone. Notably, the SBD+BD configuration results in only a 10.6% increase in turn-on energy (averaged across the four gate resistance values) compared with the SBD. However, using only the BD yields a turn-on energy that is 56.7% higher than the SBD+BD case. These results show an advantage in using the SBD configuration.

The work [90] examines how the body diode of the fourth generation SiC trench MOSFET degrades under different gate turn-off voltages. Applying a negative gate turn-off voltage leads to pronounced degradation, as confirmed experimentally. After 96 h of DC current stress on the body diode, the device shows a 22.5% rise in on-state resistance, a 4.7% increase in diode forward voltage, and >150 nA of additional drain source leakage current.

The device is evaluated using a group of samples, where it consists of four series connected devices supplied by a current source and cooled by a dedicated thermal management system, as shown in Fig. 19. The group operates with the manufacturer recommended negative gate source voltage (V_{gs} = –4 V). To apply this negative bias across the gate-source terminals of the four series connected devices, four isolated DC/DC converters are employed. The group undergoes a 96-hour stress test at a constant 10 A, corresponding to 25% of the device's rated current. This results in current densities of 168 A/cm^2. Device characterization is performed before stressing and every 48 h using a Keysight B1505A parameter analyser. The primary electrical parameters evaluated are the on-state resistance $R_{ds(on)}$, body diode forward voltage V_{sd} and drain source leakage current I_{dss}. The case temperature was continuously monitored during the entire test and kept close to 90 °C. A noticeable change in the static characteristics of the trench MOSFETs appeared after 48 h of stress. Fig. 20 shows the evolution of $R_{ds(on)}$ over the test duration. The $R_{ds(on)}$ measurements were taken at a drain current of 29 A (as specified in the datasheet), with a gate-source voltage of 18 V, and at a temperature of 25 °C. Devices exhibited a pronounced increase in $R_{ds(on)}$. After 96 h of DC current stress, all four devices showed more than a 9% rise in $R_{ds(on)}$, with device 4 (D4) reaching a maximum increase of 22.5%.

Fig. 21 illustrates the body diode voltage drop over time for the DUTs. Similar to the trends observed for $R_{ds(on)}$, they exhibit an increase in voltage drop. All devices showed a significant rise exceeding 2%, with device D4 experiencing the largest shift of 4.75% after 96 h of stress. The increase in the V_{sd} is attributed to stacking faults in the drift region,

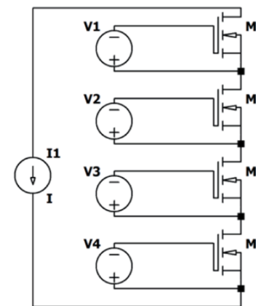


Fig. 19. *Test circuit configuration of the body diode stress* [90].

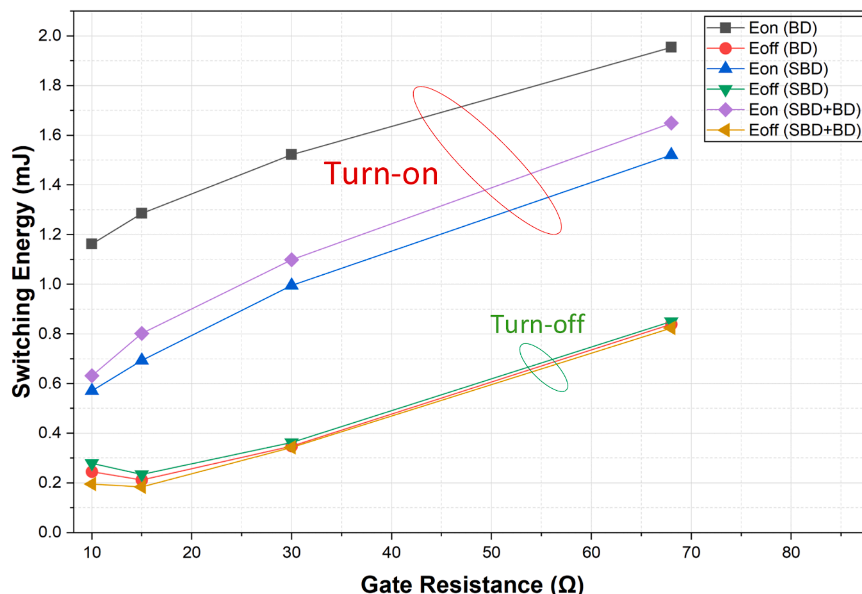


Fig. 18. *Turn-on/off switching energy of the 1.2 kV SiC planar MOSFET under three diode configuration conditions.*

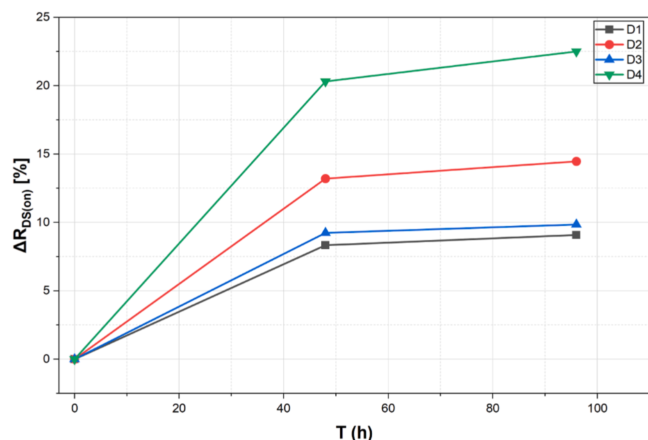


Fig. 20. *Change in $R_{ds(on)}$ for SiC trench MOSFETs after body diode stress.*

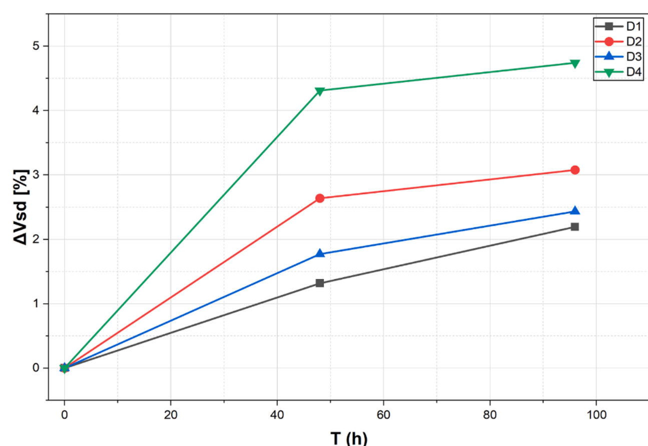


Fig. 21. *Change in V_{sd} for SiC trench MOSFETs after body diode stress.*

which reduce carrier lifetime.

Fig. 22 shows the drain source leakage current I_{dss} measured at 400 V over the stress period for the DUTs. For three of them, I_{dss} increased to approximately 100 nA, whereas one device experienced a more pronounced rise, reaching as high as 700 nA.

Table X shows a comparison of the electrical and reliability characteristics of the intrinsic body diode in SiC MOSFETs and a hybrid SiC MOSFET + SBD configuration.

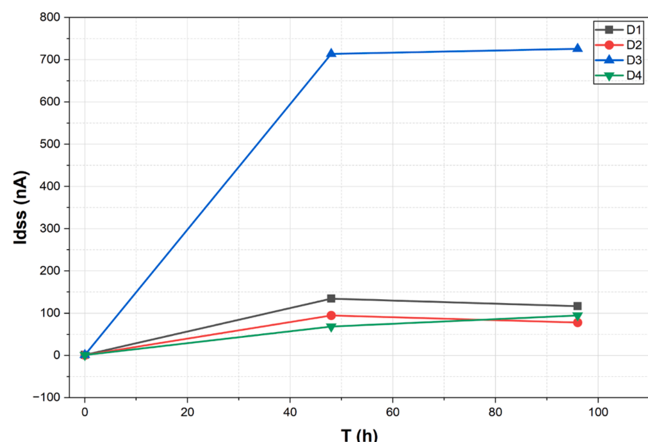


Fig. 22. *Change in I_{dss} for SiC trench MOSFETs after body diode stress.*

Table X
Comparison of SiC MOSFET Body Diode vs. Hybrid SiC MOSFET + SBD Configuration.

Aspect	Intrinsic Body Diode	Hybrid SiC MOSFET + SBD
Conduction Mechanism	Bipolar conduction (includes minority carriers)	Majority carrier conduction only
Forward Voltage Drop (V_F)	High	Low
Reverse Recovery Charge (Q_{rr})	Small but present due to minority carrier injection	Negligible
Surge Current Handling	Limited; can trigger degradation and parasitic BJT latch-up	Higher robustness; optimised for surge and reverse conduction
Power Loss During Freewheeling	Higher conduction and switching losses	Reduced losses, improved efficiency
Reliability Under Stress	Prone to V_{th} shift, $R_{DS(on)}$ increase, and oxide damage	Enhanced ruggedness; better thermal performance
Packaging Complexity	Simpler (no additional diode)	Slightly increased due to added component
Application Suitability	Light-load, low-duty reverse conduction	Heavy-duty reverse current, high-efficiency power conversion

7. Reliability tests

Reliability testing plays a central role in validating SiC power MOSFETs and ensuring their safe use in demanding applications. Manufacturers employ standardized tests to expose devices to accelerated stress conditions that mimic, and often exceed, real-world operating environments. The testing process involves applying controlled stress patterns such as thermal cycling, high humidity exposure, mechanical vibration, and rapid temperature changes. Key electrical parameters, including thermal impedance, leakage currents, threshold voltage, and on-state resistance, are continuously monitored to assess device degradation. The ultimate goals are to predict operational lifetime, confirm compliance with quality standards, and establish performance limits under harsh conditions. To ensure consistency across industries, international organizations have established well-defined reliability standards. The Joint Electron Device Engineering Council (JEDEC) [91] and the International Electrotechnical Commission (IEC) [92] provide general guidelines for evaluating electronic components under harsh conditions. In the automotive sector, more specialized frameworks, such as AQG 324 from the European Center for Power Electronics (ECPE) [93] and the Automotive Electronics Council (AEC) standards [94] are widely used to qualify power semiconductor modules for safety-critical applications.

In the subsequent parts, specific categories of reliability evaluation are outlined. For clarity, Table XI summarizes the main tests, while Table XII presents the corresponding standards for each.

7.1. Environmental tests

To assess the suitability of power electronics modules under harsh thermal and mechanical conditions, validated through phySiCal analysis and evaluation of electrical, mechanical, and insulation properties.

7.1.1. Thermal cycling

Thermal cycling tests assess the durability of power modules under repeated passive temperature variations, either by changing the ambient temperature (Thermal Shock Test, TST) or by cycling the case temperature (Thermal Cycling Test, TC) without electrical bias. The DUT is alternately exposed to heating and cooling chambers, typically completing 1–2 cycles per hour with at least 15 min at each temperature extreme to ensure stabilization. The test primarily evaluates solder joint lifetime and mechanical stress caused by mismatched thermal expansion. The test duration must allow the device to fully stabilize at both the low and high temperature extremes. Typically, the DUT is held at each temperature for at least 15 min, with 1–2 cycles completed per hour

Table XI
Summary of Standard Reliability Tests for SiC Power MOSFET [96].

Test	Objective	Stress Conditions
High Temperature Reverse Bias (HTRB)	Evaluates insulation and passivation layer stability under high reverse bias conditions.	Applied bias at 80–100% of V_{BR} near $T_{j,max}$ for 1000 h. Observe the change in leakage current.
High Temperature Gate Bias (HTGB)	Investigates gate oxide reliability and degradation under elevated gate bias stress.	±100% of maximum V_{gs} applied near $T_{j,max}$ for 1000 h. Observe the change in I_{gss} and V_{th} shift.
High Humidity High Temperature Reverse Bias (H3TRB)	Simulates degradation mechanisms caused by moisture exposure under combined electrical and environmental stress.	85 °C, 85% relative humidity, 1000 h with part reverse biased at 80% of rated breakdown voltage. Observe the change in leakage current.
High Temperature Storage Tests (HTS)	Assesses long-term degradation when exposed to elevated ambient temperatures.	Storage at >125 °C for 1000 h. DUT must remain fully operational without damage.
Low Temperature Storage (LTS)	Tests device robustness under cold storage and transportation conditions.	Storage at <–40 °C for 1000 h. DUT must remain fully operational without damage.
Thermal Cycling (TC)	Evaluates mechanical stress and fatigue caused by repeated passive temperature variations.	Cycling between –40 °C and 125 °C until R_{th} increases by >20%.
Vibration Test	Verifies mechanical integrity under vibration, particularly for automotive and transportation applications.	Sinusoidal vibration, 10–1000 Hz, 5 g acceleration. DUT must maintain full functionality.
Mechanical Shock	Evaluates resistance to sudden mechanical impacts.	Shock applied without electrical bias. DUT must maintain full functionality.
Power Cycling (PC)	Examines thermal fatigue caused by repetitive active heating and cooling of the device.	Fast cycles: $\Delta T_j > 100$ °C (wire-bond fatigue). Slow cycles: $\Delta T_j < 80$ °C (solder fatigue).

Table XII
Summary of Standard Names for SiC Power MOSFET Reliability Tests.

Test	Standard	Reference
HTRB	IEC 60,747–8 IEC 60,749–23 JESD22-A108D	[97–99]
HTGB	IEC 60,747–8 IEC 60,749–23 JESD22-A108D	[97–99]
H3TRB	IEC 60,068–2–67 JESD22-A101C	[100,101]
HTS	IEC 60,749–6 JESD22-A103D	[102,103]
LTS	JESD22-A119	[104]
TC	IEC 60,749–25 JESD22-A104D	[95,105]
Vibration Test	IEC 60,068–2–6 JESD22-B103B	[106,107]
Mechanical Shock	IEC 60,068–2–27 JESD22-B104C	[108,109]
PC	IEC 60,749–34 JESD22-A122	[110,111]

[93]. For power modules, the standard temperature range As Per AEC-Q101 is –55 °C to maximum rated junction temperature, not to exceed 150 °C [95]. Modern designs, especially those using sintered dies and baseplate-free structures, have demonstrated survival beyond 1500 cycles without failure [96]. A common failure criterion is defined as a 20% increase in thermal resistance compared to the initial pre-test value. Fig. 23 illustrates a typical test setup and the corresponding temperature profile over time.

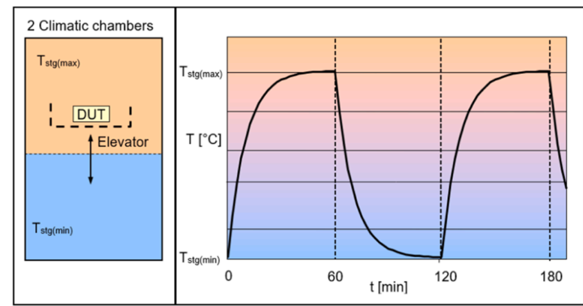


Fig. 23. *Configuration of the thermal cycling test and applied temperature profile* [96].

7.1.2. High and low temperature storage tests (HTS, LTS)

These tests evaluate the impact of prolonged exposure to extreme storage conditions on power modules, ensuring package integrity under both high and low thermal stress. In HTS, devices are stored at ambient temperatures above 125 °C for around 1000 h, while LTS subjects them to very low temperatures, typically near –40 °C, for the same duration. After tests, the modules must remain operational and free from any phySiCal damage such as cracks.

7.1.3. Vibration test

The test evaluates the mechanical robustness of power modules for automotive converter applications, and targets common structural weaknesses such as spring-contact fatigue, solder joint instability under vibration, and cracks in structural parts. The test frequency range is from 10 Hz to at least 1000 Hz with an acceleration of 5 g, although lower limits may vary depending on the equipment. The device must remain fully operational

7.2. Mechanical shock test

The test verifies a device's resistance to sudden impacts and the ability of solder joints to withstand external mechanical stress and identifies potential failure modes such as cracks or detachment within the module structure. The test is performed without electrical bias, and the DUT must retain full functionality.

7.3. Lifetime tests

lifetime tests subject the DUTs to various operating conditions to deliberately trigger typical degradation mechanisms in power electronics modules.

7.3.1. High temperature reverse bias (HTRB)

The test assesses long-term device stability under high drain source bias, identifying weaknesses in the passivation layer and chip-edge sealing. DUTs are stressed at 80–100% of the reverse V_{BR}, with the gate shorted to the source, at ambient temperatures near the maximum junction rating for 1000 h. A healthy device shows only slight leakage current increase, while failure is defined by excessive leakage leading to thermal runaway [112]. Leakage is continuously monitored, and advanced setups often employ a gradual voltage ramp ("soft bias") to reduce initial overstress [113].

7.3.2. High temperature gate bias (HTGB)

The HTGB test evaluates degradation in gate oxide under combined electrical and thermal stress. It detects V_{th} drift caused by random oxide defects and ionic contamination. The test applies the maximum rated positive and negative gate source voltages, with the drain shorted to the source, at ambient temperatures near the maximum junction rating for 1000 h. Variations in V_{th} during the test reveal gate oxide reliability issues [112].

7.3.3. High humidity high temperature reverse bias (H^3TRB/THB)

The H^3TRB test, also known as Temperature and Humidity Bias (THB), examines moisture-induced degradation in power devices and modules. Since most designs are not hermetically sealed, moisture diffuses through silicone gel encapsulation and reaches the passivation layer, potentially affecting active regions and interconnects. DUTs are subjected to 85% relative humidity, 85 °C in an environmental chamber, and AEC-Q101 recommend using 80% of the rated voltage for 1000 h while biased, with drain source leakage current continuously monitored to identify weak points in both the device and module structure [114]. The test can be extended to High Voltage, High Humidity, High Temperature, Reverse Bias (HV-H^3TRB), this test applies the same environmental stressors but with higher reverse or blocking voltage (for high-voltage power devices such as SiC MOSFETs) to more aggressively accelerate failure mechanisms [115].

7.3.4. Power cycling

In power cycling (PC) tests, the devices are repeatedly heated through electrical losses and cooled afterward by switching off the load current. This process creates steep internal temperature gradients over successive cycles. Two modes are typically used: active cycling, where heating occurs from power dissipation, and passive cycling, where the device is externally heated and cooled. Fast cycling (on the order of seconds) with large temperature swings ($\Delta T > 100$ °C) often leads to wire-bond failures, whereas slower cycling (minutes) with smaller swings ($\Delta T < 80$ °C) primarily causes solder fatigue. Test outcomes are usually expressed as curves of maximum cycles versus ΔT, with high ΔT values enabling accelerated testing that can be extrapolated to real operating conditions [116]. According to the ECPE Guideline, power cycling is classified into two categories: Power Cycling with seconds (PCsec), using short power pulses (< 5 s) that mainly stress chip-near interconnections, and Power Cycling with minutes (PCmin), with longer pulses (> 15 s) that affect both near and remote interconnections. Fig. 24 illustrates a typical test setup and the corresponding temperature profile over time.

Depending on the intended stress conditions and level of realism, power cycling tests can be implemented using many configurations as stated in the literature [117], while the two main configurations are conventional DC, and AC circuits, each designed to impose thermal loading on the device through different mechanisms. Each configuration offers distinct advantages and limitations: the conventional DC circuit provides simplicity and cost-effectiveness but lacks full operational realism, and the AC configuration, though more sophisticated and resource-intensive, delivers the most representative evaluation by incorporating both conduction and switching losses under converter-like conditions. Table XII highlights the differences while Fig. 25 illustrates the configurations.

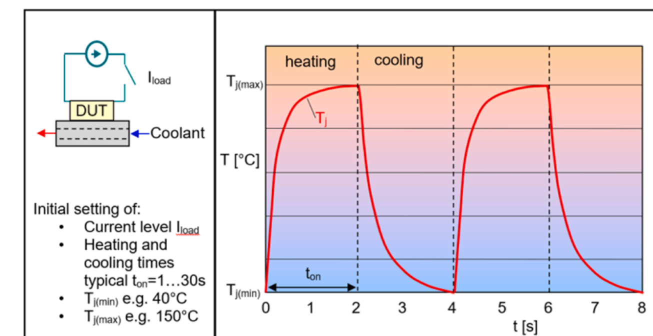


Fig. 24. *Configuration of the power cycle test and applied temperature profile [96].*

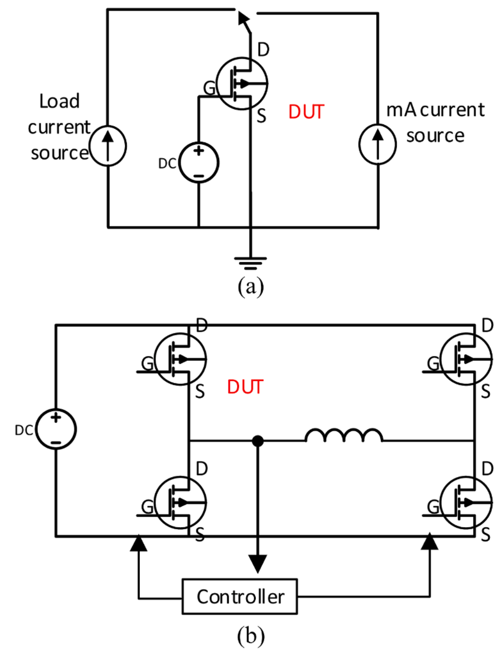


Fig. 25. *Configurations of the power cycle test (a) Conventional DC test (b) AC test.*

7.4. Other tests

These tests are currently not included in standard product qualification procedures, nor are they referenced in the IEC standard. A possible reason is that the test conditions remain under debate, given the rapid evolution of new chip generations. While the guideline was originally developed for power modules in electric vehicles, such tests are increasingly being adopted for qualifying power modules in industrial applications. Another reason is that the previously mentioned tests are well matured for Silicon devices however with the emerging of SiC devices and due to the significantly higher switching speed, there is a growing need to introduce dynamic reliability tests.

7.4.1. Dynamic reverse bias (DRB)

The MOSFET is exposed to a high dv/dt stress (equal or higher than 50 V/ns) between drain and source at room temperature. Stress can be applied through active switching or an external pulsed voltage source. The device carries no load current; only capacitive current flows to charge and discharge output capacitance C_{oss}. To avoid self-heating, the switching frequency is kept relatively low (25 kHz up to 1000 kHz as per AQG [93]). The objective is to confirm that trapped charges do not induce V_{th} drift or $R_{ds(on)}$ increase [96]. An alternative approach is the dynamic HV-H^3TRB test.

7.4.2. Dynamic gate stress (DGS)

Here, the gate is cycled on and off at high frequency (25 kHz $\leq$ f $\leq$ 1000 kHz [93]) using the recommended negative and maximum positive gate voltages, with V_{ds} and load current kept at zero. The aim is to verify minimal V_{th} drift throughout the device's expected lifetime.

7.4.3. Dynamic high-humidity, high-temperature reverse bias (dyn. H3TRB)

Unlike the conventional H^3TRB, which applies static bias, the dynamic version introduces high switching activity to emulate real operating conditions. The test is performed at 85 °C and 85% relative humidity for 1000 h, with a drain–source voltage between 0.8 and 0.95 V_{DSS} and switching frequencies from 15 kHz to 25 kHz. During testing, rapid voltage transitions are applied with slew rates up to ±30 V/ns to assess insulation and passivation stability under dynamic bias and

humidity exposure [93]. The device can be tested either in active mode (the MOSFET switches itself, creating the dv/dt stress) or passive mode (external circuitry generates the alternating voltage for diodes or non-switching devices). A gate voltage of $V_{gs,on}$ and $V_{gs,off}$ is used, and the drain current is kept at zero ($I_{ds} = 0$ A) to isolate humidity degradation mechanisms. This test helps identify weaknesses in surface passivation, chip sealing, and edge termination under realistic dynamic electrical stress.

7.4.4. Reverse current pulse test

Bipolar degradation is cause due to Basal Plane dislocation which form in the substrate during crystal growth and further propagate in the *epi* layer. Under the electrical and thermal stress this BPD expand into stacking fault causing shift in $R_{ds(on)}$, V_{sd}, I_{dss} and in some cases V_{th}. When bipolar reverse current flows through the body diode, crystal defects and trapped charges may accumulate, raising forward voltage and accelerating device degradation. This effect is intensified under high current densities in the pn-junction. Although MOSFET channels normally conduct in reverse, during dead times in half-bridge operation the diode must carry current for ≈1 μs. To replicate this stress, high current pulses (equal to or above rated current) of 1 μs duration with ∼1% duty cycle are applied to the body diode while keeping the MOSFET switched off.

8. Summary of reliability indicators

After discussing the main degradation mechanisms at the gate oxide, body diode, and package levels, it is beneficial to consolidate the findings into a single overview. Table XIII summarizes the most relevant diagnostic indicators that have been reported for SiC MOSFETs, linking each to the corresponding failure site. The table highlights the relative sensitivity and diagnostic value of parameters such as threshold voltage shift, on-state resistance, leakage current, and forward voltage variations. While these indicators are widely adopted in reliability studies, it is important to note that their quantitative behaviour depends strongly on device technology, packaging, and stress conditions. Therefore, the information provided should be regarded as a comparative guideline for identifying suitable monitoring parameters, rather than as absolute thresholds.

Table XIII
Diagnostic Indicators for Reliability Assessment of SiC MOSFETs.

Failure Site	Representative Indicators	Diagnostic Value
Gate Oxide	- V_{th} shift	- high sensitivity, semi-linear change, widely used in lifetime monitoring
	- $R_{ds(on)}$	- moderate sensitivity, medium linearity, complementary indicator
	- I_{gss}	- low sensitivity, mainly visible near breakdown
	- g_m - Miller plateau voltage	- moderate indicators with acceptable linearity
	- Capacitances (C_{gs}, C_{gd}, etc.)	- secondary, nonlinear, strongly test-dependent
	- Switching delay times	- secondary, affected by circuit parasitics but reflect degradation
Body Diode	- Drain leakage current ($I_{d,leak}$)	- highly sensitive early-warning parameter
	- Forward voltage drop (V_f)	- medium sensitivity, useful for gradual degradation
	- Switching transients	- moderate indicator but system-depemdent
Package (Bond Wires & Solder)	- Bond wire resistance	- Bond wire resistance: moderate sensitivity, reflects fatigue and lift-off
	- Forward voltage variation	- indicative of interconnect degradation
	- Die-attach/solder resistance	- signals cracks/voids, though harder to measure directly in operation

9. Future directions and emerging technologies for SiC MOSFET reliability

This section highlights emerging approaches that go beyond incremental improvements, focusing on innovative gate oxide processes, advanced packaging schemes, AI-driven reliability modelling, and next-generation device architectures. Together, these developments represent the technological frontiers shaping the next era of SiC MOSFET reliability.

9.1. Innovations in gate oxide technology

Traditional thermal oxidation techniques and post-deposition annealing have shown diminishing returns in reducing interface trap densities, especially at the 4H-SiC/SiO_2 interface. To address this, Atomic Layer Deposition (ALD) has emerged as a promising alternative for achieving ultra-thin, conformal oxide films with precise control over stoichiometry and defect incorporation. Unlike conventional methods, ALD enables layer by layer growth, which reduces oxygen vacancies and provides superior uniformity across large-area wafers, essential for high voltage applications [118].

Looking beyond standard dielectrics, next-generation interface engineering strategies are exploring the use of 2D materials (such as hexagonal boron nitride or graphene oxide) as interfacial buffers between SiC and high-k oxides. These materials offer the potential to suppress interface states, reduce Coulomb scattering, and improve channel mobility, all without compromising thermal stability [119]. Furthermore, plasma enhanced ALD and digital nitridation techniques, which introduce nitrogen at sub-monolayer levels during growth, are being investigated to passivate carbon related interface defects more effectively than bulk NO annealing, while enabling compatibility with non-thermal process flows [120]. As device scaling continues and trench architectures become more common, these innovations in dielectric and interface formation will be key to achieving long-term threshold voltage stability in next generation SiC MOSFETs.

9.2. Advanced packaging technologies

While silver sintering and copper clip bonding have already demonstrated their value in enhancing thermal cycling performance, the next wave of SiC MOSFET packaging innovations is focused on multi-functional reliability, addressing not only thermal management, but also electrical performance, form factor, and system integration. One promising approach is double-sided cooling (DSC), which enables symmetrical heat dissipation through both the top and bottom of the die, significantly reducing peak junction temperatures and mechanical stress gradients. This is especially advantageous in high power SiC modules, where localised heating under high current density can trigger long-term failure modes [121]. Fig. 26 illustrates the baSiC architectures of conventional single-sided cooled (SSC) and DSC power modules. In the DSC structure, the top of the power device is re-metallised to allow soldering or sintering, enabling connection to an upper substrate through metal blocks. This configuration creates a second heat flow path from the device top, theoretically reducing the thermal resistance from junction to case ($R_{th,j-c}$) by up to 50%.

In parallel, parasitic inductance reduction has become a critical packaging objective, particularly for fast switching SiC devices. Techniques such as embedded die packaging, planar interconnects, and co-packaging with gate drivers are being explored to shorten interconnection paths, suppress voltage overshoot, and reduce Electromagnetic Interference (EMI) susceptibility in high-frequency applications [122]. Furthermore, 3D integration and power module miniaturisation are gaining traction, enabling compact, low-inductance layouts that are better suited for electrified vehicles and aerospace systems. Research also points toward the adoption of flexible substrates and additive manufacturing, which offer novel pathways for custom

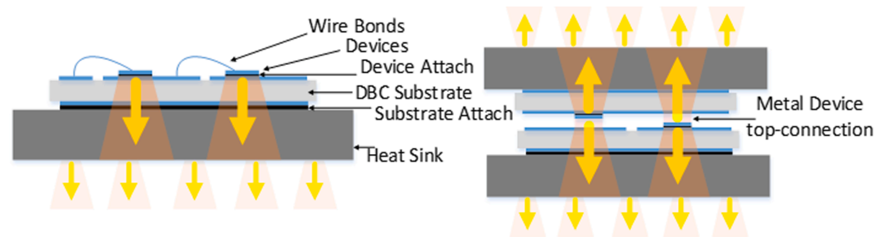


Fig. 26. *Conventional single-sided cooled (SSC, left) and novel double-sided cooled (DSC, right) power module architectures.*

thermal/electrical routing, mechanical stress buffering, and scalable assembly [123]. Collectively, these advancements represent a shift toward system-aware packaging, where electrical, thermal, and mechanical co-optimisation is essential for ensuring long-term SiC MOSFET reliability in mission-critical applications.

9.3. AI-Based reliability prediction models

As SiC MOSFETs continue to penetrate safety and mission-critical sectors such as automotive, aerospace, and grid infrastructure, the ability to predict device degradation in real-time is becoming increasingly essential [23]. Traditional reliability assessment methods, based on accelerated life testing and empirical models, are often time-consuming, device-specific, and limited in predictive power. In contrast, machine learning (ML) techniques offer a data driven framework for modelling complex degradation behaviours by analysing large datasets of operational and environmental parameters. Recent studies have shown that supervised algorithms such as Random Forests, Support Vector Machines (SVM), and Neural Networks can successfully correlate stress conditions (e.g., temperature, gate bias, duty cycle) with failure indicators like V_{th} drift or $R_{DS(on)}$ increase, enabling early fault detection and remaining useful life (RUL) estimation [124,125].

More advanced approaches are integrating real-time sensor data from embedded thermal, voltage, and current monitors with recurrent neural networks (RNNs) or Long Short-Term Memory (LSTM) models to capture temporal degradation trends. These models can support predictive maintenance strategies, where system level actions, such as derating or reconfiguration, are dynamically adjusted based on health indicators [126]. Additionally, AI is being used to classify failure modes, optimise gate driving schemes under varying stress conditions, and guide accelerated testing protocols, reducing experimental overhead. As part of the broader shift toward digital twins and smart power electronics, AI-enabled reliability frameworks promise to redefine how SiC device health is monitored and managed throughout their lifecycle.

9.4. Next generation SiC devices

The future of SiC power devices is being shaped by architectural innovations that aim to enhance performance, efficiency, and long-term reliability. One key advancement is the Superjunction (SJ) SiC MOSFET, which employs alternating p and n-type pillars to achieve ultra-low $R_{\mathrm{DS(on)}}$ at high voltages while minimising chip area. This enables higher current densities and switching efficiency but also introduces new challenges in voltage balancing and breakdown control, particularly under avalanche or surge conditions, where uniform electric field distribution becomes critical [127].

Further design evolution is seen in vertical JFETs and integrated Junction Barrier Schottky (JBS) structures, which combine high surge ruggedness with efficient reverse conduction, reducing system complexity and external component count [128]. In support of higher integration and reduced parasitics, Schottky Barrier Diodes (SBDs), previously discussed for their role in mitigating body diode limitations, are now being explored in monolithically integrated configurations. These efforts aim to simplify packaging, minimise inductive losses, and improve reverse recovery behaviour in compact power modules, especially for high-speed and automotive applications.

10. Conclusion

SiC MOSFETs offer transformative benefits in efficiency, high temperature performance, and compact design, but also present distinct reliability challenges unlike those in silicon devices. This review analysed dominant failure mechanisms such as gate oxide degradation, short circuit and avalanche breakdown, packaging stress, and body diode instability under various electrical, thermal, and mechanical stresses. Key degradation pathways such as trap-assisted tunnelling, parasitic BJT activation, bond wire lift-off, and diode degradation were examined alongside mitigation approaches including interface nitridation, termination engineering, mobility enhancement, silver sintering, and hybrid topologies. Experimental results from SCWT testing, UIS characterization, and BD evaluation are presented to illustrate how modern SiC MOSFETs behave under critical stress events and to validate several of the reliability concerns highlighted in the literature. In addition to failure mechanisms, this paper consolidated the wide range of reliability tests applied to SiC MOSFETs and summarized the most relevant diagnostic indicators at device, package, and system levels, highlighting their relative sensitivity and linearity as health monitoring metrics. Finally, forward-looking strategies were discussed, emphasizing progress in gate dielectric engineering, advanced packaging methods, AI-assisted reliability prediction, and next generation device structures. Together, these insights provide a comprehensive framework for advancing the robustness and durability of SiC MOSFETs and guiding future research in their long-term reliability.

CRediT authorship contribution statement

Ahmed Abdelaleem: Conceptualization, Data curation, Formal analysis, Investigation, Methodology, Validation, Visualization, Writing – original draft, Writing – review & editing. **Mohammad Monfared:** Funding acquisition, Supervision, Writing – review & editing. **Mike Jennings:** Funding acquisition, Supervision, Writing – review & editing. **Saeed Jahdi:** Supervision, Writing – review & editing. **Mohammed Amer Karout:** Supervision, Writing – review & editing. **Barry Nel:** Writing – review & editing. **Jon Evans:** Writing – review & editing. **Craig A. Fisher:** Writing – review & editing.

Conflict of interest

There are no conflicts of interest to report.

Data availability

Data will be made available on request.

References

[1] B. Baliga, Fundamentals of Power Semiconductor Devices2 ,nd Edition, Springer, 2018.

[2] M.F. Yaakub, M.A.M. Radzi, F.H.M. Noh, M. Azri, Silicon carbide power device characteristics, applications and challenges: an overview, Int. J. Power Electr. Drive Syst. 11 (4) (Dec. 2020) 2194–2202, https://doi.org/10.11591/ijpeds.v11.i4.pp2194-2202.
[3] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, J. Rebollo, A survey of wide bandgap power semiconductor devices, IEEe Trans. Power. Electron. 29 (5) (May 2014) 2155–2163, https://doi.org/10.1109/TPEL.2013.2268900.
[4] C. Langpoklakpam et al., "Review of Silicon carbide processing for power MOSFET," Feb. 01, 2022, MDPI. doi: 10.3390/cryst12020245.
[5] J. Rąbkowski, D. Peftitsis, H.P. Nee, Silicon carbide power transistors: a new era in power electronics is initiated, IEEE Indus. Electr. Mag. 6 (2) (2012) 17–26, https://doi.org/10.1109/MIE.2012.2193291.
[6] N. Hinov, Smart energy systems based on next-generation power electronic devices, Technologies 12 (6) (Jun. 2024), https://doi.org/10.3390/technologies12060078.
[7] Q. Yan, X. Yuan, Y. Geng, A. Charalambous, X. Wu, Performance evaluation of split output converters with SiC MOSFETs and SiC Schottky diodes, IEEe Trans. Power. Electron. 32 (1) (2016) 406–422.
[8] A. León-MaSiCh, H. Valderrama-Blavi, J.M. Bosque-Moncusí, L. Martínez-Salamero, Efficiency comparison between Si and SiC-based implementations in a high gain DC–DC boost converter, IET Power Electr. 8 (6) (2015) 869–878.
[9] H. Wang, M. Liserre, F. Blaabjerg, Toward reliable power electronics: challenges, design tools, and opportunities, IEEE Indus. Electr. Mag. 7 (2) (2013) 17–26, https://doi.org/10.1109/MIE.2013.2252958.
[10] R. Yu, et al., Measurements and review of failure mechanisms and reliability constraints of 4H-SiC power MOSFETs under short circuit events, IEEE Trans. Device Mater. Reliab. 23 (4) (2023) 544–563.
[11] L. Ceccarelli, P.D. Reigosa, F. Iannuzzo, F. Blaabjerg, A survey of SiC power MOSFETs short-circuit robustness and failure mode analysis, Microelectr. Reliab. 76 (2017) 272–276.
[12] A. Abuelnaga, M. Narimani, A.S. Bahman, Power electronic converter reliability and prognosis review focusing on power switch module failures, J. Power Electr. 21 (6) (2021) 865–880.
[13] E. Agirrezabala, I. Aizpuru, D. Garrido, A. Portillo, Reliability of power semiconductor modules: a State-of-the-art review, IEEe Open. J. Power. Electron. (2025).
[14] Infineon Technology AG, "Understanding the importance of power system reliability modelings," 2024.
[15] Y. Li, et al., State-of-the-art medium- and high-voltage silicon carbide power modules, challenges and mitigation techniques: a review, IEEe Trans. Compon. PackAging Manuf. Technol. (2024), https://doi.org/10.1109/TCPMT.2024.3391653.
[16] X. Deng, et al., Investigation of failure mechanisms of 1200 V rated trench SiC MOSFETs under repetitive avalanche stress, IEEe Trans. Power. Electron. 37 (9) (Sep. 2022) 10562–10571, https://doi.org/10.1109/TPEL.2022.3163930.
[17] R. Tambone, A. Ferrara, R. Siemieniec, A. Wood, F. Magrini, R.J.E. Hueting, Ruggedness of silicon power MOSFETs - part I: cell structure design related failure: a review, IEEe Trans. Electron. Devices 71 (6) (Jun. 2024) 3445–3457, https://doi.org/10.1109/TED.2024.3394452.
[18] H.C. Cheng, C.W. Hsu, Solder die attach lifetime characterization of SOT-227 power MOSFET module in a 3-phase inverter under power cycling, J. Mech. 39 (2023) 518–528, https://doi.org/10.1093/jom/ufad043.
[19] Y. Zhong, X. He, Z. Wang, J. Luo, B. Wang, Q. Li, Review of HTRB and HTGB reliability of SiC MOSFETs, in: 2024 7th International Conference on Energy, Electrical and Power Engineering, CEEPE 2024, Institute of Electrical and Electronics Engineers Inc., 2024, pp. 1161–1168, https://doi.org/10.1109/CEEPE62022.2024.10586507.
[20] T.T. Nguyen, A. Ahmed, T.V. Thang, J.H. Park, Gate oxide reliability issues of SiC MOSFETs under short-circuit operation, IEEe Trans. Power. Electron. 30 (5) (May 2015) 2445–2455, https://doi.org/10.1109/TPEL.2014.2353417.
[21] T. Aichinger, G. Rescher, G. Pobegen, Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs, Microelectr. Reliab. 80 (Jan. 2018) 68–78, https://doi.org/10.1016/j.microrel.2017.11.020.
[22] A. Fayyaz, G. Romano, A. Castellazzi, Body diode reliability investigation of SiC power MOSFETs, Microelectr. Reliab. 64 (Sep. 2016) 530–534, https://doi.org/10.1016/j.microrel.2016.07.044.
[23] S. Rahimpour, H. Tarzamni, N.V. Kurdkandi, O. Husev, D. Vinnikov, F. Tahami, An Overview of Lifetime Management of Power Electronic Converters, Institute of Electrical and Electronics Engineers Inc, 2022, https://doi.org/10.1109/ACCESS.2022.3214320.
[24] R. Siemieniec, et al., A SiC trench MOSFET concept offering improved channel mobility and high reliability, in: 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe), IEEE, 2017. P-1.
[25] J. Wei, et al., Review on the reliability mechanisms of SiC power MOSFETs: a comparison between planar-gate and trench-gate structures, IEEe Trans. Power. Electron. 38 (7) (Jul. 2023) 8990–9005, https://doi.org/10.1109/TPEL.2023.3265864.
[26] L. Shi, et al., Gate oxide reliability in silicon carbide planar and trench metal-oxide-semiconductor field-effect transistors under positive and negative electric field stress, Electronics 13 (22) (Nov. 2024), https://doi.org/10.3390/electronics13224516.
[27] A. Kumar et al., "Wide band gap devices and their application in power electronics," Dec. 01, 2022, MDPI. doi: 10.3390/en15239172.
[28] T. Kimoto, J.A. Cooper, Fundamentals of Silicon Carbide technology: growth, characterization, Devices and Applications, John Wiley & Sons, 2014.
[29] B.J. Baliga, Silicon Carbide Power Devices, World scientific, 2005.
[30] M. Kang, et al., Body diode reliability of commercial SiC power MOSFETs, in: 2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), IEEE, 2019, pp. 416–419.
[31] J. Li, A. Shekhar, W.D. Van Driel, G. Zhang, A review on gate oxide failure mechanisms of silicon carbide semiconductor devices, IEEe Trans. Electron. Devices (2024), https://doi.org/10.1109/TED.2024.3482252.
[32] D.K. Ngwashi and L.V. Phung, "Recent review on failures in silicon carbide power MOSFETs," Aug. 01, 2021, Elsevier Ltd. doi: 10.1016/j.microrel.2021.114169.
[33] L. Wu, et al., An approach for extracting the SiC/SiO2 SiC MOSFET interface trap distribution and study during short circuit, Mater. Sci. Semicond. Process. 163 (Aug. 2023), https://doi.org/10.1016/j.mssp.2023.107581.
[34] Y.J. Kim, R.H. Baek, S.K. Chang, K.K. Choi, Effect of hydrogen plasma treatment on the electrical properties for SiC-based power MOSFETs, Microelectron. Eng. 258 (Apr. 2022), https://doi.org/10.1016/j.mee.2022.111769.
[35] G.R. Selesen and A.-9371 Brückl, "Behavior of SiC-MOSFETs under temperature and voltage stress." [Online]. Available: http://www.ub.tuwien.ac.athttp://www.ub.tuwien.ac.at/eng.
[36] G. Wang, L. Yuan, X. Wang, Y. Zhang, R. Jia, High temperature reliability and performance evaluation of 1200 V SiC MOSFETs, J. Cryst. Growth 606 (Mar. 2023), https://doi.org/10.1016/j.jcrysgro.2023.127086.
[37] Y. Yang, Y. Wen, Y. Gao, A novel active gate driver for improving switching performance of high-power SiC MOSFET modules, IEEe Trans. Power. Electron. 34 (8) (Aug. 2019) 7775–7787, https://doi.org/10.1109/TPEL.2018.2878779.
[38] K. Puschkarsky, T. Grasser, T. Aichinger, W. Gustin, H. Reisinger, Review on SiC MOSFETs high-voltage device reliability focusing on threshold voltage instability, IEEe Trans. Electron. Devices 66 (11) (Nov. 2019) 4604–4616, https://doi.org/10.1109/TED.2019.2938262.
[39] T. Watanabe, Y. Fukui, S. Hino, S. Tomohisa, N. Miura, K. Nishikawa, Categorization of PBTI mechanisms on 4H-SiC MOSFETs by the stress gate voltage and channel plane orientation, IEEE Trans. Device Mater. Reliab. 23 (1) (Mar. 2023) 99–108, https://doi.org/10.1109/TDMR.2023.3234979.
[40] J.A.O. Gonzalez, O. Alatise, A novel non-intrusive technique for BTI characterization in SiC MOSFETs, IEEe Trans. Power. Electron. 34 (6) (Jun. 2019) 5737–5747, https://doi.org/10.1109/TPEL.2018.2870067.
[41] L. Shi, et al., Investigation of different screening methods on threshold voltage and gate oxide lifetime of SiC Power MOSFETs, in: IEEE International Reliability PhySiCs Symposium Proceedings, Institute of Electrical and Electronics Engineers Inc., 2023, https://doi.org/10.1109/IRPS48203.2023.10118276.
[42] T. Liu, S. Zhu, M.H. White, A. Salemi, D. Sheridan, A.K. Agarwal, Time-dependent dielectric breakdown of commercial 1.2 kV 4H-SiC power MOSFETs, IEEE J. Electron Devices Soc. 9 (2021) 633–639, https://doi.org/10.1109/JEDS.2021.3091898.
[43] M.K. Das, Recent advances in (0001) 4H-SiC MOS device technology, in: Materials Science Forum, Trans Tech Publications Ltd, 2004, pp. 1275–1280, https://doi.org/10.4028/www.scientific.net/msf.457-460.1275.
[44] A. Siddiqui, R.Y. Khosa, and M. Usman, "High-kdielectrics for 4H-silicon carbide: present status and future perspectives," Apr. 21, 2021, Royal Society of Chemistry. doi: 10.1039/d0tc05008c.
[45] G.L. Rodal, D. Peftitsis, Gate-drive circuits for adaptive operation of SiC MOSFETs, IEEe Trans. Power. Electron. 39 (7) (Jul. 2024) 8162–8186, https://doi.org/10.1109/TPEL.2024.3382335.
[46] T. Kimoto and H. Watanabe, "Defect engineering in SiC technology for high-voltage power devices," Dec. 01, 2020, IOP Publishing Ltd. doi: 10.35848/1882-0786/abc787.
[47] O. Avino-Salvado, et al., PhySiCs-based strategies for fast TDDB testing and lifetime estimation in SiC power MOSFETs, IEEE Trans. Indus. Electr. 71 (5) (May 2024) 5285–5295, https://doi.org/10.1109/TIE.2023.3281705.
[48] U. Chand, et al., High-K gate dielectric for High-performance SiC power MOSFET technology with low interface trap density, good oxide lifetime (ttddb≥ 104s), and High thermal stability (≥ 800°C), Solid State Phenomena 359 (Aug. 2024) 217–221, https://doi.org/10.4028/p-a6qptx.
[49] W.C. Lin, et al., Investigation of the time dependent gate dielectric stability in SiC MOSFETs with planar and trench gate structures, Microelectr. Reliab. 150 (Nov. 2023), https://doi.org/10.1016/j.microrel.2023.115141.
[50] X. Hou, et al., High-temperature time-dependent dielectric breakdown of 4H-SiC MOS capacitors, Case Stud. Therm. Eng. 63 (Nov. 2024), https://doi.org/10.1016/j.csite.2024.105371.
[51] P. Samanta, K.C. Mandal, Leakage current conduction, hole injection, and time-dependent dielectric breakdown of n-4H-SiC MOS capacitors during positive bias temperature stress, J. Appl. Phys. 121 (3) (2017).
[52] K. Matocha, G. Dunne, S. Soloviev, R. Beaupre, Time-dependent dielectric breakdown of 4H-SiC MOS capacitors and DMOSFETs, IEEe Trans. Electron. Devices 55 (8) (2008) 1830–1834, https://doi.org/10.1109/TED.2008.926595.
[53] J. Qian, et al., Investigation of the electron trapping in commercial thick silicon dioxides thermally grown on 4H-SiC under the constant current stress, in: IEEE International Reliability PhySiCs Symposium Proceedings, Institute of Electrical and Electronics Engineers Inc., 2024, https://doi.org/10.1109/IRPS48228.2024.10529389.
[54] J.W. McPherson, J. Kim, A. Shanware, H. Mogul, J. Rodriguez, Trends in the ultimate breakdown strength of high dielectric-constant materials, IEEe Trans. Electron. Devices 50 (8) (Aug. 2003) 1771–1778, https://doi.org/10.1109/TED.2003.815141.
[55] Z. Wang, Z. Zhang, C. Shao, J. Robertson, S. Liu, Y. Guo, Defects and passivation mechanism of the suboxide layers at SiO/4H-SiC (0001) interface: a first-principles calculation, IEEe Trans. Electron. Devices 68 (1) (Jan. 2021) 288–293, https://doi.org/10.1109/TED.2020.3039480.

[56] G. Lyu, H. Ali, H. Tan, L. Peng, X. Ding, Review on short-circuit protection methods for SiC MOSFETs, in: Multidisciplinary Digital Publishing Institute (MDPI), Sep. 01, 2024, https://doi.org/10.3390/en17174523.
[57] G. Romano, et al., A comprehensive study of short-circuit ruggedness of silicon carbide power MOSFETs, IEEe J. Emerg. Sel. Top. Power. Electron. 4 (3) (Sep. 2016) 978–987, https://doi.org/10.1109/JESTPE.2016.2563220.
[58] L. Ceccarelli, P.D. Reigosa, F. Iannuzzo, F. Blaabjerg, A survey of SiC power MOSFETs short-circuit robustness and failure mode analysis, Microelectr. Reliab. 76–77 (Sep. 2017) 272–276, https://doi.org/10.1016/j.microrel.2017.06.093.
[59] Rich Quinnell, "Short-Circuit Ruggedness in SiC MOSFETs," SemiEngineering.
[60] J. Zhang, Z. Guo, Y. Jiang, G. Tan, Active gate drive for short-circuit current suppression of SiC MOSFET in hard switching fault. Frontier Academic Forum of Electrical Engineering, Springer, 2022, pp. 249–257.
[61] M. Nawaz, Evaluation of SiC MOSFET power modules under unclamped inductive switching test environment, Microelectr. Reliab. 63 (Aug. 2016) 97–103, https://doi.org/10.1016/j.microrel.2016.05.011.
[62] M.S. Jang, J.H. Jeong, H.J. Lee, Analysis of ruggedness of 4H-SiC power MOSFETs with various doping parameters, Appl. Sci. 13 (1) (Jan. 2023), https://doi.org/10.3390/app13010427.
[63] A. Fayyaz, et al., A comprehensive study on the avalanche breakdown robustness of silicon carbide power MOSFETs, Energies 10 (4) (Apr. 2017), https://doi.org/10.3390/en10040452.
[64] X. Deng, et al., Investigation of failure mechanisms of 1200 V rated trench SiC MOSFETs under repetitive avalanche stress, IEEe Trans. Power. Electron. 37 (9) (Sep. 2022) 10562–10571, https://doi.org/10.1109/TPEL.2022.3163930.
[65] H. Luo, et al., Characteristics and avalanche investigation of SiC VDMOSFETs with enhanced P-based implantation, Microelectr. Reliab. 160 (Sep. 2024), https://doi.org/10.1016/j.microrel.2024.115451.
[66] Z. Bai, et al., Investigation on single pulse avalanche failure of 1200-V SiC MOSFETs via optimized thermoelectric simulation, IEEe Trans. Electron. Devices 68 (3) (Mar. 2021) 1168–1175, https://doi.org/10.1109/TED.2020.3048921.
[67] C. Ionita, M. Nawaz, K. Ilves, On the short-circuit and avalanche ruggedness reliability assessment of SiC MOSFET modules, Microelectr. Reliab. 71 (Apr. 2017) 6–16, https://doi.org/10.1016/j.microrel.2017.02.004.
[68] J. Lu, et al., Impact of varied buffer layer designs on single-event response of 1.2-kV SiC power MOSFETs, IEEe Trans. Electron. Devices 67 (9) (Sep. 2020) 3698–3704, https://doi.org/10.1109/TED.2020.3008398.
[69] Y. Wang, et al., Single-event burnout hardness for the 4H-SiC trench-gate MOSFETs based on the multi-island buffer layer, IEEe Trans. Electron. Devices 66 (10) (Oct. 2019) 4264–4272, https://doi.org/10.1109/TED.2019.2933026.
[70] M. Hosseinzadehlish, S. Jahdi, X. Yuan, J. Ortiz-Gonzalez, O. Alatise, High-energy dynamic avalanche to failure by incremental source-voltage increase in symmetric double-trench & asymmetric trench SiC MOSFETs, IEEE Open J. Indus. Appl. 5 (2024) 235–252, https://doi.org/10.1109/OJIA.2024.3409153.
[71] Y. Huang, Y. Jia, Y. Luo, F. Xiao, B. Liu, Lifting-off of Al bonding wires in IGBT modules under power cycling: failure mechanism and lifetime model, IEEe J. Emerg. Sel. Top. Power. Electron. 8 (3) (Sep. 2020) 3162–3173, https://doi.org/10.1109/JESTPE.2019.2924241.
[72] F. Karakaya, A. Maheshwari, A. Banerjee, J.S. Donnal, A.J. Morgan, W. Sung, Situ detection of bond wire lift-off events in operational SiC MOSFETs, IEEe Trans. Power. Electron. (2024), https://doi.org/10.1109/TPEL.2024.3446750.
[73] T. Huang, B.P. Singh, Y. Liu, S. Norrga, Failure characterization of discrete SiC MOSFETs under forward power cycling test, Energies 17 (11) (Jun. 2024), https://doi.org/10.3390/en17112557.
[74] L. Xie et al., "State-of-the-art of the bond wire failure mechanism and power cycling lifetime in power electronics," Aug. 01, 2023, Elsevier Ltd. doi: 10.1016/j.microrel.2023.115060.
[75] M. Yun, M. Cai, D. Yang, Y. Yang, J. Xiao, G. Zhang, Bond wire damage detection method on discrete MOSFETs based on two-port network measurement, Micromachines 13 (7) (Jul. 2022), https://doi.org/10.3390/mi13071075.
[76] C. Durand, M. Klingler, M. Bigerelle, D. Coutellier, Solder fatigue failures in a new designed power module under Power Cycling, Microelectr. Reliab. 66 (Nov. 2016) 122–133, https://doi.org/10.1016/j.microrel.2016.10.002.
[77] Y.C. Jang, H.E. Kim, A. Schuck, Y.S. Kim, Developed non-destructive verification methods for accelerated temperature cycling of power MOSFETs, Microelectr. Reliab. 128 (Jan. 2022), https://doi.org/10.1016/j.microrel.2021.114442.
[78] Y.H. Mei, Z. Wang, K.S. Siow, Reliability and failure mechanisms of sintered silver as die attach joint, Die-Attach Mater. High Temperature Appl. Microelectr. Packag. (2019) 125–150.
[79] P. Wu, et al., Investigation on the electrical-thermal-mechanical performance of multi-chip SiC power device with Cu clip interconnect, IEEe J. Emerg. Sel. Top. Power. Electron. (2025), https://doi.org/10.1109/JESTPE.2025.3544806.
[80] C. Ding, H. Liu, K.D.T. Ngo, R. Burgos, G.Q. Lu, A double-side cooled SiC MOSFET power module with sintered-silver interposers: I-design, simulation, fabrication, and performance characterization, IEEe Trans. Power. Electron. 36 (10) (Oct. 2021) 11672–11680, https://doi.org/10.1109/TPEL.2021.3070326.
[81] K. Peng, S. Eskandari, E. Santi, Characterization and modeling of SiC MOSFET body diode, in: 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), IEEE, 2016, pp. 2127–2135.
[82] A. Fayyaz, G. Romano, A. Castellazzi, Body diode reliability investigation of SiC power MOSFETs, Microelectr. Reliab. 64 (Sep. 2016) 530–534, https://doi.org/10.1016/j.microrel.2016.07.044.
[83] M.R. Ahmed, R. Todd, A.J. Forsyth, Switching performance of a SiC MOSFET body diode and SiC schottky diodes at different temperatures, in: 2017 IEEE Energy Conversion Congress and Exposition (ECCE), IEEE, 2017, pp. 5487–5494.
[84] D. Ma, et al., Degradation evaluation and defects analysis for 1.2-kV planar-gate SiC MOSFETs under repetitive surge current stress, IEEe Trans. Electron. Devices 70 (12) (Dec. 2023) 6473–6479, https://doi.org/10.1109/TED.2023.3323912.
[85] X. Jiang, et al., Investigation on degradation of SiC MOSFET under surge current stress of body diode, IEEe J. Emerg. Sel. Top. Power. Electron. 8 (1) (Mar. 2020) 877–892, https://doi.org/10.1109/JESTPE.2019.2952214.
[86] D. Nayak, M. Kumar, S. Pramanick, Analysis of switching loss reduction of SiC MOSFET in presence of antiparallel SiC schottky diode, in: 2020 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE2020), IEEE, 2020, pp. 1–6.
[87] Infineon Technologies AG, "CoolSiCTM 750 V G2 Industrial MOSFET," Munich, Germany, 2025.
[88] L. Liu, J. Wang, J. Li, N. Ren, Q. Guo, K. Sheng, Monolithic integration of SiC lateral MOSFET with lateral schottky diode for power converters, in: Proceedings of the International Symposium on Power Semiconductor Devices and ICs, Institute of Electrical and Electronics Engineers Inc., 2024, pp. 112–115, https://doi.org/10.1109/ISPSD59661.2024.10579640.
[89] M.A. Karout, M. Taha, C.A. Fisher, A. Deb, P. Mawby, O. Alatise, Impact of diode characteristics on 1.2 kV SiC MOSFET and cascode JFET efficiency: body diodes vs SiC Schottky barrier diodes, in: Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC, Institute of Electrical and Electronics Engineers Inc., 2023, pp. 202–208, https://doi.org/10.1109/APEC43580.2023.10131399.
[90] M.A. Karout, et al., Impact of gate turn-off voltage on body diode degradation of the latest generation SiC MOSFET, in: PCIM Europe Conference Proceedings, Mesago PCIM GmbH, 2025, pp. 1562–1568, https://doi.org/10.30420/566541204.
[91] "JEDEC Publication No. 194: guideline for gate oxide reliability and robustness evaluation procedures for Silicon carbide power MOSFETs, JEP 194, JEDEC Solid State Technology Association," 2023.
[92] IEC 60749-5:2023, "Semiconductor devices - mechanical and climatic test methods - part 5: steady-state temperature humidity bias life test," 2023, Accessed: Aug. 23, 2025. [Online]. Available: https://webstore.iec.ch/en/publication/77333.
[93] ECPE, "ECPE guideline AQG 324 qualification of power modules for use in power electronics converter units in motor vehicles," Mar. 2025. Accessed: Aug. 23, 2025. [Online]. Available: https://www.ecpe.org/index.php?eID=dumpFile&t=f&f=46275&token=0d6454cead46e7321e58907672861b3fcd13c0c0.
[94] AEC, "AEC-Q101 Failure mechanism based Stress Test qualification for discrete semiconductors in automotive applications," 2021, accessed: Aug. 23, 2025. [Online]. Available: http://www.aecouncil.com/Documents/AEC_Q101_Rev_E_Base_Document.pdf.
[95] JEDEC STANDARD, "JESD22-A104D Temperature Cycling," 2009. Accessed: Aug. 26, 2025. [Online]. Available: https://www.jedec.org/sites/default/files/docs/22a104d.pdf.
[96] W. Arendt, I. Ulrich, N.A. Gießmann, and S. Berberich, "A P P L I C A T I O N M A N U A L power semiconductors." accessed: Aug. 23, 2025. [Online]. Available: https://assets.danfoss.com/documents/latest/524715/AB509142199100en-000204.pdf.
[97] IEC, "IEC 60747-8 SEMICONDUCTOR DEVICES – DISCRETE DEVICES – Part 8: field-effect transistors," 2010. Accessed: Aug. 26, 2025. [Online]. Available: https://cdn.standards.iteh.ai/samples/13675/b540e8f1ee604d07abb0444138e24ce4/IEC-60747-8-2010.pdf.
[98] IEC, "IEC 60749-23 SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –," 2011. Accessed: Aug. 26, 2025. [Online]. Available: https://cdn.standards.iteh.ai/samples/19158/6ae972c851c84af7b75027b3d5d04a1a/IEC-60749-23-2004-AMD1-2011-CSV.pdf.
[99] JEDEC STANDARD, "JESD22-A108D Temperature, bias, and operating life," 2010. Accessed: Aug. 26, 2025. [Online]. Available: https://www.jedec.org/sites/default/files/docs/22A108D.pdf.
[100] IEC, "IEC 60068-2-67 ENVIRONMENTAL TESTING – Part 2-67: tests – Test cy: damp heat, steady state, accelerated test primarily intended for components," 2019. Accessed: Aug. 26, 2025. [Online]. Available: https://cdn.standards.iteh.ai/samples/802/f22802efd14c4fb7867d487c69e59e14/IEC-60068-2-67-1995.pdf.
[101] JEDEC STANDARD, "JESD22-A101C Steady State temperature humidity bias life test," 2009. Accessed: Aug. 26, 2025. [Online]. Available: https://www.jedec.org/sites/default/files/docs/22a101c.pdf.
[102] IEC, "IEC 60749-6 SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS – Part 6: storage at high temperature," 2017. Accessed: Aug. 26, 2025. [Online]. Available: https://cdn.standards.iteh.ai/samples/23473/bdf7015273724d98a6960daaa64c0baf/IEC-60749-6-2017.pdf.
[103] JEDEC STANDARD, "JESD22-A103D High temperature storage life," 2010. Accessed: Aug. 26, 2025. [Online]. Available: https://www.jedec.org/sites/default/files/docs/22a103D.pdf.
[104] JEDEC STANDARD, "JESD22-A119 Low temperature storage life," 2009. Accessed: Aug. 26, 2025. [Online]. Available: https://www.jedec.org/sites/default/files/docs/22a119_0.pdf.
[105] IEC, "IEC 60749-25 SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –," 2003. Accessed: Aug. 26, 2025. [Online]. Available: https://webstore.iec.ch/en/iec_catalog/product/preview/?id=L3B1Yi9wZGYvcHJldmlldy9pbmZvX2lIYzYwNzQ5LTI1e2VkMS4wfWIucGRm.
[106] IEC, "IEC 60068-2-6 ENVIRONMENTAL TESTING – Part 2: tests – Test fc: vibration (sinusoidal)," 2007. Accessed: Aug. 26, 2025. [Online]. Available: https://cdn.standards.iteh.ai/samples/12766/f934b36191724c11afab910c07fc347a/IEC-60068-2-6-2007.pdf.

[107] JEDEC STANDARD, "JESD22-B103B Vibration, variable frequency," 2006. Accessed: Aug. 26, 2025. [Online]. Available: https://www.jedec.org/sites/default/files/docs/22b103b.pdf.
[108] IEC, "IEC 60068-2-27 ENVIRONMENTAL TESTING – Part 2-27: tests – Test ea and guidance: shock," 2008. Accessed: Aug. 26, 2025. [Online]. Available: https://cdn.standards.iteh.ai/samples/12767/43b88e20f96940079f7665a7e90abc02/IEC-60068-2-27-2008.pdf.
[109] JEDEC STANDARD, "JESD22-B104C Mechanical shock," 2009. Accessed: Aug. 26, 2025. [Online]. Available: https://www.jedec.org/sites/default/files/docs/22b104C_0.pdf.
[110] IEC, "IEC 60749-34 SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS – Part 34: power cycling," 2010. Accessed: Aug. 26, 2025. [Online]. Available: https://cdn.standards.iteh.ai/samples/17530/b92992f6a179418fa8cee3d09d1b7548/IEC-60749-34-2010.pdf.
[111] JEDEC STANDARD, "JESD22-A122 Power Cycling," 2007. Accessed: Aug. 26, 2025. [Online]. Available: https://www.jedec.org/sites/default/files/docs/22A122.pdf.
[112] Y. Zhong, X. He, Z. Wang, J. Luo, B. Wang, Q. Li, Review of HTRB and HTGB reliability of SiC MOSFETs, in: 2024 7th International Conference on Energy, Electrical and Power Engineering (CEEPE), IEEE, 2024, pp. 1161–1168.
[113] Keithley, "V DS ramp and HTRB reliability testing of high power semiconductor devices with automated characterization suite (ACS) software." accessed: Aug. 24, 2025. [Online]. Available: https://www.tek.com/en/documents/application-note/vds-ramp-and-htrb-reliability-testing-high-power-semiconductor-devices.
[114] L. Yang, A. Castellazzi, High temperature gate-bias and reverse-bias tests on SiC MOSFETs, Microelectr. Reliab. 53 (9–11) (2013) 1771–1773.
[115] T.N. Wassermann, F. Holley, P. Salmen, Reliability of a 3.3 kV SiC MOSFET.XT, in: IEEE International Reliability PhySiCs Symposium Proceedings, Institute of Electrical and Electronics Engineers Inc., 2025, https://doi.org/10.1109/IRPS48204.2025.10982931.
[116] A. Ibrahim, J.P. Ousten, R. Lallemand, Z. Khatir, Power cycling issues and challenges of SiC-MOSFET power modules in high temperature conditions, Microelectr. Reliab. 58 (Mar. 2016) 204–210, https://doi.org/10.1016/j.microrel.2015.11.030.
[117] F. Yang, E. Ugur, B. Akin, Design methodology of DC power cycling test setup for SiC MOSFETs, IEEe J. Emerg. Sel. Top. Power. Electron. 8 (4) (Dec. 2020) 4144–4159, https://doi.org/10.1109/JESTPE.2019.2914419.
[118] Q. Huang, et al., Study of ZrO2 gate dielectric with thin SiO2 interfacial layer in 4H-SiC trench MOS capacitors, Materials 18 (8) (Apr. 2025), https://doi.org/10.3390/ma18081741.
[119] H. Elshafie, A. Alavudeen Basha, A.S. Alqahtani, A. Mubarakali, P. Parthasarathy, M. Venkatesh, Performance optimization of high-κ engineered TM-DG-InP/GaAs-TFET for ultra-sensitive biosensing applications: mechanistic insights and TCAD simulation analysis, ECS J. Solid State Sci. Technol. 14 (5) (May 2025) 057002, https://doi.org/10.1149/2162-8777/add49b.
[120] Y.-D. Guo, A.-F. Wang, Q.-M. Huang, Z.-Y. Wang, H.-P. Ma, Q.-C. Zhang, Performance comparison of Al 2 O 3 gate dielectric grown on 4H-SiC substrates via thermal and plasma-enhanced atomic layer deposition methods, ECS J. Solid State Sci. Technol. 14 (2) (Feb. 2025) 023005, https://doi.org/10.1149/2162-8777/adaee9.
[121] R. Paul, R. Alizadeh, X. Li, H. Chen, Y. Wang, H.A. Mantooth, A double-sided cooled SiC MOSFET power module for EV inverters, IEEe Trans. Power. Electron. 39 (9) (2024) 11047–11059, https://doi.org/10.1109/TPEL.2024.3397679.
[122] Y. Li, et al., State-of-the-art medium- and high-voltage silicon carbide power modules, challenges and mitigation techniques: a review, IEEe Trans. Compon. PackAging Manuf. Technol. (2024), https://doi.org/10.1109/TCPMT.2024.3391653.
[123] S. Akbari, et al., Ceramic additive manufacturing potential for power electronics packaging, IEEe Trans. Compon. PackAging Manuf. Technol. 12 (11) (Nov. 2022) 1857–1866, https://doi.org/10.1109/TCPMT.2022.3224921.
[124] K. Singh, S. Kalra, A machine learning based reliability analysis of negative bias temperature instability (NBTI) compliant design for ultra large scale digital integrated circuit, J. Integr. Circuits Syst. 18 (2) (2023) 1, https://doi.org/10.29292/jics.v18i2.
[125] M.M. Sezer, F. Akici, M. Afshar, B.T. Vankayalapati, B. Akin, Gate leakage current characterization and remaining useful lifetime prediction in silicon carbide MOSFETs, IEEE Trans. Transp. Electrif. (2025), https://doi.org/10.1109/TTE.2025.3546928.
[126] Y. Fassi, V. Heiries, J. Boutet, S. Boisseau, PhySiCs-informed machine learning for robust remaining useful life estimation of power MOSFETs, in: 2024 IEEE International Conference on Prognostics and Health Management (ICPHM), IEEE, 2024, pp. 399–406.
[127] E.O. Prado, P.C. Bolsi, H.C. Sartori, J.R. Pinheiro, An overview about Si, superjunction, SiC and GaN power MOSFET technologies in power electronics applications, Energies 15 (14) (Jul. 2022), https://doi.org/10.3390/en15145244.
[128] C.L. Hung, Y.K. Hsiao, J.N. Yao, H.C. Kuo, Well-balanced 4H-SiC JBSFET: integrating JBS diode and VDMOSFET characteristics for reliable 1700V applications, Solid. State Electron. 226 (Jun. 2025), https://doi.org/10.1016/j.sse.2025.109083.

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