β-Ga_2O_3 For Power Electronic Devices

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A dissertation submitted to Swansea University in accordance with the requirements of the degree of Doctor of Philosophy in the Faculty of Engineering.

Declarations

This work has not previously been accepted in substance for any degree and is not being concurrently submitted in candidature for any degree.

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This thesis is the result of my own investigations, except where otherwise stated. Other sources are acknowledged by footnotes giving explicit references. A bibliography is appended.

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ABSTRACT

This thesis explores the development of processes to realise β-Ga_2O_3-based devices, focusing on etching protocols, dielectric characterisation, and forming ohmic contacts.

This work started with developing a photoresist process to enable trench etching for bulk (001) β-Ga_2O_3 using SiN_x hard masks and dry etching. SiN_x was used as the hard mask due to it's selectivity to β-Ga_2O_3, and the ease of removal compared to metal masks such as Cr. A photoresist protocol for patterning was developed and tested on Si, α-Al_2O_3, and β-Ga_2O3. These processes are critical for isolating regions in devices like FinFETs and J-FETs, with SiNx demonstrated to be an effective hard mask.

The research continued with a study which characterises Al_2O_3 (ALD) and SiO_2 (PECVD) dielectrics on bulk (001) β-Ga_2O3 through MIS capacitor fabrication. The effects of prolonged post-metalisation annealing were investigated using CV measurements and the Terman method, this showed a reduction in the hysteresis and interface traps (D_{it}) after annealing at 200°C. ALD Al_2O_3 exhibited superior interface quality compared to PECVD SiO_2. TEM-EDX analysis revealed potential diffusion at the metal-dielectric interface. There was also an apparent decrease in film thickness after annealing.

The final experimental section examines ohmic contacts on β-Ga_2O_3 using Ti/Al, Ti/Au, Ti/Ag, and Ti/W metalisations. Ti/Au is the most common metal which is used as an ohmic contact, hence deemed to be the most reliable to use as the standard ohmic contact to β-Ga_2O_3. Ti/Ag had the lowest resistance, however, limited data to agree with this, and so need to be repeated with more reliable experiments.

This work lays the foundation for further work to form β-Ga_2O_3 devices. By investigating processes like etching, dielectric integration, and ohmic contact formation. Finally future work is outlined in the final Chapter, includes optimising material interfaces and refining measurement techniques.

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This is in no way exhaustive as I under no illusion that I will have forgotten someone. Such is life.

So long, thanks for all the fish.

DEFINITIONS

Table 1: The definitions of the different abbreviations which are used in this work.

Abbreviations	**Definitions**
TLM	Transfer Length Measurement, test structures.
CTLM	Circular Transfer Length Measurement, test structures.
MIS/MOS	Metal-Insulator-Semiconductor / Metal-Oxide-Semiconductor
FET	Field-Effect-Transistor
JFET	Junction-FET
MESFET	Metal-Effect Semiconductor-FET
FP	Field Plate
BJT	Bipolar Junction Transistor
SBD	Schottky Barrier Diode
CVD	Chemical Vapour Deposition.
PECVD	Plasma Enhance Chemical Vapour Deposition.
MVD	Molecular Vapour Deposition.
ALD	Atomic Layer Deposition.
LPCVD	Low Pressure Chemical Vapour Deposition.
RTA	Rapid Thermal Annealing
RIE	Reactive Ion Etching
PVD	Physical Vapour Deposition.
TEM	Trasmission Electron Microscopy.
SEM	Scanning Electron Microscopy.
XRD	X-Ray Diffraction.
IV	Voltage-Current measurement.
CV	Voltage Capacitance measurement.
t	Thickness of a insulator (Dielectric) Layer.
A	Contact Area Size.
W	Depletion Width.
r	Radius, of a circular contact.
ϵ_0	Permittivity of free space
ϵ_S	Relative permittivity of a semiconductor

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Abbreviations	Definitions
ϵ_I	Relative permittivity of a insulator (dielectric) layer
T	Boltzmann Constant
λ_{Th}	Thermal Conductivity
R	Ideal Gas Constant
ϕ_B	Barrier Height
ϕ_{MS}	metal-semiconductor work function
ϕ	Work function
χ	Electron affinity
E_{Vac}	Energy level of the vacuum.
E_{Val}	Energy level of the valence band.
E_{Con}	Energy level of the conduction band.
E_{Fer}	Fermi level.
E_g	band gap
WBG	Wide Band gap
UWBG	ultra-wide band gap
MIC	Metal Ion Containing
MIF	Metal Ion Free
TMA	Trimethylaluminium.
DI-Water	Deionised Water
IPA	Isopropanol
UV	Ultraviolet light
V_{Br}	Breakdown Voltage
V_{On}	On-state Voltage drop
R_{On}	On-state Resistance
FOM	Figure Of Merit.
PFOM	Power (Baligas) Figure Of Merit.
Q_F	Fixed charge
Q_O	Oxide charge
Q_M	Mobile charge
Q_{it}	Interface trapped charge
D_F	Density of fixed charge
D_O	Density of oxide charge
D_M	Density of mobile charge
D_{it}	Density of interface trapped charge
C_A	Accumulation capacitance
V_{FB}	Flatband voltage
C_{FB}	Flatband capacitance
R_{Sh}	Sheet resistance
L_T	Transfer length
ρ_C	Specific contact resistivity
L_D	Debyle length
V_g	gate voltage
EOT	Effective Oxide Thickness
N	Carrier Concentration
C	Capacitance

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Abbreviations	**Definitions**
σ	Standard deviation

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CHAPTER 1

INTRODUCTION

This chapter starts with a brief explanation of power electronics, and its uses in the world, followed by power electronic devices and the materials from which these devices are fabricated. After introducing wide bandgap materials and their relation to power electronics, there is an introduction to gallium oxide, discussion on the properties of gallium oxide and its electrical properties in relation to other semiconductors. This will lead into a literature review in Chapter 2, which will cover gallium oxide based devices in more depth. This will provide an overview of the current research as well as provide the reasons and rational for the experimental work undertaken.

1.1 Power Electronics

Power electronics is a multidisciplinary branch of electrical engineering. It is concerned with controlling electrical power, converting AC/DC and transforming voltages, currents, or frequency. This originates from vacuum rectifiers, however, today this is performed using semiconductor devices. Power electronics aims to manage power and increase efficiency, essential in this ever electrified world. Power electronics has an affect across nearly all aspects of our lives, so, unsurprisingly, this field has seen dramatic growth since its inception in the early 20^{th} century.

Electrical engineering ranges from semiconductor devices to the circuitry that uses these devices to perform operations. The world is continuing to develop and the demand for electrical power is expected to increase [1], all of this electrical power will have to be processed by some power device, from power generation, transition and final use. One of the driving forces behind the development of power electronics devices is the increase in electrification globally, which in turn increases demand and reliance. In this process, existing power grids will need to be improved and expanded, and new ones will need to be built. These also require more development in power generation, which will require management. This makes power electronic an essential part of power management, which should not be overlooked as it increases the effectiveness of the energy generated and efficacy [2].

Many factors, including increasing transport efficiency, are behind this insatiable hunger for more power. Electric vehicles utilize power electronics devices to power and charge them.. There is a desire for these devices to be as light and compact as possible. The increase in high-performance computing and the data economy is another force that is increasing the demand for electrical power, which needs to be managed. Every sector uses power electronics to a greater or lesser extent. Where equipment is becoming increasingly power-hungry, so there is increasing demand for power electronic devices. More robust power electronic devices are also desirable for dealing with harsh environments. As a result, power electronic devices are of interest to aerospace, oil and gas exploration, and mining, where they can be exposed to various radiation and temperatures. All these aspects are driving the need for the development of more efficient power electronic devices. All electrical energy will go through a power device at some point, from generation to transport and final use, it is critical to manage this power effectively, and the development of power devices aims to increase the efficiency. A small increase in efficiency and any decrease in investments needed in these systems will impact the world as it continues to electrify.

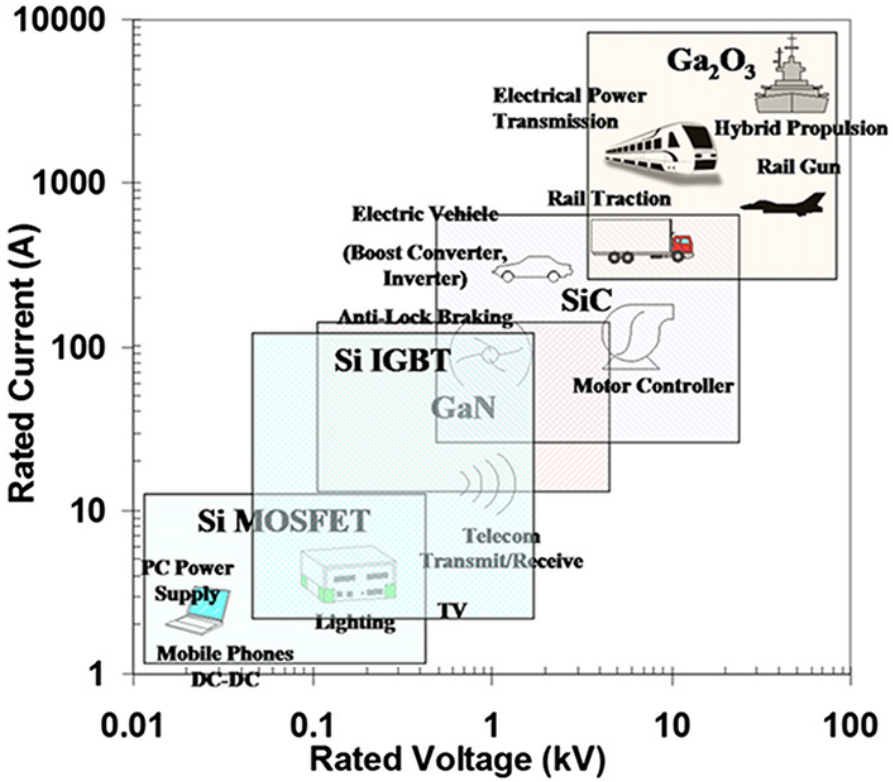
This work is interested in the semiconductor materials used to fabricate power electronic devices. These devices were first fabricated in Si, which is still the most common one to date, which was followed by wide bandgap material and more specifically in this work an investigation into gallium oxide for power electronic devices was performed.

1.2 Wide Bandgap Semiconductors

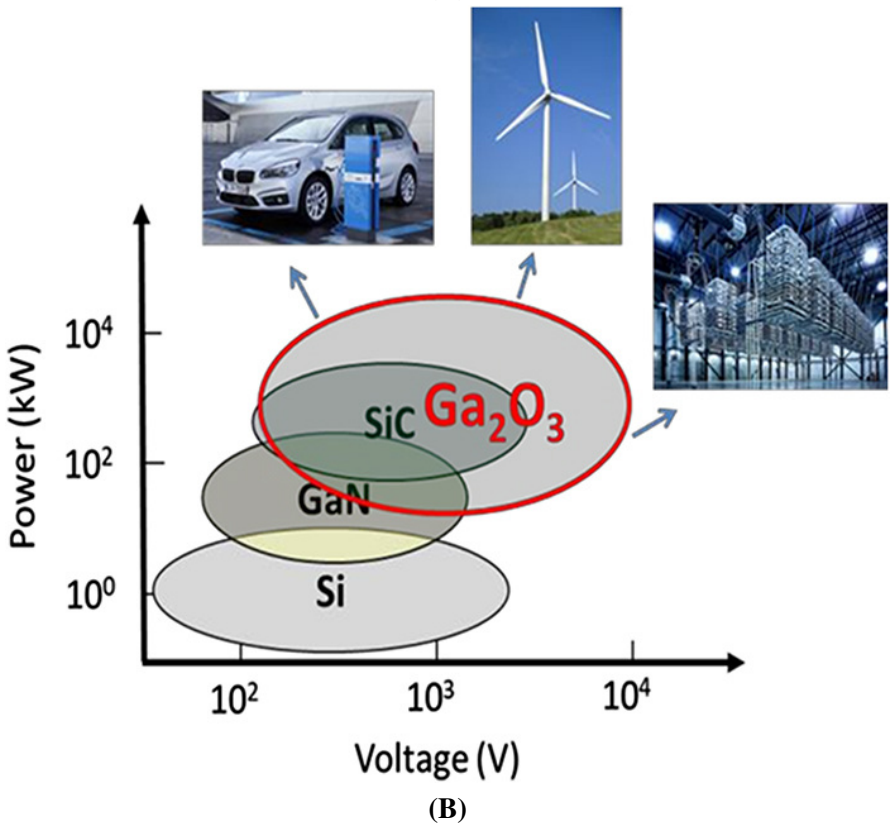
Due to their properties, wide bandgap semiconductors (WBG) offer advantages compared to Si, which has been of interest since the 1980s. WBG semiconductors can produce more effective devices than their traditional counterparts. Bandgap (E_g) is related to the critical electrical field (E_c), the electric field needed to cause avalanche breakdown. A high critical electrical field strength means that devices fabricated with wider bandgaps can couple with higher voltages before breaking down. Supporting higher voltages means the devices can have higher power density, and be made smaller, making them lighter and more compact with less cooling concern. Minimising devices is of interest to many areas, particularly electric vehicles, where space and weight are required. The reduced size and weight will increase electrical efficiency. As devices based in Si are superseded with WBG and Ultra-WBG (UWBG) semiconductors, this will increase efficiency and so affect the overall power consumption [3] [4]. Because of their material properties, the devices have lower theoretical on-state resistance (unipolar limit), reducing the lost power and increasing their efficiency. WBG materials can also operate at higher temperatures than the more traditional narrow bandgap semiconductors, as there is a larger energy gap. Therefore, temperature's effects on the Fermi level have less impact than narrower bandgaps. Because of the wide bandgap, they are more resilient to radiation, which is of interest to aerospace, nuclear, and high energy physics. WBG materials also have optical properties essential for photodetectors, sensors, and solar cells. One method to find wide bandgap semiconductors compound semiconductors is an avenue which has been explored, compound semiconductors are compounds with elements from two different groups, such as GaN. Compound semiconductors tend to have a wider bandgap than Si, because the system has multiple elements, each element can affect the overall

band structure and electrical and optical properties differently. One of these compound semiconductors that has gathered interest is gallium oxide. SiC and GaN are more mature materials in this regard and have a bandgap in the region of 3-3.4 eV. It should be noted that SiC is sometimes considered a compound semiconductor, while it is a compound material, both Si and C are both group IV elements which means it is not consistently considered a compound semiconductor. There is no disagreement that it is a wide bandgap semiconductor. Power devices fabricated from these materials have superior specifications. WBG semiconductors can operate at higher temperatures and handle higher voltages and currents [5]. There is a hesitancy to transition from Si-based devices, as they are well known, well-tested and low cost. WBG materials are less known or proven, so before adoption, these materials need to be tested and developed. While SiC and GaN devices are commercially available and are being adopted, the same is not true for newer materials. The adaptations for large-scale production must be determined because they will only ever see wide adoption if they are cost-effective. Compared to Si, WBG devices are still in their early stages, so device design and material aspects should be explored. These WBG materials have sparked interest in wider bandgap materials the UWBG) which offer similar advantages. These materials have different power ratings where their properties are the most effective, see Figure 1.1 for a diagram. The current devices voltage rating is between the regions of 600-3300 V [6].

Diamond has been investigated for over forty years, however, there has been limited progress, whereas devices have been demonstrated for materials such as gallium oxide and aluminium nitride. UWBG materials, partially oxides, are currently at the forefront of research for energy and electronics [7]. Oxides represent a large group of compounds that comprise a considerable amount of the earth's resources [8]. As a result of this, they can be considered to be abundant and stable compounds. Many of these have a low intrinsic carrier concentration and rely on high doping to a degenerate state. While the conductivity of other oxides is controllable, Ga_2O_3 has a tunable carrier concentration, with a much larger bandgap compared to other oxides such as ZnO_2 and SnO_2. While ZnO_2 and SnO_2 have shown more promise with p-type doping, compared to Ga_2O_3 [9]. This makes Ga_2O_3 along with other features such as growth and bandgap particularly interesting.



(A)



(B)

Figure 1.1: Diagrams showing power rating suitable for Si MOSFETs, Si IGBTs, GaN, SiC and Ga_2O_3. This is reprinted from [10]. It can be seen that β-Ga_2O_3 is predicted to be used in voltage/current ratings higher then SiC and GaN, the current leader in WBG semiconductor devices.

1.3 What is Gallium Oxide

(Ga_2O_3), also known as gallium sesquioxide, though this term does not seem to be used often, is a compound semiconductor. It exists in several different polymorphs, each with its exciting properties. It is not a new material but rather a rediscovered one. It was known and being researched into as early as 1952 with more work continuing into the 1960's [11] [12] [13] [14] [15] [16], looked into the crystal structure, and photoconductivity, and luminescence. However, the research and interest in gallium oxide has experienced a significant surge in the past decade, as evidenced by the increasing number of publications, see Figure 1.2.

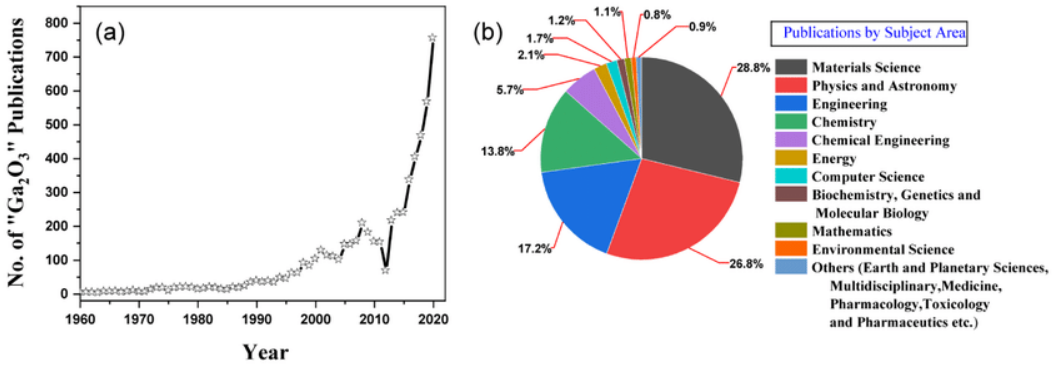


Figure 1.2: A diagram showing the publications for Ga_2O_3, between 1960-2020. This is taken from [17], this was created with data from Scopus.

This is because of the ability to grow large, high-quality crystals with controllable doping, which have realised the potential for power electronics and optoelectronics. A diagram by Roy et al. [11] illustrated the different es Ga_2O_3, the conditions which they transition into different phases. This diagram can be seen in Figure 1.3. Gallium oxide exhibits a series of beneficial properties that make it of interest for power electronic devices. Amorphous gallium oxide is an insulator, however, it can become a highly efficient semiconductor when it is crystalline and doped. It has been grown and used as a dielectric layer for GaN devices [18].

1.3.1 Phases of Gallium Oxide

There are four common phases; α phase, β phase, κ phase, and ϵ phase of Ga_2O_3. The different phases of Ga_2O_3, were described by Roy et al. [11], alongside the conditions under which it transitions. The β phase and α phase have received the most attention of these phases. It should also be noted that ϵ/κ phases are related to one another in the same structure for the most part. Two other phases, the γ and δ phase, are not discussed much. The reason behind this is possibly for the stability of the different phases, meaning that the growth of these metaphases of Ga_2O_3 is very dependent on the underlying substrate structure and the growth (and consequent) conditions. Figure 1.3 shows the conditions under which the Ga_2O_3 changes it's phases and that β phase as it is the most stable. However, the other phases have their interesting properties but have not been explored to anywhere near the same extent as β phases, which, in turn, is followed by the metastable cousin α phases. Other polymorphs of Ga_2O_3 are predicted to exist, these are determined with simulations [19].

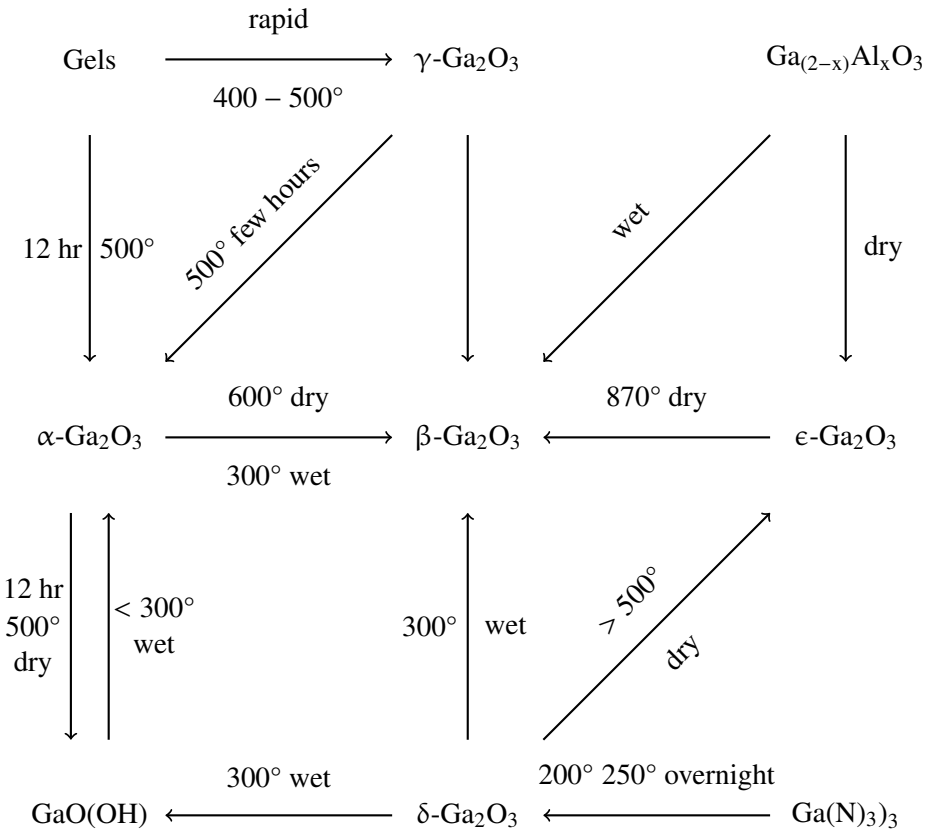


Figure 1.3: This is a diagram show the stability of the different polymorphs of Ga_2O_3 and how they change under certain conditions. This is recreated from published by Roy et al. [11].

1.3.2 Alpha Gallium Oxide

The α phase of Ga_2O_3 has a rhombohedral structure and is a meta-stable phase of Ga_2O_3, seconded only to the β phase in terms of stability. Despite this disadvantage and the necessity for more careful growth conditions, the α phase has attracted attention. α-Ga_2O_3 has a larger bandgap than the β-Ga_2O_3 with a value of 5.3 eV [20]. The bandgap of the α phase is a direct bandgap and has been calculated as 5.57 eV [21]. The wider bandgap is one of the reasons the α phase has received this attention. Like with β-Ga_2O_3, thin films of α-Ga_2O_3 have been commonly grown on sapphire substrates. Aluminum oxide (Al_2O_3) has advantages, such as the common availability of α-Al_2O_3 substrate. Another reason is the thermal expansion coefficient between Al_2O_3 and Ga_2O_3, which while Ga_2O_3 has a larger thermal expansion coefficient than Al_2O_3, it is of a similar order [22]. These thermal constraints limit its uses, potential and require that it be maintained under certain conditions. Like all the other phases, it will transition into the β phase under the right conditions. Finally the lattice matching between both α-Al_2O_3 and α-Ga_2O_3 is another reason for choosing Al_2O_3. Heterojunction pn junctions were fabricated using α-Ga_2O_3 with a low lattice mismatch to α-IrO_2 (0.3%) [23]. As mentioned, due to its lesser stability, it requires more careful growth control, so it cannot be

grown by melt methods, a privilege enjoyed by the β phase. The instability limits its uses and potential and requires that it is maintained under certain conditions like all the other phases. It will transition into the β phase under the right conditions. Large 6" Al_2O_3 wafers are produced and available and with the possibility of fast HVPE growth mean the possibility to fabricate whole wafers of α-Ga_2O_3 by growing a thick layer of α-Ga_2O_3 and then removing the substrate. At high pressures/temperatures (P ≥ 20 GPa at room temperature) β-Ga_2O_3 transitions into α-Ga_2O_3 [24]. Another potential growth mechanism at lower pressures is to use NaOH at 4.4 GPa and 1000°C to growth α-Ga_2O_3 [12].

1.3.3 Beta Gallium Oxide

The most stable phase of gallium oxide is the β-Ga_2O_3 phase [25]. It has a monoclinic crystal structure with a space group 12 (C2/m). It can be grown using melt methods, which means it has the potential for quicker, larger-scale bulk material growth. β-Ga_2O_3 can be formed by annealing thin films of Ga_2O_3 of other phases as well as amorphous Ga_2O_3 (a-Ga_2O_3). These factors are one of the main reasons why the β phase is the most explored and investigated polymorph of Ga_2O_3 over other polymorphs. β-Ga_2O_3 has four main orientations which are used: (001), (100), (010), and (201), these orientations affect the end device. Bermudez determined that (100) β-Ga_2O_3 has two possible terminations [26], Kilian et al. [27] determine that one termination should be favoured. Bermudez [26] also determined that (010) only has one type of termination. Bermudez, also determined that (001) had two types of termination where one is favoured over the other. (-201) has two types of termination, however, one of these is energetically favoured over the other [28]. These different terminations will incorporate defects, band offsets, and electrical characteristics affecting the end power devices. The orientation affects the valence band minima/bandgap. It was found for (001) 3.4/4.71, (010) 3.4/4.59, ($\bar{2}$01) 3.57/4.64 eV, and this was in respect to SiO_2 [29]. Fan et al. [19] conducted a simulation where they found that the effective electron/hole masses (in m_e) of 0.22/2.81, 0.22/3.49, 0.21/4.54, 0.23/6.06 and 0.21/2.57 for the a, b, c axis and maximum and minimum. However, experimentally, the effective electron mass has been found to be 0.28 [30] and [31]. The indirect bandgap of Ga_2O_3 is 4.43-4.48 eV [32] and the direct bandgap for the β phase has been calculated as 4.87 eV [21]. While the exact bandgap needs to be determined, it is clear that β-Ga_2O_3 has a wider bandgap than other more matured materials such as SiC and GaN.

The Structure And Arrangement Of Beta Gallium Oxide

The crystal structure win β-Ga_2O_3 is shown in Figure 1.5. Koun et al. [33] reported the monoclinic unit cell with four Ga_2O_3 molecules, and this structure being twinned along the (001) plane. Due to this twinning, the original structure was initially misreported as orthorhombic. It is interesting to note that Al_2O_3 and Ga_2O_3 are very similar. This similarity originates from the atomic radii being of similar size to the extent that the structure of β-Ga_2O_3 is the same as θ-Al_2O_3 [33]. It is ionic-bounded rather than covalent bonding, where there is a large ionic difference between the Ga and O ions. The structure of β-Ga_2O_3, the two Ga ions are Ga_I^{3+} and Ga_{II}^{3+} and four O ions which are O_I^{2-}, O_{III}^{2-}

and two $O_{II}{}^{2-}$. To consider the arrangement consider, an octrahedren and tetraheadren surrounding the two Ga ions. The $Ga_I{}^{3+}$ ion is surrounded by a distorted tetrahedra of O atoms, a $O_I{}^{2-}$, a $O_{III}{}^{2-}$ and two $O_{II}{}^{2-}$ atoms. $Ga_{II}{}^{3+}$ is surrounded by the tetrahedra, shares a corner with one other tetrahedron in the *b* axis and with octahedral at all other corners. These octahedra share their edges with adjacent octahedra. β-Ga_2O_3 has two strong cleave planes (100) and (001) [34]. Because of this the different states caused by these complexes effects the position in the bandgap.

1.3.4 The Other Phases Of Gallium Oxide

As previously stated, due to the stability and relevant research into the different polymorphs of Ga_2O_3, the polymorphs of β and α will be the most discussed. However, it is worth noting the remaining structures, if only briefly. The remaining polymorphs are κ/ϵ, γ, and δ, out of these the κ/ϵ is the most discussed. The exact structure of κ/ϵ was initially misinterpreted, as the structure appeared hexagonal systemic, however, further work has since shown that this was a pseudo system, and it is, in fact, an orthorhombic structure. Initially, it was prescribed as ϵ, and the newly accepted structure is κ [35]. As such, the phases κ/ϵ should be considered interchangeable. However, κ results likely superseded those where the material was considered ϵ, which should be remembered as there are contradicting results as the direct band gap of the ϵ phase has been calculated as 4.48 eV [21] whereas for κ the direct bandgap has been calculated as 4.84 eV [21]. In work performed by Mezzadri et al. [36], it has been shown that it is a semiconductor with ferroelectric/piezoelectric/pyroelectric properties. It could be used to fabricate high electron mobility hetero-structures [36] [37]. It has been predicted that the ϵ-Ga_2O_3 will have large polarizations, and so a 2D high electron density will form at the $(GaAl)_2O_3/Ga_2O_3$ interface, similar to Al GaN/GaN. The γ phase has had less work performed on it, and it has been shown to have a cubic-defective spinel [38], it has not been investigated as much as the β, α and κ have. Less information is available about the δ phase, however, it has been proven to exist and has been demonstrated and grown with CVD methods [39]. However, the nature of the structure has yet to be determined.

1.3.5 Discussion On The Properties Of Gallium Oxide

In Table 1.1, the material properties of Ga_2O_3 are compared to other semiconductors. This table exhibits the advantages and disadvantages of power electronics, considering only the β phase of Ga_2O_3 as it is of most interest. The wide bandgap of gallium oxide is one of the main reasons why β-Ga_2O_3 is of interest, as the bandgap is related to the critical electrical field. Different fittings empirically establish a relation between bandgap and critical electrical fields. Slobodyan et al. [40] empirically determined that this bandgap is directly proportional to the critical electrical field by,

$$E_C \propto {E_g}^{1.83}. \tag{1.1}$$

Higashiwaki et al. [41] predicted 8 $MV \cdot cm^{-1}$ as the value, this was fitted by eye. Chikoidze et al [42]. put forward that this could be higher at a value of 13.2 $MV \cdot cm^{-1}$ if unintentional doping can be

suppressed. These two features together mean that while an exact number for the critical field strength is not known, it can reasonably be predicted that this value will be higher than the current generation of wide bandgap semiconductors. High E_C is highly desirable for power devices, as it enables higher voltages for a given area. Because of the material properties of gallium oxide, it is predicted to have a lower theoretical on-state resistance. Even though its electron mobility is lower than that of other materials because of its high critical field strength, it still overcomes this. The unipolar limit can be seen in Figure 1.4, where it can be seen that β-Ga_2O_3 has the potential to outperform the other wide bandgap competitors except for diamond a material which has its issues.

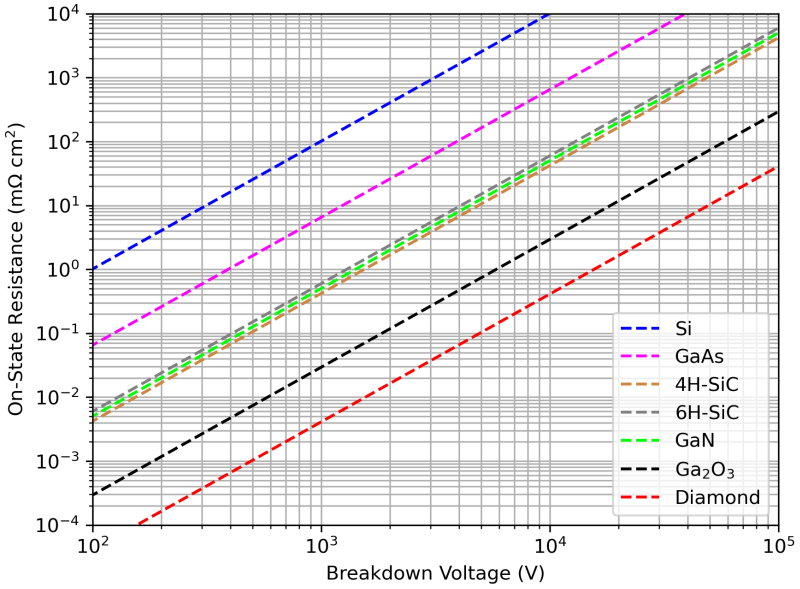


Figure 1.4: The on-state resistance as a function of voltage shows the theoretical unipolar limits for different semiconductors. It can be seen that β-Ga_2O_3 has a higher theoretical limit than its other wide bandgap counterparts, with diamond surpassing it.

Ga_2O_3 is transparent to ultraviolet light, which means that UV photodetectors and UV light-emitting diodes have potential uses. This is an active area of research where, again, its wide bandgap has been an asset for Ga_2O_3 [43] [44] [45] [46] [47]. X-ray and radiation detector applications are also being investigated with β-Ga_2O_3 as scintillators with fast decay times and light output demonstrated [48], requiring specific doping [49]. The relative refractive index of β-Ga_2O_3 is about 2 [50], the absorption edges is 270-275 nm [51]. β-Ga_2O_3 is both chemically and thermally stable with a melting point about 1800°C [52], and with its wide bandgap, it has the potential for devices that can operate in harsh conditions such as high temperature, environmental conditions, and radiation [53] and [54]. This opens potential applications for Ga_2O_3 devices to be utilised in automotive, aerospace, nuclear, and defence for power devices and logic due to their potential robustness [53]. However, it will be mentioned later, the thermal conductivity is an issue, even though it has the potential to operate at high temperature.

Dopants which cause β-Ga_2O_3 to be p-type remains elusive, where most dopants in this regard create semi-insulating material. Suitable dopants for this require an acceptor dopant with small activation energy as while theoretical studies have indicated Mg, Zn, Be, and N require large > 1 eV activation energies, most of the valence bands are based around the 2p orbitals in the O component of the band structure [21], [55] and [56]. This area will remain a distinct weakness for Ga_2O_3 until this can be realised, as work by Chikoidze et al. [57] [58] has demonstrated p-type material which has limited repeatability.

Ga_2O_3 has poor electron mobility, because the phonon has lower energies which causes Fröhlich interaction [59]. Fröhlich interaction is a common issue with oxides. Lorenz et al. [14] in 1966 found that n-type β-Ga_2O_3 had mobility in the order of 10^2 $cm^2 \cdot V^{-1} \cdot s^{-1}$. Since then it has been found that the electron mobility has a small bound of approximately 300 $cm^2 \cdot V^{-1} \cdot s^{-1}$ [59]. Ma et al. [59] derived an empirical formula to model the electron mobility for temperatures > 300 K,

$$\mu_H = \frac{56e^{\frac{508}{T}-1}}{1+\frac{N}{(T-278)\times 2.8\times 10^{16}}^{0.68}}. \tag{1.2}$$

Where T is the temperature (K), N is the doping concentration cm^{-3}. This is a lower μ compared to other wide bandgap semiconductors is mitigated by the E_C, due to the effect both have on the on-state resistance, it is still an order of magnitude lower than those for SiC and GaN. Krishnendu and Uttam Singisetti estimated the saturation velocity (ν_{Sat}) to be approximately 1×10^7 $cm \cdot s^{-1}$ [60], comparable to other semiconductors and is acceptable for high-frequency roles. The thermal conductivity (λ) of β-Ga_2O_3 is poor compared to other semiconductors, β-Ga_2O_3 is also anisotropic where λ is different along the different crystal planes. It is estimated to be 0.22-0.27, 0.11-0.14, and 0.15 $W \cdot m^{-1} \cdot K^{-1}$ along [010] [100], [001] planes, this difference is believed to originate from the differences in the speed of sound in these directions [61] [62] [63] [64] [65]. Different dopants have also been found to effect the λ as well, where Sn doped β-Ga_2O_3 was found to have higher λ then undoped β-Ga_2O_3 [64]. Metal contacts used for β-Ga_2O_3 can be used to manage the thermal properties. In a thermal study, Shi et al. [66] found that for ohmic/Schottky metal contacts, Cr/Ni, respectively, had the best thermal boundary conductance. In Table 1.2 there are different FOM, all normalised to Si. While FOM are not absolute, they indicate how different materials will compare to the theoretical limits of devices.

1.4 Figures Of Merit

A Figure Of Merit (FOM) is a quantitative way to consider something. In electronics, it is used to compare the performance of materials and devices. They are often normalised and used to compare materials looking at specific goals. FOMs have been used in power electronics to identify and compare potential materials, usually Si, as it is the dominant semiconductor. FOMs, while useful, can also be misleading if not properly understood. This underscores the importance of your expertise and caution in their use. So, Figures of merit should only be considered as a rough guide. There is a need to develop robust useful FOM, Krishna Shenai discussed this [67].

1.4.1 Johnson FOM

Johnson's FOM was proposed by Johnson [68] as a way to compare the switching frequency of transistors based on their material properties. It proposed that the limiting factor for a transistor is set by E_c and ν_s of its minority carrier saturation velocity. Johnson proposed the Johnson FOM which is given by,

$$J = \frac{E_c \nu_s}{2\pi}. \tag{1.3}$$

1.4.2 Keyes FOM

This was later disputed by Keyes who argued that thermal limitations should be accounted for. This lead to the Keyes FOM in [69] which is given by,

$$K = \lambda \sqrt{\frac{c\nu_l}{4\pi\epsilon}}, \tag{1.4}$$

where λ is the thermal conductivity, c is the speed of light, ν_l is the limiting velocity and ϵ is the dielectric of the semiconductor.

1.4.3 Baliga FOM

Baliga devolved another FOM [70], which can be used to compare materials if they are used for unipolar devices. It is given by the equation,

$$B = \mu\epsilon E^3, \tag{1.5}$$

where μ is the mobility and ϵ is the dielectric constant. The variable E has multiply definitions, it has been defined as either bandgap or critical breakdown field. As E_g and E_c are related so not entirely incorrect, however, it means curation has to be used when comparing this FOM. Because the absolute number varies a lot depends on what variable is used for E. This is called the unipolar limit.

1.4.4 Baliga High-Frequency FOM

Later, Baliga [71] proposed yet another FOM, used to compare devices and take into account the switching speed. It is shown by the equation,

$$B_{HF} = \frac{1}{R_{on,sp}C_{in,sp}} = \mu_n \mathrm{E_c}^2, \tag{1.6}$$

where $\mathrm{R_{on,sp}}$ is the specific on state resistance and $\mathrm{C_{in,sp}}$ is the specific input capacitance.

1.4.5 New High Frequency FOM

Later Kim et al. [72] proposed a different FOM, using,

$$N = \frac{1}{R_{on,sp}C_{out,sp}}. \tag{1.7}$$

Where $\mathrm{C_{out,sp}}$ is the specific output capacitance.

1.4.6 Huang FOMs

Huang [73] proposed a series of different FOM, while the focus of this work was primarily based on devices, it was generalised into looking and being able to compare materials. For comparing devices he proposed,

$$H_D = \sqrt{R_{on}Q_{gd}}, \tag{1.8}$$

where $\mathrm{Q_{gd}}$ is the gate charge, the total charge across the gate to drain. Huang proposed a material FOM in the form of,

$$H_M = \mathrm{E_c}\mu. \tag{1.9}$$

By considering an optimal chip area, he identified a collection of terms in this which are material properties which are related to how small the chip size is. This FOM for chips Huang proposed,

$$H_C = \epsilon\sqrt{\mu}\mathrm{E_c}^2, \tag{1.10}$$

continuing this method but applying it to the temperature, looking at how the temperature changes while the chip is in use. While this is looking at the chip level, Huang identified a collection of terms in this, which are material properties, which can be used as a FOM for comparing materials and how well they can deal with this thermal consideration. This thermal FOM Huang proposed,

$$H_T = \frac{\lambda}{\epsilon \mathrm{E_c}}, \tag{1.11}$$

where λ is the thermal conductivity. The three FOM 1.9, 1.10, and 1.11 are all inversely proportional, which means that the larger FOM indicates better properties.

1.4.7 Quality Factors

Shenai et al. [74] defined quality factors to consider material, these are related to Bailigas FOM (Equation 1.5). These Quality factors are effectively FOM which should vary depending on what is known. In the case where the device λ is low, then,

$$Q_1 = \lambda \frac{\mu\epsilon {E_c}^3}{4{V_B}^2}, \tag{1.12}$$

can be a useful FOM. If the device has a perfect or near perfect heat sink then the expression can be expressed as,

$$Q_2 = \lambda \frac{\mu\epsilon {E_c}^4}{4{V_B}^2}. \tag{1.13}$$

Finally a device without any assumptions was considered, based on its heat sink, to use the coefficient B from the thermal resistance as unknown,

$$R_{th} = \frac{B}{\lambda}. \tag{1.14}$$

So then a quality factor is to compare the materials used is given by,

$$Q_3 = \frac{\mu\epsilon {E_c}^3}{4{V_B}^2}. \tag{1.15}$$

1.5 Summary

β-Ga_2O_3 is a material which has attracted much attention because of its electrical properties. These properties are compared to other semiconductors, and different FOM can be seen in Tables 1.1 and 1.2. The properties and FOM of β-Ga_2O_3 indicate it has the potential to be productive for power electronics. While not all the properties of β-Ga_2O_3 are better than those of SiC and GaN, the E_C is an important one. As the on-state resistance given by BFOM has a ${E_C}^3$ dependency, so while μ_e is lower compared to other materials, this is overshadowed by E_C, to result in better performance. β-Ga_2O_3 may play an important role in developing new technologies. The wide bandgap and critical electrical field effect the FOM calculations, indicating that β-Ga_2O_3 has the potential to be significantly better over more mature semiconductors for power electronics. The FOM show that it is comparable or superior to SiC and GaN. It also benefits from being grown with melt methods, which neither SiC nor GaN can do. The ability to be grown through melt should not be ignored, as throughput times and costs are important factors. If the end product is not economically viable, it will not see widespread adoption. β-Ga_2O_3 has the potential to be processed much more quickly than other materials, which also gives it a competitive edge and superior electrical properties. The potential for high production means that it shares more with Si compared to SiC or GaN, as it has the potential for wide-scale adoption [1].

As an additional point to this potential for wide-scale adoption is how it is adaptable into Si processing lines, reducing the investment required and accelerating the commercial viability of the realising β-Ga_2O_3 device production and application in the real world, as opposed to being confined to an interesting research question.

It has been stated that there are issues in which β-Ga_2O_3 devices do need to overcome specific issues, such as thermal conductance and p-type doping. These will be discussed further in the next chapter. However, device design can mitigate thermal issues. The substrate, different layers, and packaging are all aspects that can help realise this. Using hetero-junctions and semi-insulating layers can mitigate the issue from p-type, and active work is also being research on p-type material. Both of these issues have current solutions, and as time progresses, this will be further alleviated by device design and the whole structure. β-Ga_2O_3 will have an interesting future, and while Si will remain the most dominant device substrate and other more mature materials such as SiC and GaN will still be used, however, β-Ga_2O_3 will likely carve out a region for its use.

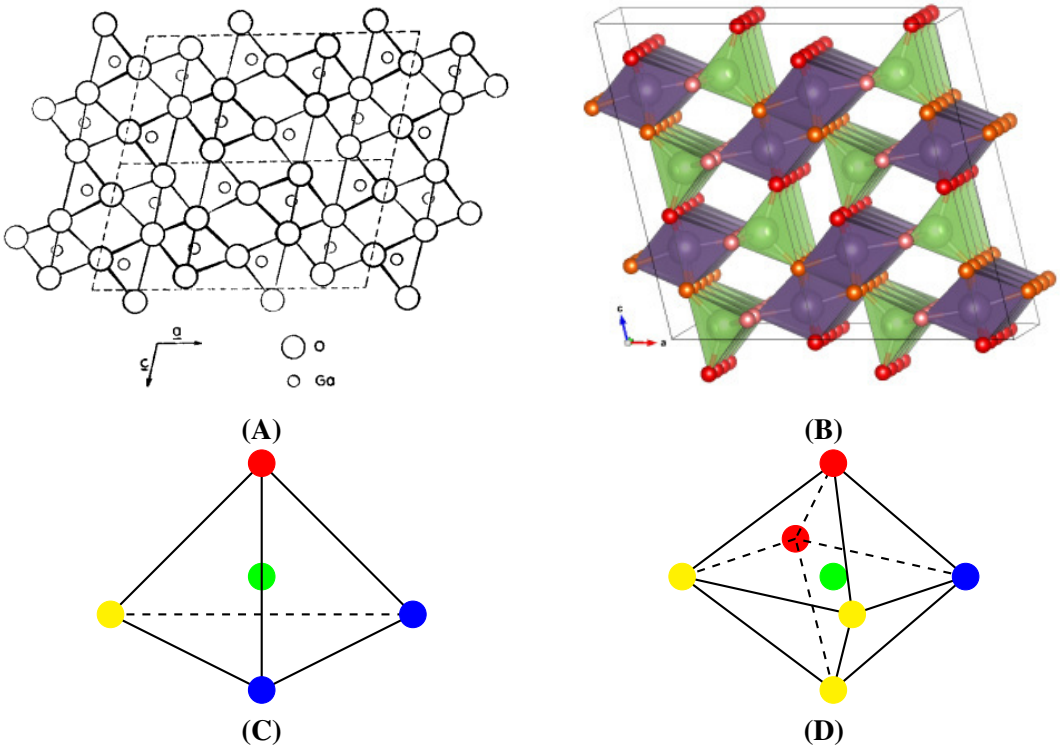


Figure 1.5: Models to describe the lattice of β-Ga_2O_3, this is adapted from [15] and [75], sub-figures **(A)** and **(B)** are reprinted taken from these respectably. Sub-figures **(C)** and **(D)** are sketches to help add clarity for the reader. Sub-figure **(A)** shows the repeating structure of β-Ga_2O_3, a monoclinic structure (dashed line) looking at th b axis, the middle dashed line cutting the distorted in half shows the flipped pattern of the unit cell. This is split into a pattern of octahedra and tetrahedra which is displayed in sub-figure **(B)** as green/purple respectably. These tetrahedra and octahedra are drawn as sub-figures **(C)** and **(D)** respectably. The bonds in β-Ga_2O_3 are predominantly ionic as the difference in charge between the Ga and O ions. Sub-figures **(C)** the green shows Ga_I^{3+} and in **(D)** the Ga_{II}^{3+} and red is O_I^{2-} yellow the O_{II}^{2-}, blue O_{III}^{2-}. The dislocations and binary nature of β-Ga_2O_3 causing these complexes effect the different energy levels that are available.

Material	**Si**	**4H-SiC**	**6H-SiC**	**3C-SiC**	**GaN**	**β-Ga_2O_3**	**α-Ga_2O_3**	**Diamond**
E_g (eV)	1.12 [76]	3.23 [76]	3 [76]	2.36 [76]	3.28 [76]	4.85 [77]	5.3 [20]	5.5 [77]
E_c ($V \cdot cm^{-1}$)	3×10^5 [76]	3-5×10^6 [76]	3-5×10^6 [76]	10^6 [76]	5×10^6 [76]	8×10^6 [41]	9.5×10^6 [78]	$10^6 - 10^7$ [77]
μ_e ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	≥ 1400 [76]	≥ 900 [76]	≥ 400 [76]	≥ 800 [76]	≥ 1000 [76]	115 [79]	200 [78]	2000 [77]
μ_h ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	≥ 450 [76]	≥ 120 [76]	≥ 90 [76]	≥ 320 [76]	≥ 350 [76]	-	-	5300 [80]
n_I (cm^{-3})	1×10^{10} [76]	4×10^{-9} [81]	1.6×10^{-6} [81]	1.5×10^{-1} [81]	7×10^{-9} [76]	1.8×10^{-23} [82]	-	-
ϵ_r	11.7 [76]	9.7 [81]	9.66 [81]	9.72 [81]	9 [76]	10 [78]	10 [78]	5.7 [80]
$v_{e,\,sat,300}$ ($cm \cdot s^{-1}$)	1×10^7 [81]	2×10^7 [81]	2×10^7 [81]	2.5×10^7 [81]	2×10^7 [81]	1.1×10^7 [80]	2.3×10^7 [80]	-
$v_{h,\,sat,300}$ ($cm \cdot s^{-1}$)	0.704×10^7[81]	-	-	-	6.63×10^6 [83]	-	-	-
λ ($W \cdot cm^{-1} \cdot K^{-1}$)	1.3 [76]	3.7 [76]	4.9 [76]	3.6 [76]	1.3 [76]	0.27 – 0.11 [78] [65]	-	22 [80]

Table 1.1: The properties of different semiconductors materials, this is to compare β-Ga_2O_3 to other semiconductors. The wide band gap of Ga_2O_3 is clearly apparent and as this is related to the critical electric field empirically ($E_c \prec {E_g}^{1.83}$) [40] it is clear why this would be advantage. It should be noted that the stated and widely quoted value for E_c for β-Ga_2O_3 of $8\ Mv \cdot cm^{-1}$ was estimated by plotting different semiconductors E_c vs E_g, fitted to with β-Ga_2O_3 estimated by eye [41]. The relatively poor thermal conductivity is one of the main issues facing β-Ga_2O_3, however, this is anisotropic hence the different values given.

Material	Si	4H-SiC	6H-SiC	3C-SiC	GaN	β-Ga_2O_3	α-Ga_2O_3	Diamond
J-FOM$_n$	1	26.7	26.7	8.33	23.3	29.3	72.8	-
J-FOM$_p$	1	38	50.3	9.23	16.7	5.54	-	564
K-FOM$_n$	1	4.42	5.87	4.80	1.35	0.236	-	-
K-FOM$_p$	1	-	-	-	1.11	-	-	-
B-FOM$_n$	1	126	559	17.6	2540	1330	3880	25800
B-FOM$_p$	1	524	391	21.9	2770	-	-	213000
BH-FOM$_n$	1	114	50.8	6.35	198	58.4	143	1590
BH-FOM$_p$	1	47.4	35.6	7.9	216	-	-	13000
HM-FOM$_n$	1	8.57	3.81	1.91	11.9	2.19	4.52	47.6
HM-FOM$_p$	1	3.56	2.67	2.37	13	-	-	393
HC-FOM$_n$	1	118	78.5	6.98	180	174	324	647
HC-FOM$_p$	1	76.1	65.6	7.78	188	-	-	1860
HT-FOM	1	0.258	0.342	1	0.078	0.00911	-	1.04

Table 1.2: Different Figures Of Merit (FOM) nominalised to Si for various semiconductors, these are based off the properties shown in Table 1.1. The subscripts of n and p refer to n or p type properties. For some of these they are nonsensical, for example BF-FOM for p-type β-Ga_2O_3 is not realisable at the current state and so should be ignored until this is not the state. These different FOM are discussed in Section 1.4, and refer to different properties from switching speeds and power loss to the resistances of the devices. It should be noted that these values vary a lot depending on the orientation of the material, as well as the units used to calculate these. It can be seen that wider bandgap materials have FOMs which surpass those of Si. It can also be seen that the FOMs for β-Ga_2O_3 is comparable and at times surpasses other wideband gap materials. These FOMs tend to get worse when thermal conductivity is considered. As a result it should be clear that β-Ga_2O_3 has potential for power electronics.

CHAPTER 2

LITERATURE REVIEW

This literature review aims to discuss β-Ga_2O_3 for use in power devices. Firstly a discussion on the growth material, both bulk and thin films of β-Ga_2O_3, then regarding dopants and surface treatments, as well as etching of β-Ga_2O_3. Following this a section regarding background physics which are related such as charge carriers, Metal-Insulator-Semiconductor interfaces structures and metal-semiconductor interfaces. Following this Ohmic and Schottky contacts to β-Ga_2O_3, the steps needed for a device, with a discussion on devices fabricated with β-Ga_2O_3.

2.1 Gallium Oxide Bulk Growth

The growth of bulk β-Ga_2O_3, and the ability to grow large bulk material is one of the main reasons β-Ga_2O_3 has generated so much interest. High quality bulk material is needed for β-Ga_2O_3 devices. There are several ways to grow bulk β-Ga_2O_3, which has been demonstrated. Namely the Verneuil [14] [13], the Czochralski [84] [85] [86] [87], the Floating-Zone (FZ) [88], the Edge-Defined Film fed Growth (EFG) [89], and the Vertical Bridgman (VB) [90]) methods. See Table 2.1 for a summary of these different methods of bulk growth. The growth conditions are essential for β-Ga_2O_3 as the different techniques produce bulk crystals with different levels of defects and orientations. It was found that there were four types of defects, which are dislocations, voids, twining and small defects [91]. During the crystal growth, the amount of dislocation is a critical factor, limiting current leakage paths [92].

Not all voids cause leakage paths, it depends on the size and crystal orientation [91] [93]. Minor defects are prominently introduced by mechanical damage, it is uncertain if they affect electrical characteristics. It has also been found that the leakage current was interdependent on the doping. These demonstrate that the growing conditions and orientation are essential for power devices.

The Verneuil method is crucible-free and which allows for both oxidising and reducing growth conditions [14], a diagram showing this can be seen in Figure 2.1. Aubay and Gourier [94] found that growth under reducing conditions improved electron conductivity. The n-type nature of β-Ga_2O_3 was realised with Zr doping at 900°C which led to carrier concentrations in the order of 10^{19} and 10^{21} cm^{-3} [95]. In this work they found Mg decreased the mobility, with a lower charge carrier concentration. The Verneuil method is not used commercially, as other methods are more efficient [96].

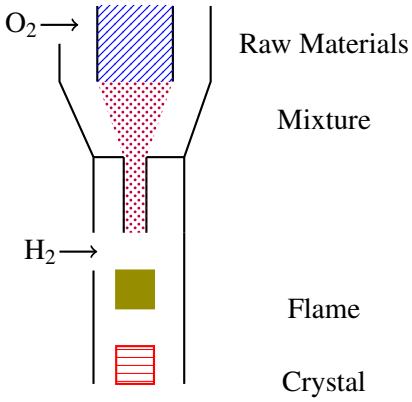


Figure 2.1: A diagram of the Verneuil method, the raw material (blue diagonal lines), this is then intermixed with O_2 (purple dots) mixed with H_2 burned in a flame (olive) then forming the crystal (red lines).

Another crucible-free method is the FZ, in which the crystal is grown between two polycrystalline materials, the raw materials and the desired material. The material is then melted, held with surface tension as the crystal is drawn out see Figure 2.2. One advantage of the FZ method is that β-Ga_2O_3 can be grown in an ambient atmosphere, which in turn leads to fewer oxygen defects [97]. The issues with greater diameter growth are due to small hot zones and steep temperature gradients, this can cause cracks as the liquid melt cools [98]. There are also limitations on the size possible, as the melt is held by surface tension, not a crucible [98].

The impurities of β-Ga_2O_3 grown by FZ were analysed by Tomioka et al. [99] using inductively coupled plasma mass spectroscopy. β-Ga_2O_3 grown by FZ was found to have impurities of Si, Sn, Al, Mg and Fe with concentrations of the order of 10^{16} cm^{-3}, Al was considered to be a neutral impurity, Mg and Fe to act as acceptors, compensating for the Si which act as donors, this is based on the mobilities measured. While there has been some success with good crystal structures [100] with X-ray diffraction (XRD) rocking with a Full Width Half Maximum (FWHM) of 22 arc sec, others over 100 arc sec, were measured [101], this is indication of how stressed the lattice is.

Oxide Crystal growth from the Cold Crucible (OCCC) method has been used to grow crystals with a diameter up to 45 mm without an Ir crucible, the impurities found were only from the raw materials [102] [103]. This indicates that the OCCC can more economically yield bulk β-Ga_2O_3.

The Czochralski method is where the raw materials are melted in a crucible, and the crystal is slowly pulled from the melt while slowly rotating, a diagram showing the Czochralski method can be seen in Figure 2.3. The Czochralski method has predicted to be able to grow a large boule of β-Ga_2O_3.

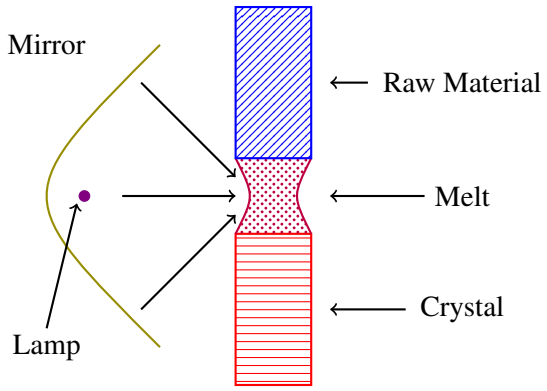


Figure 2.2: A diagram showing the floating zone method, raw material (blue diagonal lines) is melted (purple dots) via a lamp (violet) and mirror (olive) and is cooled into the crystal (red lines).

However, this has yet to be realised so far due to the evaporation and decomposition of Ga_2O_3 at high temperatures with O_2 [104] [98]. A larger surface area is needed to grow large wafers of β-Ga_2O_3. This increases the evaporation and decomposition of the Ga_2O_3 [98] [105]. Higher temperatures and O_2 also damage the Ir, Galazka et al. y. [105] present a solution to overcome this. The solution which was found was starting at low O_2 % and temperature, then at 1200°C increase the O_2 percentage until at 1800°C when the percentage reaches 100%. While the investigation was on the Czochralski method, this approach is also suitable for any melt method. This has been limited to 2", however, large crystal volumes have been grown using different methods. They usually are crack and twin-free [106]. The FWHM of the rocking curves are normally below 50 arc secs and 30 arc secs, with dislocation density below 5×10^3 cm^{-2} but as well as 1×10^3 cm^{-2} [106] [50]. Galazka et al. [85] reported that unintentionally doped β-Ga_2O_3 grown using Czochralski method had impurities on the order of 10^{16} cm^{-3} and had a Hall mobility of 80-152 $cm^2 \cdot V^{-1} \cdot s^{-1}$.

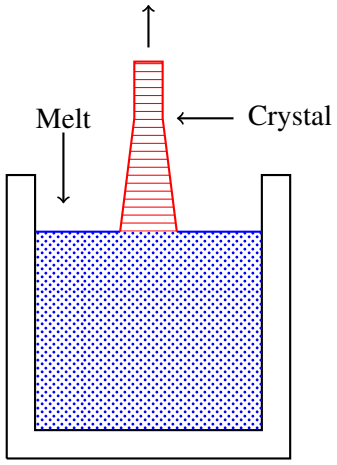


Figure 2.3: A diagram showing the Czochralski method. Where the raw material is melted (blue dots) inside a crucible (solid black) and is slowly drawn out using a seed crystal slowly cooling down into a crystal (red lines).

The EFG method, much like the Czochralski, uses an Ir crucible, while not being able to get the same thickness as the Czochralski, it can get larger wafer diameters, see Figure 2.4 showing this. Novel Crystal Technologies offering 4" β-Ga_2O_3 wafer as a commercial product, Si is the main impurity of the order of 10^{16} cm^{-3} [89]. Using 4" crystal diameters Kuramata et al. [89] showed that twinning can be easily generated, and optimisation of the growth (shouldering process) is necessary to avoid this. Heinselman et al. [107] compared the economics of the Czochralski to the EFG method being approximately twice as cost-effective due to the cost of Ir. In EFG, the crystal is grown by drawing the Ga_2O_3 melt through a capillary. Compared to other growth techniques, the melt area can be reduced, which means that the dissociation and evaporation of the melt are reduced. The growth environment should be controlled to around 98% / 2% N_2/O_2, and this is also to protect and extend the life of the Ir crucible.

In work by Ahmadi and Oshima [78] found the crystal shape is formed by the die, with the growth being a few dozen $cm \cdot day^{-1}$, the direction it is pulled in is typically [010], this is to minimise twinning and seed blistering.

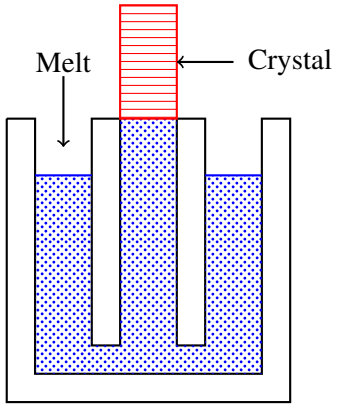


Figure 2.4: A diagram of the Edge-Defined film fed method, this is a raw material melted (blue dots) in a crucible, the crystal (red lines) is pulled from a seed crystal pulled through a die.

The VB method also uses a crucible See Figure 2.5 for a diagram regarding this. However, Pt-Rh alloy is used for the crucible, which allows high O_2 concentrations. Wafers up to 2" were grown in crucibles. These wafers can have small losses in the growth process, introducing Rh impurities [90], Sn and Si impurities from the raw materials, and Fe and Zr from the furnace [108]. The FWHM of the rocking curve appeared lower than that for the edge-defined film fed, for example, in work by Chaman et al. [109] and Taishi et al. [110] found the defect density 5×10^3 cm^{-2}. In the VB method, the crystal is grown by the Ga_2O_3 melt solidifying as it cools down through a temperature gradient. The resultant wafer is moulded into the shape of the crucible used.

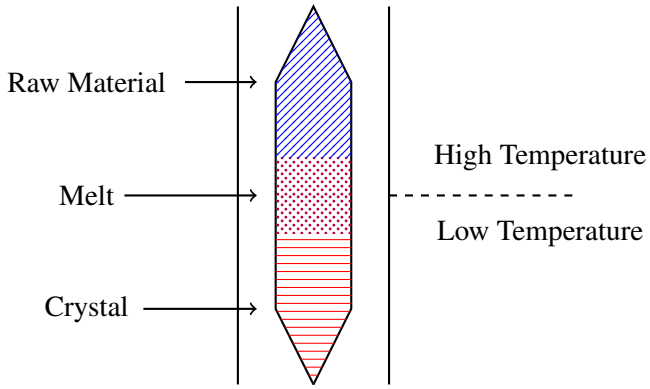


Figure 2.5: A diagram of the Vertical Bridgman method for growing crystal structures. The Raw material (blue diagonal lines) is drawn into a high-temperature oven where it is melted (purple dots) then moved into a lower oven at a lower temperature so it slowly cools into the crystal (red lines).

Ning et al. [111] demonstrated that a casting method was used to grow β-Ga_2O_3 with an FWHM less than 50 arc secs. This method opens an opportunity to reduce the number of process steps and lower the cost. The growth methods are based on a crucible and have much more potential to be scaled up, increasing the potential wafer size, which is a critical economic factor if β-Ga_2O_3 is to be adopted. Due to the growth of β-Ga_2O_3 being oxidation of Ga, crucible methods using Ir must be careful to limit the degradation of the crucible from the oxidation of Ir.

	Verneuil	Czochralski	Floating Zone	Edge Defined Film fed	Vertical Bridgman
Bulk Size Growth Rate $mm \cdot h^{-1}$	1" 10	2" diameter 20-40	2" diameter 2	6" diameter e 15	2" diameter 5
FWHM arc sec	-	22	22-50	17	10-50
Dislocations cm^{-2}			10^3	10^3	$10^2 - 10^3$
Residue Inpatients Intentional Doping cm^{-3}	2×10^{18} $\times 10^{19}$ (Mg)	10^{17} $\times 10^{19}$ (Nb, Ta),	10^{16} $\times 10^{19}$ (Sn, Si, Hf)	10^{17} $6 - 7 \times 10^{18}$ (Si, Sn)	10's $wt \cdot ppm$ 3.6×10^{18} (Sn)

Table 2.1: Overview of different bulk growth methods for β-Ga_2O_3, with different properties of the resultant wafers. Sourced from: [14] [112] [88] [101] [100] [113] [114] [115] [90] [108] [95] [101] [99] [116] [50] [117] [116] [118] [105] [89] [119] [119].

2.2 Gallium Oxide Thin-Film Growth

While bulk material is very important, epitaxial layers are essential for devices, and so is the establishment of high-quality epitaxial growth. This allows for layers of β-Ga_2O_3 with different doping concentrations, allow for n^+, n^- and semi-insulative regions. The techniques discussed here are also used for the deposition of dielectric materials, and they are needed for real devices. These are needed for devices to form channels, contacts and drift regions. Epitaxial layers of β-Ga_2O_3 have been grown on substrates, but not limited to such as Si, GaAs, TiO_2, ZrO_2:Y, MgO, SiC and GaN [120] [121] [122] [123]. There are several ways of growing thin films of β-Ga_2O_3:

- Halide Vapour Phase Epitaxy (HVPE).
- Metal-Organic Vapour Phase Epitaxy (MOVPE).
- Pulsed Laser Deposition (PLD).
- Atomic Layer Deposition (ALD).
- Molecular Beam Epitaxy (MBE).
- Mist-Chemical Vapour Deposition (Mist-CVD).
- Metal Organic Chemical Vapour Deposition (MOCVD).

There are sub-categories within these, which are split into further categories that are related to one another. It should also be noted that another important aspect of device design is the use of dielectric layers, which are deposited and grown with the same tools and processes. However, they will be described within their own subsections. Homo-epitaxially can be used to grow β-Ga_2O_3 which, is commonly (010) or (001) faces. Elaheh and Yuichi [78] found that (010) epilayers on (010) are smoother than on (001), to the extent that on (001), chemical mechanical polishing is needed before device fabrication, it was found the growth rate on (100) is slow.

2.2.1 Chemical Vapour Deposition

CVD operates by simultaneously introducing precursor gases into the reaction chamber, causing a specific chemical reaction to occur. This reaction deposits/grows the desired material, in this case β-Ga_2O_3. The reaction continues as long as the precursor materials are supplied, and so the material will keep growing. To supply energy to enable the reaction, the chamber is often heated. The continuous nature of this means also less control over the conformity and precession of the growth, as all the reactions are mixed. The temperature control for the reaction can either be a hot or cold wall. In a hot wall, the entire chamber is heated to enable the reaction, whilst in a cold wall, only the substrate is heated.

Mist-CVD is where a mist of liquid precursor is generated and introduced into the deposition chamber. Then, it is vaporised and deposited onto the substrate surface. Pressure is also a factor that can be controlled to change the nature of CVD deposition. As the name implies, Low-Pressure CVD (LP-CVD) involves holding the chamber at low pressure (1-100 Torr) and can produce high-quality films. However, compared to other CVD methods, it requires higher temperatures, which is a limiting factor. Atmospheric Pressure CVD is held at/near atmospheric pressure. It is not commonly used for growing semiconductor material or deposit dielectric layers because the quality of the film is not suitable.

Plasma can be used to induce reactions, this is Plasma-Enhanced CVD (PECVD). PECVD uses a plasma to generate reactive species from the precursors, making the reactions available at a lower temperature, and can be used to generate high-quality films, a variation on PECVD is Remote Plasma CVD, in which the plasma is separated from the substrate to minimise damage. Lasers can also induce chemical reactions, so Laser-Assisted CVD (LA-CVD) involves using a laser to create the reactive species from the precursors. The following variants are based on the precursors chemicals, where different precursors with specific elements or molecules attached to cause a specific reaction. These include metal-organic compounds (Metal Organic CVD), also known as Metal Organic Vapour Epitaxy (MOVPE) or OrganoMetallic Vapour Phase Epitaxy (OMVPE). Then, precursors with hydride (containing H, Hydride Vapour Phase Epitaxy) compounds are used to deposit layers. There is molecular beam epitaxy, where the precursors generate a controlled beam of the reactive species, which is directed at the substrate to grow the layer.

CVD is used to grow the different polymorphs of Ga_2O_3, α, β, γ, κ (ϵ) and δ [124] [125] [126] [127] [39]. An advantage CVD has is that it is a vacuum-free, low-cost, solution-based process that is saleable for mass production. It has a lot of different varieties, as mentioned above, which have their benefits and drawbacks. Mist-CVD growth of (-201) β-Ga_2O_3 on Fe doped (0002) GaN/α-Al_2O_3 substrate was demonstrated by Xu et al. [128]. The precursors were 100 ml of DI water, 1 ml of HCl, 0.5 ml of H_2O_2, 0.11 g of $SnCl_2 \cdot H_2O$ and 1.83 g of $Ga(Acac)_3$, this was atomized by sonicating at 1.7 MHz, the carrier gas used in this process was N_2. Lee et al. [129] showed Sn doped β-Ga_2O_3 with carrier concentrations up to 10^{20} cm^{-3}, they investigated growth rates with different temperatures. They found that higher temperatures lowered the growth rate and improved the surface roughness. In this work, the result was attributed to reactions occurring before reaching the materials surface and/or the coefficient of the precursors reacting to the surface. Wu et al. [130] demonstrated growth of (201) β-Ga_2O_3 epilayers with PECVD, they found at a temperature of 820°C which achieved a rocking curve of 0.8° with a growth rate of 0.58 $\mu m \cdot h^{-1}$, while this is slower, it is at a lower temperature than many other deposition method. Work by Hu et al. [131] optimized this, with a temperature of 710°C and a carrier gas of Ar/O_2 at 150/10 sccm with a radio frequency of 150 W. Tu et al. [132] investigated the growth of (010) β-Ga_2O_3 onto sapphire wafer, this was with LA-CVD which achieved a growth rate up to 40 $\mu m \cdot h^{-1}$. Fei-Peng et al. [133] investigated (-201) β-Ga_2O_3 onto sapphire wafer with temperatures between 600°C to 800°C. It was found that layers grown at 800°C formed better photodiodes.

Karim et al. [134] used β-Ga_2O_3 on (100) diamond, this is with an abrupt junction showing a possible solution to the counterbalance to the low thermal conductivity of Ga_2O_3. Gavax et al. [135] investigated the role of temperatures when using LP-CVD to grow β-Ga_2O_3, growth rates up to 3 $\mu m \cdot h^{-1}$ were achieved, the substrate was Al_2O_3 and held at 1000°C. LP-CVD growth of (010) β-Ga_2O_3 on (010) β-Ga_2O_3 substrate with 7 nm surface roughness and growth rate of 1.3 $\mu m \cdot h^{-1}$ [136] and in LP-CVD growth of (010) and (001) grew at rates between 13-21 $\mu m \cdot h^{-1}$ with roughness 1.41-7.35 nm. Saha et al. [137] found growth rates varying from 13-15.6 $\mu m \cdot h^{-1}$ with β-Ga_2O_3 with LP-CVD. This was on (001) and (010) Sn doped β-Ga_2O_3 substrates, it was found with increasing growth rate that the surface roughness also increased and overall concluded that the optimum growth range was 13-15.6 $\mu m \cdot h^{-1}$ for devices.

MOVPE is commonly used to grow epilayers for III-V compound semiconductors wafers, gallium precursors were used such as Trimethylgallium (TMGa), Triethylgallium (TEGa), and Gallium(III) tris-dipivaloylmethanate ($Ga(DPM)_3$), O_2, and H_2O were used as the oxygen precursors [78]. There is a trade-off between the speed of the growth and the quality. MOCVD has been used to grow α, β, ϵ γ, -Ga_2O_3 films [138] [139] [140]. Compared to GaN, Ga_2O_3, growth occurs at lower pressures, and the parasitic gas phase reaction occurs, MOVPE reactors are often held at a lower pressure. Homoepitaxial growth with MOVPE of β-Ga_2O_3 is affected by the orientation of the substrate. In these

films, high electron mobility 184 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at (room temperature), was with net carrier concentration 2.5×10^{16} cm^{-3} were demonstrated [141] [142] [143]. It has been found that layers grown with MOCVD, had been found to have carrier concentrations from 10^{15} to 10^{20} cm^{-3} [144] [145]. Electron concentration can be from 10^{16} to 10^{15} cm^{-3} and as high as 10^{20} cm^{-3} [146] [147]. Alema et al. [142] used a close coupled reaction that has been shown to lower this reaction, achieving high growth rates of up to 10 $\mu m \cdot h^{-1}$ on (010) orientated substrates. Meng et al. [148] were able to achieve growth rates of 3 $\mu m \cdot h^{-1}$ in the (010) orientation. Gogova et al. [149] using a hot-walled MOCVD grew $(\bar{2}01)$ β-Ga_2O_3 at 1 $\mu m \cdot h^{-1}$ at low temperatures and low reagent flow rates. This was found to have a FWHM of 118 arc sec, comparable with EDG. Zeming et al. [150] grew a film matching the substrate, this film surpassed what has been reportedly grown by MOCVD with an FWHM of 21.6 arc sec, and surface roughness of 0.68 nm. Ta-Shun et al. [151] were able to achieve growth rates of 0.6-0.9 $\mu m \cdot h^{-1}$ on (100) β-Ga_2O_3. Bin Anooz et al. [152] on (100) towards $(00\bar{1})$ achieved growth rates up to 4.3 $nm \cdot min^{-1}$. Bhattacharyya et al. [147] reported FWHM of 35-45 with mobility's up to 196 $cm^2 \cdot V^{-1} \cdot s^{-1}$.

Due to the nature of using metal-organic compounds as precursors, carbon impurities are often introduced. Carbon is predicted to be a shallow donor in β-Ga_2O_3 [153], so carbon contamination is a concern. Feng et al. [154], the carbon content was not detectable with SIMS, at 2×10^{16} cm^{-2}. However, post-deposition annealing and adding H to the growth stage can suppress carbon contamination [155] [156]. Ma et al. [123], demonstrated β-Ga_2O_3 growth on (110) TiO_2 substrate, TMGa and O_2 were used as the precusors with N_2 as the carrier gas. The pressure was held at 10 KPa, with temperatures varying from 850-1000°C in four steps of 50°C, with FWHM rocking curves of 1.54°, 0.8°, 0.7° and 0.9° respectively. Because of the lattice constants of TiO_2 and β-Ga_2O_3 matching well despite the different crystal structure (tetragonal crystal system and monoclinic) begin differently. Metal-Semiconductor-Metal photodetectors were fabricated from this grown layer, it was found that growth at 950°C produced the best photodetector with a photocurrent of 85.3 μA and responsivity 2.56 $A \cdot W^{-1}$.

HVPE is another promising candidate for large-scale mass production of Ga_2O_3 thin films, not only for the β phase but by using chlorine catalysis it is possible to achieve growth of α, ϵ and κ phases of Ga_2O_3 [157]. The nature of the polymorph grown and overall structure is determined by the substrate, while the ratio of Ga to O affected the growth rate, the substrate also impacted this [158]. α-Ga_2O_3 has a larger reported bandgap of 5.3 eV and higher theoretical dielectric constant of 12.8 and critical field of 9.5 $MV \cdot cm^{-1}$ [20] [159]. ϵ-Ga_2O_3 has potentially high power and high-frequency High Electron Mobility Transistor (HEMT), showing less strain than GaN to m-AIN and higher density if two-dimensional electron gases are at the interface [160] based on simulations. It has been reported that layers grown using HVPE without intentional doping have a carrier concentration as low as 10^{13} cm^{-3} [161] up to intentional doping up to 10^{19} cm^{-3} [162]. In 2022, Novel Crystal announced the successful growth of a thin film of β-Ga_2O_3 onto a 6" sapphire wafer using HVPE. It aims to com-

mercialise the equipment in 2024 [163].

The growth rate of β-Ga_2O_3 can also be quite high with HVPE reaching 250 $\mu m \cdot h^{-1}$ [164]. The surface roughness of HVPE-grown films is relatively high at fast growth rates, so polishing is needed [165]. Mechanical and chemical polishing is employed to remove and smooth the surface and reduce defects [166] [167]. It is crucial to optimise the polishing as the difference between polishing and unpolishing can be seen in [162], where the XRD FWHM and surface morphology were very different. Trihalide vapor phase epitaxy (THVPE) is another version of HVPE which, while having lower growth rates (32.2 $\mu m \cdot h^{-1}$), this is without particle generation [168]. The ability to grow large thick films is vital for the development of adoption Ga_2O_3 for power electronic devices. It makes vertical devices more practical to fabricate, allowing for higher voltages and switching speeds, and also more economical to make, which is vital if the technology is to be adopted. The carbon content in HVPE can be minimised with n^- doping by using carbon-free precursors [78]. It is essential to control the different impurities in the grown layer by limiting the choice of precursors. MBE is suited to research rather than commercial uses, this is because even though it can grow high quality β-Ga_2O_3 films, it is more expensive and slower to grow compared to MOCVD and HVPE. The use of catalysts can improve the growth called metal-oxide catalysed epitaxy MEB (MOCATAXY) [169] or metal-exchange catalysed MBE (MEXCAT-MBE) [170]. The growth with MEXCAT-MBE on (001) and (100) rates were 0.138 $\mu m \cdot h^{-1}$, 0.198 $\mu m \cdot h^{-1}$, and ($\bar{2}01$) 0.06 $\mu m \cdot h^{-1}$ [170]. The growth with MOCATAXY, on (010) and (001) 0.294 $m \cdot h^{-1}$ and (010) up to 0.288 $\mu m \cdot h^{-1}$ [169]. The film quality and surface roughness on ($\bar{2}01$) was rougher (1.15 nm) and worse quality than that of the (001) (0.17 nm) and (100) (0.45 nm). It is believed that is because the binding energy of In as an ad-atom to the surface free energy of the Ga_2O_3 [170]. Using Suboxide-MBE (S-MBE) growth rate of 2.5 $\mu m \cdot h^{-1}$ [171] grown on (0001) Al_2O_3. S-MBE grown at 1 $\mu m \cdot h^{-1}$ and a FWHM 122 and 43 arc secs with a surface roughness 1.9 nm [171]. The defects of P-MBE were investigated in [172] showed that surface morphology and crystalline structure depend a lot on the growth temperature where the surface roughness 5 → 1 nm and dislocation $1.1 \times 10^6 \rightarrow 6.6 \times 10^5$ cm^{-2} and twinning $7.5 \times 10^3 \rightarrow 2.1 \times 10^2$ cm^{-1} between 750 → 850°C. Free electron carriers from 10^{17} to 10^{20} cm^{-3} were achieved by Si [173], 10^{16} to 10^{19} cm^{-3} were achieved by Sn [174]. The use of O_3 instead of O can expand the growth temperature [175].

2.2.2 Pulse Laser Deposition (PLD)

PLD uses high-intensity laser pulses to ablate a target material, the material is then deposited onto the substrate surface It is used to deposit/grow thin layers of material, in this case Ga_2O_3. Removing precursor chemicals limits the amount of contaminants which can be introduced during deposition process. PLD has a comparatively lower cost than other methods of growing layers of Ga_2O_3. Petersen et al. [176] demonstrated films with low surface roughness (<1 nm), depending on the growth conditions. PLD has been used to grow both α, and β ϵ phases of Ga_2O_3 [176] [177], this is with active dopants up to 10^{20} cm^{-3} [178] [179]. Temperature and O partial pressure are critical components for PLD, higher O partial pressure lowers the growth rate and the band gap, leading to more

self-trapped holes on the O, which results in a better crystal structure [180] [181]. Temperature also plays an important part where increasing temperature leads to slower depositions and better crystalline [182]. These depend on the material being grown, as it was found that growing α phase and decreasing O both decreased the growth rate [176]. Vu et al. [180] showed how the growth rate varies depending on the conditions. Rates of 10.8 $nm \cdot min^{-1}$ were achieved by the introduction of O, and higher heating to improve the film dramatically reduces this. The deposition affects the crystalline nature, which in turn affects the mechanical properties, this should be considered depending on the device and substrate (fabrication and usage) [183]. Post-deposition anneals are also used to improve the quality of the film deposited with PLD. The annealing temperature and time are essential for re-crystallising the Ga_2O_3 crystal due to rearranging the Ga and O atoms to their optimum sites. However, it is possible to damage the crystal this way and seems to increase surface roughness [184] [185] [186]. Taeyoung et al. [187] demonstrated that Plasma-Assisted-PLD can reduce defects in the O vacancy over conventional PLD.

2.2.3 Atomic Layer Deposition (ALD)

ALD can produce highly conformal films with a very controllable growth rate, requiring a lower temperature, with a lower growth rate of 0.1 $nm \cdot cycle^{-1}$, compared to MBE CVD. ALD is derived from CVD and uses separate sequential reactions as it is a series of cycles of self-limiting surface reactions, which occur one after another with purge steps in-between to build up layer by layer to build the film slowly [188]. Post-deposition annealing is crucial as it affects the crystallinity and morphology of the deposited Ga_2O_3 films [189]. PDA also affects the active dopants, which on unannealed materials can go up to 10^{18} cm^{-3} [178] even with the doping of 10^{20} cm^{-3}, this is believed to be because of the low temperature. Plasma Enhanced Atomic Layer Deposition (PEALD) can also be used to deposit amorphous Ga_2O_3 at temperatures as low as 80°C [190], and β-Ga_2O_3 at 200°C [191] with a smooth surface (roughness < 1 nm).

Kröncke et al. [192] found that when growing thin films of amorphous Ga_2O_3, this was using a Plasma Enhanced ALD (PEALD) process at 200°C, with trimethylgallium $Ga(CH_3)_3$ as the precursor grown on (001) Si. It was found that intermediate stages of O_2 plasma for 30 s after the ALD cycle increases the regrowth of SiO_2 for the 0.27 nm of Ga_2O_3 deposited and decrease of leakage current. At a growth rate of 0.65-0.70 $Å \cdot cycle^{-1}$, this extra O_2 plasma process is only effective over the first three ALD cycles.

2.3 Doping

Oxides-based semiconductors tend to have n-type conductivity due to vaccenic in the oxygen orbitals, β-Ga_2O_3 is also a UWBG material where intrinsic conduction is also rare, and the ease of n and p-type doping is not symmetrical. As mentioned in the introduction the difference between p-type and semi-insulating is defined by hole concentration, most dopants for semi-insulating are deep valence

energies, leading to low hole concentrations. Where defects and dislocations within the lattice and because it is a binary compound the resultant complex and states can cause shallow valence states. β-Ga_2O_3 suffers from issues that are also observed in other oxides, such as:

- Acceptor point defects with high formation energy.
- Native donors with defects with low energy, resting holes.
- A high effective mass of the electron holes, causing low mobility. This is due to the top of the valence band, and the O 2-p orbitals.

The native p-type nature of β-Ga_2O_3 has been calculated that β-Ga_2O_3 is "lucky" with the hole concentration where at temperature 500°C with $N_{hole} = 10^{15}$ cm^{-3}, $P_{hole,}$ β-$Ga_2O_3 \approx 10^{-2}$ atm [57]. Compared to ZnO in same conditions and N_{hole} concentration then $P_{hole,\,ZnO} \approx 10^{3}$ atm [193]. Hole concentrations were investigated by Chikoidze et al. [193] where undoped thin films of β-Ga_2O_3 were grown on α-Al_2O_3 by PLD. The hole concentrations, resistivity and mobility were found to be $N = 2 \times 10^{13}$ cm^{-3}, $\rho = 1.8 \times 10^{2}$ $\Omega \cdot cm$ and $\mu = 4.2$ $cm^2 \cdot V^{-1} \cdot s^{-1}$. Further work on this by Chikoidze et al. [194] β-Ga_2O_3 films grown on Al_2O_3 using MOCVD the hole connection was 10^{14} cm^{-3} which increase to 10^{17} cm^{-3} after annealing in oxygen at 850 K. Real devices will require higher hole connections at room temperature.

2.4 n-Type Doping

β-Ga_2O_3 is doped very easily to be n-type, even to degenerate levels with carrier concentrations ranging between 10^{15} to 10^{20} cm^{-3} Sn and Ge by MBE, Si and Sn MOVPE and Sn by MOCVD [173] [179]. Mobility of $145 - 184$ $cm^2 \cdot V^{-1} \cdot s^{-1}$ at room temperature up to 10^4 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at 46 K, these were doped with Si [154] [144] [195] [143]. There are a couple of different n-type dopants for β-Ga_2O_3, these are shallow donors and are Si, Sn, Ge, and F. These function differently: for Si, Sn, and Ge, they replace the Ga ion, whereas F replaces the O [196]. Electron mobility up to 190 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at room temperature with a peak 3400 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at 55 K.

2.5 p-Type Doping

Doping with p-type is much more difficult to achieve than with n-type, where the same dopants often produce semi-insulating material. Deep acceptors like Fe, Mg Zn in β-Ga_2O_3 are often used to fabricate semi-insulating material. Seyidov et al. [197] demonstrated that Co doping in β-Ga_2O_3 results in semi-insulating β-Ga_2O_3, Neal et al. [198] discussed deep acceptors for β-Ga_2O_3, and Fe, Mg all act as deep acceptors. Dopants which show p-type behaviour include Cu, N, Mg and Zn [199] [200] [201] [202]. Li et al. [203] demonstrated that Cu doping had p-type behaviour and could fabricate a FET. Saikumar et al. [199] also demonstrated that Cu doping had p-type behaviour, which was achieved by co-sputtering in a Physical Vapour Deposition (PVD) system using Cu and Ga_2O_3 targets. The

sample was then annealed at 800 and 900°C in N_2 environment, and the film was measured to have a resistivity of 60 $\Omega \cdot$ cm. Thin films of N doped β-Ga_2O_3 were grown on sapphire wafers. N doping in β-Ga_2O_3 has been achieved using GaN to ($\bar{2}$01) β-Ga_2O_3 [200]. This was thermal oxidised in N_2O at 1100°C for one hour. The hole concentration was found to be 1.64×10^{17} cm^{-3}, the hole mobility 4.98 cm$^2 \cdot$ V$^{-1} \cdot$ s^{-1}, and the resistivity 7.66 $\Omega \cdot$ cm. Wu et al. [204] demonstrated p-type GaN to n-type ($\bar{2}$01) β-Ga_2O_3 with thermal oxidation in O_2 environment. The P63mc GaN transformed to R3C α-$(GaN_xO_3)_{\frac{(1-x)}{2}}$ into a thin layer of p-type β-Ga_2O_3 with an accepter energy of 0.165 eV. In this, the hole concentration was found to be 1.56×10^{16} cm^{-3}, hole mobility 23.6 cm$^2 \cdot$ V$^{-1} \cdot$ s^{-1}, and resistivity 17 $\Omega \cdot$ cm, which was then used to fabricate a lateral field effect transistor based on this p-type. Feng et al. [205] demonstrated that Zn doped β-Ga_2O_3 nano wires saw pn junction behaviour. Chikoidze et al. [42] suggested that Zn can be either an accepter or donator for β-Ga_2O_3 depending on which site it bonds are on.

2.5.1 Simulation Density Functional Theory

There are extensive theoretical studies of doping in β-Ga_2O_3 to identify possible acceptor dopants to realise p-type material. Lyons et al. [206] investigated group 5 and 12 elements (Be, Mg, Ca, Sr, Zn, and Cd) to act as acceptor dopants in β-Ga_2O_3 using hybrid DFT. These showed ionisation levels over 1.3 eV, Mg, then Be appeared stable. Sun et al. [207] investigated P, Ge, Sn, Si, N and Cl using ab initio calculation, and they found that P, Ge, Sn, Si replace Ga ion where N and Cl replace an O. It was found that P, Ge, Sn, Si, and Cl were n-type, and N was predicted to act as a p-type dopant. Kyrtsos et al. [208] investigated with DFT Li, Na, K, Be, Mg, Ca, Zn, Cu and Au where they found Zn, Li, and Mg were deep acceptor levels with ionisation levels over 1 eV, indicating that they can not contribute to p-type conductivity. However, an underestimation of the bandgap may affect this due to the semi-local approach. Varley et al. [209] predicted that self-trapped holes are more favourable than delocalised ones due to the energies of self-trapping energy 0.53 eV and barrier height 0.1 eV. This indicates that free holes will localise towards polarons. Using hybrid DFT, Sabino et al. [210] predicted Bi to act like a p-type dopant. However, this has yet to be realised.

2.5.2 Hydrogen

Varley et al. [211] predicted that with UID β-Ga_2O_3, H present during the growth to be the cause for the n-type behaviour based on DFT. Ritter et al. [212] found that when annealed in H, it is incorporated into Mg-doped β-Ga_2O_3 over UID β-Ga_2O_3. This indicates that Mg lowers the Fermi level when incorporated into β-Ga_2O_3. It was found that Mg dopant, when doped into β-Ga_2O_3, is passivated by Si, Ir and H. Islam et al. [213] found that annealing in H could reduce the resistivity and reach a N_{hole} of 10^{15} cm^{-3} at room temperature and by different incorporations of H into the lattice Ga_2O_3 can act as both n or p-type. Where H is diffused into the lattice, H^+ is attracted to the $V_{Ga}{}^{3-}$ lowering the acceptor level, this leads to p-type behaviour. Goyal et al. [214] used first principles defect theory and defect equilibrium calculations to simulate a growth-annealing-quench sequence, hydrogen-assisted

Mg doping in Ga_2O_3. It was found that the H_2O and H partial pressure could affect the Mg concentration, increasing Mg solubility and suppressing O valences. They predict that growth under reducing conditions in the presence of H_2 followed by O-rich anneal will result in p-type material.

2.5.3 Co-Doping

DFT has predicted co-doping (doping with two elements) as a way to reach p-type doping, surpassing the limitation of mono-doping. It has been successful for II-V compounds containing N (Zn-N, N-P, Al-N), being demonstrated as a way to improve p-type conductivity [215] [216] [217]. Zhang et al. [217] found N-Zn to have acceptor levels 0.149 and 0.483 eV above the valence band, whereas N-P was found to be 0.55 eV above the valence band. Yuanli et al. [218] attempted Zn-Mg co-doping with Ga_2O_3, where it was shown to be β phase, and Mg and Zn acted as deep acceptors. Ling et al. [215] found that there were two shallow impurity levels above the valence band, 0.149-0.483 eV in N-Zn co-doped β-Ga_2O_3. N-P co-doping decreased the acceptor level to 0.8 eV, with an impurity level appearing 0.55 eV above the valence band, reducing the effective hole mass.] Suet al. [218] found Mg-Zn was a deep accepter 0.79 and 1.0 eV form co-doping.

2.6 Ion Implantation

In addition to doping during growth another approach is to ion implant the material in order to dope the material. β-Ga_2O_3 O_2 can be doped by ion implantation, where ions are accelerated into the crystal, they are annealed to activate them. Then, the energies of the accelerated ions will determine the depth of the implant, which needs to be considered to achieve the desired doping profile. Donors impurity Si, Sn and Ge were implanted into β-Ga_2O_3 O_2 to increase the carrier concentration, and acceptors like Mg. The post-implantation annealing conduction plays an essential role in work by Sharma et al. [219] Si was implanted into (201) β-Ga_2O_3 O_2. It was then annealed at 1100°C between 10 to 120 s, in O_2 and N_2 atmosphere. It was found that annealing in O_2, and the Si distributed far more than aneling in N_2. It was believed the cause was due to vacancies on the Ga ions in N_2, trapping the Si. The same effects were also seen in Sn and Ge implanted samples, as demonstrated by further work from Sharma et al. [220]. Wong et al. [221] implanted Mg and N into (001) β-Ga_2O_3, this was annealed at 600-1000°C for 30 minutes in N_2 environment. Mg and N were found to create an insulating region, and N ions were found to diffuse less, starting diffusing at 1100°C, whereas the Mg diffused at 900°C. Xu et al. [222] used H ions to exfoliate a layer of β-Ga_2O_3 where it was transferred onto 4H-SiC wafer. This thin film had a surface roughness of 5.3 nm and FWHM of 230 arc sec, which was reduced to 0.8 nm and 90 arc sec after chemical mechanical polishing. Liao et al. [223] demonstrated that He ion implantation can also be used to exfoliate along non-cleavage planes (010), increasing the potential for β-Ga_2O_3 based devices, as the thin layers could be bonded to other materials to mitigate the issues with β-Ga_2O_3 while taking advantage of its properties.

2.6.1 Spin On Glass

Spin On Glass (SOG) is another method to dope β-Ga_2O_3, this has been to create insulative or highly conductive layers. SOG has been used to create both conductive and insulative regions on β-Ga_2O_3, this can be done by introducing Sn with an anneal of 1200°C, for five minutes or Mg with an anneal of 950°C for one hour [224] [225]. This anneal was to diffuse and activate the dopants into the material.

2.7 Quick Overview

So far, the growth topics, both bulk and thin films, have been discussed. The quality of the material grown and a number of ways to dope the material to achieve semi-insulate, n^+ and n^- regions. Many of the same deposition methods are also used for dielectric deposition layers, the need and purpose of these will be described later when the topic of real power devices are discussed. This is an issue with a topic such as this, there is a need to discuss topics in isolation from one another before their utilities begin to converge.

2.8 Wet Etching

Etching is significant for devices, this is needed to create different geometry and treat the surface. Wet etching Ga_2O_3 has been investigated, predominantly on β-Ga_2O_3. The different orientations of β-Ga_2O_3 have different etch rates, it is believed to originate from the number of dangling bonds which are exposed [77], this is true for both wet and dry etching. Dangling bonds are incomplete chemical bonds on the surface, as there are not enough atoms to bind with nearby. Oshima et al. [226] investigated the etch rates of H_3PO_4 and H_2SO_4 on (100) β-Ga_2O_3 between 100-194°C. It was found that H_2SO_4 was unsuitable at temperatures at and above 190°C because of the formation of a thin polycrystalline film. This film was found to contain sulphur and to be composed of Ga:S:O in a ratio of 8:9:12:5:78:6. This suggests that the film is a mixture of $Ga_2(SO_4)_3$ and $Ga_2(SO_4)_3 \cdot xH_2O$. Ohira and Arai [227] investigated a series of wet etchants at room temperature for Sn doped/undoped (100)/(001) β-Ga_2O_3.

It was found that Sn-doped samples etched at a slower rate than their undoped counterparts. It was also found that (100) etched at around three times faster than (001) these results were found with etching with 47% HF at room temperature which was found to uniformly etch β-Ga_2O_3. It was found that 20% NaOH at room temperature and 60.5% HNO_3 at 120°C etched into β-Ga_2O_3. Jang et al. [228] compared $(\bar{2}01)$/(010) β-Ga_2O_3 etch rates using Photo Enhanced Chemical (PEC) etching with a 5 M solution of KOH, it was found that the etch rate was three to four times higher for $(\bar{2}01)$ compared to (010). PEC is where energy is supplied through a lamp to increase the reaction rate, with UV illumination with a power of 120 W Hg lamp, and the solution was 300 rpm at 80-95°C.

The lack of p-type material for Ga_2O_3 means that hetero-structures are a possible solution, these structures like other devices will require etching, and so the selectivity of β-Ga_2O_3 over other materials also need to be investigated. Chiang et al. [229] investigated the selectivity of NiO over β-Ga_2O_3, it was found that dilute HNO_4 (1:4) is a suitable wet etchant for this purpose. Inductively Coupled Plasma (ICP) dry etching with Cl_2/Ar with an etch rate of 80 nm $\cdot$ min^{-1} had a selectivity > 1 for β-Ga_2O_3 to NiO, with etch rates above 125 nm $\cdot$ min^{-1} with wet etching to remove the NiO without etching the β-Ga_2O_3 with dilute HNO_4. Alhalaili et al. [230] investigated KOH solution with PEC etching. The sample is in a chemical solution in which β-Ga_2O_3 is stable. However, when illumination provides energy, it undergoes a chemical reaction which produces an ion. A potential is applied to cause a reaction, etching the material so that the ion travels to the reference electrode. This enables a highly controllable form of etching, as the illumination, the electrolyte solution and the anodic voltage are all controllable. Ou et al. [231] investigated HF etching of thin films of PLD deposited β-Ga_2O_3, it was found that the more the film was amorphous, the higher the etch rate. They also determined the etch chemistry for β-Ga_2O_3 in HF follows the form,

$$Ga_2O_3 + 6 \cdot HF \rightarrow 2 \cdot GaF_3 + 3 \cdot H_2O. \tag{2.1}$$

Metal Assisted Chemical etching is related to wet etching, first demonstrated by Li and Bohn [232]. This form of electrochemical etching involves depositing metal onto the surface of the material being etched while submerged in a solution. Then, a potential is applied to the semiconductor and the solution. The metal acts as a catalyst for the solution to etch the material. Post-reaction, it is redeposited, which allows for further reactions. As a result, it continues in the direction according to the metal patterned onto the surface, thus controlling the etch. The inverse operation exists, where the metal acts as a catalysis mask and undergoes a UV version. This technique has been applied to β-Ga_2O_3, demonstrated by Kim et al. [233], on (010) β-Ga_2O_3, where a Pt mask was used in a solution of $K_2S_2O_8$ and HF. The overall chemical reaction is given by,

$$2 \cdot Ga_2O_3 + 6 \cdot {S_2O_8}^{-2} + 12 \cdot HF \rightarrow 4 \cdot GaF_3 + 12 \cdot {SO_4}^{-2} + 12 \cdot H^+ + 3 \cdot O_2 \tag{2.2}$$

under the presence of UV and Pt catalysts.

2.9 Dry Etching

Dry etching combines chemical and physical reactions based on plasma energy and etch chemistry [235]. Dry etching is used as it is anisotropic, and like wet etching, it is needed to fabricate different geometry on β-Ga_2O_3 for devices. β-Ga_2O_3 has a strong bond that requires significant energy to overcome. Hence, high-density/energy plasma etching techniques are required, there are a couple of suitable plasma etching techniques [236]. These include Electron Cyclotron Resonance (ECR), which operates at microwave frequencies, inductively coupled plasma (ICP), and Magnetron RIE (MRIE), which operates at Radio Frequency (RF). ICP is a commonly used plasma etching technique because it has a fast etch rate and causes lower damage to the surface material [237]. Due to the bonding in

Chemical	β-Ga_2O_3	Rate $nm \cdot min^{-1}$	Comments	Ref
85% H_3PO_4	(100)	100	At 160°C	[226]
97% H_2SO_4	(100)	100	At 175 °C, issue above 190°C.	[226]
47% HF	UID-(100)	0.9783	At room temperature.	[227]
47% HF	UID-(001)	0.5217	At room temperature.	[227]
5M KOH	Sn-($\bar{2}$01)	75	At 80°C, in PEC	[228]
5M KOH	Sn-(010)	22.5	At 80°C, in PEC	[228]
32% HCl	Sn-α	30	At 60°C.	[234]
20% NaOH	(100)	0.0867	At 60°C	[227]

Table 2.2: Different wet etchants for β-Ga_2O_3 at different conditions. The dopants and orientation of the β-Ga_2O_3 are displayed as well as the etch rates vary depending on both. Note, PEC stands for photo enhanced chemical etching.

β-Ga_2O_3, it is likely that ion-assisted etching will be required for a practical etch rate. The plasma-induced damage in β-Ga_2O_3 is of n-type character and thus will increase the conductivity of the etched surface. Shi et al. [238] demonstrates that H-plasma treatment of β-Ga_2O_3 can be utilised to improve the conductivity dramatically but also to help passivate defects. This treatment has been employed to improve the properties of n-type Ohmic contacts [239]. Um et al. [240] investigated dry etching of α-Ga_2O_3, this was with an ICP. The gases investigated were CF_4/Ar and SF_6/Ar, and they found that SF_6/Ar had the highest etch rate. Shah et al. [241] investigated the temperature dependence of β-Ga_2O_3 with ICP-RIE etching for Cl-based etching (BCl_3/Ar and Cl_2/Ar), there was very little temperature dependence with a slight uptake at around 75°C, which was attributed to the same mechanism seen in Cl etching into Al_2O_3, which was seen in [242]. As part of the study performed by Shah et al. [241] etch rates were also investigated for the ICP-IRE O_2/Ar, SF_6/Ar, CHF_3/Ar, Cl_2/Ar and BCl_3/Ar looking at the selectivity of ($\bar{2}$01) β-Ga_2O_3 to SiN_x. Temperature dependants were also investigated on ($\bar{2}$01) β-Ga_2O_3 etch rate between 22-205°C with Cl_2/Ar and BCl_3/Ar. An increase in etch rate was observed, which was speculated to be because of sublimation of $GaCl_3$, increasing the surface of β-Ga_2O_3 which can take part in the reaction. They also looked at the concentration of Cl in a mixture of BCl_3 + Cl_2/Ar and its effect on etch rate. It was found that the etch rate decreases with increasing Cl_2 percentage, at around 50%, the rate decrease considerably. It was found that this etching in β-Ga_2O_3 is similar to Al_2O_3 rather then GaN. The selectivity is critical as it is necessary to determine effective hard masks for use in etching β-Ga_2O_3 otherwise, the directional nature of the plasma etching is not practical. This search for masks is difficult due to the strong bonds in β-Ga_2O_3. These require high plasma density/energy, eroding the masks altered [236]. The photoresist can be used as a mask. However, Yang et al. [243] found that the selectivity needed to be higher, as this selectivity was deemed impractical. Okumura and Tanaka [244] used Ni as a hard mask, and the selectivity was found to be favourable, at a ratio of approximately 6. However, this then creates the issue of stripping the mask post-etch, which was performed using piranha solution, which was also used to help smooth the post-etch damage. RIE BCl_3/Ar is often employed to lower the contact resistance as it increases the doping in the surface states. Okumura and Tanaka [244] investigated the etch rates for (010) β-Ga_2O_3 comparing BCl_3 and Cl_2 ICP-RIE etching. It was found that a ratio of 1:1 of BCl_3:Cl_2 resulted in smoother side walls after etching rather than BCl_3. It was found that a ratio of 1:1 with 10 sccm produced a smoother finish than 20 sccm. The etch rate increased with higher ICP-RIE power, and the sidewall roughness was also found to be independent of the power. Man-Kyung et al. [245] found BCl_3 etch chemistry has the lowest etch rate on (100) orientated β-Ga_2O_3, this was where N_2

was used as the carrier gas with a ratio of 25/15 sccm. It was found that ($\bar{2}01$) was etched faster than (010), which was faster than (100), which was concluded to be due to low rates of Ga-O bond breaking and a lack of dangling bonds on the surface.

Work by Wang et al. [246] investigated the damage induced to the surface states by dry etching. They explored different post-etch treatments, such as annealing in O_2 and piranha solution. The sample etched was an epilayer of UID (001) β-Ga_2O_3 grown with HVPE on top of a highly doped substrate, which was etched with ICP using 40 W where BCl_3 as the enchant, which was performed for 20 minutes. The O_2 anneal was at 900°C for two hours, and the piranha solution was at 90°C for 3 minutes. Schottky diodes were fabricated to investigated the interface states and it was determined that the combination of treatments effectually reduced the trapped states. It was found that the O_2 anneal affected the surface electronic structure of the β-Ga_2O_3. Similarly Lee et al. [247], considered sulphuric acid and hydrogen peroxide mixture 1:1 H_2SO_4:H_2O_2 and tetramethyl ammonium hydroxide (TMAH) post-dry etching with BCl_3/Cl_2 Inductively Coupled Plasma-Reactive Ion Etching (ICP-RIE) etching. These were both at 25% held at 90°C for 5 minutes. They found that TMAH was the most effective, but both sulfuric acid and hydrogen peroxide mixture (SPM) and TMAH reduced the surface roughness, see Table 2.4. It was found that the process with TMAH removes the dry etch damage without leaving residue.

Table 2.3: Different dry etching on β-Ga_2O_3 along with information on the nature of the β-Ga_2O_3 (were known) and the conditions of the etch. The ratio A:B or the sccm A/B of the etchant gas is also given. It is generally found that doped β-Ga_2O_3 has slower etching than UID. Where found, the selectivity was also stated, as this is important for hard mask choice. Horizontal lines represent it was performed as part of a different study.

Plasma	**β-Ga_2O_3**	**Rate** $\mathbf{nm \cdot min^{-1}}$	**Comments**	**Ref**
BCl_3	Sn-(010)	40	ICP-RIE, ICP power, bias power, cooling temperature, and pressure were 150 W, 30 W, 20°C, and 0.6Pa respectively. Ni hard mask had a selectivity 6.	[244]
1 : 1 BCl_3:Cl_2	Sn-(010)	80	Same as above.	[244]
1 : 1 BCl_3:Cl_2	Sn-(010)	40	ICP-RIE power 150 W. BCl_3 gas flow, bias power, cooling temperature, and pressure were 10 sccm, 30 W, 20°C, and 0.6 Pa respectively.	[244]
1 : 1 BCl_3:Cl_2	Sn-(010)	100	ICP-RIE power 400 W. Rest is the same as above.	[244]
5 : 15 SF_6/Ar	Sn	30	Flow rate total 20 sccm, ICP 2 MHz, upper/down RF source was 600/150 W, pressure was 1.5 Pa.	[248]
BCl_3	UID-(010)	12	ICP source/bias power 200/30 W, 15 mTorr	[249]
20/2 CF_4/O_2	UID-(010)	1.5	Same as above.	[249]
15/5 BCl_3/SF_6	UID-(010)	3.1	Same as above.	[249]
5/15 BCl_3/O_2	UID-(010)	2.3	Same as above.	[249]

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Table 2.3 – Continued From Previous Page

Plasma	β-Ga_2O_3	Rate $nm \cdot min^{-1}$	Comments	Ref
35/5 BCl_3/Ar	UID-($\bar{2}$01)	160	Almost vertical sidewalls, 350/60 W ICP/RIE, 5 mTorr.	[250]
30/30 O_2/Ar	Sn-($\bar{2}$01)	15.5	Pressure 1 Pa, ICP/RF power 500/30 W. SiN_x selectivity 0.06.	[250]
50/10 SF_6/Ar	Sn-($\bar{2}$01)	8.5	same as above, SiN_x selectivity 0.03.	[250]
50/10 CHF_3/Ar	Sn-($\bar{2}$01)	11.1	same as above, SiN_x selectivity 0.04.	[250]
50/10 Cl_2/Ar	Sn-($\bar{2}$01)	16.1	same as above, SiN_x selectivity 0.12.	[250]
50/10 BCl_3/Ar	Sn-($\bar{2}$01)	135	same as above, SiN_x selectivity 2.7.	[250]
50 SF_6	UID	16	RIE 200 W, 13.56 MHz and 3.5×10^{-2} Torr	[251]
15/5 BCl_3/Ar	UID-(−201)	69.2	ICP/RF 400/200, 2 MHz	[243]
15/5 BCl_3/Ar	UID-(−201)	12.1	ICP/RF 150/15, 2 MHz	[243]
25/15 BCl_3/N_2	(100)	52	ICP/RF 300 W, −100 DC bias 13.56 MHz	[245]

Process	Surface Roughness (nm)
As Grown	0.5
Post ICP-RIE etch	3.5
SPM treatment	2
TMAH treatment	< 0.5

Table 2.4: Surface Roughness on β-Ga_2O_3 as grown, and after ICP-RIE etching and post-etch wet etching treatment. This is recreated from work by Lee et al. [247]. This demonstrates that post-dry etching steps reduce surface roughness by wet etching.

Table 2.5: Different samples, doping, pretreatment, and band bending.

Sample	N cm^{-3}	Pre-treatment	Band Bending (Bulk to vacuum) eV	Ref
($\bar{2}$01) β-Ga_2O_3	10^{18}	-	+0.12	[252]
($\bar{2}$01) β-Ga_2O_3	10^{18}	600°C for 15 minutes	+0.82	[252]
($\bar{2}$01) β-Ga_2O_3	10^{18}	NaOH	+0.27	[252]
($\bar{2}$01) β-Ga_2O_3	10^{18}	NaOH 600°C for 15 minutes	+0.47	[252]
($\bar{2}$01) β-Ga_2O_3	10^{18}	(100°C) H_2SO_4	+0.07	[252]
($\bar{2}$01) β-Ga_2O_3	10^{18}	(100°C) H_2SO_4 600°C for 15 minutes	+0.93	[252]
($\bar{2}$01) β-Ga_2O_3	10^{18}	wet O_2	−0.02	[252]
($\bar{2}$01) β-Ga_2O_3	10^{18}	wet O_2 600°C for 15 minutes	+0.33	[252]
(100) β-Ga_2O_3	10^{18}	-	+0.28	[253]
(100) β-Ga_2O_3	10^{18}	800°C for 30 minutes	+0.48	[253]
($\bar{2}$01) β-Ga_2O_3	10^{18}	-	+0.26	[254]

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Table 2.5 – Continued From Previous Page

Sample	N cm^{-3}	Pre-treatment	Band Bending (Bulk to vacuum) eV	Ref
$(\bar{2}01)$ β-Ga_2O_3	10^{18}	attached nitrophenyl	+0.77	[254]
$(\bar{2}01)$ β-Ga_2O_3	10^{18}	attached octadecylphosphonic acid	−0.10	[254]
(010) β-Ga_2O_3	10^{18}	-	−0.12	[254]
(010) β-Ga_2O_3	10^{18}	attached nitrophenyl	+0.41	[254]
(010) β-Ga_2O_3	10^{18}	attached octadecylphosphonic acid	−0.109	[254]
$(\bar{2}01)$ β-Ga_2O_3	10^{18}	-	− 0.2	[254]
$(\bar{2}01)$ β-Ga_2O_3	10^{18}	200°C for 30 minutes	− 0.2	[254]
$(\bar{2}01)$ β-Ga_2O_3	10^{18}	400°C for 30 minutes	− 0.1	[254]
$(\bar{2}01)$β-Ga_2O_3	10^{18}	600°C for 30 minutes	− 0.05	[254]
$(\bar{2}01)$ β-Ga_2O_3	10^{18}	800°C for 30 minutes	− 0.25	[254]
(001) β-Ga_2O_3	10^{16}	-	0.91	[246]
(001) β-Ga_2O_3	10^{16}	BCl_3 ICP etch	1.23	[246]
(001) β-Ga_2O_3	10^{16}	BCl_3 ICP etch, piranha	1.15	[246]
(001) β-Ga_2O_3	10^{16}	BCl_3 ICP etch, piranha, 900°C for 120 minutes in O_2	1.78	[246]
(001) β-Ga_2O_3	10^{16}	BCl_3 ICP etch, 900°C for 120 minutes in O_2, then piranha cleaned	1.78	[246]

2.10 Background Semiconductor Physics

In the following subsections, charge carriers, the band diagram, Metal-Insulator-Semiconductor and impact ionisation will be discussed. After this section it will move onto metal contacts to semiconductors and β-Ga_2O_3, parts of this section should be defined before metal contacts are discussed. The subsection on charge carriers, CV models and band diagram is to define equations and background used later on. The subsection on hetero-junctions explains some of the issues, and potential uses of hetero-structures. Impact ionisation subsection provides additional reasons as to why β-Ga_2O_3 should be investigated. ;

2.10.1 Metal-Insulator-Semiconductor

A Metal-Insulator-Semiconductor is a type of structure which can be modelled. An equivalent circuit model where parallel plate capacitors can be made to model MIS and Schottky capacitors, which can characterise the structure. This is where a potential is applied to a metal gate, due to a insulative layer or a Schottky barrier the current is blocked. This electric field then affects the charge carriers in the underlying semiconductor, either enriching the layer or depleting the layer. When enriching charge is accumulating on either side of the interface, this is viewed as a single capacitor. This is called the accumulation or oxide capacitance, in this work accumulation capacitance (C_A). As the polarity

of the charge switches and the charge carriers are pushed from the interface into the semiconductor, depleting the semiconductor layer. This can be modelled as a second capacitor in series with the first, this is depletion or semiconductor capacitance. C_A, this is where, instead of depleting the charge carriers and before reaching the flat band condition, the dominant charge carriers are drawn to the dielectric layer as the gate is applying the opposite charge. This creates a structure that can be viewed as a parallel plate capacitor. This is the case as the voltage is brought to the flat band voltage, called the accumulation region. After this, as it goes from flat band to threshold voltage, the band diagram is bent and causes the relative position of the Fermi level to change, depleting the charge carriers causing the depletion region. This can also be viewed as a parallel plate capacitor as the charge that is being displaced is pushed into the bulk material, so there is another layer of charges that builds up. This means that a MIS structure can be modelled as two parallel plate capacitors in series [255], one across the insulating layer which is given by,

$$C_I = \frac{\epsilon_0 \epsilon_I A}{W}. \tag{2.3}$$

Where ϵ_0 is the permittivity of free space, ϵ_I is the relative dielectric constant of the dielectric layer (insulator), A is the area of the parallel plate (of the capacitor) and W is the thickness of the insulting layer. As the voltage applied to this capacitor changed, the charge changed in the semiconductor, this was the effect of inverting the natural charge, causing a region to deplete charge. This depletion region acts like another insulating layer and is the second capacitor given by,

$$C_S = \frac{\epsilon_0 \epsilon_S A}{W_{eff}}. \tag{2.4}$$

Where ϵ_S is the relative dielectric constant of the semiconductor layer and W_{eff} is the effective width of the deletion region in the semiconductor. W_{eff} is defined by,

$$W_{eff} = \frac{t\epsilon_S}{\epsilon_D}\left(-1 + \sqrt[2]{1 + \frac{V_g}{V_\delta}}\right) \tag{2.5}$$

where t is the thickness of the dielectric layer, V_δ is defined by,

$$V_\delta = \frac{q}{2}\frac{\epsilon_S t^2}{\epsilon_D{}^2 \epsilon_0} N. \tag{2.6}$$

where N is the carrier concentration. These equations (2.3 and 2.4) result in the total being given by,

$$\frac{1}{C_T} = \frac{1}{C_I} + \frac{1}{C_S}, \tag{2.7}$$

which can be rearranged into,

$$C_T = \frac{S_S C_I}{C_S + C_I}. \tag{2.8}$$

This is often expressed as,

$$\frac{C_T}{C_I} = \frac{C_S}{\frac{C_S}{C_I} + 1}. \tag{2.9}$$

Equation 2.8 refers to the total and 2.9 the normalised capacitance.

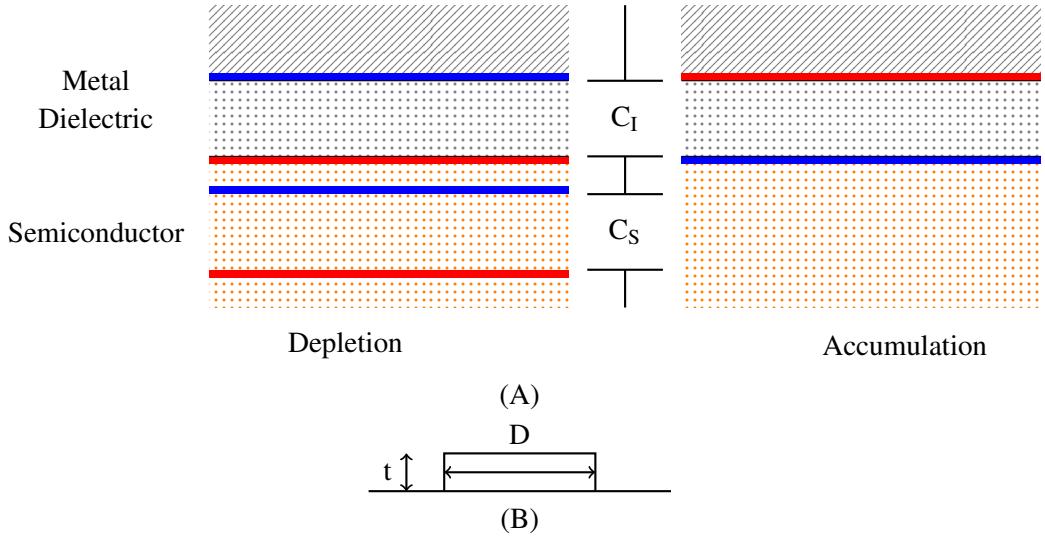

Figure 2.6: In subfigure (A) diagram of the charges in a MIS structure as a potential is swept, causing going from accumulation (on the right) and depletion (on the left) with the equivalent circuit drawn in the middle. Where C_I is the capacitance due to the dielectric layer and C_S is the capacitance due to the depletion region in the semiconductor. (B) an example of the contact used with a dielectric thickness of t and diameter of (D).

MIS interfaces have been investigated on β-Ga_2O_3. Matsubara et al. [256], investigated the Al/GeO_2/Ge MIS structure, where they incorporated PDA and PMA over an extended time period. It was found that an extended PMA could be relevant to this work as the PMA performed were 200-400°C for 30 minutes, it was found that in the range 300-400°C in forming gas H^+ or N_2 increased the D_{it}. This showed it was a thermal effect which was believed to be an effect on the Al electrodes rather then the GeO_2/Ge portion of the structure as PDA did not have the same effect. This conclusion seems to disagree with what was found in this work, where an increase of D_{it} was observed, believing to be a result of some degradation of the gate electrode. As the gate electrodes were different here, Al compared to Ti this could explain the difference or perhaps the capping and overlayers employed in this work adequately resisted the degradation which could have occurred.

Zhang et al. [257], investigated MIS capacitors on (001) β-Ga_2O_3 , with thermal ALD Al_2O_3. In this work the Al_2O_3 was deposited at 300°C where the precursors were tri-methyl-aluminum (TMA) and H_2O. In the worked performed by Zhang et al. [257], the gate electrode was formed by evaporating Ni on the topside, and the ohmic contact by evaporating Al onto the backside. The β-Ga_2O_3 was pretreated by piranha cleaning and PDA, the piranha clean was believed to introduce hydroxyl groups onto the surface of the β-Ga_2O_3. This promotes the initial growth of Al_2O_3 layers due to the mechanism described in Section 3.1.7. The piranha cleaning may also remove valence defects which can act as trapped charge. Zhou et al. [258], decreased D_{it} down to 2.3×10^{11} $cm^{-2} \cdot eV^{-1}$. This was on (−201) β-Ga_2O_3, with a combination of PDA and piranha cleaning. Piranha cleaning was shown to smooth the surface of the β-Ga_2O_3, reducing the RMS of the surface 0.26 → 0.17 nm. This reduced the hysteresis 0.45 → 0.1 V, after a PDA of 500°C, which was observed in both N_2 or O_2 atmosphere, this PDA was for period of 2 minutes. They found that the O_2 anneal was more effective at reducing the D_{it}, 3.3×10^{11} $cm^{-2} \cdot eV^{-1}$ to 2.3×10^{11} $cm^{-2} \cdot eV^{-1}$ N_2/O_2. It has been demonstrated by Shibata et al. [259], that a small change in carbon contamination can lead to a significant optoelectronic effect increasing the D_{it}. This makes quantifying the percentage of carbon responsible for these changes challenging. The D_{it} appeared to lower with annealing for both samples with Al_2O_3 having a lower D_{it} then SiO_2. This improvement was unexpected as MIS capacitors Hiroshi et al. [256], found that for GeO_2Ge an increase in D_{it} was seen after post mentalisation anneal, this was attributed to the degradation of the metal contact. This was because it was observed after a 300°C annealing post-metallisation but not observed post-deposition anneal.

2.10.2 Band Diagram

The background justification for the equivalent circuit refers to enriching or depleting the underlying semiconducting layer, the effects of applying a potential to the gate to the band diagram can be seen in Figure 2.7. In a Schottky contact rather than a MIS the barrier is from the metal-semiconductor work function rather than the insulate layer, however, the same principles apply and n and p type semiconductors have their respective band diagram. As this work is interested in β-Ga_2O_3 the description for n-type material will be used, however, p-type material follows the same ideas but with the polarity reversed. This band diagram is formed from the metal and semiconductor work function, there are three regions, accumulation, depletion and inversion/deep depletion.

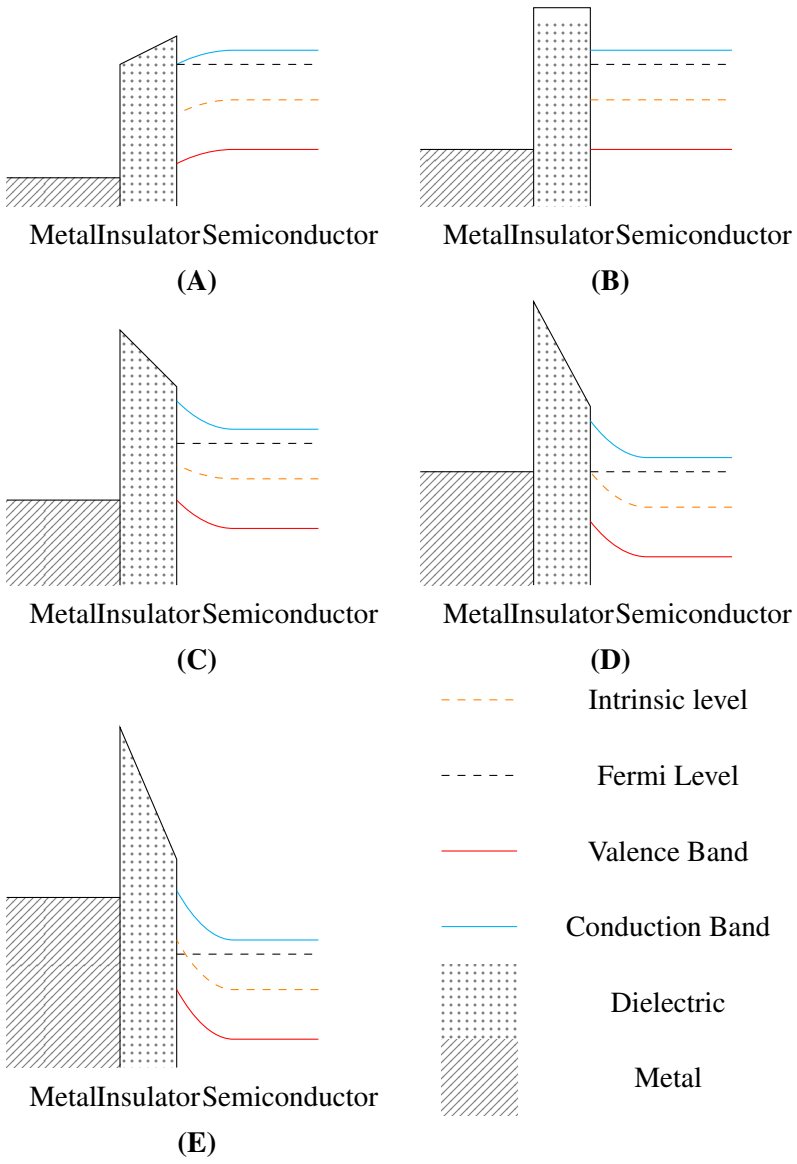

Figure 2.7: The schematic different band stages for a MIS interface. This is considering a n-type substrate, with a metal/p-type gate. The band diagram for the semiconductor is shown where, red line is the valence band, the blue line the conduction band, the green line the intrinsic and black dashed line the Fermi level. As the gate passes from positive bias to negative bias it passes though **(A)** to **(E)**. Sub-figures (B) and **(D)** are transition points flat band and threshold respectively, occurring at flat band voltage (V_{FB}) and threshold voltage (V_{Th}). Sub-figures **(A)**, **(C)** and **(E)** are the accumulation, depletion and inversion regions respectably. These bands are created with respect to the vacuum level and work functions.

In the ideal case, when the applied potential (V_A) is equivalent to the barrier height, this is the flat band conduction / flat band voltage (V_{FB}). This is given by,

$$V_{FB} = \phi_{m'} - \phi_{s'}, \tag{2.10}$$

[260]. This is when the applied potential is zero, for a band diagram of this. As a positive potential is applied to the metal negative charge is drawn from the semiconductor towards the interface, in an n-type material this enriches the layer as the charge carrier concentration increases. This is the origin of the accumulation capacitance and the first of the parallel plate capacitors, this can be found by forcing the capacitor further into accumulation. While as the potential increases the accumulation slowly increases but reaches a saturation point, this can be used to estimate the accumulation capacitance. S. Kar [261] proposed a way to estimate the accumulation capacitance from the c intercept from fitting the function f(C) in the accumulation region. The function f(C) is given by,

$$f(C) = C^{-\frac{1}{2}} \sqrt[2]{\frac{dC}{dV}}. \tag{2.11}$$

As the polarity shifts from positive to negative then a positive charge is drawn from the semiconductor towards the interface, this causes the dominant charge carrier to be repulsed from the interface. This depletes the a region into the semiconductor with a new negative layer beyond it, this acts as the second capacitor in the equivalent circuit model. As this is pushed further it results into either deep depletion or inversion. As the potential continues to change and the bands keep bending, the E_F is drawn more to the midpoint E_i, between the E_C and E_V, and so the charge carriers become depleted. Eventually, the bands are bent so far that the E_i is drawn below E_F, and the region is inverted. This is where the dominant charge carriers and the opposite from the bulk material, and is defined as the threshold voltage V_{th} see Figure 2.7.

$$V_{th} = V_{FB} + 2\phi_b + \frac{\sqrt{4qN\epsilon_S \phi_b}}{C_A} \tag{2.12}$$

where,

$$\phi_b = \frac{kT}{q} \log\left(\frac{N}{n_i}\right) \tag{2.13}$$

from [260]. The C_A is capacitative due to the accumulation of charge carriers and how this is modelled as a capacitor. However, this is in the ideal case, really there are additional charge present. This charge can be introduced during fabrication or operation. The flat-band voltage (V_{FB}) is really given by,

$$V_{FB} = \phi_{MS} + \frac{Q_F}{C_A} + \frac{Q_D}{C_A} + \frac{Q_M}{C_A} + \frac{Q_{it}}{C_A}, \tag{2.14}$$

from [262], where ϕ_{MS} is the metal-semiconductor work function, Q_F is the fixed charge, Q_D is the charge within the dielectric, Q_M is the mobile charge and Q_{it} trapped. Q_F fixed charge is a charge which is fixed very close to the interface, so it is considered a part of it. For this work, Q_D is used rather than Q_O, for the same reason as the MIS/MOS terminology. From the historical point of view

the dielectric was an oxide on a semiconductor, but the term gets strange when the dielectric and semiconductor are both oxides. This is the charge which is distributed throughout the dielectric layer. Q_M is mobile charge, these are charges which are mobile and move across the dielectric layer. Q_{it} is the charge which is at the interface and has trapped within an energy state. It is worth explaining trapped states at this point, these are caused by defects which create possible energy states which can exist, with an energy level which exists within the band gap. A diagram showing what is meant by this can be seen in Figure 2.8.

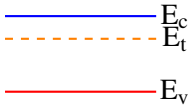

Figure 2.8: Diagram showing an example trapped state existing within band gap of the semiconductor, where E_c and E_v are the conduction and valence and E_c is the energy level of the trapped state. These trapped states are caused by a defect in the material.

2.10.3 Hetero-Junction Band Structure

While homo-structure does not require an introduction as most semiconductor devices are inhomogeneous homo-structure, any Si device with p and n junctions hetero-structure uses different semiconductors to create this inhomogeneity. Hetero-structures are junctions between different materials, which may be doped as p or n-type. This hetero-structure has quite a few different features from a homo-structure. As opposed to homo-junctions, the work functions are different relative to the vacuum level that determines what acts as a p or n-type material, and this is interesting as it opens the way for n-n or p-p diodes in a similar vein as Schottky diodes where they are unipolar devices as the barrier height caused by ΔE_{Con} or ΔE_{Val} are similar to Schottky barriers [263]. When the semiconductors are brought into contact with one another, as with a homojunction, the work functions reach equilibrium, and so the bands are bent. The material result as the band gaps and work functions are different, which means there are three types of junctions resulting from this:

- Type-1: Where the narrow bands are within the wider, called straddling junction.
- Type-2: Where the bands step up from one into the other, called step junction.
- Type-3: Where there is a brake in the band gaps, called a broken junction.

The Hetero-junction types can be seen in Figure 2.9 [263].

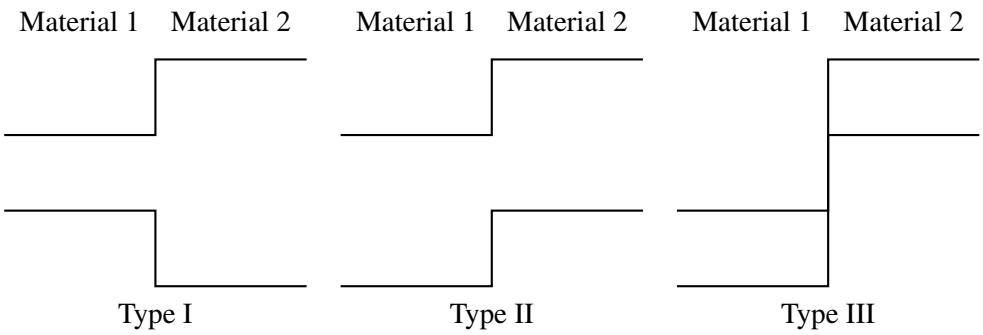

Figure 2.9: Diagram of the three different profiles of hetero-junction form, which is considered without band bending. Type I straddling, type II staggered, and type II broken. Named such because in type I, the one is encompassed by the other. In type II, they step from one to another and in type III it is broken [260].

The lattice matching is also a significant consideration in hetero-structure. If the lattices do not match well, then this causes many interface traps, which become increasingly a problem the thicker the layer [260] [264], and ideally a hetero-structure should be the same crystal form and match to 50% [263]. The lattice mismatch causes stress to be introduced into the structure as it deforms to match the substrate. The lattice mismatch is defined as,

$$\Delta \equiv \frac{|a_e - a_s|}{a_e} \tag{2.15}$$

where a_e and a_s are the lattice coefficients of the epitaxy and substrate layers respectively [260]. An empirical relation for the critical thickness,

$$t_c \approx \frac{a_e}{2\Delta} \tag{2.16}$$

t_c is the point where the strain in the film is too much, causing dislocations at the interface and relaxing the film. Lattice mismatching not only applies to semiconductors but also to dielectric layers, a form of hetero-structures, this is relevant later.

The mismatch between Si and β-Ga_2O_3 causes (100) orientation is preferred, with a buffer layer of TiN (111) (-201) β-Ga_2O_3 with a mismatch of Δ of 0.76% [265]. The lattice mismatch between c-GaN/(100) β-Ga_2O_3 is approximately 2.6% [266] [267]. On thicker films of β-Ga_2O_3 Fedor Hrubišák et al. [268], found 4H-SiC to have a mismatch of1.3% with Si and diamond with mismatches of 20.8% and 14.8% respectively. The growth and processing of each structure should be performed to try and limit the unintended doping caused by diffusion or process from the growth, impurities in each material but also the materials themself [263]. This applies to processing prior to, affecting the surface, during, such as epaxial growth, or after, such as metal contacts or annealing. There is also the management of heat, such as how the impurity's diffuses in the material, and how the materials expand and contract as the temperatures change, not only for the junction but also everything it is connected to [263].

2.10.4 Band Diagram For a Hetero-Junction

This section uses a lot of information from Heterojunctions and Metal-Semiconductor Junctions [263], to begin with the work functions of the two materials has to be calculated. Each semiconductor separately, where E_v is zero and E_c is equal to E_g, the E_f needs to be calculated. The term δ is defined, this is the energy between the E_f and E_v/E_c (p/n). In a non-degenerate semiconductor,

$$\delta = \frac{K_b T}{q}\left(2^{\frac{-3}{2}\frac{N}{\eta}} + \log\frac{N}{\eta}\right) \tag{2.17}$$

where η is η_v/η_c for p/n type. Where as for a degenerate semiconductor,

$$\delta = E_g - \left(E_i \mp \frac{K_b T}{q}\log\frac{N}{n_i}\right) \tag{2.18}$$

for p/n types. Where E_i is the intrinsic energy level. E_i is,

$$E_i = \frac{E_g}{2} + \frac{K_b T}{q}\log\frac{\eta_v}{\eta_c} \tag{2.19}$$

and the intrinsic carrier concentration (n_i) is,

$$n_i = \sqrt[2]{\eta_v \eta_c}\, e^{-\frac{qE_g}{2K_b T}}. \tag{2.20}$$

η is the effective density of states, for either the conduction or valence bands (η_c/η_v). This is calculated by,

$$\eta^* = 2M\left(\frac{4k_b T \pi^2 m^* m_e}{\hbar^2}\right)^{\frac{3}{2}} \tag{2.21}$$

where m^* is the effective hole/electron mass for the valence/conduction band, and M is the number of conduction/valence band minima/maxima. These allow for estimating the E_f, with respect to E_v being zero, however, to compare the two, there has to be a common reference. This is the E_{Vac}, and this is used because it is defined as zero for all materials, from χ and δ then ϕ can be calculated, this is performed for both materials, which can be drawn with reference to E_{Vac} being zero.

2.10.5 Determining the Band Structure

If the work functions is known then the potential difference between them can be calculated as,

$$\Delta\phi = \phi_i - \phi_j = V_D, \tag{2.22}$$

which is the built-in potential between materials i and j. As this is not a homo-junction, the bands are not continuous across the junction, only the vacuum band is. To model this bending in the vacuum band V_D is spilt into,

$$V_D = V_{Di} + V_{Dj}, \tag{2.23}$$

where each component is given by,

$$V_{Di/j} = \frac{qN_{i/j}{x_{Bi/j}}^2}{2\epsilon_{i/j}}, \tag{2.24}$$

where x_B is the distance from the junction to the bulk material. Hence,

$$\frac{V_{Di}}{V_{Dj}} = \frac{2q\epsilon_j N_i {x_{Bi}}^2}{2q\epsilon_i N_j {x_{Bj}}^2}. \tag{2.25}$$

As,

$$\frac{N_j}{N_i} = \frac{x_i}{x_j}, \tag{2.26}$$

then Equation 2.25 this can be re-written as,

$$V_{Di} = \left(\frac{N_j\epsilon_j}{N_i\epsilon_i}\right)V_{Di}. \tag{2.27}$$

This can then be substituted into Equation 2.23 to get,

$$V_D = \Delta\phi = \left(1 + \frac{N_j\epsilon_j}{N_i\epsilon_i}\right)V_{Dj}, \tag{2.28}$$

Rearranging and substituted into Equation 2.24 then $V_{Di/j}$ can be calculated as,

$$V_{Dj/i} = \frac{\Delta\phi}{(1 + \frac{N_{j/i}\epsilon_{j/i}}{N_{i/j}\epsilon_{i/j}})} = \frac{\Delta\phi(N_{i/j}\epsilon_{i/j})}{N_{i/j}\epsilon_{i/j} + N_{j/i}\epsilon_{j/i}}, \tag{2.29}$$

This means the depletion into each region can be calculated.

Rearranging 2.29 them the depletion region can be calculated as,

$$x_{Bi/j}{}^2 = \frac{2\epsilon_{i/j}V_{Di/j}}{qN_{i/j}}, \tag{2.30}$$

so,

$$|x_{Bi/j}| = \sqrt[2]{\frac{2\epsilon_{i/j}V_{Di/j}}{qN_{i/j}}}, \tag{2.31}$$

and the total depletion width is then found by,

$$W_{total} = |x_{Bi}| + |x_{Bj}|. \tag{2.32}$$

Now that the bulk depletion width components are known, the vacuum level across the junction can be calculated. A note on convention here: choosing an appropriate reference point is vital. In this work, the default maximum of the vacuum level was set to zero. So the band bending is going from zero into being negative, therefore considering which semiconductor has the highest ϕ that was considered the starting position. This is for each material the E_f and ϕ are set and ϕ to E_{Vac} is continues across the junction. Going forward, this is going to be $\phi_i > \phi_j$, defining x = 0 to be the junction with x positive into i and negative into j. With these defined then the E_{Vac}, This describes the E_{Vac}, from this on each side of the junction E_C, E_V and E_f can be calculated and plotted in respect to the E_{Vac} from the relevant χ, E_g and ϕ. At the junction, the Conduction and Valence bands are not continuous. The ideal conduction and valence band offsets are,

$$\Delta E = \begin{cases} \chi_j - \chi_i, & \text{Conduction} \\ \Delta E_g - \Delta E_c & \text{Valence} \end{cases} \tag{2.33}$$

In the case of a homo-junction then both ΔE_c and ΔE_v are both 0. Experimentally, the band offsets are different from this ideal model, considerations such as Fermi-level pinning are also a factor. For more accurate modelling the band diagram these values should be taken from the experimentally determined values if they are known for that particular junction. A diagram showing an example of this can be seen in Figure 2.10.

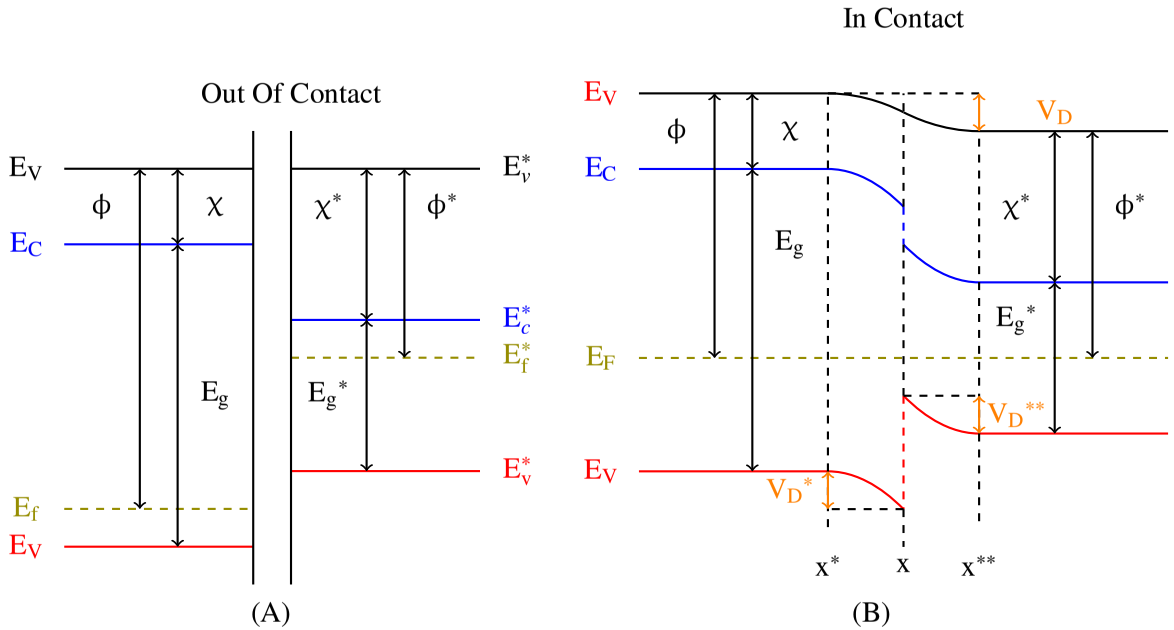

Figure 2.10: The energy band diagrams of the two materials out of and in contact, (A) and (B) respectively. Where E_v is the vacuum level, E_c is the conduction band, E_f, E_g is the band gap, E_v, χ is the electron affinity, ϕ is the work function, V_D is the total diffusion voltage. The E_v, E_c, E_f, E_v, E_g, ϕ and ϕ are denoted with *. $V_D{}^*$ and $V_D{}^{**}$ and the components from material one and two which form V_D. x is the point the two materials meet, and the bands bend x^* into material one and x^{**} into material two.

2.10.6 Impact Ionisation

One of the main motivations for investigating β-Ga_2O_3 is its high critical electric field strength, the electric field strength which can be applied to a semiconductor before undergoing Avalanche breakdown. This enables β-Ga_2O_3 based devices to operate at higher reverse voltages before they fail, this is highly desirable for power electronic devices. This was mentioned earlier when discussing Bailgia figure of merit, however, here a more mathematical expression of this can be shown by the impact ionisation of β-Ga_2O_3. Currently β-Ga_2O_3 is limited to n-type material, with n^- drift regions to support the electric field. The mechanism behind avalanche breakdown is impact ionisation, where the applied electric field provides the energy to cause a cascade of charge carriers pairs being generated. β-Ga_2O_3 high critical electric field strength means that it can withstand higher reverse voltages before this cascade can occur. The generation of electron/hole pairs due to impact ionisation is given by,

$$G_{np} = \alpha_{in}\mu_n n + \alpha_{ip}\mu_p p \tag{2.34}$$

In [269] Chynoweth put forth the idea that the ionisation can be expressed as,

$$\alpha, \beta = a \exp^{-\frac{b}{E}} \tag{2.35}$$

where a and b are consents, following the same for the ionisation in gases. This was further refined to,

$$\alpha, \beta = a \exp^{-\left(\frac{b}{E}\right)^c} \tag{2.36}$$

[270]. This empiric formulation is often used to express impact ionisation α in semiconductors. Fulop [270] put forth a empirical formula for the ionisation coefficient in the form of,

$$\alpha \approx CE^g \tag{2.37}$$

where C and g are materials specific. This relatively simplistic approximation is found by fitting this expression to the 2.35. Fulop [270] calculated it for Si where they argued that $\alpha_{\text{hole}} \approx \alpha_{\text{electrons}}$ and obtained the expression

$$\alpha_F \approx 1.8 \times 10^{-35} E^7. \tag{2.38}$$

Later Baliga [5] following the same kind of approximations for 4H-SiC getting the result

$$\alpha_B \approx 3.9 \times 10^{-42} E^7 \tag{2.39}$$

There have seen some work determining this for β-Ga_2O_3, the power fitting for the impact ionisation for β-Ga_2O_3 has been performed. Wentao Meng fitted flops power law for β-Ga_2O_3 [271] to get,

$$\alpha = 9.5 \times 10^{-45} E^7 \tag{2.40}$$

[271] using Chynoweth parameters calculated by Krishnendu and Uttam [272], these were,

$$\alpha = 2.52 \times 10^6 e^{\frac{-3.9\times10^7}{E}}. \tag{2.41}$$

Using the same parameters in this work the fitting was,

$$\alpha = 1.2 \times 10^{-44} E^7 \tag{2.42}$$

Using the Chynoweth parameters calculated Sugiura and Nakano [273] the,

$$\alpha = 4 \times 10^5 e^{\frac{-3.1\times10^6}{E}}, \tag{2.43}$$

where the fitting in this work was,

$$\alpha = 4.22 \times 10^{-38} E^7 \tag{2.44}$$

The fittings performed here can be seen in Figure 2.11.

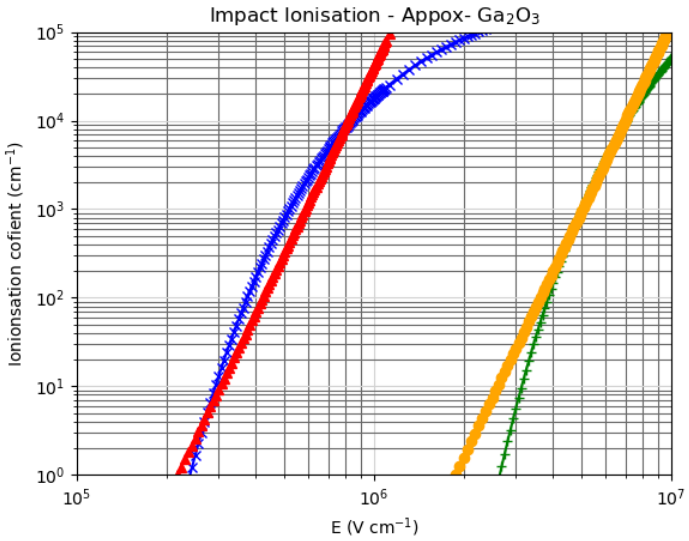

Figure 2.11: The plotted Chynoweth & Fulop expressions for the ionisation at avalanche breakdown for β-Ga_2O_3. The Chynoweth constants where taken from [272] and [273]. The blue cross and green + are Chynoweth expressions, red triangle and orange circle are Fulop expressions for electrons and holes respectively.

The multiplication factor is defined as the number of electron-hole pairs generated as it moves. Considering a N^+ and a p^- junction, an e^- and e^+ pair is generated, the two charges travel towards the N^+ and p^- regions respectively. As they travel, they will generate αdx βdx e^- and e^+ pairs through the depleted regions on either side of the junction. This is x though the N region and W_{del} through the p-region, the total number of e^- and e^+ pairs generated is given by the multiplication coefficient,

$$M(x) = 1 + \int_0^x \alpha M(x)dx + \int_0^{W_{dep}} \beta M(x)dx \tag{2.45}$$

where α and β is the ionisation rate for electrons and holes respectively [274]. Mc Intyre [274] showed that this can be differentiated to,

$$\frac{d}{dx}M(x) = \alpha M(x) + \beta M(x) = (\alpha - \beta)M(x), \tag{2.46}$$

meaning that Equation 2.45 can be expressed as,

$$M(x) = M(0)e^{\int_0^x (\alpha-\beta)dx} \int_0^x \alpha M(x)dx, \tag{2.47}$$

where,

$$M(0) = \frac{1}{1 - \int_0^{W_{dep}} \beta e^{\int_0^x (\alpha-\beta)dx} dx}. \tag{2.48}$$

This can be expressed as,

$$M(x) = \frac{\int_0^x e^{\int_0^x (\alpha-\beta)dx}}{1 - \int_0^{W_{dep}} \beta e^{\int_0^x (\alpha-\beta)dx} dx}, \tag{2.49}$$

if e^- and e^+ are generated in equal amounts then, while not strictly true it is necessary to,

$$\alpha = \beta, \tag{2.50}$$

then,

$$e^{\int_0^x (\alpha-\beta)dx} = e^{\int_0^x (\alpha x - \beta x\,x|_0)dx} = e^0 = 1, \tag{2.51}$$

$$M(x) = \frac{1}{1 - \int_0^{W_{dep}} \beta dx}. \tag{2.52}$$

In avalanche breakdown a e^-/e^+ pair generate more pairs which causing a cascade of carriers. This occurs when,

$$M(x) \rightarrow \infty, \tag{2.53}$$

which is when,

$$1 - \int_{x_0 - x_{d1}}^{x_0 + x_{d2}} \beta dx \rightarrow 0, \tag{2.54}$$

is true so when,

$$\int_{x_0 - x_{d1}}^{x_0 + x_{d2}} \beta dx \rightarrow 1. \tag{2.55}$$

So to calculate this at avalanche we set,

$$\int_{x_0 - x_{d1}}^{x_0 + x_{d2}} \beta dx = 1, \tag{2.56}$$

If the junction has a highly doped n to a lowly doped p, we can assume that the depletion into the n region is negligible and the entire deletion occurs within the p region. This means that,

$$x_0 - x_{d1} = 0, \tag{2.57}$$

and,

$$x_0 + x_{d2} = W_{del,Ava}. \tag{2.58}$$

In turn be can replace the bounds of the integral to be,

$$\int_0^{W_{del,Ava}} \beta dx = 1, \tag{2.59}$$

using the approximation that,

$$\beta \approx \beta_E = aE^7, \tag{2.60}$$

substituting Equation 2.60 into Equation2.59,

$$1 \approx \int_0^{W_{del,Ava}} \alpha_E dx = \int_0^{W_{del,Ava}} aE^7 dx. \tag{2.61}$$

As the E is related to x from the interface to W_{del} ,

$$E(x) = \frac{qN}{\epsilon_0 \epsilon_s}\left(W_{del} - x\right). \tag{2.62}$$

By differentiating Equation 2.62,

$$\frac{dE}{dx} = \frac{qN}{\epsilon_0 \epsilon_s}, \tag{2.63}$$

this can be rearranged into,

$$dx = \frac{\epsilon_0 \epsilon_s}{qN} dE, \tag{2.64}$$

which can be substituted into Equation 2.61 in order to get,

$$1 = \int_0^{W_{del,Ava}} aE^7 \frac{\epsilon_0 \epsilon_s}{qN} dE. \tag{2.65}$$

Looking at Equation 2.62 it can be said that,

$$\begin{aligned} E(0) &= \frac{qN}{\epsilon_0 \epsilon_s}\left(W_{del,Ava} - 0\right) = \frac{qNW_{del,Ava}}{\epsilon_0 \epsilon_s} \\ E(W_{del,Ava}) &= \frac{qN}{\epsilon_0 \epsilon_s}\left(W_{del,Ava} - W_{del,Ava}\right) = 0 \end{aligned} \tag{2.66}$$

Equation 2.66 which can be used to change the bounds of the integral seen in Equation 2.65 into,

$$1 = \int_{\frac{qNW_{del,Ava}}{\epsilon_0 \epsilon_s}}^{0} aE^7 \frac{\epsilon_0 \epsilon_s}{qN} dE. \tag{2.67}$$

This can be rewritten as,

$$1 = \frac{\epsilon_0 \epsilon_s}{aqN} \int_{\frac{qNW_{del,Ava}}{\epsilon_0 \epsilon_s}}^{0} E^7 dE, \tag{2.68}$$

which can further be arranged into,

$$\frac{aqN}{\epsilon_0 \epsilon_s} = \int_{\frac{qNW_{del,Ava}}{\epsilon_0 \epsilon_s}}^{0} E^7 dE. \tag{2.69}$$

This can then be integrated into,

$$\frac{aqN}{\epsilon_0 \epsilon_s} = \frac{E^8}{8}\Bigg|_{\frac{qNW_{del,Ava}}{\epsilon_0 \epsilon_s}}^{0}. \tag{2.70}$$

This can be evaluated into,

$$\frac{aqN}{\epsilon_0 \epsilon_s} = \frac{q^8 N^8 {W_{del,Ava}}^8}{8{\epsilon_0}^8 {\epsilon_s}^8} - 0 = \frac{q^8 N^8 {W_{del,Ava}}^8}{8{\epsilon_0}^8 {\epsilon_s}^8}, \tag{2.71}$$

This can be arranged into,

$${W_{del,Ava}}^8 = \frac{8a{\epsilon_0}^7 {\epsilon_s}^7}{q^7} N^7, \tag{2.72}$$

which can rewritten as,

$$W_{del,Ava} = \sqrt[8]{\frac{8a{\epsilon_0}^7 {\epsilon_s}^7}{q^7}} N^{\frac{7}{8}}. \tag{2.73}$$

Relating the depletion width at avalanche breakdown to the doping consent, based off estimation ionisation coefficient to electric field strength. This means that the E_{Cr} for avalanche can be written as,

$$E(0, Ava) = E_{Cr} = \frac{qN}{\epsilon_0 \epsilon_s}\left(W_{del,Ava}\right), \tag{2.74}$$

substituting Equation 2.73 into this,

$$E_{Cr} = \sqrt[8]{\frac{8^7 a^7 q}{\epsilon_0 \epsilon_s}} N^{\frac{15}{8}}. \tag{2.75}$$

In the same manor the breakdown voltage V_{br} can be calculated,

$$V_{br} = \int \frac{qN}{\epsilon_0 \epsilon_s}\left(W_{del,Ava}\right)dx = \frac{qN}{\epsilon_0 \epsilon_s}\left(W_{del,Ava}\right)^2, \tag{2.76}$$

by substituting Equation 2.73 into this to get,

$$E_{Cr} = \sqrt[8]{\frac{8^{14} a^{14} {\epsilon_0}^6 {\epsilon_s}^6}{q^6}} N^{\frac{23}{8}} \tag{2.77}$$

An approximation of the critical breakdown field strength, using the fitted values for the impact ionisation coefficients it is possible to calculate this for β-Ga_2O_3. This section was to demonstrate that due to the material properties of β-Ga_2O_3, β-Ga_2O_3 based devices theoretically can withstand higher voltages before undergoing avalanche breakdown. This is important for aspect for power electronics, which desires devices to withstand high voltages without failing. While other mechanicians exist for device failure avalanche breakdown one of the most appropriate for high voltage applications. In Figure 2.12 the plots showing the depletion width, electric field strength and breakdown voltage as a function of doping can be seen for Si, 4H-SiC, GaN and both fittings for β-Ga_2O_3. While the fitting performed here shows β-Ga_2O_3 underperforming to GaN, 4H-SiC the fitting performed in [271] shows it out performs them. In both cases it significantly out performs Si, and the accuracy of the fitting in the initial Chynoweth and Fulop equations. The fitting performed here is likely erroneous and overly underperforms, this will likely improve as more experimental data is generated and more fittings are performed.

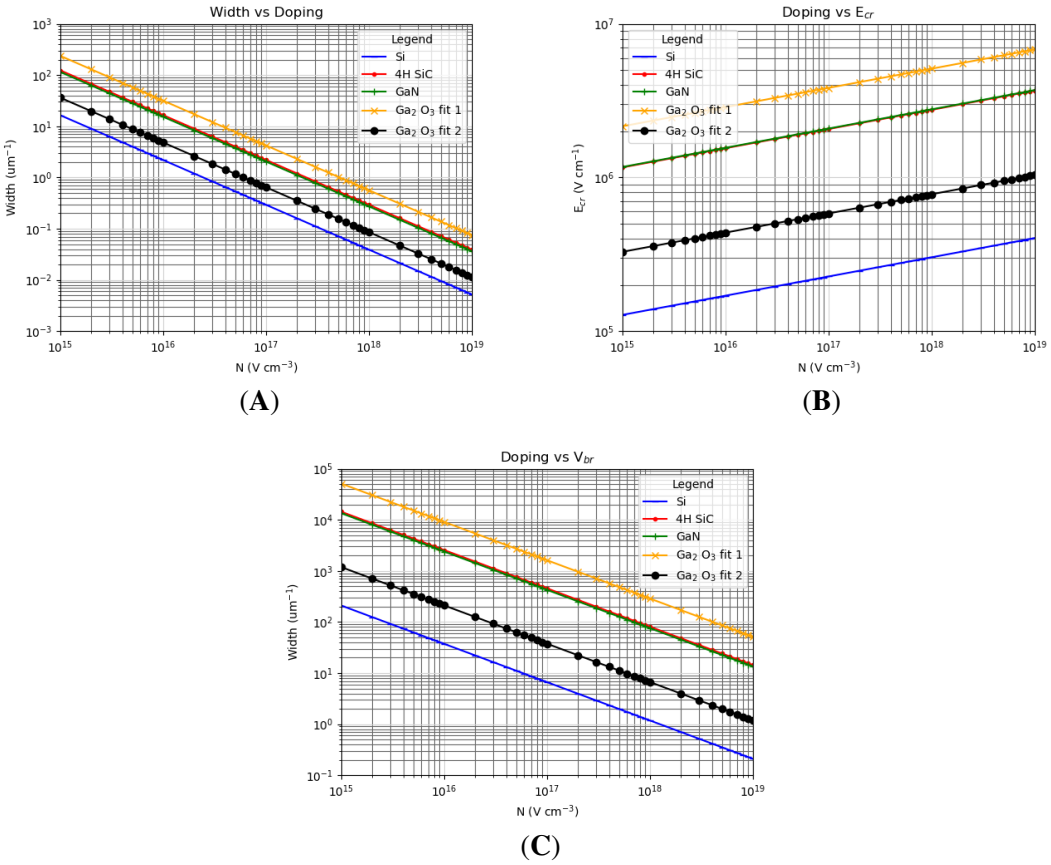

Figure 2.12: The maximum depletion width (**A**), the maximum critical breakdown field (**B**) and theoretical breakdown voltage (**C**). This is for Si, 4H-SiC, GaN and two different fitting for β-Ga_2O_3.

2.11 Metal Contacts to β-Ga_2O_3

Metal contacts to semiconductors either form ohmic or Schottky contact, where it is based upon the metal work function and the electron affinity. This is because when the two come into contact, the difference will create a barrier to overcome. The nature of this barrier will cause the material to either behave like an ideal ohmic contact, in which there is "no" barrier or Schottky, where the barrier has to be overcome. The metal-semiconductor ideally follows the Schottky Mott Rule, this section is to describe this and a diagram in Figure 2.13. Considering the two materials separated when the vacuum level is 0, as the materials come into contact with one another and the Fermi level E_F reaches equilibrium, this results in the vacuum level (E_{Vac}) being bent by a potential from 0. This potential is given by,

$$V = \phi_M - \phi_S, \tag{2.78}$$

where V is the potential difference from the vacuum level of the metal to the semiconductor, ϕ_M is the metal work function and ϕ_S is the semiconductor work function. It should be noted that the E_{Vac} maximum should be 0 eV, and so the whole diagram should be shifted to reflect this. The E_{Vac} within the semiconductor is bent by this V across distance x_{lim} the energy bands in the semiconductor are bent with x_{lim} given by,

$$x_d = \sqrt{\frac{2\epsilon_s\epsilon_v|V|}{qN_c}}, \tag{2.79}$$

where x_d is the bend length, ϵ_s is the semiconductor dielectric, ϵ_v is permittivity of free space, q is the electron charge and N_c is the carrier density. There is no potential inside the metal as the dielectric consent is ∞. In the semiconductor at x_d and beyond the energy band diagram is unchanged, as the it moves (x) from x_d towards the interface the band starts to bend. The conduction band bends following,

$$E_c(x) = E_c + V(x), \tag{2.80}$$

and valence band E_v is,

$$E_v(x) = E_v + V(x), \tag{2.81}$$

where V(x) is,

$$V(x) = \frac{qN_c(x)^2}{2\epsilon_s\epsilon_0}. \tag{2.82}$$

It should be noted that this is band bending relative to the Fermi level E_{fermi}. For current to flow from the metal to the semiconductor, depending on electrons (n-type) or electron hole (p-type) current the barrier is ϕ_{BC} (ϕ_{BV}) from metal to E_c (E_v) where,

$$\phi_{BC} = \chi_s + E_g - \phi_m, \tag{2.83}$$

and,

$$\phi_{BV} = \phi_m - \chi_s. \tag{2.84}$$

This barrier height is also effected by charges which build up at the metal-semiconductor contact which causes a slight lowering of the barrier height. this is given by,

$$\phi_{IFL} = \sqrt[2]{\frac{q\epsilon_M}{4\pi\epsilon_s}}, \tag{2.85}$$

where,

$$\epsilon_M = \sqrt[2]{\frac{2qN(\phi_B - V - \frac{k_bT}{q}\log(\frac{N_c}{N}) - \frac{k_bT}{q}}{\epsilon_s}}. \tag{2.86}$$

The reason this is of interest is because this means the work function of the metal and doping play an important role in the formation of ohmic contacts. This helps show why,

2.12 Current Transport

The barrier height determines the nature of the current transport, and hence from this if the contact behaves ohmic or Schottky contact. There are three ways the current is transported thermionic, field emission and thermionic-field emission, where thermic and field thermionic describe the Schottky case and field emission the ohmic behaviour. As described at the metal-semiconductor junction there is a barrier which is formed, this is the Schottky barrier height. In thermionic emission the charge carriers have to have the energy to overcome the barrier height, this limits the current transport and means that it is temperature dependant. This is what is dominates in Schottky contacts where a potential applied to this contact provides the energy to allow movement. This is dominant when the barrier height is high and the depletion width is long hence low doping. To contrast this is field emission, this is where the charge carriers tunnel through the barrier rather than over coming the barrier. This is independent of temperature, and describes the Ohmic contacts.

This is caused by a low barrier height and short depletion width, hence high doping which means that there are many charge carriers near the junction which allow for tunnelling. The intermediate between these two is rather unimaginatively named thermionic-field emission, where both aspects play their roles into the current transport. The result of this in regard for this work is that, for an ohmic contact it ideally should have a barrier height which is zero however in practice a low barrier height is suitable. This is dependent on other factors than the metal work function but also the surface states and the interface.

Thermionic emission, this is where the charge carrier has to over come the barrier height. This is dominant when the barrier height is high, the temperature is high and the semiconductor carrier concentration is low.

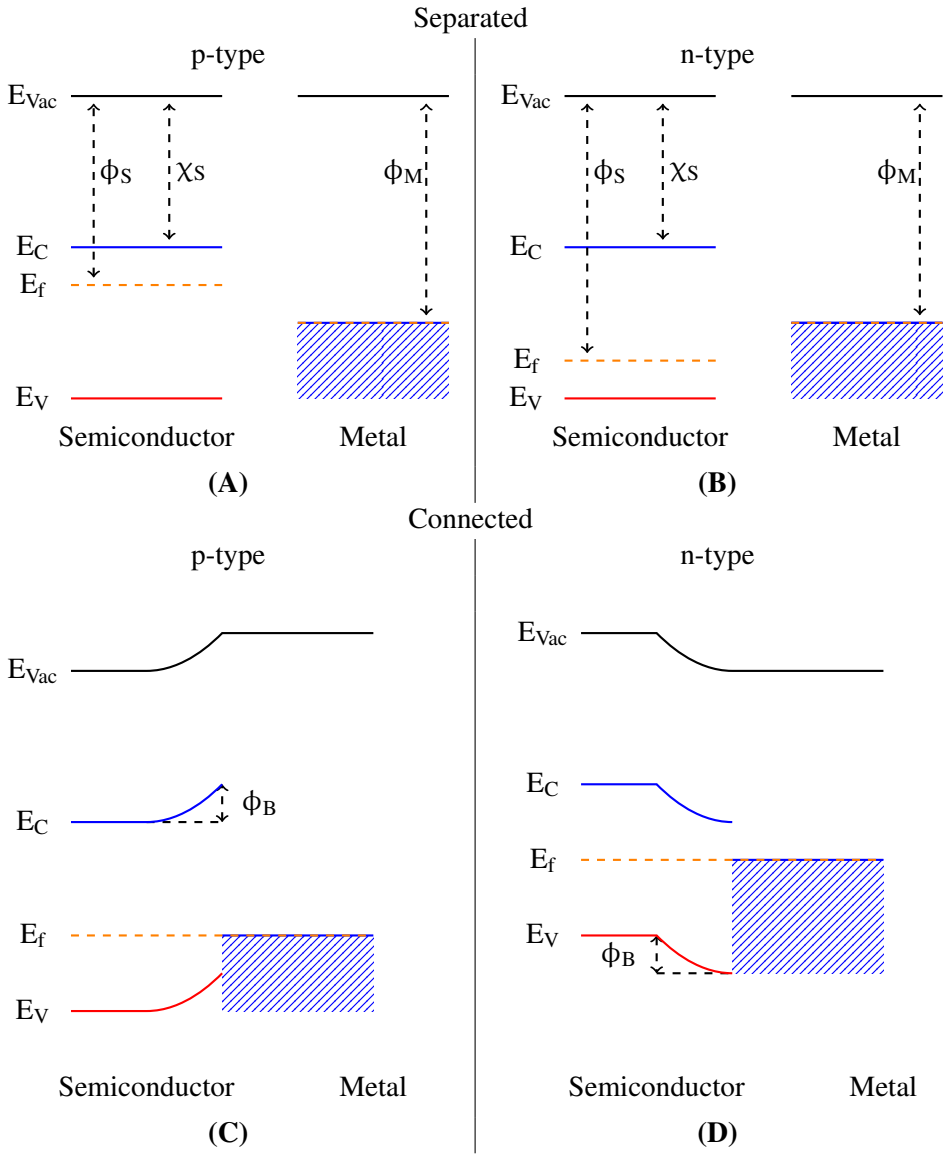

Figure 2.13: Band diagrams describing what happens to the band diagram at the metal semiconductor interface. Where the metal is on the right hand side and the semiconductor on the left. In **(A)** and **(B)** show out of contact and **(C)** and **(D)** are in contact, **(A)** and **(C)** are for n-type semiconductor and **(B)** and **(D)** are p-type. The Fermi level is shown in E_f, the conduction band in E_C, the valence band in E_V and the vacuum level in solid E_{Vac}. ϕ_S is the work function of the semiconductor, χ_S is the electron affinity of the semiconductor, ϕ_M is the metal work function and ϕ_B is the barrier height.

2.13 Ohmic Contacts

Ohmic contacts act as if there is no barrier height to overcome, so the voltage-current is linear. It was shown in the previous section that this is highly dependent on the semiconductor-metal barrier height and doping. This illustrates the need to control doping and surface treatments on β-Ga_2O_3 to forum Ohmic contacts. As the electron affinity of β-Ga_2O_3 is 4 ± 0.05 eV [275], the ideal work

function of the contact should be below or near to this to form an ohmic contact. Ohmic contacts on wide bandgap semiconductors are more challenging than their narrow counterparts as nearly all metals form Schottky contacts [4]. This limits the ideal metals to Ti (4.33 eV), Ag (4.26 eV), In (4.1 eV), Zr (4.05 eV), Sc (3.5 eV), La (3.5 eV), and Gd (2.9 eV). Yao et al. [276] investigated some of these metal contacts, on (201) β-Ga_2O_3, where the morphology and electrical characteristics as-deposited, and after annealing, between 400-700°C, it was found that Zr/Au, Sn/Au, Ag and Ag/Au were shown to be pseudo ohmic. Yao et al. [276] suggested that the surface states are dominant, transforming Shottky to Ohmic contacts rather than the choice of metal. Sc did not appear as ohmic even after annealing, it was found that Zr/Au, Ag, Ag/Au and Sn/Au as deposited were measured to be pseudo ohmic, which degraded after annealing. Sn surface morphology dewetted even in the as-deposited state and after annealing, whereas Ag was pseudo ohmic as deposited, but dewetted after annealing, a capping layer of Au did not change this. Zr/Au did not dewetted as deposited or after annealing. It appears ohmic after annealing, however, the surface dewetted as-deposited and melted with the annealing, and a capping layer of Au did not appear to alleviate this. Ti/Au forms an ohmic contact and is the common ohmic contact, despite the fact that it should form a low Schottky barrier. The Ga_2O_3-metal interface plays a vital role in determining the nature of the contact. The exact alloying and metal stack are essential for optimising contact resistance for ohmic contacts, an example can be seen on AlGaN/GaN [277]. The development of ohmic contacts to β-Ga_2O_3 closely resembles that of GaN. These metal layers were outlined for GaN by Greco et al. [278] and are:

- Contact layer.
- Overlayer.
- Barrier Layer.
- Capping Layer.

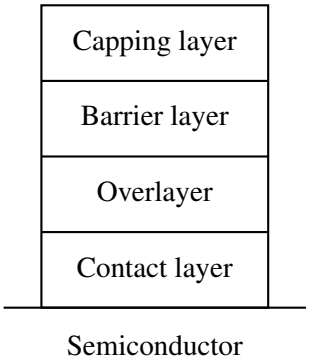

Figure 2.14: A diagram to illustrate the different layer of metal used in a contact, in a given contact not all layers are used. The contact layer is to bound to the semiconductor, it is to alloy to the overlayer to improve conductivity. The capping layer is to limit oxidation and to limit diffusion the barrier layer is used to prevent this.

Figure 2.14 illustrates these layer. Each layer is for a purpose, the contact layer is required in any contact, which adheres to the surface of the material. As it is in contact with the semiconductor, its work function should be close to the electron affinity to help form an ohmic contact. This layer forms an interfacial layer, in Si and SiC, these silicides impact the contact considerably, and are often formed after some metal deposition, and anneal to form the silicide. For β-Ga_2O_3, an interfacial oxide layer formed with Ti, Al, and Cr ohmic contacts, is based on the Gibes free energy, whereas Au and Pt don't [66]. The other layers are not necessary but are there to improve the contact. In β-Ga_2O_3, it is typical only to include the contact and the capping layer, predominantly Ti/Au. The capping layer's purpose is to limit oxidation to the surface and is highly conductive to make contact with, this is why common capping metals are Au and Ag. The two layers in between are the overlayer and the barrier layer.

The overlayer is to build on the contact and form compounds with the other metals with a low work function. This is also very important if the contact is annealed or is to work in high-temperature environments. This is because as the contact metals alloy and diffuse, the nature of the contact will naturally change.

The barrier layer is used to limit the diffusion of the capping layer into the rest of the metal contact. If the contact starts to alloy and diffuse, the capping metal no longer protects the surface, which is its purpose. Secondly, diffusion into the metal stack can change the work function and the nature of the contact. As a result, an ideal metal will have a low barrier height, with a high melting point and a low diffusion coefficient. Mohammed et al. [279] put forward that this layer also plays a role in affecting surface morphology and specific contact resistance. While the development of contacts in β-Ga_2O_3 is following a similar path to that of GaN, these design considerations and metal choice for them form an initial appropriate for β-Ga_2O_3 shown in Table 2.6.

Layer	**Metal**
Contact	Ti & Ta
Overlayer	Al
Barrier	Ti, Ni, Pt, Pd, Mo, Re & Au
Capping	Au

Table 2.6: Commonly used in metals for different layers in the fabrication of ohmic contacts onto GaN described by Greco et al. [278]. The development of metal contacts has followed a similar path to those of GaN, so similar metal/stacks will likely apply to β-Ga_2O_3.

While the exact metals for this process have yet to be determined for ohmic contact onto β-Ga_2O_3, different ohmic contacts, with their doping, metallisation and processing conductions as well as the specific contact resistance are shown in Table 2.8. It is worth noting that the most common ohmic contact is Ti/Au, however, Ti/Al/Au, Ti/Al/Ni/Au [239] [280] have been demonstrated. Another consideration is also how well the metal adheres to the surface of the β-Ga_2O_3, this is determined when the metal is deposited, what surface reactions occur and how it bonds to the surface. Pre-treatments affecting the surface, deposition methods, annealing, and contact metal are all critical to forming whether a contact is ohmic or not. This also affects the longevity of the contact depending on it is conditions. Ti is the most common contact metal, as the contact metal, meaning that at the interface, it is fabricating an interlayer of TiO_x. This is because Ti oxidises so readily, this is why it adheres to the surface of the β-Ga_2O_3.

All these considerations are regarding the metals, but pre-treatments to the surface are also important. Doping the surface or surface layer so that it is degenerate is highly beneficial in forming an ohmic contact, partly because it shortens the area of band bending into the semiconductor-metal junction, allowing more charge carriers to tunnel through, hence forming an ohmic contact.

Plasma etching, which induces damage to the surface, is known to improve ohmic contacts, this is attributed to it generating dangling bonds. Dangling bonds are incomplete chemical bonds on the surface, making them more prone to react with the contact layer, forming better contact. This has been shown by Zhou et al. [239] where a short plasma etch, 30 s Ar bombardment, to improved the n-type conductivity of the β-Ga_2O_3 and Higashiwaki et al. [41] where RIE BLC_3/Ar for 1 minute was performed prior to metallisation. Annealing is commonly done to fabricate ohmic contacts and comes in two formats. Prolonged, high-temperature, pre-deposition annealing is often used to activate dopants, these anneals are in the order of ≈ 1000°C for 15-30 minutes, this has been done in N_2 and O_2 atmospheres, and this anneal is to pre-treat the surface for the metal contact. The other commonly implemented anneal is raid thermal anneals (RTA), which are performed after the metal deposition to improve the as-deposited contact. It should be noted that there have been reports of long temperature annealing improving a 300°C [281], which was Ti/Au in Ar atmosphere, for 180 minutes. Post metalisation anneals have two effects, it improves the contact between the contact layer and the β-Ga_2O_3, it also alloys the metal stack. These anneals are normally, between 400-500°C for 1-2 minutes, often in N_2 or Ar_2. Longer and/or higher temperatures often degrade these metal contacts. Lee et al. [282] showed that TiO_2 was at the interface improving the morphology of the contact between the contact layer and β-Ga_2O_3. The TiO_2 interface is also why longer annealing times and higher temperatures can degrade these contacts, which is the continued growth of the TiO_2 layer. One way to limit the growth of TiO_2 is to limit the Ti layer deposited, Callahan et al. [283] demonstrated 5 nm Ti layer, which fully oxidised into TiO_2. The ohmic contact was thermally stable under a long 500+ hours at 600°C in N_2 environment. Lee et al. [282] attributed this to the diffusion of Ga out into the contact and of the metals (commonly Au) into the material. This diffusion of Au could show the need to develop different metal stacks to limit this. The orientation of the β-Ga_2O_3, also plays a role, Lee et al. [282] noticed that the optimum anneal was found to be 420°C for (100) rather a 470°C for (010). Apart from Ti, Indium doped Tin Oxide (ITO) or Allium doped Zinc Oxide (AZO) are used to form ohmic contacts. These are doped until they are degenerate, they often require long temperature annealing to form contact onto the β-Ga_2O_3, see Table 2.8 for these conditions. These require a metal contact to connect to these layers. Tetzner et al. [284] demonstrated TiW alloy has also been used as an ohmic contact to (100) β-Ga_2O_3, the cross-sectional TEM seemed to indicate an interlayer of TiO_x. Mg with an Au capping layers was able to fabricate an ohmic contact on $(\bar{2}01)$ β-Ga_2O_3 [285]. Mohamed et al. [275] demonstrated that an ohmic contact was formed by printing a thin eutecticGa-In (low melting point alloy of Ga-In).

Metal	Morphology	Ohmic	Issues
Sc	Continues, smooth	No	-
Zr	Continues, smooth as deposited, rough after annal	Pseudo	As deposited, only Zr/Au
In	Dewets	Yes	600°C anneal for 1 minute
Ag	Dewets	Pseudo	As deposited
Zn	Continues, rough	No	-
Ti	Continues, smooth	Yes	400 to 600°C anneal for 1 minute
Sn	Dewets	Pseudo	As deposited
W	Continues	No	-
Mo	Continues	No	-

Table 2.7: This is adapted from Yao et al. [276], investigation showing different metal contacts onto (201) β-Ga_2O_3. Looking at the nature of the contact and how the surface morphology changed.

Table 2.8: Different ohmic contacts to Ga_2O_3, this is predominately to just the β phase, however, some α will also be listed. These will be listed as ranges of different orientations on the β, as well as a range of different doping and pre and post-treatments to the material. While detailing all aspects is not necessary to convey much more information. R_s specific contact resistance, R_c contact resistance.

Contact	Doping cm^{-3}	Process	Comments	Ref
Au/Ti (300/50) - (010) β-Ga_2O_3	5×10^{19}	Si-implantation with pre-deposition anneal of 900 – 1000°C in N_2 for 30 minutes, post deposition RTA 450°C for 1 minute in N_2.	R_s 4.6×10^{-6} $\Omega \cdot cm^2$, ρ 1.4 mΩ · cm	[286]
Au/Ti (230/20) - (010) β-Ga_2O_3	5×10^{19}	Si-implantation with pre-deposition anneal of 925°C in N_2 for 30 minutes, post deposition RTA 470°C for 1 minute in N_2.	R_s 8×10^{-6} $\Omega \cdot cm^2$	[287]
Au/Ti (230/20) - (010) β-Ga_2O_3	5×10^{19}	solvent clean, Si-implantation with pre-deposition anneal of 925°C in N_2 for 30 minutes & BCl_3/Ar RIE for 1 minute, post deposition RTA 470°C for 1 minute in N_2.	R_s 8.1×10^{-6} $\Omega \cdot cm^2$	[288]
Au/Ti/(010) β-Ga_2O_3	5×10^{19}	Si-implantation with pre-deposition anneal of 950°C in N_2 for 30 minutes & BCl_3/Ar RIE for 1 minute, post deposition RTA 470°C for 1 minute in N_2.	R_c 0.25 $\Omega \cdot mm$, R_s 7.5×10^6 $\Omega \cdot cm^2$	[289]
Au/Ti/β-Ga_2O_3	1×10^{18}	Spin On Glass Sn 10^{21} cm^{-3} with pre-deposition anneal of 1200°C for 5 minutes BCl_3/Ar RIE for 1 minute, post deposition RTA 470°C for 1 minute in N_2.	R_s $2.1 \pm 1.4 \times 10^{-5}$ $\Omega \cdot cm^2$	[224]

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Table 2.8 – Continued From Previous Page

Contact	Doping cm^{-3}	Process	Comments	Ref
Ni/Au/Ti/(010) β-Ga_2O_3	$\approx 10^{19}$	Si δ doped BCl_3/Ar RIE pretreatment, post deposition RTA 470°C for 1 minute in N_2.	R_c 0.35 $\Omega \cdot$ mm, R_s 4.3×10^{-6} $\Omega \cdot cm^2$ R_{Sh} 320 $\Omega \cdot \square^{-1}$	[290]
Au/Ti/AZO 80/20/10) (−201) β-Ga_2O_3	$\approx 10^{19}$	Si implantation with pre-deposition anneal of 950°C, post deposition RTA 400°C for 30 s in N_2.	R_c 0.42 $\Omega \cdot$ mm, R_s 2.82×10^{-5} $\Omega \cdot cm^2$	[291]
Au/Ti/ITO (80/20/140) - (−201) β-Ga_2O_3	$\approx 10^{-19}$	Si implantation with pre-deposition anneal of 950°C, post deposition RTA 500-600°C for 30 s in N_2.	R_s 6.3×10^{-5} $\Omega \cdot cm^2$	[292]
Au/Mg (600/820) - ($\bar{2}$01) β-Ga_2O_3	4×10^{17}	solvent & piranha clean, post deposition RTA 300-500°C for 2 minutes in Ar	R_s $2.1 \times 10^{-5} \Omega \cdot cm^{-2}$	[285]
Au/Ti/AZO (80/20/10) - (−201) β-Ga_2O_3	$\approx 2.2 \times 10^{17}$	HCl clean, Si implantation with pre-deposition anneal of 950°C, post deposition RTA 300-600°C in N_2.	R_C 0.42 $\Omega \cdot$mm R_s 2.82×10^{-5} $\Omega \cdot cm^2$	[293]
Pt/Ti/ITO 140/100/140 - (010) β-Ga_2O_3	2×10^{17}	pre-deposition anneal of 800-1200°C in N_2, post deposition RTA 450-700°C in N_2 for 30 s.	-	[294]
Au/Ti (80/20) - (010) β-Ga_2O_3	3×10^{19}	solvent cleaned, Si implantation with pre deposition anneal at 950 and 975°C in N_2 for 30 minutes, RIE BCl_3, post deposition 470°C for 1 minute in N_2.	R_s 3.93×10^{-5} $\Omega \cdot cm^2$	[295]
Au/Ti (80/20) - (010) β-Ga_2O_3	3×10^{19}	solvent cleaned, Si implantation with pre deposition anneal at 950 and °C in N_2 for 30 minutes, RIE BCl_3, post deposition 470°C for 1 minute in N_2	R_s 1.51×10^{-4} $\Omega \cdot cm^2$	[295]

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Table 2.8 – Continued From Previous Page

Contact	Doping cm^{-3}	Process	Comments	Ref
Au/Ti (80/20) - (010) β-Ga_2O_3	1.8×10^{18}	solvent cleaned, post deposition 470°C for 1 minute in N_2., post deposition 470°C for 1 minute in N_2.	R_s 3.29×10^{-3} $\Omega \cdot cm^2$	[295]
Au/Ti (80/20) - (010) β-Ga_2O_3	1.8×10^{18}	solvent cleaned, RIE BCl_3, post deposition 470°C for 1 minute in N_2.	R_s 4.32×10^{-2} $\Omega \cdot cm^2$	[295]
Au/Ti (300/50) - (010) β-Ga_2O_3	10^{19}	Si implantation with pre deposition anneal at 900-1000°C in N_2, post deposition 450°C for 1 minute in N_2.	R_s 4.6×10^{-6} $\Omega \cdot cm^2$	[296]
TiW (150) - (100) β-Ga_2O_3	1×10^{19}	RIE VCl_3-Ar, post deposition RTA at 700°C.	R_s 1.5×10^{-5} $\Omega \cdot cm^2$	[284]
Al/Ti (100/20) - (100) β-Ga_2O_3	$10^{17} - 10^{18}$	annealed for 10 minutes in N_2		[297]
Ga-ZnO (201) β-Ga_2O_3	1.6×10^{18}	annealed for 10 minutes in N_2 at 500°C		[298]
Au/Ti (100/15) - (100) β-Ga_2O_3	2×10^{17}	annealed at 600°C for 1 minutes in N_2	wet chemical clean, E-beam	[299]
Au/Ti (80/20) - (100) β-Ga_2O_3	2.6×10^{18}	annealed at 370(420)°C, 1 min in N_2	R_C $1.47 \times 10^{-4}/2.49 \times 10^{-5}$ $\Omega \cdot cm^{-2}$, R_C 5.28/2.19 $\Omega \cdot$ mm, R_{Sh} 1900/1930 $\Omega \cdot \square^{-1}$.	[282]
Au/Ti (80/20) - (100) β-Ga_2O_3	2.8×10^{18}	annealed at 470(520)°C, 1 min in N_2	R_S $3.55 \times 10^{-5}/1.36 \times 10^{-3}$ $\Omega \cdot cm^{-2}$, R_C 2.38/14.57 $\Omega \cdot$mm, R_{Sh} 1590/1570 $\Omega \cdot \square^{-1}$.	[282]

2.14 Schottky contacts

As opposed to Ohmic contacts Schottky contacts, have a barrier at the metal-semiconductor interface. This has to be overcome, different Shottky contacts are shown in Table 2.9 with the barrier heights, as well as the method to measure them, the doping, the orientation all effect the barrier height. The most widespread contact is Ni.

Mohamed et al. [275] found the metal-β-Ga_2O_3 interface plays an important role, they found a barrier height of 1.07-1.01 eV by IV-PhotoEmission Spectroscopy (PES), however, from the Schottky-Mott rule, it should theoretically be 1.23 eV. The difference was attributed to interface states between the metal-β-Ga_2O_3, as they were confident it was not caused by other external factors. This is further demonstrated by Yao et al. [300], with two different studies. One was comparing different pre-treatments with the same Schottky metal Ni and comparing different Schottky metals onto the bulk ($\bar{2}01$) and epitaxial (010) with the same pre-treatment clean with HCl and H_2O_2. The work function of the metal did not have much of an impact, it was found W/Pd had a barrier height of 0.91 ± 0.09/1.05 ± 0.03 eV despite the work function being 1.1 eV different. Conversely comparing bulk (201) to epitaxial (010) for Pd the barrier height was $1.05 \pm 0.03/1.34 \pm 0.1$ eV. It was put forward that the surface state of Ga_2O_3, are more of a determining factor than the barrier height. This is also a point touched on when discussing the ohmic contacts to β-Ga_2O_3. Farzana et al. [301] saw a range of different barrier heights, indicating that Fermi level pinning is not the dominant feature, meaning more gate engineering is possible. Additional metals on the contact do play a role much like their ohmic counterparts. They can be characterised into the same ideal four layers. The capping and barrier layers play the same role as in the ohmic borders the contact layer has to adhere to the surface and is the most important when determining the barrier height of the contact. The overlayer, is to form compounds to tailor the desired work function, with another consideration being the resistance of the contact. By fabricating a polar contact to the top it has been possible to generate higher barrier height than the Schottky-Mott would suggest, with layers of Pd/CoO_2 barrier height of 1.8 eV have been achieved [302]. There are a number of possible polar oxides which could be used for this purpose, hence this is a possible avenue to approach [303]. For β-Ga_2O_3, metal-oxide based Schottky contacts have demonstrated a barrier height up to 2.5 eV [304], determined using CV method.

Table 2.9: Different metals which form Schottky contacts with Ga_2O_3, predominate on β phase. This is on a variety of different orientation of β-Ga_2O_3 The majority of these were onto bulk substrate.

Metal	**Material**	**Doping cm^{-3}**	**ϕ_B eV**	**Comment**	**Ref**
Au (20)	(100) β-Ga_2O_3	$10^{17} - 10^{18}$	1.2	IV, solvent, HF clean. E-beam deposition. ϕ_B decreased with annealing.	[297]
Au	(100) β-Ga_2O_3	10^{16}-10^{17}	1.07-1.01	IV/PES, Au was E-beam shadow mask.	[275]
Au	α-Ga_2O_3	10^{17}	1.7-2	Mist-CVD on α-Al_2O_3	[305]
Au	(010) β-Ga_2O_3		1.97-1.71	CV, IPE	[301]
Pt	"	"	1.53- 1.57	IV, IVT,	"
"	"	"	1.59-1.58	CV, IPE	"
Ni	"	"	1.50-1.52	IV, IVT	"

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Table 2.9 – continued from previous page

Metal	Materiel	Doping cm^{-3}	ϕ_B eV	Comments	Ref
"	"	"	1.54-1.54	CV, IPE	"
Pd	"	"	1.29	IV	"
"	"	"	1.28-1.27	CV, IPE	"
Ni	(100) β-Ga_2O_3	10^{16}-10^{17}	1.1 ± 0.1	IV	[87]
Ni	($\bar{2}$01) β-Ga_2O_3	5-8 × 10^{18}	0.87 ± 0.01	IV, organic	[300]
"	"	"	0.89 ± 0.01	IV, HCl	"
"	"	"	0.89 ± 0.01	IV, BOE	"
"	"	"	0.94 ± 0.01	IV, H_2O_2	"
"	"	"	0.90 ± 0.01	IV, BOE, H_2O_2	"
"	"	"	1.04 ± 0.02	IV, Lateral	"
"	"	"	1.16 ± 0.1	CV, Lateral	"
"	"	"	1.00 ± 0.06	IV, Vertical	"
"	(010)	"	1.08 ± 0.01	IV, Lateral, epi	"
Cu	($\bar{2}$01)	"	1.13 ± 0.1	IV, Lateral	"
W	"	"	0.91 ± 0.09	IV, Lateral	"
"	"	"	1.94 ± 0.1	CV, Lateral	"
"	(010)	"	1.05 ± 0.03	IV, Lateral, epi	
Ir	($\bar{2}$01)	"	1.29 ± 0.1	IV, Lateral	"
"	"	"	2.3 ± 0.4	CV, Lateral	"
"	(010)	"	1.40 ± 0.08	IV, Lateral, epi	"
Pt	($\bar{2}$01)	"	1.05 ± 0.03	IV, Lateral	"
"	"	"	1.9 ± 0.1	CV, Lateral	"
"	(010)	"	1.34 ± 0.01	IV, Lateral, epi	"
Cu	($\bar{2}$01)	1.6 × 10^{16}	1.36	IV	[298]
Pt	(010)	10^{17}	1.36-1.52	IV/CV	[306]
Pt	(001)	≈ 10^{16}	1.15-1.09	room temp/200°C, IV/CV in agreement	[307]
Pt	(100)	2.3 × 10^{14}	1.3-1.39	IV	[308]
W	(−201)	2 × 10^{17}	0.97-0.39	IV, 25-500°C	[309]
Mo	(100)	2 × 10^{17}	1.55 ± 0.186	IV, E-beam	[299]
($PdCoO_2$)	(−201)	7.8 × 10^{17}	1.8	IV, Layers of Pd/CoO_2, polar layer structure.	[302]

2.15 Diodes

The diode is the first device to consider, semiconductor diodes replaced the older vacuum rectifiers which started during the mid 20th century. While Si diodes surpassed vacuum rectifiers depending on the applications, as more materials mature, Si will be surpassed for specific uses.

There are reports of p-type β-Ga_2O_3, however, widespread, high-quantity, repeatable growth has been elusive. Without developing this p-type material, this limits the current development of Ga_2O_3 to semi-insulating and n-type doping. The lack of p-type material limits the devices which can be fab-

ricated and restricts the traditional homo-junction-based diode. As a result, there are currently only two types of junctions relevant to diodes: the Schottky junction, which avoids the need for p-type material altogether by using the semiconductor-metal interface. There are many Schottky contacts onto β-Ga_2O_3, and using this, there are Schottky diodes. An alternative is to use heterojunction-based designs, where two different semiconductors are used, the difference in the work function impacts the nature of the junction. This setup means it is possible to fabricate bipolar devices with β-Ga_2O_3, however, other considerations come into play. These designs often require large epitaxial drift n^- regions, this is to distribute the electric field helping to increase the breakdown voltage where as in an n^+ region this field is restricted to a small region causing breakdown to occur at a lower voltage. These can be grown with methods already discussed in previous sections.

There is some discussion of photo and light-emitting diodes, however, they are not the domain of power electronics. Schottky diodes are used in power electronics because they offer advantages over their bipolar counterparts. Schottky diodes do not rely on minority charge carriers, and there is no need to recombine the minority carriers. They also move directly from the semiconductor to the metal, resulting in less transition time and a lower turn-on voltage. These end with Schottky diodes, which have faster switching speeds and lower energy losses and are used to deal with high current density. β-Ga_2O_3 does not have simple access to p-type material, a pn junction, and traditional diodes are not realisable. The increase in efficiency means that the amount of heat generated is reduced, this is quite important for β-Ga_2O_3 considering it has poor thermal conductivity, as commented in Tables 1.1. In their simplest format, Schottky diodes require two contacts: an Ohmic and a Schottky contact. These were previously discussed in Sections 2.13 and 2.14. Schottky diodes based on Ga_2O_3 were demonstrated on both α-Ga_2O_3[234], [305], [310], [311]. β-Ga_2O_3 has received the most interest, however, α-Ga_2O_3, while not as stable as its β counterpart, α has a higher bandgap and is seconded only to the β phase in terms of stability. Oda et al. [305] fabricated vertical α-Ga_2O_3 Schottky diodes. This was achieved by growing α-Ga_2O_3 Schottky diodes epitaxial layers with MOCVD onto 4 inch α-Al_2O_3 substrate. These layers were then peeled off the substrate to realise a vertical device. Yang et al. [310] demonstrated α-Ga_2O3 Schottky diodes that were able to achieve V_{Br} up to 0.68 and 0.53 kV, which utilised a simple lateral structures and due to the high quality of the growth of the α-Ga_2O_3. The devices were fabricated on α-Al_2O_3 with cavities patterned into the underlying substrate, which affected the mist CVD deposition of the α-Ga_2O_3, leading it to be of high quality and crack-free. This metallisation was Pt for the Schottky contact and Ti/Au for the ohmic contact. Boldbaatar et al. [311] quasi-vertical α-Ga_2O_3 Schottky diodes were fabricated on α-Al_2O_3 substrates, these layers were grown with HVPE epitaxy. These had a Ti/Au and Ni/Au for the ohmic and Schottky metallisation, respectively. The ohmic contact was annealed at 500°C for one minute in N_2.

The diode without edge termination or guard rings that the V_{Br} was 0.21 kV, the temperature dependence of Ni as a Schottky contact was investigated by taking IV measurements between 100-425 K. The Ni contact was found to follow thermionic emission. β-Ga_2O_3 based diodes are more explored

than α-Ga_2O_3. The metal contact impacts the nature of the Schottky diode In the previous section, where different Schottky contacts were discussed, all impact the device fabricated. Most Schottky contacts are formed with Ni, with a barrier height around 1 eV. Polar metals have been used to increase the barrier height of the Schottky contact, in [302] $PdCoO_2$ was used as the contact to (-201) β-Ga_2O_3. This was discussed earlier where the barrier height was 1.8 eV, the diode was found to have an on/off ratio of 10^8 and was operational at temperatures up to 350°C. As mentioned before, these polar oxides are potential advancement for Schottky diodes, and there are many such polar oxides available to explore [303]. β-Ga_2O_3 forms rectifying contacts easily and with simple structures approach the theoretical unipolar limit for Si [312]. Xu et al. [128] fabricated lateral Schottky diodes with (-201) β-Ga_2O_3 grown with Mist-CVD onto Fe doped (0002) GaN/α-Al_2O_3 substrate. The resultant V_{Br} was 2.4 kV and a R_{on} of 40 $\Omega \cdot cm^{-2}$, Ti/Au and Ni/Au were used for the ohmic and Schottky contacts. Wang et al. [246], as part of their investigation for post dry-etching plasma treatments (see Section 2.9). Vertical Schottky diodes were fabricated on an epitaxial layer of UID (001) β-Ga_2O_3 grown with HVPE on a highly doped substrate. The contacts were deposited by electron beam evaporation. As part of the characterisation to determine surface states for the post-etch treatments, it was found that the diodes followed thermionic emission for all post-treatments.

To improve Schottky diodes, work has been performed to investigate the edge termination of the Schottky contact. There are different types of edge termination, which are all ways of managing the electric fields and current flow in the device. One approach to limiting the current is to fabricate insulating regions to limit the current flow through the device, which can be achieved in a couple of different ways. Zhou et al. [313] used ion implanted Mg to create a highly damaged structure which was semi-insulative, an increase in of approximately 1 kV for the B_{Br}, with a PFOM of 0.47 GW $\cdot$ cm^{-2} with a low $R_{on,sp}$ of 5.1 m$\Omega \cdot cm^{-2}$ was observed. Lin et al. [314] followed a similar approach where N_2 was implanted. In this work, they also investigated field plates leading to a matrix of four different structures which were investigated. Both Mg and N act as deep dopants, which create the semi-insulating region alongside the damage to the lattice. Another approach is to implant inert species to damage the lattice and create highly resistive regions. This was done with ion implantation He [315], which was compared He, Mg edge termination to no termination. It was found that the V_{Br} was 0.5 kV with no termination to 1/1.5 kV for He/Mg, demonstrating that Mg is more suitable for this purpose. Ar has also been shown to create a highly resistive region in the device, which was used as edge termination for a Schottky diode [316]. As opposed to damaging a region to generate an insulating region, depositing an insulating layer has been demonstrated by Dong et al. [317], where it was shown to outperform the 1D unipolar limit for SiC with a PFOM of 7.4-10.6 GW $\cdot$ cm^{-2}.

Plasma treatment, as stated in earlier sections affect the surface (states and structure) of β-Ga_2O_3, which affects the electrical characteristics. Hu et al. [318] terminated Schottky diodes using RIE CF_4. This was believed to impact the electric field in two ways. First, it introduced a negative charge along the surface, helping spread the electric field to avoid crowding at the edge of the contact. F is believed

to interact with Si impurities in β-Ga_2O_3 to form a neutral species [319] in the lattice, hence acting like the neutral species.

A field plate is where an insulative layer made from a dielectric material is deposited so that the metal contact (for the Schottky contact) overlaps with the dielectric. This will be discussed more in-depth later, as this structure is often referred to as an MIS/MOS structure. This generates an electric field across the dielectric layer. As mentioned earlier, when discussing ion implantation by Lin et al. [314], field plates were also investigated. SiO_2 deposited by PECVD was used to fabricate field plates onto β-Ga_2O_3, it was found that inclusion increased the V_{Br} from 0.75 kV to 1.38 kV with a field plate, which was improvement on the guard ring from the ion implantation 0.86 kV, the combination of both achieved 1.43 kV, this was no edge termination compared to Mg ion implantation. SiN_x has also been used to fabricate field plate structures to Schottky diodes [320], SiN_x/SiO_2 bilayers have also been used for field plate structures [321]. Al_2O_3/SiN_x has also been used as a bi-layer structure for field plate design [322]. Yang et al. [322] commented that one of their device's limitations was due to material defects. Devices that used large field plates were realised, achieving forward currents over 100 A [320] [323]. The large contact size and field plates used in these Schottky diodes, unfortunately, meant the impact of defects is more pronounced than in their smaller counterparts, this seems to have limited the effectiveness of the field plates [324] [322], [325], [326], [93], [327]. Al_2O_3 has also been used as a field plate with 3 kV, an R_{On} of 24.3 $m\Omega \cdot cm^{-2}$ and a PFOM grater then 0.37 $GW \cdot cm^{-2}$ with an anode-cathode spacing 24 μm. The field plate's size is used to fabricate these layers, where different dielectric materials and combinations change how the electric field is distributed. This is also related to the thickness of the dielectric layer(s) used in this fabrication, as both are factors in how they distribute the electric field. Lee et al. [328] put forward that high-k dielectrics as a way to manage the electric field in WBG materials in a simple way that limits the number of process steps to avoid dealing with the processing limitations which exist in WBG materials. In simulations by Liu et al. [329] they compared field plates (bevelled field plates, this will be discussed later) using SiO_2, Al_2O_3 and HFO_2. It was determined that the the higher-k dielectrics did increase the V_{Br} of the simulated Schottky diode. Field plates fabricated with high-k dielectrics have been found [330] using $BaTiO_3$ and bi-layers of $BaTiO_3$ and $SrTiO_3$, after annealing, it was believed to have intermixed into a single layer.

MIS capacitors were used to investigate these dielectrics, it was found that the intermixed layers, specifically the $BaTiO_3$ layers, increased the electric field into the β-Ga_2O_3 compared to no field plate. The intermixed $BaTiO_3/SrTiO_3$ was more effective than pure $BaTiO_3$, achieving a BFOM value of 1.47 $GW \cdot cm^{-1}$. It was found that between no FP, BTO FP and interlayer FP, the V_{Br} increase from 148 V, to 486 V, to 687 V Field plates can be etched or deposited so that they are not parallel to the Schottky contact but angled towards it, which means that the electric field inside the semiconductor is not as abrupt. Consequently, there are fewer crowding effects to the contact, increasing the V_{Br}. Allen et al. [331], compared no field plate, field plate, bevelled field plates (45°), and a 'small angle'

bevelled field plate (≈ 1°). It was found that these treatments increasingly increased the V_{Br}. Spin on glass (SOG SiO_2 not doping in this case), and PECVD deposited SiO_2. However, it demonstrates that such treatments can improve device performance. It was found that the V_{Br} was increased from 200 V, 400 V, 650 V and 1100 V for no FP, small angle FP, bevelled FP and small angle bevelled FP. This is displayed in Table 2.10, which compares different diodes.

Another improvement is using the idea of junction terminations. In β-Ga_2O_3, these junctions are formed from either Schottky or heterojunction due to the limitation of realising p-type Ga_2O_3. Guard rings are fabricated by a highly doped pn junction that overlaps with the Schottky metal contact. The highly doped region blocks out the electric field generated at the edge of the contact, lowering crowding effects caused by a sharp junction. Unlike a pn heterojunction-based diode, the quality of the material is not as important. It does not matter how resistive this material is, only the quantity of positive charge, this is because the current is not travelling through this junction, rather it is used to manage the electric field. Simulations by Roy et al. [332] investigated the potential of p-type GaN, p-type non-polarised AlGaN and polarised graded AlGaN, as guard rings for β-Ga_2O_3, this was simulated using Sentaurus. It was determined that lowly doped non-polarised AlGaN was the most suitable, however, this has yet to be realised. Experimentally, p-type NiO_x has been realised to fabricate guard rings [333] [334]. Wang et al. [335] designed a more complex structure to grade the electric field across the device. This lowered the impact in the active regions but depletes the regions as the contact terminates. This was without implantation or etching but with multiple bi-layer photoresists. Hao et al. [336] investigated different hole concentrations in the NiO_x, which was performed by changing the deposition conditions. The ratio of $O_2/Ar + O_2$ the percentage was tested at 0%, 5% and 60% out of these 5% appeared to be most optimal. These more complex structures are Field Limiting Rings. Their impact is to grade the electric field dose not an abrupt change in the electric field caused by the metal contact. Where bevelled edge termination achieves this with dielectrics and physical spacers from the metal contact, field limiting rings achieve this by applying an additional charge to manage it. This can be with p-type material or separate isolated Schottky contacts. This was first realised by Hu et al. [337] on an exfoliated layer of β-Ga_2O_3, in this was used an outer floating Schottky contact. This was also achieved with NiO_x [338]. These rings can be used in conjunction with one another to spread the electric field gradually. It should also be noted that these rings can have their field plate structures built into them to manage the field further. These allow for greater control and management of the electric field [339]. This approach manages the electric field profile in such a way that the peak is drawn away from the metal-semiconductor interface when the device is in reverse bias. This can be achieved by burying p^+ material under the Schottky contact, these types of devices are referred to as Junction Schottky Barrier Diodes (JSBD). This p^+ interacts with the n^- drift region of the Schottky diode, reducing the effect the bulk semiconductor has on the metal barrier height. This reduction of the electric field is referred to as the REduced SURface Field (RESURF) effect. This lowers the leakage current and the V_{Br} [340]. The quality of the p-type material has to form a heterostructure because current is not flowing through it. NiO_x has been used to form these

junction and were demonstrated [338] [341] [342]. The p-type material can be deposited on top of the β-Ga_2O_3 and the Schottky contact was buried around it, where Lu et al. [342] demonstrated this with thermally grown NiO_x. Another approach that can be used with the same RESURF effect is to etch trenches/fins into the β-Ga_2O_3, then deposit a dielectric and use the MIS structure to manage the electric field in the pillar. In β-Ga_2O_3 this was first demonstrated by Sasaki et al. [343] where HfO_2 was used to insulate the edges of the pillar and the metal contact. The exact geometry of these fin widths, trench depths and the pitch size all effect how the electric field is managed [344] [345] [346] [347] [348] [349] [350] [351] [352] [353]. It was commented on in earlier sections that different orientations of β-Ga_2O_3 etch and have different characteristics. It is natural that the orientation of the fins also plays an important role in the nature of the trench Schottky diodes [351]. The etch quality, how many defects, impurities are introduced, and the resultant surface roughness [354], these devices still benefit from the edge termination. The termination of the trench should be considered [349] [350] [351]. The RESURF effect leads to a new crowding of the electric field caused by the abrupt termination of the trench [351]. To deal with this, it is expected to round the bottom of the trenches so that the applied field has a more gradual change than a sharp right-angle turn [352]. Rama et al. [355] investigated a Schottky-based diode with an interface layer of Hexagonal Boron Nitride Film, which acted as a barrier layer, increasing the turn-on voltage. Tetzner et al. [356] investigated a SnO/β-Ga_2O_3 vertical hetero-diode as part of a gate for a β-Ga_2O_3/SnO/β-Ga_2O_3 based MISFET. The MISFET will be discussed later, as this section is only looking at diodes. This diode had a PFOM of 1.38 $GW \cdot cm^{-2}$. SnO has also been used to form pn junction on κ-Ga_2O_3 [357]. Sohel et al. [358] showed a hetero-diode with p-type NiO_x to n-type β-Ga_2O_3, these were investigated for the potential for high operational temperatures which showed promise over Schottky-based junctions. Lu et al. [359] investigated the effect of etching and pre-treatments on β-Ga_2O3 prior to the growth of NiO_x to form heterojunctions. It was found that the etching did increase the roughness, which was restored with hot TAMH treatment. The barrier height of the pn junction was speculated to increase compared to without this process, this was due to an increase in the surface potential observed on the β-Ga_2O_3 of 0.11 eV. This comparison was for devices fabricated to have the same geometry, comparing etched, etched, and treated without any processing. The thermal stability of NiO_x/β-Ga_2O_3 was investigated by Li et al. [360], where annealing temperatures up to 500°C were investigated. The contacts degraded after 400°C and damage was critical after 500°C. There was minimal damage to the crystal, however, it could be quite damaging to the whole device. It was found that an anneal in O_2 at 300°C for one minute did improve the device performance. While this was considering pn heterojunction devices, these results are also of interest when NiO_x is used for edge termination. Chiang et al. [361] investigated the doping and layer thickness of NiO_x in the NiO_x/β-Ga_2O_3 hetero-junction, as well as a guard ring. This study was using Silvaco TCAD, they found that these parameters are highly important and affect the nature of the breakdown. Watahiki et al. [362] investigated using Cu_2O as a p-type material for a pn Ga_2O_3 based diode, Cu_2O was sputtered onto the Ga_2O_3 surface and had an ohmic contact Pt to Cu_2O, the results indicated a low band offset between the two. While the smaller band gap of Cu_2O restricts the breakdown voltage, it was speculated that high doping could mitigate

this. Hao et al. [363] optimised post deposition anneals in β-Ga_2O_3/NiO_x achieve a HPFOM of 0.65 GW · cm^{-2}. This has been overcome by [364] where, HPFOM of 1.38 GW · cm^{-2} as well as a 0.39 GW · cm^{-2} for a hetero-junction based FET device. To date β-Ga_2O_3/NiO_x is the most explored pn heterojunction based diodes and shows promise [364] [365] [366] [367] [363]. The hetero-junction between β-Ga_2O_3 and NiO_x is a type II (staggered) hetero-junction [368]. Between a type I and type II a type II is preferred as the two increases the conduction band offsets ($\Delta E_c/\Delta E_v$), are higher. This increase the turn on voltage and breakdown voltage and should result in a lower leakage current. There should be an increase in on-state resistance, however, this has less effect on power electronic devices due to the relatively lower switching speeds. A type III is suited for tunnelling biased devices [369], which is not suitable for a power electronic device. Ghosh et al. [370] determined the band offsets to be ΔEc/ΔEv 0.3/1.6 eV. Gong et al. [338] integrate heterostructures to realise β-Ga_2O_3 devices is also to use the p-type material to create guard rings for the edge termination of Schottky diodes. This resulted in HPFOM of 0.46 GW · cm^{-2} and a breakdown of 1.89 kV. Kan et al. [23] investigated using α-Ga_2O_3 and α-In_2O_3 hetero-diode. Due to the difference in doping (10^{17} to 10^{20}) cm^{-3} the whole α-Ga_2O_3 was depleted, hence there was no avalanche breakdown information. The heterojunction was found to be type II, and both layers were grown in Mist-CVD on an α-Al_2O_3 wafer.

A further note on devices should be made here regarding development when dealing with thermal management. Some devices have already been demonstrated that could alleviate the thermal conductivity problem of β-Ga_2O_3. The poor thermal conductivity of β-Ga_2O_3 has been noted as an issue. As a result, thermal management is an essential aspect of device design, which can provide longevity issues where consistently high temperatures slowly degrade the device due to diffusion of all the different layers, dopants and impurities. High temperatures lead to higher leakage currents, which can result in failing devices with Schottky contacts. One solution has been to fabricate lateral devices on non-native substrates, which have better thermal conductivity. This has been demonstrated with both growth or wafer bonding [371] [372] [373] [223] [374] [375]. Xu et al. [223] used H ions to exfoliate a layer of Ga_2O_3, which was then bonded to Si and SiC. Wafer bonding like this avoids the issues that arise from epitaxial growth of Ga_2O_3 on non-native substrates, as it can be grown on native substrates, extracted, and applied to another substrate with a greater thermal conductivity. Xu et al. [376] demonstrated this on whole 2 inch wafers, where β-Ga_2O_3 was exfoliate onto 4H-SiC and Si. Zhou et al. [120] fabricated a GaAsP/β-Ga_2O_3 pn junction, by "grafting" AlGaAs/GaAsP onto β-Ga_2O_3. This 'grafting' is where an ultra-thin buffer layer which mitigates the lattice mismatching [377]. This grafting approach generated a heterostructure that has also been applied to Si to form Si/β-Ga_2O_3 heterojunctions [378]. These issues arise from lattice mismatching and affect other heterojunctions, impacting pn heterojunctions. This is an issue with such solutions due to the lack of native p-type material in Ga_2O_3 [374] [376]. Double-sided packaging of the β-Ga_2O_3 diodes has been investigated, this disperses the heat, dealing with the thermal conductivity [379] [380].

This concludes the discussion about Ga_2O_3-based diodes, which are the most explored type of de-

vice. The lack of p-type material means heterostructures are used for edge termination, guard and limiting rings, interaction at the junction to limit the electric fields, or pn heterojunctions. Regarding this, NiO_x has been the most promising candidate. MIS structures and Schottky contacts (where the barrier acts like the insulator in MIS), edge termination, guard and limiting rings, and trench structures have also been demonstrated to help manage these fields. There is research into extreme high-k dielectrics for electrical field management in WBG semiconductors. Roy et al. [381] used TCAD simulations (Sentaurus) to simulate an SBD with realistic dimensions which could have a high PFOM 40 GW $\cdot$ cm^{-2} surpassing the theoretical unipolar BFOM of β-Ga_2O_3 SBD by four times. In the case of trenches and bevelled field plates the angles and exact structure also plays an important role to limit the amount crowding of the electric field caused by sharp transitions in geometry. These lessons are not only of interest to diodes for β-Ga_2O_3, but also can be taken forward into devices with more complex operational mechanisms. The management of the electric field is pivotal to any device that can be turned on or off, as the enhancement or depletion modes require this management across a channel.

Table 2.10: Different diodes fabricated using Ga_2O_3, predominately the β phase for different structures. When dealing with a Schottky Barrier Diode (SBD), the Ohmic contact will be omitted, when dealing with hetero-junction based pn diodes (HPN), then both ohmic contacts will be omitted. Unless otherwise stated, the material is β-Ga_2O_3, D is the diameter in μm and T the layer thickens. Edge Termination ET.

Structure	**Carriers** $\mathbf{cm^{-3}}$	$\mathbf{V_{Br}}$ **V**	$\mathbf{V_{On}}$ **V**	$\mathbf{R_{On}}$ $\mathbf{m\Omega \cdot cm^2}$	**PFOM** $\mathbf{MW \cdot cm^{-2}}$	**Comment**	**Ref**
Pt/Ti/Au-(010)	3×10^{16}	150	1.23	7.85	2.9	SBD, T/D 600/100 μm.	[306]
Pt/Ti/Au-(100)	2.3×10^{14}	> 40	1.07	80	-	SBD, T/D 600/100	[308]
Au/Ti/Pt-(100)	2×10^{17}	200	0.63	2.9	0.5	SBD, T/D 0.48/30.	[382]
Mo/Au-(100)	2×10^{17}	260	-	-	–	SBD, T/D 15/100.	[299]
Ni/Au-(001)	2×10^{16}	100	-	23	0.435	SBD, T 15, A 0.1×0.3	[324]
"	3.6×10^{18}	466	-	0.59	368	SBD, T 650, A 40×40.	"
Ni/Au-(001)	2×10^{16}	1016	-	6.7	154	SBD, T/D 10/105	[383]
Ni/Au-(-201)	4×10^{15}	1600	-	1.6 – 25	102	SBD, TD 10/20	[384]
Ni/Au-(001)	1.2×10^{16}	1720	-	2.25	1320	SBD, T/D 9/100.	[385]
Pt/Ti/Au	1×10^{17}	532	-	0.1	2830	SBD, α phase, T/D 0.43/30.	[386]

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Table 2.10 – Continued From Previous Page

Structure	Carriers cm^{-3}	V_{Br} V	V_{On} V	R_{On} $m\Omega \cdot cm^2$	PFOM $MW \cdot cm^{-2}$	Comment	Ref
"	1×10^{17}	855	-	0.4	1827	SBD, α phase, T/D 2.5/30.	"
Ni/Au-(001)	1.5×10^{16}	1550	0.82	5.1	470	SBD, Mg-implanted ET, T/D 10/90	[313]
Pt/Ni/Au-(001)	1.5×10^{16}	750	1.8	5.3	106	SBD, T/D 7.8/200	[314]
"	"	860	1.5	4.9	150	SBD, N-implanted GR, T/D 7.8/200	"
"	"	1380	1.8	5	380	SBD, FP, T/D 7.8/200	"
"	"	1430	1.6	4.7	430	SBD, N-implanted GR, FP, T/D 7.8/200	"
Pt/Ti/Au-(001)	4×10^{16}	391	1	4	38	SBD, Ar-implanted ET, T/D 8/200	[316]
Ni/Au/Ni-(001)	3×10^{16}	1050	0.7	2.5	44	SBD, bevelled F-implanted ET, T/D 650/100	[318]
Ni/Au-(001)	3×10^{16}	940	-	3	295	SBD, thermally oxidised ET, T/D 6/150.	[387]
Ni/Au-(001)	1.6×10^{16}	1000	0.73	4.8	210	SBD, He-implanted ET, T/D 10/65	[315]
Ni/Au-(001)	3×10^{16}	6000	1.45	3.4	10600	SBD, SiO_2 ET, T/D 10/90.	[317]

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Table 2.10 – Continued From Previous Page

Structure	Carriers cm^{-3}	V_{Br} V	V_{On} V	R_{On} $m\Omega \cdot cm^2$	PFOM $MW \cdot cm^{-2}$	Comment	Ref
Pt/Au-(001)	n^-	400	0.7	4	40	SBD, thermally oxidised, SiO_2, SiN_x air space field plate, T/D 7/100.	[388]
Ni/Au-(001)	4.35×10^{15}	650	-	0.518	26.5	SBD, bevel FP, SiN_x, T/A 8/10000 × 10000	[389]
Ni/Au-(001)	1.6×10^{16}	240	2.9	12	4.8	SBD, Al_2O_3/SiN_x FP, T/A 20/1000 × 1000	[322]
Ni/Au-(001)	3×10^{15}	1100	-	2	600	SBD, small bevel angle, Spin On Glass, T/D 10/200.	[331]
Ni/Au-(-201)	2.9×10^{17}	2250	1.32	5.1	223	SBD, Lateral, Al_2O_3 FP.	[390]
Ni/Au	3×10^{16}	3108	-	3.29	2940	Silvaco, SBD, small bevel angle, HfO_2	[391]
Cu/Au/Ni	6×10^{16}	240	-	2.9	28.8	SBD, MIS-trench 2.5 HfO_2, T/F 7/1.2.	[343]
Mo/Ni/Al-(001)	6×10^{16}	300	0.5	3.09	29	SBD, MIS-trench HfO_2/SiO_2.	[392]
Ni/Pt-(001)	2×10^{16}	1232	-	15	101	SBD, MIS-trench 2, T/F 10/2.	[347]
Ni/Ti/Pt-(001)	2×10^{16}	2440	1.25	11.3	390	SBD, MIS-trench 1.55, T/F 10/2.	[348]

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Table 2.10 – Continued From Previous Page

Structure	Carriers cm^{-3}	V_{Br} V	V_{On} V	R_{On} $m\Omega \cdot cm^2$	PFOM $MW \cdot cm^{-2}$	Comment	Ref
-	2×10^{16}	3400	-	6	1926	SBD, Sentaurus TCAD, MIS-trench 1.55, Al_2O_3/HfO_2, T/F 10/1, rounded corners.	[352]
/p-Cu_2O-(001)	N>10^{18}	1490	1.7	8.2	270	hetero-diode type II, T/D 200/100.	[393]
NiO_2-(001)	$1 \times 10^{19}/4 \times 10^{16}$	1059	1.2	3.5	320	hetero-diode NiO_2 type II, T/D 0.2/8/200.	[394]
$NiO_2{}^{+/-}$-(001)	$4 \times 10^{19/17}/1.5 \times 10^{16}$	1860	2.2	10.6	330	hetero-diode, type II, T 0.1/0.3/7.7, D 200.	[394]
$NiO_2{}^{+/-}$-(001)	$3 \times 10^{19/16}/2 \times 10^{16}$	1370	1.73	2.6	720	hetero-diode, type II, T 0.1/0/3/10, D 1000	[395]
NiO_2	$1 \times 10^{19}/2 \times 10^{16}$	1630	1.65	4.1	650	hetero-diode, type II, T 0.3/10, D 100.	[363]
NiO_2-(001)	$1 \times 10^{18}/2 \times 10^{16}$	1715	1	3.45	850	J-SBD, 2.9/1.3, A 100 × 100, ET.	[342]
NiO_2-(001)	$1 \times 10^{18}/1.5 \times 10^{16}$	1890	1.1	7.7	460	J-SBD, Field liming rings, T 0.28/7.7, D 200.	[338]
NiO_2-(001)	$1 \times 10^{18}/6 \times 10^{16}$	2410	1.6	1.12	5180	J-SBD, small angle bevel FP, SiO_2.	[396]

2.16 Transistors

A number of transistors have also been demonstrated. These devices exist in either a normally 'off' or 'on' state and can be turned 'on' or 'off' by a signal. In power electronics, normally off devices are preferred, however, this is not always the case and, at times, not the most efficient solution. There are two main families of transistors: Bipolar Junction Transistors (BJT) and Field-Effect Transistors (FET).

2.16.1 Bipolar Junction Transistors

The BJT first of these, as its appropriateness for Ga_2O_3, is limited. In a basic sense, BJT consists of three layers of semiconductor doped in an alternating pattern, npn or pnp, with the middle layer being thin. This acts as two back-to-back diodes. This depletes the thin region, which means that current cannot flow across the junctions. Due to this nature, they are normally off devices. It is a three-terminal device with an Anode (Emitter), Cathode (Collector), and Gate (Base). The mid-section is depleted so that no current can flow. However, by allowing a current to flow into the base, some of the current starts flowing from the emitter to the base. However, this means that the midsection is no longer depleted, and so the current is passing into the midsection, and as the collection has much more potential on it draws more of the newly added charge towards the collector, and hence the device is turned on. A simple diagram showing a BJT's setup shown in Figure 2.15. As p-type Ga_2O_3 has yet to be realised, so a homo-junction fully Ga_2O_3-based BJT is not currently possible. However, this does not mean that Ga_2O_3 can play no role in such a device, as with diodes, hetero-junctions could be a possible solution for this. Mehta and Avasthi [397] investigated such a possibility where they performed a simulation and found that Cu_2O/β-Ga_2O_3 could have high performance.

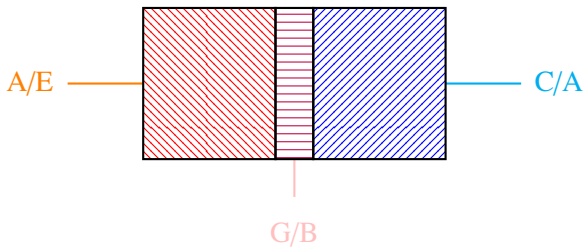


Figure 2.15: A cartoon of a bipolar Junction Transistor (BJT), where red and blue diagonal lines are the same doping and the purple horizontal lines is the opposite. There are three connections to the device, the Emitter (E), the Collector (C) and the Base (B). These are either pnp or npn, with the mid region depleted. As this region is depleted, then the current cannot flow E → C. This device is turned on by introducing current to B, this the middle is no longer depleted and so current is now free to pass E→C.

2.16.2 Field Effect Transistors

Unlike the BJT, FETs are much more applicable for Ga_2O_3 devices, given that FET designs can be unipolar as well as bipolar. Given the nature of β-Ga_2O_3 and the current lack of native p-type material, this is very beneficial. The FET works by applying some electric field to act on a region of a device

to "enhance" or "deplete" a region of charge carriers. This is how the device can be turned "on" or "off". These devices can be either normally "on" or normally "off" devices. This makes this general discussion on FETs a bit difficult, as they are not uniform, with quite a few mutations on the idea. There are a number of different transistor designs to consider in the FET family.

Metal Oxide/Insulator Semiconductor Field Effect Transistors

The most significant and most relevant of these to Ga_2O_3 is the Metal-Insulator/Oxide Semiconductor (MIS/MOS) FET branch. It should be noted that the historical term is MOSFET because it was developed with Si and SiO_2. However, as Ga_2O_3 is an oxide, and considering the deployment of other oxide-based semiconductors, the more accurate term of MISFET has been adopted. However, Ga_2O_3 can be used as a native oxide on GaN [18], so it is not wholly untrue to renegade Ga_2O_3 to the "oxide" in a MOS. FETs benefit from the ideas used to develop β-Ga_2O_3 based diodes to manage the electric field in the device in much the same manner. The MIS structure controls the device, where a potential is applied to the metal. This potential then affects the underlying semiconductor, where it is either enhanced, and the carrier concentration increases, or it is depleted, and the concentration decreases. These "Enhancement" or "Depletion" modes are used to turn the device "on" or "off." In the case of β-Ga_2O_3, as there is a lack of p-type, the channel is often a lowly doped n^- region to create a channel. In β-Ga_2O_3, these devices started as planar films on top of some insulator, commonly α-Al_2O_3. However, insulating β-Ga_2O_3 doped with Fe or Mg is also used. By controlling the channel size, it is possible to realise both Enhancement and Depletion modes for lateral devices fabricated in such a way [239]. Zeng et al. [398] have demonstrated vertical planar MISFET. This enhanced mode device used Mg diffusion to create a semi-insulating channel. The dielectric layer in the MIS structure is vital, and the choice of dielectric is highly important. The gate choice is also important to avoid current injection due to bandgap and band offsets. This is also while balancing dielectric constants and thickness to fabricate channels with more control over the charge carriers [399]. As β-Ga_2O_3 does not have a native dielectric like Si, this means that the dielectrics used to fabricate the MIS structure have to be deposited and not thermally grown. SiO_2, Al_2O_3, ZrO_2 and HfO_2 were investigated for gate dielectrics [400] [401] [402]. Inter-mixture of different dielectrics have also been used to fabricate Al_2O_3/HfO_2 [403]. This intermixing Al_2O_3/HfO_2 appeared to have a lower leakage and higher dielectric value. These dielectrics can be deposited differently, similar to how β-Ga_2O_3 can be grown. Predominantly, ALD has been utilised to deposit dielectric layers onto β-Ga_2O_3, however, some CVD methods have also been used. The operating conditions and deposition method impact the quality of the deposited dielectric film. Ultra-high-k ferroelectric dielectrics, such as $BaTiO_3$ have been impermanent to manage the uniformity of the electric field profile for FET designs. Kalarickal et al. [404], performed this on the lateral FETs. This was a β-Ga_2O_3 depletion-based MISFET with high average breakdown fields of 1.5 MV $\cdot$ cm^{-1}, 918 V and 4 MV $\cdot$ cm^{-1}, 201 V were demonstrated for gate-drain spacings of 6 μm and 0.6 μm, respectively, where the channel has a sheet charge density of 1.8×10^{13} cm^{-2}. This had a PFOM of 376 MW $\cdot$ cm^{-2} with gate-drain spacing of 3 μm.

Defects, trapped charge, and interface states that occur during deposition (with pre- and post-treatments) which affect the quality of the MIS structure. This presents as an increased charge, which interferes with the optimisation of the MISFET. The additional charges are affected when the channel is depleted or enhanced, hence the turn-off/on the voltage of the MISFET. The charges are at the interface and spread across the dielectric, as well as trapped states. One way to characterise the quality of a MISFET's MIS structure is to fabricate a test structure known as an MIS capacitor, which simplifies the MISFET by not considering the source/drain connections and modelling the device as a set of capac-

itors. Taking Voltage-Capacitance (CV) measurements makes it possible to determine the interface traps density (D_{it}) and the amount of charge in the device. This is highly dependent on the deposition method, the material, and the pre- and post-treatments, all of which affect the end result. For example, for Al_2O_3 deposited by ALD, it has been seen that Piranha cleaning before deposition and post dielectric deposition annealing at 500°C in O_2 improved the interface [258]. Zeng et al. [405] deposited SiO_2 using ALD onto ($\bar{2}01$) β-Ga_2O_3, and then RTA at 470°C for 1 minute, in this work the Terman method was used to calculate the D_{it}, to be 6×10^{11} $cm^{-2} \cdot eV^{-1}$. Jayawardena et al. [406] deposited SiO_2 LPCVD has been used and compared to ALD Al_2O_3, where it was found that LPCVD deposition had lower leakage and D_{it} but a higher breakdown field. It was found that annealing at 500°C degraded the Al_2O_3, as D_{it} was observed to increase. It was found that cleaning with HF and HCl increased the D_{it}, making the interface worse. The Terman method has also been used to measure D_{it} for Al2O3 deposited by ALD [407], with post-deposition annealing, the D_{it} was 1.2×10^{12} $cm^{-2} \cdot eV^{-1}$.

However, relatively few studies are investigating at post-metallisation anneal on MIS structures. Jian et al. [408] performed a study where the dielectric was AlSiO on (001) β-Ga_2O_3. It was found to reduce the hysteresis and trapped charge and improve stability in reverse operation. This improved stability in reverse operation should also be compared to work performed by Matsubara et al. [256], which found post-metallisation anneals detrimental to MIS capacitors. While this was on Ge/GeO_2 they speculated that this was due to desegregation in the metal-dielectric interface. Hawkins et al. [409] showed Ti diffused into Al_2O_3 after annealing at 430°C for 30 minutes. The work performed in [408] [256] [409] were not rapid thermal anneals but long temperature anneals, which are substantially different from the rapid thermal anneals mostly explored for post dielectric deposition (before metallisation) annealing. The different pre-treatments and post-treatments impact the resultant MIS capacitor, affecting the MISFET. The field plate, also a MIS structure, uses the same principles to manage the electric field. The field plate is not to be used to the extent of depleting the underlying semiconductor but to manage the device's extreme peaks. Field plates were used to improve the aspects of β-Ga_2O_3 MISFETs, these were shown to improve the V_{Br} [410] [411]. Qu et al. [412] used diamond, which was grown epitaxially to be used as a field plate, which was not only to manage the electric field but also to disperse the heat and manage the thermal issues which arise from β-Ga_2O_3 poor thermal conductivity.

Priyanshi and Harsupreet [413] performed simulations with Silvaco to investigate incorporating air gaps, passivation and field plates into a lateral MISFET design. It was found that these improved the devices dramatically, where the PFOM increased from 106 $MV \cdot cm^{-2}$ with no features to 1680 $MV \cdot cm^{-2}$ with a field plate and further to 2159 $MV \cdot cm^{-2}$, with a field plate and air gap. The inclusion of the air gap did increase R_{On} (62.2 → 85.98 Ω), however, the increase to V_{Br} (3510 → 4520 V) overshadowed this, it should be remember this was a simulation.

Tetzner et al. [414] fabricated D-mode β-Ga_2O_3 devices with sub μm gate lengths (with gate recesses), with implantation using SiN_x to passivate and isolate the devices. This achieved a breakdown voltage of 1.8 kV and PFOM of 155 $MW \cdot cm^{-2}$. Sharma et al. [415] used a polymer for passivation on a β-Ga_2O_3 D-mode MISFET, this achieved a PFOM 7.73 $kW \cdot cm^{-2}$. This was lower than expected due to damage to the channel from plasma, lowering the current. This shows that, just like in the case of diodes, the development of field plate structures onto β-Ga_2O_3 is necessary to see β-Ga_2O_3 based MISFETs reach their full potential. Similarity to how NiO was used in Schottky diodes to manage the electric field for MISFET's superinjunction equivalent MISFETs were demonstrated for β-Ga_2O_3 [416]. Trenches have also been applied to MIS designs and were utilised to help manage the electric field. Sasaki et al. [417] have demonstrated a vertical β-Ga_2O_3 MISFET, the gate dielectric was HfO_2,

and Cu was the gate metal. Field plates were incorporated into the design to help manage the electric field, this was a depletion mode MISFET. Enhancement and depletion mode trench MISFETs have also been demonstrated [418] [417]. The low mesa-to-trench depth ratio determines if it is a 'FinFET' or a Trench MISFET and has been used almost interchangeably for β-Ga_2O_3. Lu et al. [419] conducted a study on a normally off vertical β-Ga_2O_3 FinFET using TCAD Sentaurus, it was found that thermal issues in β-Ga_2O_3 could be catastrophic. Tetzner et al. [420] demonstrated vertical FinFET on (001) β-Ga_2O_3, these broke down at a strength of 2.7 $MV \cdot cm^{-2}$. It was speculated to have reached a peak of 5 $MV \cdot cm^{-2}$ inside the β-Ga_2O_3. Field plates were shown to improve FinFET's [421], contributing to how interconnected these design aspects are. FinFET's have achieved V_{Br} over 1000 V [422]. The profile of the etch/Fin also should be considered. In a simulation study by Junsung and Sung-Min [423], the geometry of the Fin was investigated. The Fin width, height and profile were all found to affect the characteristics of the device, and it is their hope that this information can help feed into β-Ga_2O_3 FinFET devices. Huang et al. [424] simulated a hetero-junction-based MISFET with SILVACO, where SnO was used as the channel on β-Ga_2O_3. NiO, Cu_2O, WO_3, and MoO_3 were also considered. These showed promise to be integrated into β-Ga_2O_3 based MISFETs. These are fabricated using epitaxial growth or exfoliation of a layer of β-Ga_2O_3 bonded to a different substrate. While these are heterostructures, they are often not based on a hetero-junction. However, these devices are still important. The reason for this is due to the poor thermal conductivity of β-Ga_2O_3 and so a lateral β-Ga_2O_3 based device on a substrate with high thermal conductivity can manage the self-heating issues [374] [376].

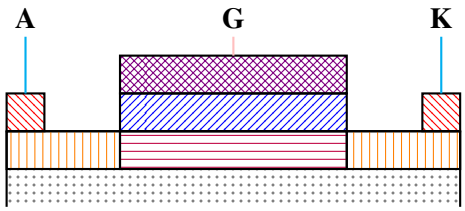


Figure 2.16: Diagram of a lateral MISFET, in this case the red ↖ is an ohmic metal contact to the doped semiconductor orange ↑, this is connected to a lightly doped channel purple → with a dielectric layer above it blue ↗ and a metal contact on top violet x. This is all on top of an insulating substrate grey ·'s. Two ohmic contacts are the anode **A** and cathode **K**. The "on"/"off" is determined by the channel where when a voltage is applied to the gate **G**, the charge in the metal contact causes the charge to build up on either side of the dielectric layer. In turn either depletes or enhances the carriers in the channel controlling the flow of current.

2.17 Metal-Semiconductor Field Effect Transistors (MESFET)

MESFETs are like MISFETs, however, there is a Schottky contact to the channel rather than an MIS interface. The Schottky barrier across the channel acts like the insulator in the MIS structure, where current is blocked by the barrier height. The cathode has a Schottky contact to a lightly doped region, allowing current to flow in forward bias and blocking in reverse. This approach allows for FETs to be fabricated with fewer process steps. There is no need to deposit a high-quality conformal insulating layer and then deposit a metal contact on that. It removes the dielectric and requires a single step, this also removes a possible compatibility issue arising from any other processing, such as in the deposition of the dielectric to everything else and the rest of the steps to the dielectric. While this remains true

with the metal deposited, this was always going to be the case, removing a possible issue. Because of the nature of MESFET where the gate is a reverse Schottky diode, this means that it has a lower capacitance than the MISFET structure, Compared to MISFET, MESFETs are relatively unexplored or Schottky Barrier diodes. The first β-Ga_2O_3 based MESFET was demonstrated by Higashiwaki et al. [41], this was a (010) lateral device on a lightly doped epitaxial layer. Dang et al. [234] demonstrated thin film lateral MESFETs using α-Ga_2O3, Ti/Au was the ohmic contact and AgO_x as the gate contact. The device was able to withstand 48 V at the drain. This was grown in a Mist-CVD system at atmospheric pressure, realizing the potential for cost-effective α-Ga_2O_3 devices. The initial work performed on MESFETs was depletion-based FET. However, enhancement-based normally-off MESFETs were fabricated in β-Ga_2O_3 [425]. Improvements which applied to diodes and MISFETs, also apply to MESFETs, field plates were implemented and transferred onto MESFETs [426] as well as trench and FinFET designs have also been transferred across to and applied to MESFETs [427]. Suhyun and Jihyun demonstrated double-gated MOSFETs [428] and Xia et al. [429] demonstrated Si delta-doped β-Ga_2O_3 MESFET's. Dariush and Ali [430] simulated lateral MESFETs, it was found that including an insulator on the channel could be used to improve the electrical characteristics for high power/speed applications.

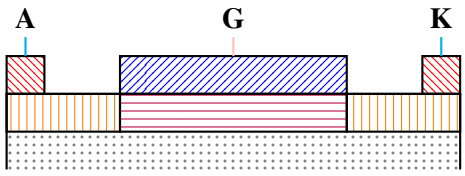


Figure 2.17: Simplistic diagram of a lateral MESFET, in this case, the red ↖ is an ohmic metal contact to the doped semiconductor orange ↑, this is connected to a lightly doped channel purple → with a Schottky contact metal above it blue ↗. This is all on top of an insulating substrate grey ·'s. Two ohmic contacts are the anode **A** and cathode **K**. The "on"/"off" is determined by the channel where when a voltage is applied to the gate **G**, the charge Schottky contact/channel interface either depletes or enhances the carriers in the channel controlling the flow of current.

2.17.1 Junction Field Effect Transistors

Currently, homo-JFETs are not feasible, meaning a heterostructure must be utilised for a JFET. JFETs use the p-type material similarly to a Schottky contact for a MESFET. The potential is applied to the p-type material to manipulate the electric field, not to pass a current through. To clear up some nomenclature, JFETs in β-Ga_2O_3 are hetero JFETs (HJFET). However, this does not define anything different because of the lack of p-type β-Ga_2O_3, meaning that all JFETs in β-Ga_2O_3 are heterostructures, so the terms are interchangeable. The p-type material in β-Ga_2O_3 is similar to the p-type in guard rings in that it is used to control the electric field. In the JFET case, it forms a gate much like a Schottky contact in a MESFET. As current is not passing through the p-type material, normal issues that arise from heterostructures, the quality of the interface, and the growth of the material causing defects, lattice matching, and so on, are less impactful. The p-type material, along with any passivation, can help disperse the heat generated and alleviate the poor thermal conductivity of β-Ga_2O_3 [431]. NiO_x has been used for guard rings and hetero-junction-based diodes, that NiO_x has been used

to make JFETs [364]. While NiO_x is the most explored and promising candidate for most heterostructures, JET's were demonstrated to utilise other materials, some using thin membrane structures with WSe_2, $MoTe_2$, black phosphorus and 4H-SiC [432] [433] [434] [431]. Tetzner et al. [356] have fabricated more traditional MESFETs based on SnO/β-Ga_2O_3 with a lateral recessed gate, this had a PFOM of 178 $MV \cdot cm^{-2}$. JFETs also have used field plates to manage the electric field [435] [436]. Jiaweiwen et al. [437] investigated a JFET with a FinFET design. Note that in this work, they referred to them as HJFET, but that is true for all JFETs, which is purely due to the lack of native p-type material for β-Ga_2O_3, and hence the alternative is to use heterostructures with an aligned p-type semiconductor. They will be referred to as JFETs. In either respect, the utilisation of p-type material over more conventional MIS structures is believed to result in lower $R_{On,\,Sp}$. This work was performed by simulation using Sentaurus. Wang et al. [438] investigated a combination of both a MISFET and JFET into a single lateral device. This device was a depletion-type device that used NiO_x as the p-type material, and the dielectric layer was SiO_2.

Summary on Field Effect Transistors

This demonstrates that research into β-Ga_2O_3 for power electronic devices is ongoing, and there are still many avenues to explore and develop. The lessons learned and still being developed in diodes have and will continue to help realise and develop FETs based on β-Ga_2O_3. Managing the electric field by including field plates with MIS structures to help push the boundaries of Schottky diodes has improved all types of FETs. Using trench designs has also allowed for FinFETs to be developed, which were realised with MIS, MES and p-hetero junction structures. While the lack of a native p-type material has hindered realising β-Ga_2O_3, it has not stopped the progression. The development of NiO as a suitable p-type material to be incorporated into hetero-structures to realise pn junctions is a advantage for β-Ga_2O_3 development. This is to manage the electric field, as guard rings and JFETs in β-Ga_2O_3 devices, has increased the types of devices possible and helps reach new limits in β-Ga_2O_3, where it is hoped it will eclipse other more mature materials. This is without commenting that these features are not in a vacuum, and multiple designs were applied to all of these. The development of hetero-structures also opens up the possibility of realistic bipolar devices based on hetero-structures. However, the quality of the hetero interface will impact this. In addition to the electrical issues, the exfoliation and incorporation onto other substrates deal with the thermal issues that arise. In Table 2.11 an array of different FETs for power devices is shown with some of properties and designs, this is by no means all-encompassing. These solutions all require different processes and optimisation to deal with, so there is not really an avenue that is entirely separate from one another. Etching is required for any device beyond a vertical Schottky diode with epitaxial layers grown onto a substrate, whether this is to create trench/Fin geometry (depth, width and pitch) to create channels or regulate the electric field in the device. Epitaxial growth, either hetero or homo, will be required, highly likely both, not only for drift regions but also for the inclusion of pn junctions. This could be for direct pn junction current transfer and to manage the electric field with guard rings and junction effects. The incorporation of MIS structures, whether this is for the field to help manage the electric field, which can be incorporated into all devices, or for MISFET structures, which create channels, will also be required. Finally, the continued development of ohmic contacts which are more thermally robust contacts for β-Ga_2O_3 due to its poor thermal conductivity. Incorporating hetero-structures and packaging to mitigate thermal issues with β-Ga_2O_3, is an active area of research. While β-Ga_2O_3 FETs are behind more mature materials like SiC or GaN, β-Ga_2O_3 devices, they already impressive and outperform those of Si.

Table 2.11: Different FET fabricated using Ga_2O_3, predominately the β phase. Showing the V_{Br}, R_{On} and PFOM $\left(\frac{{V_{Br}}^2}{R_{On,\,Sp}}\right)$. There are also relevant comments on this specific device.

Structure	**V_{Br}** **V**	**R_{On}** **$m\Omega \cdot cm^2$**	**PFOM** **$MW \cdot cm^{-2}$**	**Comments**	**Ref**
JFET	1115	3.19	0.39	Lateral, NiO_x	[364]
JFET	980	$151 \cdot mm$	-	E-Mode, Lateral, Recessed-Gate, NiO_x	[439]
JFET	1057	13 – 18	-	E-Mode, Vertical, FinFET, NiO_x	[422]
JFET	2660	25.2	28	E-Mode, Vertical, FinFET, NiO_x, FP	[435]
JFET	2145/1977	6.24/13.75	0.74/0.28	D/E modes, Lateral, Recessed-Gate, FP	[436]
JFET	750	< 4	178	Lateral, Recessed-Gate, FP SiN_x, SiO	[356]
MISFET	-	364	-	E-mode, Lateral, Trench, (010), Al_2O_3 ALD	[440]
MISFET	505	215	–	E-mode, Lateral, Trench, ALD SiO_2	[280]
MISFET	1830	185	155	D-mode, Lateral, Trench, thermal ALD Al_2O_3,	[414]
MISFET	445	70	76	D-mode, Lateral, Trench, thermal ALD Al_2O_3, FP	[414]
MISFET	354	24	174	D-mode, Lateral, Recessed Gate, thermal ALD Al_2O_3, exfoliated β-Ga_2O_3 on SiC	[441]
MISFET	1014	101	100	D-mode, Lateral, Recessed Gate, thermal ALD Al_2O_3, exfoliated β-Ga_2O_3 on SiC	[441]
MISFET	480	4.75	50.4	SiN_x FP, ALD Al_2O_3 D-mode	[442]
MISFET	505	17.1	1.5	E-mode, Lateral, ALD SiO_2	[280]
MISFET	1057	13/18	62 – 86	E-Mode, Vertical, ALD Al_2O_3	[422]
MISFET	961	7.34	125	E-Mode, Vertical, ALD Al_2O_3	[443]
MISFET	479	15.9	14.4	D-Mode, Lateral, ALD Al_2O_3	[444]
MISFET	2440	63.1	94.3	Lateral, E-Mode, duel source field plates, ALD Al_2O_3	[445]
MISFET	1400	7	277	lateral, D-Mode, Al_2O_3/SiN_x by ALD/PECVD, T-shape & source FP	[446]
MISFET	480	4.57	50.4	Lateral, D-mode, Source FP, ALD/PECVD Al_2O_3/SiN_x	[442]
MISFET	8030	-	0.008	Lateral, D-mode, gate FP, polymer passivisation, ALD SiO_2	[415]
MISFET	800	49	13	Lateral, E-mode, mounted on SiC, ALD Al_2O_3	[376]

Next Page

Table 2.11 – Continued From Previous Page

Structure	V_{Br} V	R_{On} $m\Omega \cdot cm^2$	PFOM $MW \cdot cm^{-2}$	Comment	Ref
MISFET	840	1.72	408	Lateral, D-Mode, ALD $Al_2O_3/BaTiO_3$	[447]
MESFET	4400	-	100	Lateral, D-Mode, FP, Ni/Au/Ni	[426]
MESFET	267	3.7	25	Lateral, D-Mode, Ni/Au/Ni	[448]
MESFET	2800	-	0.44	Lateral, D-Mode, FinFET, Ni/Au/Ni	[427]

2.17.2 Insulated Gate Bipolar Transistors

Insulated Gate Bipolar Transistors (IGBT) are a combination of both FET and BJT ideas. This is similar to a MISFET design, where the channel is a thin doped layer of semiconductor opposite to that on either side of it. Similar to the comment on the BJT, such a design in Ga_2O_3 is not possible as there is no p-type material. Therefore, it has the same conclusion that a heterojunction-based device would be the only solution. These ideas are still being investigated in comparatively more mature materials such as Si to 4H-SiC [449], and it will likely be some time before it is reported on in β-Ga_2O_3.

2.18 Ga_2O_3 Based Semiconductors

Apart from hetero-junction devices, there is another aspect of development for Ga_2O_3, these are compounds based on Ga_2O_3. These can be considered as materials in their own right or incorporated into hetero-structures with Ga_2O_3, indeed the large scale growth of bulk β-Ga_2O_3 could be beneficial to realise such materials. It is possible to engineer Ga_2O_3 with modulated doping and hetero-structures β-$Al_xGa_{1-x}O_3/Ga_2O_3$ to generate a highly mobility at the interface [450]. The incorporation of p-type semiconductors could be used to fabricate normally-off β-Ga_2O_3 with positive threshold potentials [451]. β phase is not alone in this regard. The other phases have received attention and could be used to generate 2-D electron gas in the same way as GaN/AIN transistors [21]. The incorporation of Al into Ga_2O_3 to form aluminium gallium oxide $Al_xGa_{1-x}O_3/Ga_2O_3$ is a alloy between Ga_2O_3 and Al_2O_3. It was noted by Roy et al. [11] that the gallium ion resembles the aluminium ion and can substitute for it in several structures. The β-phase is not favoured, so with large Al composition, the structure when it is grown on β-Ga_2O_3 results in two competing structures [452]. It has been difficult to attain gallium oxide-based materials with bandgaps over 6 eV, however, they are available in the nitride family through AIN. Jinno et al. [453] grew single crystalline layers of α-$(AlGa)_2O_3$ with molecular beam epitaxy, it was found to have a bandgap between 5.4 and 8.6 eV with a bowing parameter of 1.1 eV. This was found by varying the composition of the alloy, and this means that α-$Al_xGa_{1-x}O_3$ has the largest bandgap of this material family to date. If these layers can be doped in controllable ways then α-$Al_xGa_{1-x}O_3$ would be of high interest for high power electronic and photonic devices, with a bandgap far beyond the materials available today [454]. Spinel zinc gallate $ZnGa_2O_4$ is a mixed oxide of ZnO and Ga_2O_3, it offers advantages based on how it can be doped, which is due to the spinel nature of $ZnGa_2O_4$ allowing diverse coordination possible [455]. Spinels normally have (A) cations in the tetrahedral site and (B) cations in the octahedral site, in this case, Zn-tetrahedral site $Zn^{2+}(T_d)$ and Ga-octahedral site $Ga^{3+}(O_h)$ so that normal structure of $ZnGa_2O_4$ is $Zn(^{2+}[T_d])Ga_2(^{3+}[O_h])O_4{}^{2-}$. There are known routes to dope compounds like this, where defects like Zn_{Ga} are antisite donors and donors like $Ga^{3+}(O_h)$ on T_d and antisite acceptor GaZn with acceptor like $Zn^{2+}(T_d)$ on O_h, these result in an

intrinsic bipolar semiconductor [456]. $ZnGa_2O_4$ is a potential candidate for other power electronic devices, based on Ga_2O_3, with a bandgap about 5 eV. Over 1000 compounds can form spinel crystal structures, these offer an avenue to explore UWBG oxides in a spinel structure. This subgroup has properties of interest to batteries, fuel cells, catalysis, photonics (phosphors, bio-imaging, photodetectors), spintronics (magnets, bio-magnets), or thermoelectricity [457], with active work on Ga based spinels such as $MgGa_2O_4$ and $Zn_{1-x}Mg_xGa_2O_4$ [458] [459] Amorphous composites of semiconducting oxides, of Ga_2O_3, ZnO and In_2O_3 have been investigated for use in flexible thin film transistors [460]. It was found that by varying the composition of the material it was possible to engineer the carrier concentrations and mobilities, this is shown in Figure 2.18. Combinations of oxides like this are a possible alternative to more covenantal semiconductors like Si.

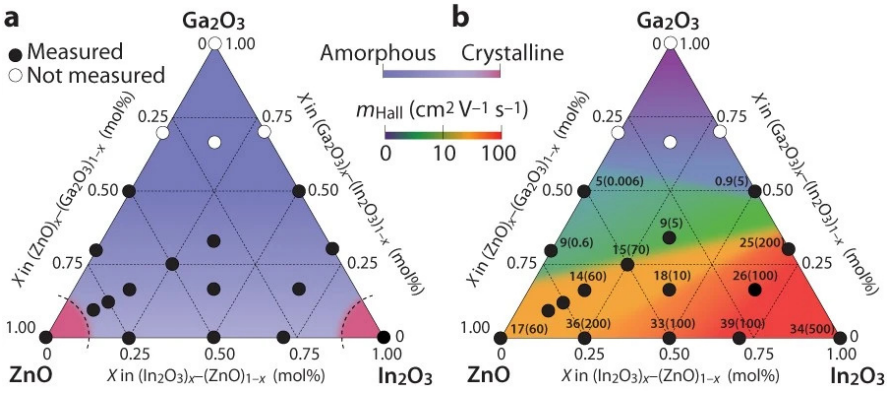


Figure 2.18: Diagram descibeing the crystallinity (A) and mobility (B) of composites of amorphous Ga_2O_3, ZnO and In_2O_3. In sub-figure B, the values presented are the hall at room temperature in $cm^2 \cdot V^{-1} \cdot s^{-1}$ and carrier concentrations in 10^{18} cm^{-3} shown in parentheses. This is republished from [461] which in turn is modified from [460]. It can be seen that the properties of of the material can be engineered to have high carrier concentrations up to 10^{20} cm^{-3} and mobilities > 10 $cm^2 \cdot V^{-1} \cdot s^{-1}$

2.19 Closing Remarks

The continued electrification and use of electrical energy is becoming evermore important in the 21st century. UWBG semiconductors such as β-Ga_2O_3 are promising candidates for power electronic devices. The critical electrical field is far beyond Si and other wider band gap materials, such as SiC and GaN, with relatively similar mobilities. High-quality bulk substrates and epitaxial layers can be grown relatively cheaply and with high throughputs. Hetero-structure material has also been demonstrated using β-Ga_2O_3, due to the lack of p-type material, high-k dielectrics and hetero-structures are needed. β-Ga_2O_3 power devices diodes and transistors have progressed dramatically, reaching the forefront of power devices. Optoelectronics are also an option open to β-Ga_2O_3 devices, owing to its wide band gap which lies in the UV-C range. β-Ga_2O_3 has also shown the potential for other UWBG oxides which could be developed in the future, UWBG oxides are the largest subgroup of UWBG semiconductors. These include $ZnGa_2O_4$, with others anticipated, representing even more of an expansion of the forefront of UWBG materials opening up more power device solutions going forward.

CHAPTER 3

MATERIALS AND METHODS

In this chapter the equipment, materials and processes which are required for the following experimental chapters is discussed and described. While each experimental section will have its own methodology section there are certain commonalities as well as the opportunity to look in-depth into the materials and methods to limit repetition and distraction.

3.1 Tools

The equipment which was used for the work for this thesis.

3.1.1 LatticeAxe and Scribe

It was necessary to resize samples to better emulate the β-Ga_2O_3 samples but more importantly to cleave across features to inspect the cross-section. This was very dependent on the samples crystal structure, however, for process optimization it was a necessity, this was either performed with a diamond scribe or more accurately with a LatticeAx sold by Mercia Semiconductor Limited. These tools can be seen in Figure 3.1. Cleaving with the LatticeAx has a much higher level of precision compared to diamond scribe and can be performed in a way which limits the damage to the surface. This means when investigating the cross-section of a sample to inspect the profile of photoresist post development, limiting the handling along the edges is a benefit.

3.1.2 Sonicator

In this work a sonicator was often used as part of a solvent cleaning process or for difficult metal lift-off processes. This is a bath which agitates samples at a high frequency which can be used to help physically remove particles. It was not always used, however, as this agitation can cause damage to the surface and delamination of thin films. While it can also perform this at elevated temperatures, in this work it was only used at room temperature. An example can be seen in Figure 3.2.

(A) (B)

(C)

Figure 3.1: The tools used for cleaving sample when required, (A) the LatticeAxe and (B) the handheld tool. These were used used as sample preparation often to look at the cross-section of samples often in combination with a diamond scribe. The LatticeAxe can be used to cleave a sample with a high degree of precision and limited damage to the surface.

Figure 3.2: The sonicator used in this work, this was used for solvent cleaning as well as some lift-off procedures. This is a bath which applies a high frequency agitation, which can be used to physically dislodge and dissolve particles into a solvent. This is not always used as it can cause some level of damage to samples.

3.1.3 Plasma Asher

In this work a plasma asher was used to clean the samples, the PE-50 sold by Plasma Etch, this can be seen in Figure 3.3. This was used to descum samples after the photoresist was developed, this was to clean the exposed regions, while also potentially creating dangling bonds to help improve the chances of ohmic contacts. The process used in this work was an oxygen plasma, at 150 W, with 5 sccm of oxygen, for 60 s.

Figure 3.3: PE-50 Plasma asher sold by Plasma Etch. This tool was used to de-scum the sample after the photoresist was developed. This is to remove contaminates in the developed regions. This uses an O_2 plasma to do this. This is a light etching process to remove contaminates from the surface rather than etching into the sample.

3.1.4 Photolithography

In this work photolithography was used to fabricate devices, which is an optical method used in the semiconductor and microfabrication industry as it is a highly precise and repeatable process to create intricate pattern(s) on a substrate, which can then be etched into or deposited onto. A sample is coated in a chemical and then has a mask placed over the top of the sample. A UV light source is then exposed to a sample (smaller wavelengths can be used in the right system to achieve higher resolutions), this causes a chemical reaction to occur in which effects the chemical solubility of the exposed region. This is then submerged into a developing solution which removes the more soluble photoresist, leaving the insoluble resist as a pattern formed from the photo-mask. It should be noted that the developing solution etches into the different photoresist at different rates, and potentially the sample as well, hence consideration should be made so that the processes are compatible.

In general the process for Photolithography is as follows:

- A sample is prepared, cleaned and depends on the process dehydrated.
- A photoresist is spun onto the surface, creating a thin film which is sensitive to UV light and temperature.
- The sample then has a mixture of heat and UV light, likely in combination with a mask in order to pattern the photoresist.
- Then the sample is submerged into a developing solution, etching away the patterned photoresist and leaving behind a pattern on the sample.

The exact process will vary depending on the resist and sample being used. As different photoresists require different UV doses, different wavelengths and different heat treatments, the substrate can also

effect the transfer of heat and absorption and reflection of the UV light. For example transparent samples often require higher UV doses than their opaque count parts. It is important to limit the samples exposure to UV and heat during this process. One of the ways to improve the photolithography is to deposit the photoresist onto the sample using a syringe, the photoresist is drawn into a syringe and left to hang overnight. As a result of this, particles within the photoresist fall to the bottom and air bubbles rise to the top. The resultant photoresist deposited on the sample are more uniform rather than the same photoresist which is poured directly onto the sample. Another method is to use a pipette to transfer the photoresist, however, this can introduce a new source of particles and impurities into the solution. This also has the potential to contaminate the whole bottle of photoresist unless it is decanted.

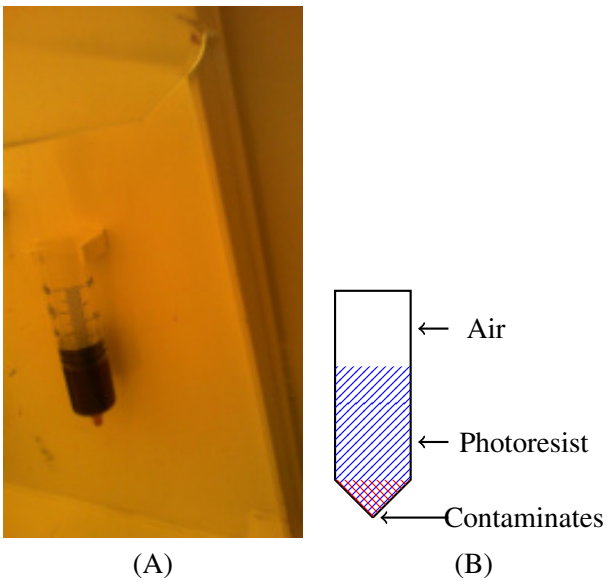


Figure 3.4: In subfigure (A) An example of photoresist being stored in a syringe, this is performed the day before and stored hanging, and (B) a diagram for clarity. The syringe is filled with photoresist and it is hung up. Air bubbles within the syringe float to the surface, after sufficient time when applying the photoresist later it has the air bubbles removed resulting in a more consistent application. Contaminates also sink to the bottom so before application to the sample the initial dose is discarded to remove these contaminates.

The different photoresist used in this work are referenced in Section 3.2.1, with different issues, such as material no longer being available and protocols changing and being further developed, the exact protocol for each will be stated where it is relevant.

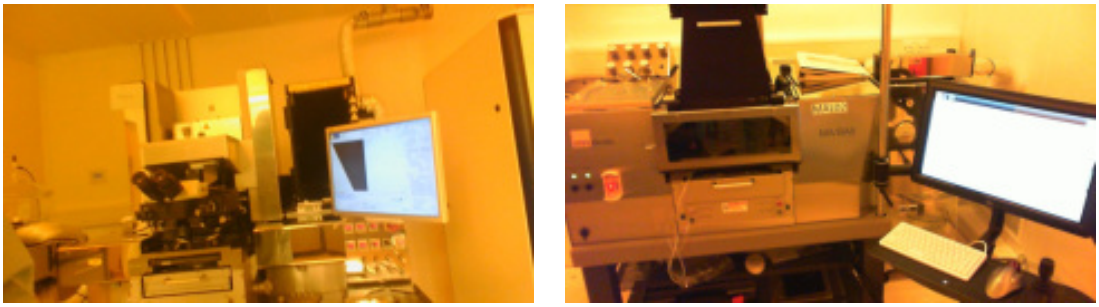
3.1.5 Spin coating

A spin coater is a common tool in microfabrication and semiconductor industries, they work by spinning a liquid photoresist material onto a substrate at high speeds to spread the photoresist and generate a thin and uniform coating. The sample shape and spin speed will effect the variation across in the film, it is common to have a build up of resist at the edges. All photoresist spin coating was performed with a Laurell Spin Coater 200 mm, Laurell (USA). This can be seen in Figure 3.5.

Figure 3.5: One of the Laurell spin coaters used in this work, this was used in all processes which require a photoresist spun on to a sample, or adhesive agent. Depending on the process the parameters can be changed from spin speed, acceleration, duration, a process can be multiply steps. It is able to hold wafers up to 200 mm with adaptors down to 10 mm.

Mask Aligner

There were two mask aligners used in this work, both of these are manufactured and sold by Microtech suss MA/BA gen 4, Series semi-automated mask aligner. These mask aligners can be seen in Figure 3.6. In these mask aligners, three different marks were used, these were purchased from Photonics and are shown in the relevant Chapters, as the mask are not relevant outside their chapter.



(A) (B)

Figure 3.6: The two mask aligners used in this work, (A) is and (B) is. These are both from SUSS MicroTec MA8 mask aligner, SUSS GmbH (Germany).

3.1.6 Metal Deposition System

In this work metal deposition was required, there were three different metal deposition systems which were used. Firstly the Lesker 75 PVD system, then the Moorefield magnetron sputtering and the Moorefield Electron beam evaporation system (E-evaporation) evaporation system.

Lesker 75 PVD system

The Lesker 75 PVD system produced by Kurt. J. Lesker company, it is a magnetron sputtering PVD system. The system was pumped down until the pressure was in the order of 10^{-5} torr this was often left to pump overnight, then Ar is passed into the system. A potential is applied between the target

material and the gun, this ignites a plasma above the target. This plasma vaporises the target material, and this material is then drawn towards the sample due to the magnetic field. In this system the distance between the target and the sample are at a distance, this is beneficial as it is does not fill the undercut in a negative photoresist to any degree. This is Figure 3.7 where the closer the target is to the sample, the more metal is deposited into the undercut region. The target material is often burned off for a while in order to remove surface contaminates and surface oxide layers. Another method for reducing contamination is to deposit a getter layer of Ti, this is to trap any contaminates in the chamber and O_2 within the chamber. The deposition rate is measured using a crystal monitor, which is within the chamber. The sample is held at the top, where it is covered by shutter which has to be opened before material is deposited onto the sample. The target material is purchased from Kurt. J. Lesker, where 2" targets of Ti, Al, Ag and Au were used. The tool can be seen in Figure 3.8.When dealing with small samples, they are secured on using polyamide tape covering the outermost edges or double sided to the back of the sample. As the tool was not designed for 2" wafers a specific holder had to be machined for the purpose, this held the wafer in a inlet avoiding the need for polyimide tape. This can be seen in Figure 3.9.

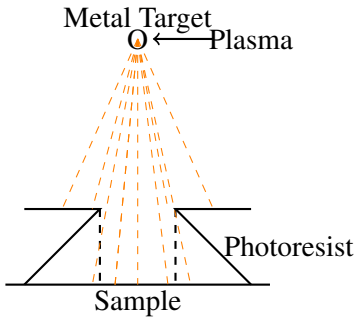
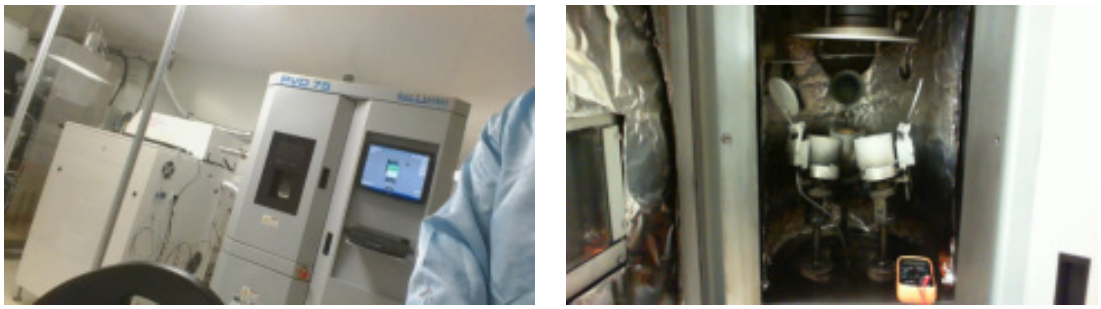


Figure 3.7: A diagram to illustrate why having a long distance from the metal targets to the sample is advantageous for a PVD system for metal lift off. A plasma forms below the metal target, this removes material from the metal target creating ions. these than bombard the sample to deposit metal onto the surface. In this diagram these are shown with dashed lines. The photoresit blocks these ion with exposed areas of the sample being coated with metal. With a lift off process an undercut is used so the angle the ion enters an exposed region in can flll in this undercut. The further away form ion source the less ions fill in this undercut.

Moorefield Magnetron Sputtering

Much like the Lesker 75 PVD system the Moorefield MiniLab 125 is another magnetron sputtering PVD system, this means that it operates in a very similar manner as KLesker PVD Section 3.1.6. There are a couple of differences, firstly to load the chamber it utilises a load lock system. This is where a sample is loaded into a separate chamber which is connected to the main chamber. This means that the main chamber is kept under vacuum most of the time, unless the targets need to be replaced or for maintenance purposes. This means that the time to reach a vacuum is much faster and the contaminates going into the chamber are limited. However, it does add extra considerations as

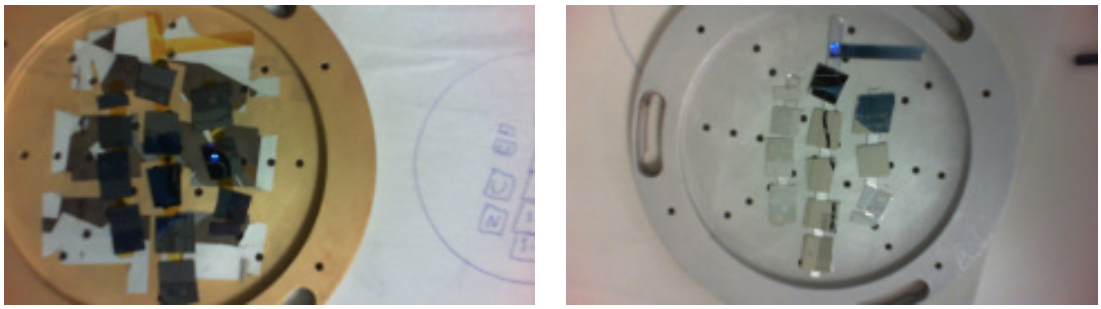


(A) (B)

Figure 3.8: The Lesker PVD system used in this work, (A) the tool and (B) inside the chamber. In (B) you can see the three separate guns which hold the metal targets at the bottom and the shutter and sample holder at the top.

Figure 3.9: The 2” holder which had to be made for this tool in order to hold 2” wafers without the need for tape. This is a simple holder with a small inlay to hold a wafer without the need for clips or polyimide tape. This results in a

the target has to be moved into the main chamber, which means there is more risk of damage to the sample and tool in this process. Another difference between this system and KLesker PVD 3.1.6 is the size of the target material used. In this system the targets are 4”, this means that it has a much higher deposition rate. The chamber length is not as long as the KLesker PVD, so the deposition is not as well suited for metal lift off processes. This can be seen in Figure 3.11, the targets were purchased from KLesker.



(A) (B)

Figure 3.10: An example of small samples being held in the PVD, before (A) and after (B) the deposition. This has to be done using polyimide tape or clips.

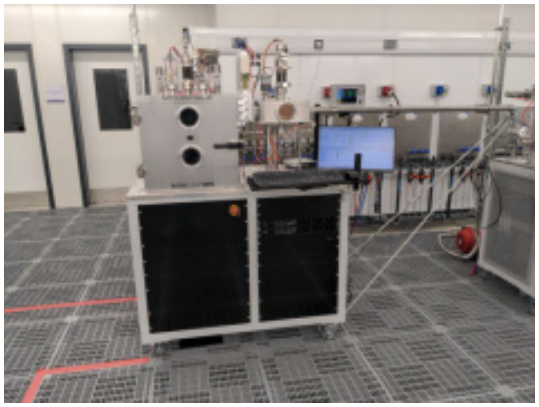


Figure 3.11: The Moorefeild PVD used in this work, the Moorefield MiniLab 125. This has a load lock system to insert samples into the chamber, resulting in a cleaner chamber and faster pump down times. This dose mean it is limited to how many metals it can deposit as it requires the main chamber to be vented and targets to be switched out.

Moorefield Electron Beam Evaporation

An E-evaporation evaporation system was also used in this work, also a Moorefield MiniLab system variation 80. This system has thermal and E-evaporation capabilities, for this work only the E-evaporation was used. In this system material is kept in crucibles initially as pellets which are targeted by an electron beam, this progressively melts and then vaporises the material which in turn creates the plume of material which is deposited on to the substrate. Care has to be taken with the ramp rate for the electron beam hitting the material, this is for increasing and decreasing. This is because the crucible can easily be damaged by a quick temperature change. Much like in Section 3.1.6 the sample is loaded using a load lock system, with the same benefits and risks associated with this. The equipment is shown in Figure 3.12, the pellets used for this system were purchased from KLesker, as were the crucibles.

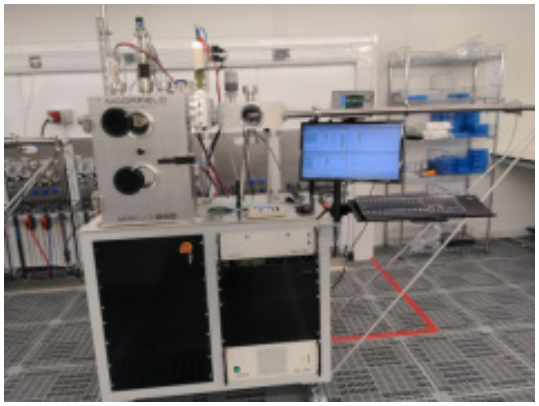


Figure 3.12: The Moorefeild E-evaporation system used in this work, Moorefield MiniLab system, variation 80. This has a load lock system to insert samples into the chamber, resulting in a cleaner chamber and faster pump down times. The metals are limited as the system it kept under vacuum. The pellets and crucibles are roated

3.1.7 Plasma Enhanced Chemical Vapour Deposition

Plasma Enhanced Chemical Vapour Deposition (PECVD) STS PECVD (STS Technologies, UK). This tool which uses a plasma to enable reactions to occur on the sample surface which would normally require higher operating temperatures in normal CVD systems. In this work it was only used to deposit SiO_2, this is done by passing SiH_4 and O_2 into the chamber (105 sccm and 300 sccm). The temperature of the sample was held at 100°C. An image can be seen in Figure 3.13. It has a load lock system where a wafer is held on a susceptor, pumped down to vacuum and then transferred inside the chamber. Once inside then the PECVD process can start by igniting the plasma and introducing the gases into the chemical shower on to the surface of the sample. As this tool was not designed for 2" wafers, a specific carrier wafer had to be fabricated for this. This was done by using a 6" Si wafer, placing a 2" Si wafer on top of this. This was then transferred into the chamber and a few μm of SiO_2 was deposited. This left a 6" wafer with a 2" exposed Si, this was then etched into to create an inlet which could secularly hold 2" wafers.

(A) (B)

Figure 3.13: The Plasma Enhanced Chemical Vapour Deposition (PECVD) used in this work, (A) is the front section and (B) is the back section. The back section was kept in the grey area of the clean room.

Molecular Vapour Deposition (MVD©)

The molecular vapour deposition (MVD©) is a tool which is produced by SPTS Technologies which is able to perform ALD processes. As discussed in Section 2.2.3, a precursor is introduced into the chamber, reacts with the surface, then the chamber is purged where a new precursor is introduced to react to the new surface Each cycle grows the layer and this is continued until the layers have been grown to the desired thickness. The MVD is an interesting tool because it can perform ALD processes, without the need for carrier gases and it is able to do this at low temperatures to fabricate highly conformal thin films [462]. As this does not require carrier gases the precursors can be left

Figure 3.14: This is the carrier wafer which had to be fabricated in order to process the 2" Ga_2O_3 samples. This was done using both the PECVD to create a carrier wafer to securely hold samples.

to react indefinitely inside the chamber. It is also worth noting that the MVD© also had Molecular Layer Deposition (MLD) capability, this is where it is able to deposit long chain molecules as well as reactions which are not self limiting. In this work the ALD process was used to generate a thin film of Al_2O_3 onto the surface of β-Ga_2O_3.

This was performed using the precursors in a cyclic manner:

- Trimethylaluminium (TMA) deposited first to react with native hydroxyl groups.
- DI water, to reacts with the methyl groups releasing CH_4 to generate more hydroxyl groups for the next round of TMA to react with.

The cycle is repeated, growing the film thickness each round and is continued until it has reached the desired growth. This was performed at 100°C over a 24 hour process, the tool can be seen in Figure 3.15. This process was used as in other work it has been show to deposit a amorphous layer of Al_2O_3 [462]. The chemistry growth cycles are also shown in Figure 3.16. The samples are placed inside and then pumped down to vacuum, after this the cycle starts by introducing the precursors in a cyclical manner.

Figure 3.15: The molecular vapour deposition (MVD) this uses an ALD process to grow thin films of Al_2O_3 onto β-Ga_2O_3 and Si, this was done using an ALD process without the need for carrier gases, at 100°C.

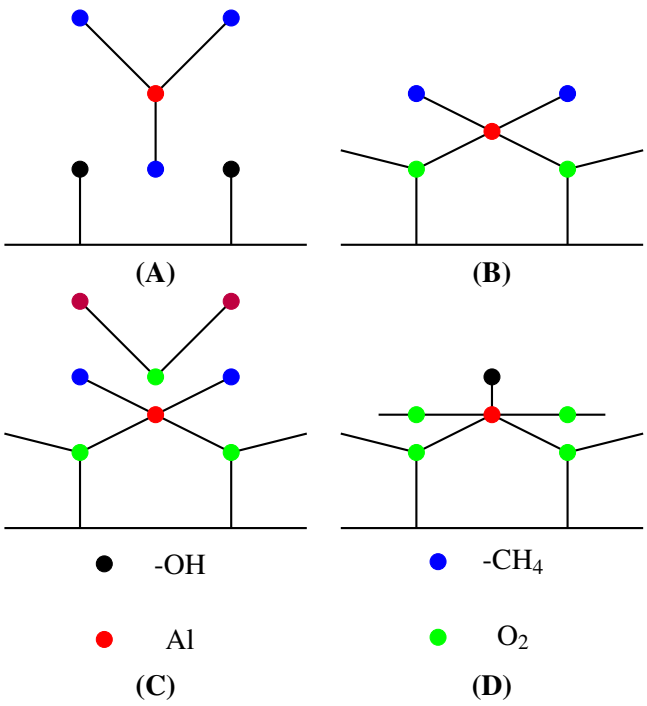


Figure 3.16: Diagram showing the MVD deposition cycle. In (A) TMA is introduced into the chamber and reacts to hydroxyl groups, then (B) the system is purged removing all unreacted TMA, (C) DI water is introduced reacting with CH_3 groups regenerating the hydroxyl groups as the system in (D) is purged again ready to return back to (A).

3.1.8 Annealing Systems

In this work annealing was required, the two RTA systems used in this work were the Jetfirst Jipelec Annalsys RTA and Annalsys AS Mater RTP-system, the samples are held in a graphene coated, SiC susceptor. The susceptor is used as it can hold samples which are not whole wafers, it also means that the samples are held at a more uniform temperature. The temperature can either be measured using a thermocouple or pyrometer. The thermocouple works by measuring the potential generated by the Seebeck effect where as the pyrometer operates by measuring the intensity and the wavelength of the light given off from the susceptor. This is another reason for the use of the susceptor, as different samples will react and give off wavelengths of light at a given temperature so keeping the susceptor constant means the sample should be kept the same. The heating element is provided by lamps above the susceptor. The samples are pumped down to vacuum to begin with and then Ar is passed though system. The tool can be seen in Figure 3.17.

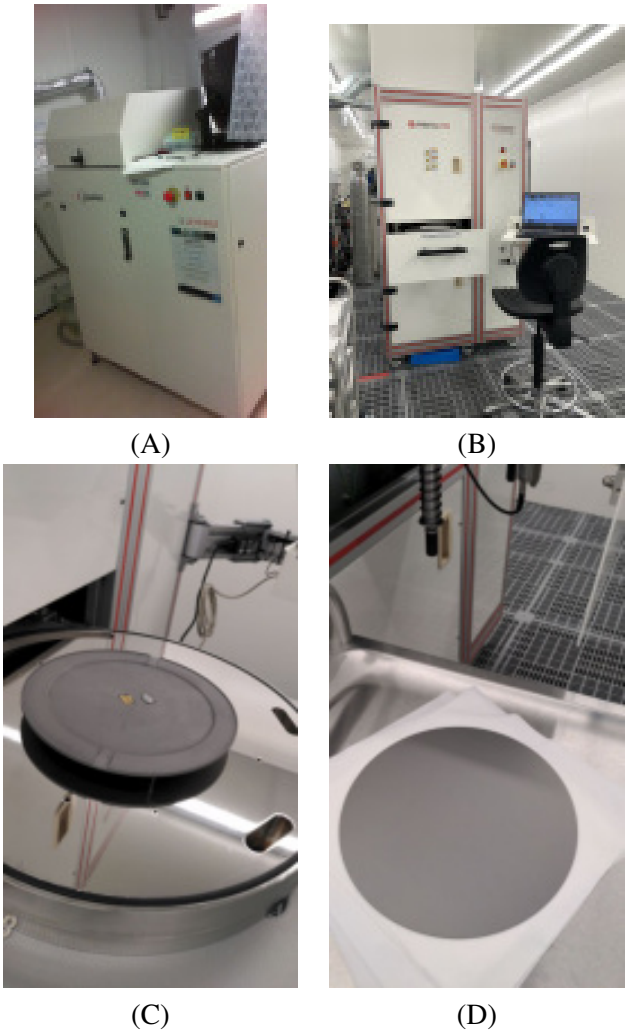
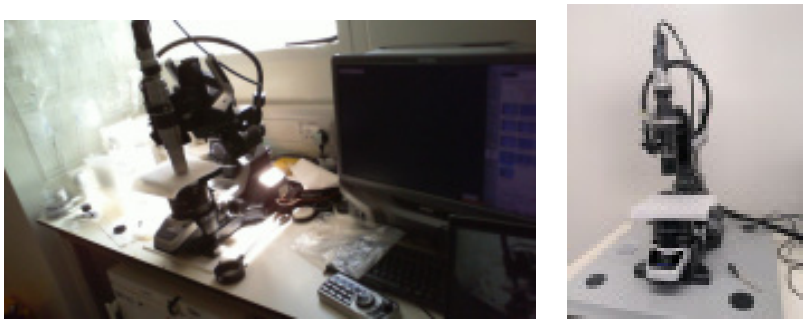


Figure 3.17: The RTA systems which was used, in (A) the whole Jipelec Jetfirst used in this work and (B) the Annalsys AS Mater RTP-system. The SiC susceptor coated with graphene which was used to hold the samples can be seen in Figures (C) and (D). The thermocouple is connected into the side of the susceptor, this is to get a more accurate reading of the temperature.

3.1.9 Keysight Microscope

In this work it was necessary to image the sample under a microscope, the microscope used was the Keysight Micro and is shown in Figure 3.18.



(A) (B)

Figure 3.18: The Keynest microscope used in this work, (A) is in high resolution and (B) in low resolution.

3.1.10 SEM

Scanning electron microscopy (SEM) uses high energy electrons are focused into a beam which interacts with the surface of the sample as it scans across the sample. The image is created from the combination of backscattered electrons, elastic collisions with atoms in the sample. Secondary electrons, which are ionised from the surface, are detected and used to generate an image of the sample surface. The SEM used in this work was the Hitachi S-4800 field emission scanning electron microscope. The voltage can vary between 0.5-30 kV and current 1-20 μA. The highest resolution is was 1 nm available is, higher than was necessary in this work. The SEM also had the capabilities to perform Energy-dispersive X-ray spectrometry (EDX), this is where the electron beam is used to excite a region of the sample. This is in order to generate photons, which are generated by changes in the energetic states of ionisation of the sample producing X-rays. These X-rays have unique energy levels (due to the nature of electronic orbitals and energy levels). These wavelengths of light are detected by a detector on the EDX and can generate a model of the composition of the sample. This tool was available on the Hitachi S-4800 field emission scanning as Oxford instruments EDX detector, these are shown in Figure 3.19

Ellipsometry

In this work the M-2000 Spectroscopic Ellipsometer manufactured by J. A. Woollam Co was used, and can be seen in Figure 3.20. Ellipsometry is a common technique used to investigate the sample optically, in a quick non-destructive manner. It is able to be used on a wide range of materials, and investigate the refractive index and extinction coefficient) as well as the thickness of thin layers. Because of this, it is used in numerous fields, such as semiconductors, material science, sensors and optics. In this work only the surface layers were measured, no through measurements were taken.

(A) (B)

Figure 3.19: The SEM used in this work, (A) is the Hitachi S-4800 SEM and (B) is the Oxford instruments EDX detector.

A beam of polarised light is directed towards the surface of a sample, as it hits the sample it reacts to it. This changes the lights creating some transmission and reflection pattern. Through different interactions based on the optical dielectric, thickness of the layers and amount of layers it will emit a diffraction pattern of light where the light is constative/destructive as it moves out of phase with itself. A detector is used to pick up the resulting light, collecting its new polarization in relation to the incident plane (both perpendicular and parallel) and amplitude. To use this data a mathematical model has to be generated and fitted to data.

The model is used to describe how polarization and amplitude should change after interacting with a layer, more layers should be modelled as multiple models which then have to be fitted. As this is a mathematical model which is based from a single measurement it is important to be approximately correct values for the constants and thickness, the fitting process will adjust these to match the real data as much as possible. It should be noted, as with all fittings like this it is possible for a fitting to be trapped in local minimum or in a mathematically stable but non-physical state. Once this has been fitted well then it is possible to calculate the film thickness, refractive index, extinction coefficient and roughness. This can be used to create a map across the wafer to look at how conformal it is. In our work the Ellipsometry was used to measure the deposited thin films. In this work Cauchy models were used to model the optical properties of different thin films, this is where the refractive index is approximated as,

$$n(\lambda) = n_0 + \frac{n_1 \times 10^2}{\lambda^2} + \frac{n_2 \times 10^7}{\lambda^4} + ... \tag{3.1}$$

and the extinction coefficients as,

$$k(\lambda) = k_0 + \frac{k_1 \times 10^2}{\lambda^2} + \frac{k_2 \times 10^7}{\lambda^4} + ... \tag{3.2}$$

This allows for a simplistic approximation which is suitable for many thin films, with many photoresists having the optical constants as part of their technical data sheet. Note that the terms in Equation 3.1 are expressed as A, B and C in model used in this work.

This was the dominant use of the ellipsometer in this work, as the initial stages of developing a process for patterning a sample with photoresist is to determine the thickness of photoresist which is spun onto the surface. In this work the fitting parameters expressed as A, B and C are the optical constants n_0, n_1 and n_2 respectively. These were used to generate an n, refractive index of the material as well as generate a model of the thickness and surface roughness. This fitting has an associated MSE, Mean Squared Error which is a calculation as to how well the model fits the data, which is different to the standard deviation of the fitting itself. This is important as thinner, faster spun films tend to be more uniform, however, there is less photoresist present meaning lift-off processes and plasma descum or over development could be problematic. Apart from measuring photoresist, other thin films were also measured, such as Al_2O_3, SiO_2 and SiN_x performed in this work. In this work these layers where relatively thick (50 nm), in chapter 5 these were to investigate the dielectric-semiconductor. This is much larger then what is typically used, normally about 20 nm, it should be clear that thinner film will breakdown at a lower voltage, and cause more leakage current, however, it means that the gate voltage has far more of an impact on the underlying semiconductor. The different deposition techniques effect the purity, leakage current, etch rate and refractive index For example PECVD can have a refractive index from 2-1.5 [463], or about 1.46 with ALD deposition [405]. For Al_2O_3 deposited by ALD under the same conditions used here had a refractive index of about 1.6 [462]. The refractive index for the photoresists were taken from the manufacture technical data sheet, the thickness of these layers were typically in the micrometers.

While not performed in this work, this method can also be used to characterise epi-layers of β-Ga_2O_3, in this work it was performed on spectator wafers or as part of some optimisation before transferring onto β-Ga_2O_3. This was because β-Ga_2O_3 is transparent, something which makes ellipsometry more difficult, while possible it was not performed here as it would require knowledge of the backside substrate reflections or to either roughen the back surface to remove backside reflections or through measurements. Analysis was performed using the software CompleteEASE which was pre-installed also manufactured by J. A. Woollam Co.

Figure 3.20: The Ellipsometer used in this work, the M-2000 Spectroscopic Elipsometer by J. A. Woollam Co. Predominately this was used to determine and confirm the thickness of photoresist which was spun onto the surface of predominately Si. This was often the first stage of optimising the protocol for a particular photoresist.

3.2 Materials

In this section the different materials will be described and listed.

3.2.1 Photoresist

In general when using photoresists there is a common issue depending on the sample size. If the sample was small then a pipette is used to extract a portion from the bottle before applying to the sample, if the sample is large enough then it can be poured directly onto the sample. Another method for applying the photoresist is to use a specific syringe. This is to get a better result from the deposition. This is because after decanting into the syringe, and left for adequate time afterwards, the trapped air will rise to the top. Which means that there should not be any air bubbles in the photoresist after it is applied. Particles will fall to the bottom of the syringe, which means that these contaminants can be removed, this results in a pure photoresist solution being applied to the sample. Figure 3.4 shows an example of a photoresist syringe. There are three types of photoresist:

- Positive photoresists is one where the exposed resist becomes more soluble to an appropriate developer. The unexposed regions remain less soluble, and so after development, they remain on the samples surface. Positive photoresists are used to achieve straighter side walls, which is desirable for plasma etching.
- Negative photoresists is when the exposed resist becomes more insoluble to the developer. This means the unexposed regions are etched faster and leaving behind exposed patterns on the sample. It should be noted that this means the deeper into the resist layer is more soluble. It is in fact a feature utilised to create an overhang of the photoresists to allow the metal lift off processes to work.
- Image reversal photoresists, can either act as a positive or negative photoresist, depending on the treatments which it has been though.

In this work both Bi and single layer photoresists were used. Bi-layer photoresist protocols are where both positive and negative photoresists are used in conjunction with one another. A positive and negative resists, are utilised to get better precision where a positive photoresist on a negative. This is used to achieve straight side walls and allow a large undercut. In this work, positive, negative, image reversal and bi-layers processes were used.

3.2.2 ECI 3027

In this work, one of the photoresists used was ECI 3027, which is a photoresist produced by MicroChemicals, this can be seen in Figure 3.21. It is a thin positive photoresist which is capable of producing straight-side walls, the technical data sheet is available online at [464]. It can be developed with MIF and MIC developers. In this work, it was used in Chapter 4, where a protocol was developed with the intent to etch Ga_2O_3. This was patterning the photoresist on SiN_x/β-Ga_2O_3.

3.2.3 AZ 5214 E

In this work AZ 5214 E was one of the photoresists used, this is a photoresist produced by MicroChemicals. It is an image reversal resist, designed for lift-off protocols and it can be used as a positive

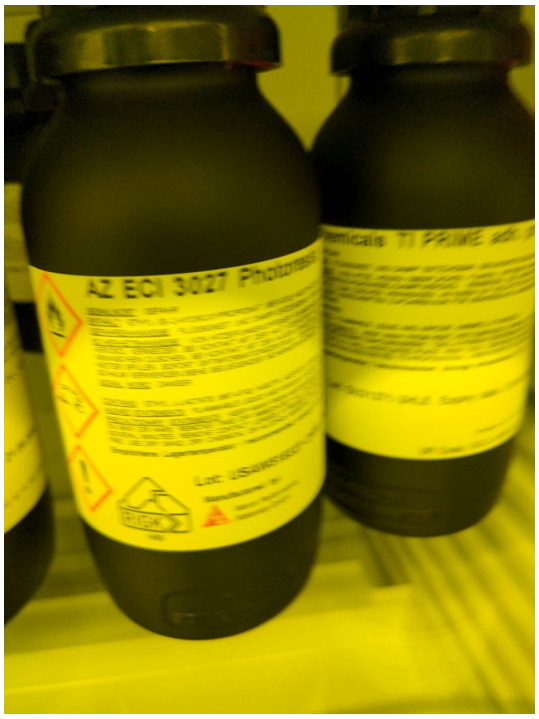


Figure 3.21: AZ ECI 3027 photoresist, this is a positive photoresist manufactured by MicroChemicals.

or negative photoresist depending on the protocol used. In this work it was only used as a negative photoresist, in Chapter 6, the technical data sheet is available online at [465]. This photoresist has since been discontinued, as a result of this it was necessary to change protocols and develop new ones. This can be seen in Figure 3.22, in this work, the protocol used was as the negative variant. The negative behaviour is caused by a cross-linking agent in the photoresist which is active above 110°C only in the exposed regions. This causes the photoresist to be insoluble in the developer and stops these areas from being sensitive to UV light, which is left behind after the development process.

Figure 3.22: AZ 5214E used in this work.

3.2.4 AZ LNR-003

In this work AZ LNR was one of the photoresists used, this is a photoresist produced by MicroChemicals, this is shown in Figure 3.23. It is a negative photoresists designed for lift-off protocols, the

technical data sheet is available online at [466]. It was used in Chapters 5 and 6. In both cases, AZ LNR 003 was used for a metal lift-off process. TMAH-based developers are recommended, however, TMAH etches into Al_2O_3. TMAH is also quite a hazardous substance, hence a MIC-based developer was preferred. The MIC developer used was AZ-developer from MicroChemicals, which is discussed in Section 3.2.7. AZ LNR 003 was a replacement for AZ 5214 E for metal lift-off protocols, as the supply dwindled due to it being discontinued.

Figure 3.23: AZ LNR-003 negative photoresist, this was used for lift off processes in this work.

3.2.5 LOR 3B

This is a positive photoresist which is designed for simple bi-layer processes, it is manufactured by Kayakli and the technical data sheet is available online [467]. It is used as the under layer in a bi-layer process, with the etch rate determined by the soft bake. It can be developed in TMHA and metal-ion containing solutions, this was used in Chapter 6.

3.2.6 AZ 1512 HS

AZ 1512 HS is a positive photoresist manufactured by MicroChemicals, the technical data sheet is available online at [468]. It is a general use photoresist and was used as part of a bi-layer metal-lift-off process, where this was used as the top patterned layer. This can be seen in Figure 3.25, it was used in Chapter 6.

3.2.7 Ti-Prime

Whilst not a photoresist, it is appropriate to list Ti-Prime alongside the photoresist used in this work. Ti-Prime is an adhesion agent applied to samples before the photoresist was applied. After being spun and baked onto the sample, it improves the adhesive of the photoresist to the sample. Ti-Prime is produced by MicroChemicals, the data sheet is available online at [469]. Ti-prime was used throughout this work, this is shown in Figure 3.26 and was used in Chapters 6 and 5.

Figure 3.24: LOR 3B positive photoresist, produced by Kayakli, for bi-layer photoresist processes. This was used as part of a bi-layer, metal lift-off process.

Figure 3.25: AZ 1512 HB, a positive photoresist, produced by MicroChemicals, used in a bi-layer photoresist processes. This was used as part of a bi-layer, metal lift-off process.

Figure 3.26: The adhesive agent used in this work, Ti-Prime.

AZ Developer

In this work AZ Developer was predominately used for the development step for different photoresists, it is produced by MicroChemicals and the technical data sheet is available online at [470] and can be seen in Figure 3.27. It is an inorganic MIC developer solution with low etch rates for Al_2O_3, the active components are disodium metasilicate and tri-sodium phosphate. This and the relative safety compared to other developers are one of the reasons this was used throughout this work. It was used in all the experimental Chapters.

AZ 726

AZ 726 was used in this work, predominately used in Chapter 4, which can be seen in Figure 3.28. This is a TMAH-based developer which is produced by MicroChemicals, the data sheet is available online at [471]. As it is a TMAH-based developer, it etches into Al is approximately 100 $\text{Å} \cdot \text{min}^{-1}$. While the etch rates for β-Ga_2O_3 are low compared to KOH etching [244], however, in Chapter 4 this was SiN_x/β-Ga_2O_3 so more resilient. As Al was used in Chapter 5 and 6 of this work, where possible MIC developer were preferred.

3.2.8 TechniStrip Micro D350

In this work TechniStrip Micro D350 was used to strip photoresist and is considered non-toxic, in this work it was used to strip the photoresist in a metal lift-off process. TechniStrip Micro D350 is a Dimethyl sulfoxide (DMSO) based solvent solution, this can be seen in Figure 3.29. This was performed at temperatures up to 80°C or the solution was left covered overnight. This was purchased from MiceroChemicals and the technical data sheet is available online at [472]. In certain processes when the metal-lift-off was not successful then the solution was sonicated. This was used in Chapters 5 and 6.

Figure 3.27: AZ Developer, this was used in many different sections of this work.

Figure 3.28: AZ 726 developer, a TMHA based developer used in this work.

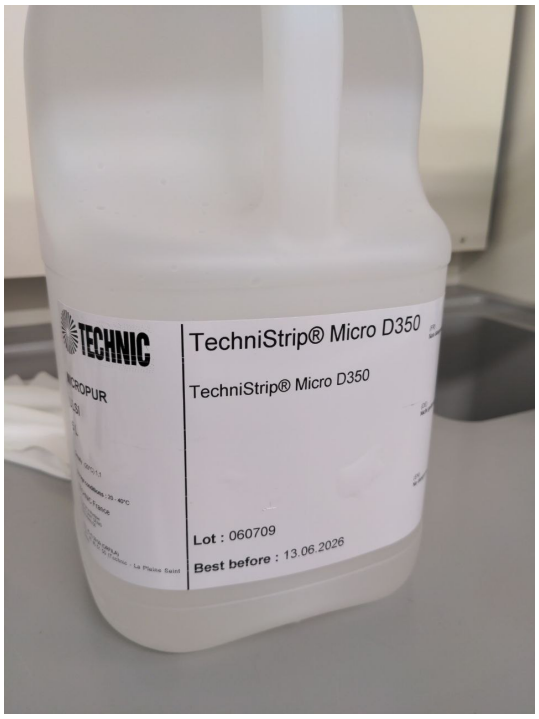


Figure 3.29: TechniStrip Mirco D350, this is a DMSO based mixture of solvents used as part of the lift-off processes in this work.

3.2.9 Epitaxial wafer

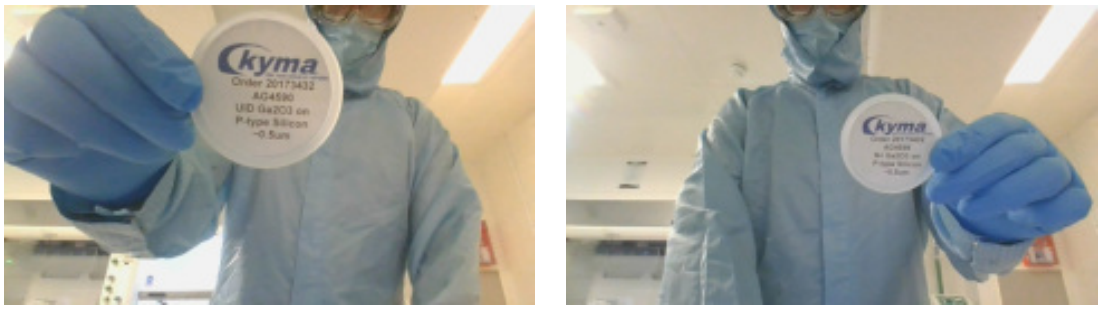
In this work two 2" wafers, diced into 10 mm die were used. These were grown on a Si and SiC substrates with a layer of (-201) β-Ga_2O_3 grown on the surface. This layer was either intentionally doped with Si to mid 10^{18} cm^{-3} or unintentionally doped β-Ga_2O_3 layer. The Si substrates were doped p-type with Boron and the SiC were nominally-type. These were purchased from Kyma, in 2017 hence why there is some details unknown. These can be seen in Figure 3.30.

3.2.10 Beta Gallium Oxide Wafers

In this work three β-Ga_2O_3 wafers were purchased from Novel Crystal, these were 2" wafers and one of them was diced. The doping was in the order of 10^{18} cm^{-3}, this was confirmed in two of them by CV measurements. These are shown in Figure 3.31 and the specifications can be seen in Table 3.1. Wafer N02613 additionally diced into 10 mm die.

Sapphire Wafers

In this work α-Al_2O_3 were used, this is because there are similarities between β-Ga_2O_3 and Al_2O_3. While the β phase of β-Ga_2O_3 is associated with the θ phase for Al_2O_3 the α phase was chosen. This is because it is commercially available at a reasonable price, like β-Ga_2O_3, it is also a transparent substrate which can affect the optimisation of the photoresist patterning process. While the thermal properties are different, it was used in the development for some of the process optimisation in Chapter



(A) (B)

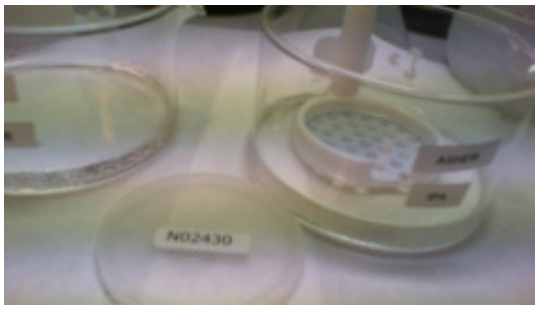
(C)

Figure 3.30: The epi-wafers used in this work where Sub-Figures (A) and (B) were on of p-type Si substrates. These have an epitaxial layer of β-Ga_2O_3 grown on top of them, (A) are unintentionally doped and (B) are intentionally doped with Si likely to be in the mid 10^{18} cm^{-3}. The p-type Si was doped with Boron, the concentration was not known. Sub-Figure (C) is intentionally doped with Si, epi layers of β-Ga_2O_3 grown on 6H-SiC. All these epi-layers of β-Ga_2O_3 were (-201) oriented.

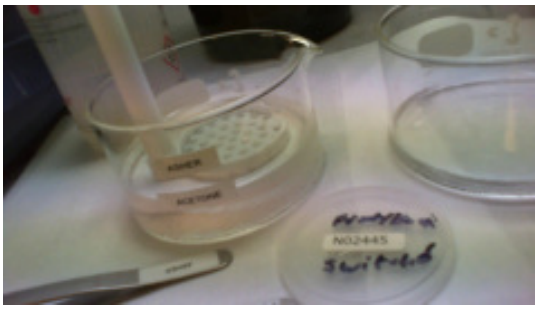
	N02430	N02445	N02613
Diameter (mm)	50.8	50.8	50.8
OF (mm)	15.9	15.9	15.9
IF (mm)	8.0	8.0	8.0
Thickness (mm)	0.65	0.66	0.66
Orientation	(001)	(001)	(001)
Fount	CMP	CMP	CMP
Back	CMP	CMP	CMP
Dopant	Sn	Sn	Sn
Doping (cm^{-3})	8.6×10^{18}	1.1×10^{19}	7.0×10^{18}
Offset [001]	0.0	0.0	−0.1
Offset [010]	−0, 2	−0, 2	−0, 1
FWHM [001]	23	24	22
FWHM [010]	23	23	24

Table 3.1: The β-Ga_2O_3 wafer specifications, from the manufacture Novel Crystal. Where OF is the outer flat, IF is the inner Flat, FF front finish, BF is the back finish, the offset angles where in degrees and FWHM are in arc sec. CMP stands for chemical and mechanically polished.

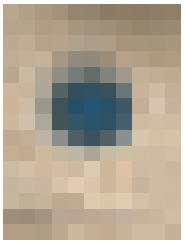
4. These wafers were purchased from Inseto and can be seen in Figure 3.32, with the specification in Table 3.2.



(E)



(F)



(C)

Figure 3.31: The (001) β-Ga_2O_3 used in this work, these were purchased from Novel Crystal and used in all the chapters throughout this thesis. Sub-Figures (A) and (B) are wafers N02445 and N02430 respectively, these were taken during solvent cleaning as the whole wafers were used and not diced. Sub-Figure (C) is wafer N02613, this was diced into 10 mm die.

(A)

(B)

Figure 3.32: One of the sapphire α-Al_2O_3 wafers used in this work, these were purchased from Inseto. These were 2", double side polished prime grade wafers orientated on the c-plane (0001), these were grown with the Kyropoulos method. Kyropoulos is similar to the Czochralski however the gradient of the heating is more gradual.

3.2.11 Si wafers

Throughout this work for many reasons many Si were used, often for developing a process or testing that a process or tool were operating correctly. This involved wafers with SiO_2 layers on the wafer, both thermal grown or deposited. In this wafers were purchased from inseto and Pi-KEM. These were 2", 4" and 12" wafers, 2" and 4" were test grade wafers and 12" were dummy grade wafers. The specification can be seen in Table 3.4. Predominantly p-type, though n-type wafers were used when mimicking processing which was to be performed on β-Ga_2O_3. Examples of these wafers can be

Wafer Type	Sapphire	Diameter (mm)	50.8 ± 0.1
Crystal Orient	C-Plane (0001)	Growth	Kyropoulos method
Grade	Prime	Purity	99.998%
Edge Geometry	ground	Thickness	430 ± 20 µm
Polish	SSP	Surface Roughness	< 0.3 nm
TTV	< 10µm	Bow	< 15 < 10µm
Warp	< 15 < 10µm	Alignment	SF

Table 3.2: The specifications for the α-Al_2O_3 wafers which were used in this work. Where SSP is surface fide polish, SF is standard flat and TTV is the total thickness variation.

seen in Figure 3.33. Test grade wafers were used in test runs, operatisation, and spectator wafers, and dummy grade wafers were used as carriers, or initial process testing. The specifications for the SiO_2 can be seen in Table 3.3. These were p-type, doped with boron.

,

(A) (B)

Figure 3.33: Si wafers used in this work, (A) is an example of a 4" wafer this was at test grade and (B) a 12" wafer which is dummy grade. Test grade wafers were used in dry runs, optimisation, and prime grade wafers for spectator wafers, and dummy grade wafers were used as carriers, or initial process testing.

Quantity	6	Batch	312621
Diameter	100 ± 0.3 mm	Substrate	Si
Type	P	Orientation	(100 ± 0.5°)
Dopant	Boron	Growth	Czochralski
Grade	Prime	Thickness	525 ± 20 µm
Resistivity	1-5 Ω · cm	Coating	ATOX
Coating Thickness	50 nm	Polish	SSP
Alignment	SSF	TTV	< 5 µm
Bow	< 30 µm	Warp	< 30 µm
Surface Roughness	< 0.3 nm		

Table 3.3: The specifications for the SiO_2 ordered from inseto. Where SSP is surface fide polish, SF is standard flat, TTV is the total thickness, ATOX stands for a thermally grown oxide layer performed in atmosphere.

Wafer	Silicon wafer	Grade	Prime
Diameter	4”	Type	p-type
Dopant	Boron	Resistivity	0.077-0.078 $\Omega \cdot$ cm
Growth	Czochralski	Centre thickness	675 ± 25 μm
Polish	Single side		
Wafer	Silicon wafer	Grade	Prime
Diameter	8”	Type	p-type
Dopant	Boron	Resistivity	Not stated
Growth	Not stated	Resistivity	Not stated
Growth	Czochralski	Centre thickness	Not stated
Polish	Double side		

Table 3.4: Specification of Si wafers ordered from PI-kem.

3.3 Test Structures

In this section, the logic and mathematics explains the design for the test structures used in this work. This explains the TLM/CTLM test structures which are used to calculate the contact resistance R_c and the sheet resistivity R_{Sh}, the derivation here is mostly taken from Semiconductor Material And Device Characterization by Dieter K. Schroder [473].

3.3.1 Transfer Length Measurements

Transfer Length Measurements (TLM) structures are test structures which are often used to measure the contact resistance R_c and the sheet resistance R_s. By plotting the total resistance vs the contact spacing, the R_s is determined from the gradient and from the intercept at zero spacing intercept the R_c. In their most basic sense, these are rectangles contacts with regular sizes and different spacing between them. This can be modelled as an equivalent circuit as a series of resistors modelling the contact resistance of the metal-semiconductor junction and the resistance of the semiconductor. This design requires isolation etching, so the current path is limited and certain approximations can be made. The different dimensions of these effect the current paths and how to interpret the results, see Figure 3.34. These are effected by a number of variables such as the contact different spacings, contacts widths, as well as the isolated channel width and spacing between the contact and edge of the channel. These dimensions affect the effective area of the contact. A basic idea of a TLM structure can be seen in Figure 3.34 the geometry is important requiring etching. One way to circumnavigate this is to multisite devices with circular designs, where a correction factor and the same mathematics can be used, avoiding the need for etching.

The total resistance R_T is given by,

$$R_T = R_{C1} + R_{C2} + R_S, \tag{3.3}$$

where R_C is the resistance from the two contacts (1/2) and R_S is the resistance from the current spreading inside the semiconductor. This depends heavily on the geometry of the device, then for the

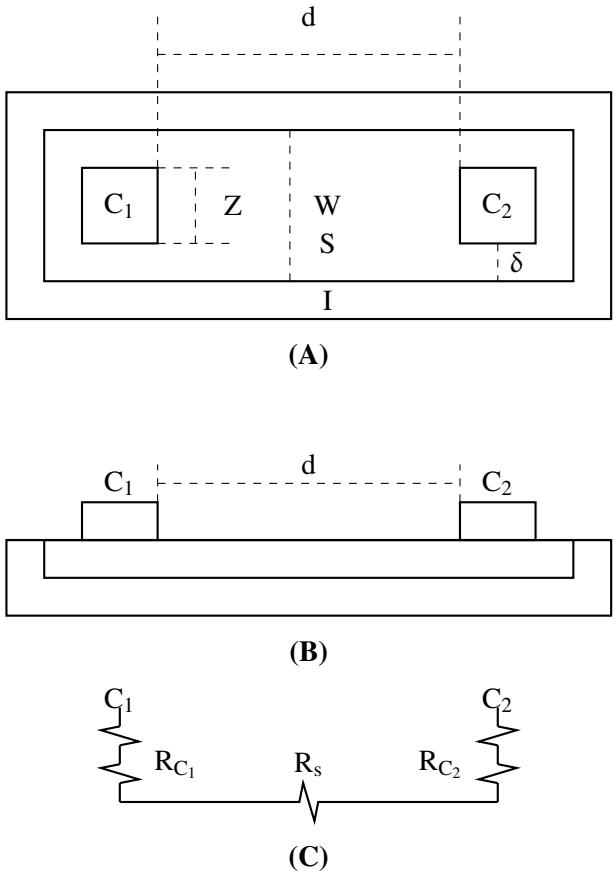


Figure 3.34: A diagram of the TLM test structure, these are top down (A) and a cross-section (B) and an equivalent circuit diagram in (C). The metal contacts C_1/C_2 have ohmic connection to the layer S, this is then isolated from other contacts by layer I. The spacing between the contacts is d, channel W's width and metal contact Z's width. The combined total resistance R_T is the combined metal resistances R_m, the two semiconductor-metal contact resistances R_c and the sheet resistance of the semiconductor R_s.

contacts R_c tend to follow the form,

$$R_C = \frac{\rho_C}{A_C}, \tag{3.4}$$

where ρ_C is the resistivity of the contact and A_C is the area of the contact. As the current passes between the two contacts the current as it is draw from the substrate into the surface starts to crowd, this is the current junction between the semiconductor and the contact. This occurs of a distance known as the transfer length (L_T) and is given by,

$$L_T = \sqrt[2]{\frac{\rho_C}{R_{Sh}}}, \tag{3.5}$$

where R_{Sh} is the sheet resistance. The exact geometry changes the total measured resistance.

With linear TLM the total resistance is given by,

$$R_T = \frac{R_{Sh}d}{Z} + 2R_C \approx \frac{R_{Sh}}{Z}(d + 2L_T) \tag{3.6}$$

where Z is the vertical length of the contact, d the spacing between the contacts, this is from [473].

3.3.2 Circular Transfer Length Measurements

Circular Transfer Length Measurements (CTLM) are derived from TLMs, however, CTLMs do not require isolation etching on the thin films, only requiring slight corrections to the measurements. This also avoids some geometry concerns seen in TLMs, removing the need to consider the variables W, Z and δ. It also removes the need for etching, which makes the fabrication process simple. It removes the need for masking the surface patterning and multiplying alignments, adding their own errors. Chapter 5 explores the requirements for suitable etching in more detail. CTLM, due to their simplest, can be fabricated with simple process steps and can compare the contact resistance with progressive annealing steps [474]. If certain conditions are met then there are several approximations which can be made to generate a "corrections" to the R_T measurements so that the same analysis can used from TLM measurements. The approximations used can overestimate the values calculated, so they should be thought of relative to the R_s The total resistance for a CTLM can be expressed by,

$$R_T = \frac{R_S}{2\pi}\left(\frac{I_0(\alpha)}{\alpha I_1(\alpha)} + \frac{L_T}{L+d}\frac{K_0(\alpha)}{K_1(\alpha)} + \log\left(1 + \frac{d}{L}\right)\right), \tag{3.7}$$

where,

$$\alpha = \frac{L}{L_T} \tag{3.8}$$

and I and K are the modified Bessel functions of the first order, L is the radii and d is the spacing between the contacts, this was taken from [473] however is part of a continual development process. If,

$$L \gg 4L_T, \tag{3.9}$$

is true then,

$$I, K \to 1, \tag{3.10}$$

can be approximated. This in turn means Equation 3.7 can be simplified to,

$$R_T \approx \frac{R_S}{2\pi}\left(\alpha + \frac{L_T}{L+d} + \log\left(1 + \frac{d}{L}\right)\right). \tag{3.11}$$

If,

$$L \gg d, \tag{3.12}$$

then Equation 3.11 can be rewritten as,

$$R_T \approx \frac{R_S}{2\pi}\left(\frac{L_t}{L} + \frac{L_T}{L} + \log\left(1 + \frac{d}{L}\right)\right), \tag{3.13}$$

so,

$$R_T = \frac{R_S}{2\pi}\left(\frac{2L_t}{L} + \log\left(1 + \frac{d}{L}\right)\right). \tag{3.14}$$

This is then often expressed as,

$$R_T = \frac{R_S}{2\pi L}\left(d + 2L_t\right)C \tag{3.15}$$

where,

$$C = \frac{L}{d}\log\left(1 + \frac{d}{L}\right). \tag{3.16}$$

It should be noted here that Equation 3.15 is the CTLM analogous to the TLM in Equation 3.6, where Z is equivalent to 2ϕ, L and C is one. To discuss why in this work an oversight was made, the use of CTLM does not require the use of an isolation etch. However it is the authors beliefs that underline Equation 3.7 is the assumption that,

$$\rho_C > 0.2 R_{Sh} t^2, \tag{3.17}$$

where t is the thickness of the sheet. The authors has been trying to track down the exact deviation of Equation 3.7, as the condition Equation 3.17 is for TLM structures not CTLM. The language which is often used is not wrong but was misinterpreted, as it is true a lateral isolation is not needed in CTLMs it is still required to vertically isolate and perform the measurement on thin films. Woelk et al. [475] found that these corrects if the condition in Equation 3.17 is not true then further corrections must be made for the CTLMs.

3.4 Mathematical Model for Ideal CV

In this work it was necessary to create a model for the MIS capacitor. The description of the Equation 2.8 does not model the measurements, to this, a mathematical model to generate the capacitance values. To start with, C_A is given by Equation 2.3, which requires the dielectric constants, the contact area and the thickness of the dielectric layer. C_A is a static value, as the values which make it up do not change, making it simple to model. However, this is not true for C_S, which is due to the nature effective depletion width (W_{eff}), a reaction of the charge build-up at the interface between the semiconductor dielectric interface. The reaction is due to the inversion of charge, making an effective region blocking charges from flowing. As the applied potential to the metal charges, this impacts the potential in the semiconductor, hence changing the charge build-up, ergo affecting the region is blocking charges from flowing, therefore, changing the W_{eff} of the capacitor model. So to model the capacitance, the vital

step is modelling this W_{eff}, to do this, a series of potentials was generated and the corresponding W_{eff} was calculated as well as the corresponding gate voltage V_g. The calculations for W_{eff} and V_g require quite a few values needed. In [476] an effective model was outlined it starts with generating a list of potentials using,

$$U(x) = \frac{\phi(x)q}{kT} = \frac{E_{i(bulk)} - E_i(x)}{kT}, \tag{3.18}$$

This is then used to defined a uniform potential at the semiconductor surface as,

$$U(s) = \frac{\phi(s)q}{kT} = \frac{E_{i(bulk)} - E_i(s)}{kT}. \tag{3.19}$$

and the Fermi level as a uniform potential as,

$$U(F) = \frac{\phi(F)q}{kT} = \frac{E_{i(bulk)} - E_F}{KT} \tag{3.20}$$

Using this it is possible to calculate the effective depletion width at this potential,

$$W_{eff} = \begin{cases} \hat{U}_S L_D \left(\dfrac{2F(U_S, U_F)}{e^{U_F}(1 - e^{-U_S}) + e^{-U_F}(e^{U_S} - 1)} \right) & \text{In accumulation.} \quad (3.21) \\ \dfrac{\sqrt{2}L_D}{\sqrt{e^{U_F} + e^{-U_F}}} & \text{At Flat band condition} \quad (3.22) \\ \hat{U}_S L_D \left(\dfrac{2F(U_S, U_F)}{e^{U_F}(1 - e^{-U_S}) + \frac{e^{-U_F}(e^{U_S} - 1)}{1+\Delta}} \right) & \text{In depletion} \quad (3.23) \end{cases}$$

It should be noted that at the flat band condition, the uniform potential is zero, hence why there is no factor of U_S. The Δ term is frequency dependent and describes if the result is going to go to inversion or deep depletion. Δ is given by,

$$\Delta = \begin{cases} 0 & \text{Low frequency} \quad (3.24) \\ \dfrac{\frac{e^{U_s} - U_s - 1}{F(U_S, U_F)}}{\int_{0^+}^{U_s} \frac{e^{U_F}\left(1 - e^{-U}\right)\left(e^{U} - U - 1\right)}{2F(U, U_F)^3} dU} & \text{High frequency} \quad (3.25) \end{cases}$$

Depending on whether it is low or high frequency, in high frequency, this is to recreate deep depletion. The term $\hat{U}$ is given by,

$$\hat{U}_S = \begin{cases} +1 & U_S > 0 \quad (3.26) \\ -1 & U_S < 0 \quad (3.27) \end{cases}$$

The function $F(U,U_F)$ is given by,

$$F(U, U_F) = \sqrt{e^{U_F}(e^{-U} + U - 1) + e^{-U_F}(e^{U} - U - 1)}. \tag{3.28}$$

Finally, the Debye length, which is calculated by,

$$L_D = \sqrt{\frac{\epsilon_0 \epsilon_r kT}{2q^2 n_i}} \tag{3.29}$$

The calculation of W_{eff} in respect to a normalised potential. However, this has to be converted into an ideal gate voltage V_g. V_g can be calculated from the normalised potential by,

$$V_G = \frac{kT}{q}\left(U_S + \hat{U}_S \frac{\epsilon_S x_0}{\epsilon_I L_D} F(U_S, U_F)\right) \tag{3.30}$$

From these equations, it means that an ideal CV measurement can be generated with respect to an ideal V_g. These equations produce a CV measurement for a p-type material to convert so that it is appropriate for n-type U_S to be flipped positive to negative. This method not only provides a theoretical framework for generating expectations, but also serves as a practical tool for reading in data and extracting parameters.

3.4.1 Accumulation Capacitance

There are two methods used in this work for determining the C_A. When the capacitor is driven into accumulation C_A plateaus where it is very slowly increasing. The maximum capacitance can be approximated to be the C_A. While in reality, this then trends upwards to a normally non-realised value. A more accurate approximation is explained in Chapter 5, which is generated from fitting data from the accumulation region. For the work in Chapter5, it was required as the CV sweep was limited, however, for this model and its planned use, this was not necessary, and appropriate fitting to data is time-consuming and not appropriate for a Python script where the location of data points and shape of the plot are considerations. This could be addressed later, where a separate script could be used to create a suitable fitting and then fed into the rest of the model.

3.4.2 Equivalent Oxide Thickness

The dielectric value or the oxide thickness can be estimated from the C_A, this is because the two are related by,

$$\frac{C_A}{\epsilon_0 A} = \frac{\epsilon_I}{T}, \tag{3.31}$$

this ratio is true for both quantities, estimating either or generating an equivalent SiO_2 thickness (EOT). This is given by the ratio,

$$EOT = \frac{T}{\epsilon_I}\epsilon_{SiO_2} = \frac{C_A}{\epsilon_0 A}\epsilon_{SiO_2}. \tag{3.32}$$

EOT is often used to compare high-k dielectrics to SiO_2, and this also is more of a true statement as, without additional confirmation, the thickness. Using EOT also addresses the point that without

additional confirmation, the dielectric layer could be affected by contaminates, and so ϵ_A for it might be misleading. EOT is also used as when multi layers of dielectrics are used.

3.4.3 Doping Calculation

One of the uses for the model of the CV curve was to determine the doping concentration. Confirming the doping is essential. It is imperative for the Terman method to know this value accurately, as it can cause significant errors in the interface states determined. The total capacitance due during the depletion of the MIS capacitor is given by,

$$C = \frac{C_A}{1 + \frac{K_I W}{K_S T}}. \tag{3.33}$$

[476]. This W terms needs to be transformed into terms of gate voltage V_G and the reliance of the doping concentration. Considering the surface potential,

$$\phi_s = \frac{qNW^2}{2K_S\epsilon_0}, \tag{3.34}$$

[476], this can be rearranged for W to get,

$$W = \sqrt[2]{\frac{2K_S\epsilon_0\phi_S}{qN}}. \tag{3.35}$$

Then consider the gate voltage which is given by,

$$V_G = \phi_S + \frac{K_S T}{K_D}\sqrt[2]{\frac{2qN\phi_S}{K_S\epsilon_0}}. \tag{3.36}$$

This can be rearranged into,

$$2\phi_S = A^2 \pm \sqrt[2]{A^4 + 4A^2V_g} + 2V_g, \tag{3.37}$$

where A is,

$$\frac{K_S T}{K_D}\sqrt[2]{\frac{2qN}{K_S\epsilon_0}}. \tag{3.38}$$

This can be substituted into 3.35 to get,

$$W = \frac{K_S T}{K_D}\left(\sqrt[2]{1 + \frac{V_g}{V_\delta}} - 1\right), \tag{3.39}$$

where V_δ is,

$$V_\delta = \frac{qK_S T^2}{2{K_I}^2\epsilon_0}N. \tag{3.40}$$

This means that Equation 3.33 can be rewritten,

$$C = \frac{C_A}{\sqrt[2]{1 + \frac{V_G}{V_\delta}}} \tag{3.41}$$

Equation 3.41 can re rearranged into,

$$\frac{C}{C_A} = \frac{1}{\sqrt[2]{1 + \frac{V_G}{V_\delta}}}, \tag{3.42}$$

which in turn can be expressed as,

$$\frac{C}{C_A}^2 = \frac{1}{1 + \frac{V_G}{V_\delta}}, \tag{3.43}$$

then into,

$$\frac{C_A}{C}^2 = 1 + \frac{V_G}{V_\delta}. \tag{3.44}$$

Then Equation 3.44 can be differentiated in respects to the gate voltage,

$$\frac{d\frac{C_A}{C}^2}{dV_G} = \frac{1}{V_\delta}. \tag{3.45}$$

Then expanding the term V_δ from Equation 3.40 to get,

$$\frac{d\frac{C_A}{C}^2}{dV_G} = V_\delta = \frac{2{K_I}^2\epsilon_0}{qK_S T^2}\frac{1}{N}. \tag{3.46}$$

So from the gradient the doping concentration N can be determined by,

$$N = \frac{2{K_I}^2\epsilon_0}{qK_S T^2}\frac{1}{\left(\frac{d\frac{C_A}{C}^2}{dV_G}\right)}. \tag{3.47}$$

3.4.4 Flat Band Voltage

As described in Section 2.10.2, the flat band voltage experimentally is affected by the charges which are present at the interface. To determine the ideal V_{FB}, first the value which has to be calculated is finding the flat band capacitance C_{FB},

$$C_{FB} = C_A\frac{1}{1 + \frac{\epsilon_D W}{\epsilon_S T}}, \tag{3.48}$$

where W is given by,

$$W = \frac{\sqrt[2]{2}L_D}{\sqrt[2]{e^{U_F} + e^{-U_F}}}. \tag{3.49}$$

So the C_{FB} can be determined for both ideal and experimental data. From the ideal case of the V_{FB} is ϕ_{MS} with no charge present is given by,

$$V_{FB,I} = \phi_{MS}. \tag{3.50}$$

Then by matching when the experimental curve capacitance matches C_{FB}, the experimental V_{FB} can be found. Note that in this work liner interpolation was used, as the measured capacitance does not exactly match C_{FB}. From this the the difference between the ideal and experimental Flat band voltages ($V_{FB,\,I}$, $V_{FB,\,E}$ respectively) is,

$$\Delta V_{FB} = V_{FB,I} - V_{FB,E}, \tag{3.51}$$

where the root of this difference at this point is given by the additional charges present,

$$\Delta V_{FB} = \frac{Q_F}{C_A} + \frac{Q_D}{C_A} + \frac{Q_M}{C_A} + \frac{Q_{it}}{C_A}. \tag{3.52}$$

As a CV curve is swept from accumulation to depletion, it is distorted by these charges present. From the depletion to accumulation CV sweep can be used to calculate charge (Q_T) the total oxide, mobile, fixed and D_{it} at the flat band voltage. This is,

$$\Delta V_{FB,I-E} = \frac{Q_O + Q_F + Q_M + Q_{it0}}{C_A} = \frac{Q_T}{C_A} \tag{3.53}$$

note D_{it0} means the interface states at the flat band voltage, this is included as the states at this point could not discern from the Q_F as they both will be contributing at this point. By comparing the CV sweeps from depletion to accumulation and back to depletion a hysteresis can be caused by a difference in charge. This difference is due to mobile and oxide charge.

$$\Delta V_{FB,DA-AD} = \frac{\Delta Q_O + \Delta Q_M}{C_A} \tag{3.54}$$

As stated before, Q_O can be introduced during device operation, as well as the moment of Q_M. These change depending on the operation, causing a hysteresis in the CV sweep, between seeps depletion to accumulation and back to depletion.

$$\Delta V_{FB,I-E} = \frac{Q_O + Q_F + Q_M + Q_{it0}}{C_A} = \frac{Q_T}{C_A} \tag{3.55}$$

where Q_{it0} is the interface states at the flat band condition, and Q_T is the total charge change.

Between the depletion to accumulation and back to depletion the hysteresis caused by a combination of Q_M and Q_O. This is because Q_F and Q_{it} should not change but the movement of the mobile charge and charge injected into the dielectric layer. This is the

$$V_H = \Delta V_{FB,DA-AD} = \frac{\Delta Q_O + \Delta Q_M}{C_A} \tag{3.56}$$

This can be used to approximate the amount of charge which has changed in the sweep direction.

3.4.5 Terman Method

As described in Section 2.10.2, due to defects states exist within the bandgap, which can be measured using CV techniques. In this work, the Terman method was used to do this, L.M. Terman first developed the Terman method in [477], using a high-frequency CV measurement. At a sufficiently high frequency, the contribution of the D_{it} to the total capacitance is zero, as the AC signal has such a quick switching frequency so that the D_{it} do not have time to be occupied. Hence without sufficient time to charge the trapped states, the AC measurement does not see any effects of these states. By applying a DC potential to the CV measurement, these states can be filled from the flat band position, when the surface potential is zero as this increases more states within the band gap that can be filled. A diagram in Figure 3.35 has been drawn to help explain.

The Terman method measures the difference between an ideal CV measurement to an experimental one. The states which are filled by the DC voltage, cause a shift and stretch in the experimental CV measurement. This has to be centred at the flat band position, when the surface potential is zero, then the gate voltage corresponds to a surface potential. This surface potential corresponds to the location in the bandgap for the states which are causing this shift in the CV measurements. This location in the bandgap from the surface potential is the position of the D_{it} which cause the shift in the CV measurement. The Terman method has known issues, however, it is used as a quick method to determine D_{it} and as a tool for comparison. This is given by,

$$D_{it}(\phi) = \frac{Q_{it}\phi}{qA} = \frac{C_A}{q^2 A}\frac{d}{d\phi}\left(V_g - V_g'\right) = \frac{C_A}{q^2 A}\frac{d\Delta V_g}{d\phi}, \tag{3.57}$$

where ϕ is the surface potential, A is the area of the gate contact, q is the charge of an electron, V_g is the experimental gate voltage, $V_{g'}$ is the ideal gate voltage. Where ΔV_g is the difference between the experimental to ideal gate voltage defined as,

$$\Delta V_g = V_g - V_g'. \tag{3.58}$$

As described in Equation 3.36, the ideal gate potential (V_g') is calculated from an ideal surface potential (ϕ), which is calculated from a normalised idea surface potential U. By definition, the flat band condition is then when,

$$U = \phi = V_g' = 0. \tag{3.59}$$

When the band gap is at the conduction band, it incorporates all D_{it} that exist above and at the conduction band. The factors then impact this described in Equation 5.10, so when the V_A is shifted by ΔV_{FB} into $V_A \rightarrow V'_A$ so that the flat band capacitance for both experimental and ideal model match. The shifted ideal and experimental curves diverge as the MIS capacitor is driven from the flat band into depletion, which is accounted for by D_{it}. This means that the D_{it} from Equation 5.12 is located ϕ below the conduction band $E_c - E_t$ as $-q\phi$. While the Terman method is a mid bandgap method to calculate the D_{it} as it overestimates near the band edges, however, one of the issues is that many of the D_{it} appear invisible as they have to populate and depopulate. Due to low electron-hole generation, this is not true unless other methods are used such as UV-assisted or thermal-assisted CV measurements, in wide bandgap materials such as β-Ga_2O_3 this limits the energy range to under 1 eV [478] [479].

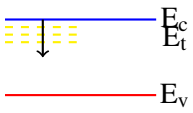


Figure 3.35: Diagram showing an example trapped state existing within band gap of the semiconductor, where E_c and E_v are the conduction and valence and E_c is the energy level of the trapped state. These trapped states are caused by a defect in the material are shown as yellow dashed lines. As the surface potential is draw from the flat band condition, down though the different trapped states that exist by the applied DC voltage. These states become occupied. This diagram is slightly misleading and should be considered with Figure 2.7, where the trapped states also bend.

3.5 Keithly Analysers

In this work a Keithly 4200A-SCS Parameter Analyser was used to measure the IV characteristics of different samples, this can be seen in Figure 3.36. While this setup was predominately used in this work, the Keithly 2636B System Source Meter was also used. The dark box was used were appropriate in order to limit the effects of UV light.

3.6 Wentworth Probe station and Keysight Analyser

In this work a Kegight Analyser and Wentworth probe station were used to measure the CV Characteristics of samples, this can be seen in Figure 3.37. This probe station has the potential to go up to high voltages, it is in an enclosed environment which acts like a dark box. This is a semi-automated system which can be used to perform the same test across many locations on the same wafer

(A) (B)

(C) (D)

Figure 3.36: The Keithly 4200A-SCS Parameter Analyser used in this work (A), and the Keithly 2636B System Source Meter (B) which were used for IV and CV measurements. These were connected to a probe stations such as in (C) and (D), where deemed necessary (D) was used in order to keep the samples inside dark box which affected the electrical measurements as it removed sources of ambient light inter reacting with the samples.

(A) (B)

Figure 3.37: The Wentworth probe station (A) and Keysight analyser (B) which were used to make the CV measurement. This system is able to be automated, however due to an issue someone had to be with the equipment to make sure it kept working. While the Keysight analyser is able to test both packaged devices and die though the use of the connected probe station.

3.7 Summary

The aim of this chapter was to help introduce the chemicals, materials, tools and processes which were used in this thesis. The purpose is to facilitate and support the following experiential chapters, while each chapter has its own methodology section and will discuss details when they are relevant, they will refer back to this this chapter for more detailed points regarding equipment and material.

These are to help prepare and fabricate test structures on β-Ga_2O_3 as well as on test wafers, Si and Al_2O_3, which were performed to confirm processes were operating correctly. The ellipsometer was used to confirm that the processes were operating correctly on spectator wafers, this was for photoresists and dielectric depositions, this was a part of all three chapters. Tools such as the PVD's and evaporate were used for metal deposition in chapters 5 and 6. PECVD and MVD were used chapter 5, to deposited SiO_2 and Al_2O_3 respectably. The test structures were used in chapter 6, the CTLM were for the purpose of characterising ohmic contacts. The ideal CV and Terman method were used in chapter 5, this was to characterising a MIS capacitor to investigate the dielectric/β-Ga_2O_3 interface. The electrical test equipment was used to perform CV and IV measurements in Chapters 5 and 6.

In the following three experimental chapters, in Chapter 4 a iterative process to developed an photoresist process enable etching into β-Ga_2O_3. Following in chapter 5 this a study into annealing β-Ga_2O_3 MIS capacitors was performed, and finally in chapter 6 a iterative set of development trails to achieve ohmic contacts which was successful.

CHAPTER 4

β-GALLIUM OXIDE TRENCH ETCH DEVELOPMENT

In this chapter, a process for patterning the photoresist in order to etch β-Ga_2O_3. This work was in collaboration with the KLA SPTS division, with the etching was performed by KLA SPTS. Silicon nitride (SiN_x) was used as a hard mask, and a photoresist process for β-Ga_2O_3/SiN_x was developed. The cross-section of the trench of the photoresist was inspected by hand-cleaving perpendicular to the trench and imaging in an SEM. In later Chapters this was superseded by using the LatticeAx to achieve a more consistent cleave, however, at this point in time this was not available. This began with establishing a protocol for Si substrates, which was then transferred to Si/SiN_x. This protocol was subsequently transferred to α-Al_2O_3 and, finally, to β-Ga_2O_3. Using this process the photoresist was successfully patterned and the SiN_x and β-Ga_2O_3 were etched. The initial recipe for the development was based off of a pre-existing process already used in CNH for patterning the photoresist. While in retrospect a more streamlined process could have been adopted, as the most impactful layer to the photoresist which would be the SiN_x, as it is in direct contact with the photoresist. This achieved etch depths between 700 nm and 1100 nm in β-Ga_2O_3 with sidewall profiles ranging from 72° to 78°. The selectivity of SiN_x as a hard mask relative to β-Ga_2O_3 was observed to range between 0.13 and 0.4.

In order to fabricate β-Ga_2O_3 power devices, it is essential to develop reliable and accurate etching techniques, which require the patterning beforehand. Precise etching enables the creation of various structures which are required for different devices. Etching is especially critical for fabricating structures, such as FinFETs and edge terminations, where controlling the geometry is necessary before depositing dielectric layers or to generate heterojunctions. Using a photoresist as a soft mask can be used for etching, however, soft masks etch quickly. Hard masks, like SiN_x, are used over soft

masks due to their durability and resistance to the etching processes. This work focuses on patterning photoresist for an etching process being developed by KLA, for β-Ga_2O_3 with SiN_x as a hard mask.

The development process presented here for achieving the target β-Ga_2O_3/SiN_x structure was iterative. This chapter is presented in the following manner. First, the introduction to the chapter, then followed by the initial stages of the development process, which began with Si substrates. This section outlines the process steps, confirming the photoresist thickness, the choice of development solution, and a comparison of mask contact methods, as well as the implementation of edge bead removal. Subsequently, the process was transferred to SiN_x/Si substrates. The protocol was then transferred onto Al_2O_3 substrates, where the UV exposure and development solution were optimized, along with a discussion of the development process on Al_2O_3. Finally, the process was transferred to β-Ga_2O_3, this involved two attempts. The chapter concludes with a discussion of the final results from this work and the resultant etch.

4.1 Introduction

This work optimised a photoresist protocol on β-Ga_2O_3 with SiN_x as a hard mask which was subsequently etched. Various materials can serve as hard masks, including Cr_2O_3, Al_2O_3, W, SiO_2, and SiN_x [480], [481], [482], [483]. Commonly used masks include Ni, Au, and SiN_x [244], [230], [484].

SiN_x was chosen as the hard mask in this work, despite a more favourable selectivity with Ni, 0.06/6 for Ga_2O_3/Ni). The issue with Ni as a hard mask is stripping, as stripping a Ni hard mask requires a mixture of HF and H_2O_2 [485], while SiN_x can be removed using hot phosphoric acid (H_3PO_4) [486]. Although SiN_x has a lower selectivity than Ni, it remains an effective choice as a hard mask. The photoresist selected was ECI 3024 from MicroChemicals, a positive photoresist capable of producing straight sidewall features, which are crucial for etch development [464]. ECI 3024 is a diazonaphthoquinone (DNQ) sulphonate-based photoresist, which reacts with H_2O under i-line or g-line UV light (365/435 nm) to form indene carboxylic acid, releasing N_2 and rendering the material soluble. In this work, only i-line exposure was used.

4.2 Development on Si

The initial process was performed on Si due to the availability of a pre-existing protocol optimised in CNH by previous colleagues that required validation. First, the thickness of the photoresist was measured after spin-coating, which was followed by verification of the development solution. A comparison between different mask pressures was then performed to determine which was most appropriate. Edge bead removal was implemented at this stage to reduce the effect of edge bead. Once these steps were validated on Si, the process was subsequently transferred to SiN_x/Si, then the initial phase is

concluded. The adhesive agent application was standardised and, therefore, kept the same throughout this process. The initial stages of this process were performed on Si following the manufacturer's specifications for ECI 3024 [464], with a process flow depicted in the Appendix A.4.

The mask design consisted of a series of trenches repeated across the quartz mask to enable full wafer patterning, with Cr patterned features. This mask, purchased from Photonics, is shown in Figure 4.1. The trenches spanned the wafer with widths ranging from 2 to 20 μm, this was a wide range designed for the etch trail.

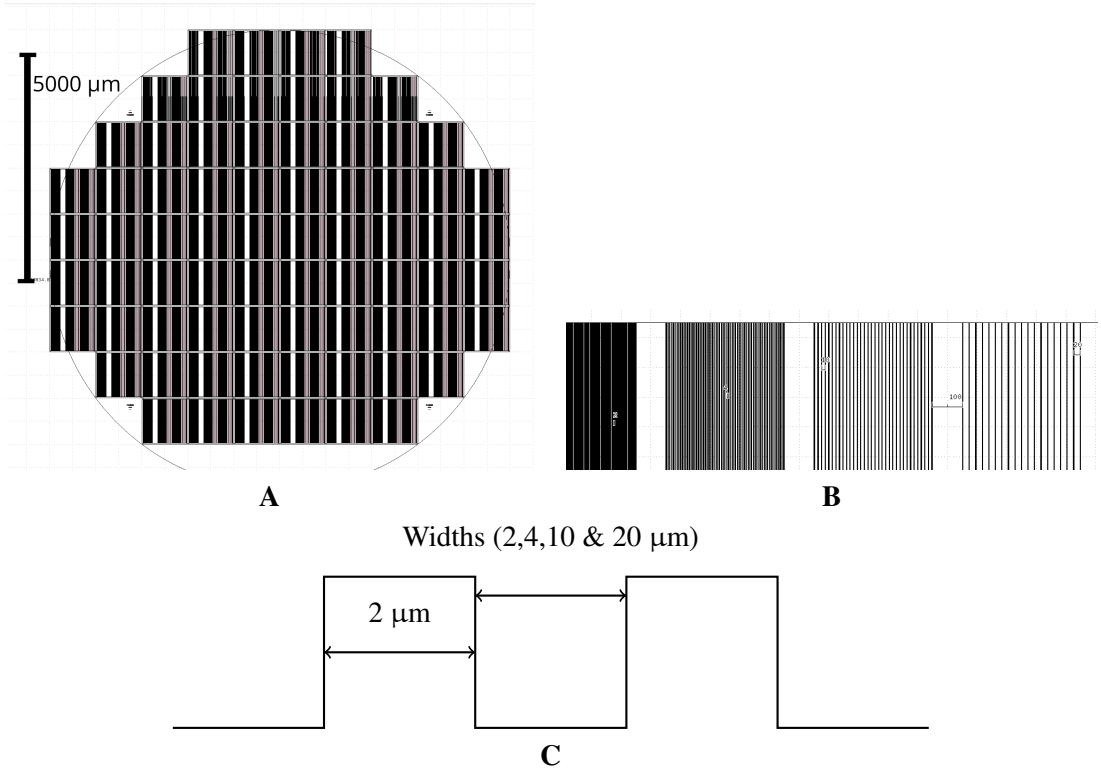


Figure 4.1: The mask design and schematic which was used in this work, **(A)** the whole mask and **(B)** a subsection. While the gaps in **(B)** are too small to distinguish so diagram **(C)** was used to clarify the design. It is a series of trenches across the mask. This pattern is a repeating set of patterns, it starts with a trench with a width of 125 μm which was designed to be measured with a profilometer. The other trench has a 9500 μm separation and an array of trenches with widths: 2, 4, 10 and 20 μm.

4.2.1 Determining Photoresist Thickness

The initial optimising focused on determining the optimal spin speed for depositing the photoresist. The spin speed affects both the thickness and uniformity of the photoresist layer, with faster speeds producing thinner but more uniform films. This determination was conducted on Si wafers, where ECI 3024 was spun at 3000, 4000, and 5000 rpm, which were expected to yield film thicknesses in the range of 3–2.5 μm. The thickness of the resulting films were measured using an ellipsometer, employing a Cauchy model to assess the photoresist layer thickness. The results, shown in Table 4.1, A.2, and A.3, indicate measured thicknesses of 2601.91, 2249.42, and 1996.60 nm for spin speeds

of 3000, 4000, and 5000 rpm, respectively. An example measurement is presented in Figure 4.2, with additional measurements available in Appendix A.1. This example illustrates the measurement process and the locations across the wafer where measurements were taken.

Spin Speed	Thickness (nm)			
(rpm)	Average	Min	Max	σ
5000	1996	1977	2020	13.4
4000	2249	1933	2310	130.7
3000	2601	2590	2611	7.1

Table 4.1: Measured thickness of the ECI spun at 3000, 4000 and 5000 rpm, this was measured on the ellipsometer. The fitting parameters and wafer maps can be seen in Appendix A.1. These are based of 13 point measurements across the surface of a 4" Si wafer.

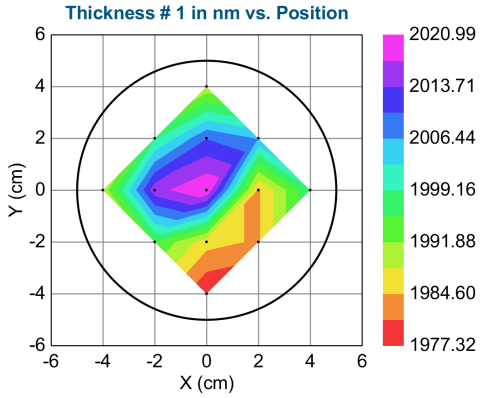


Figure 4.2: Example of the ellipsometry measurements fitting displaying the thickness of the ECI photoresist spun at 5000 rpm, this is to demonstrate the distribution of the measurements across the wafer. The full set of these measurements are available within the Appendix A.1. At each point on the wafer map marked with a point the ellipsometer took a measurement the reflection refraction of light, then generates a model of the optical constants and calculated thickness of the layer.

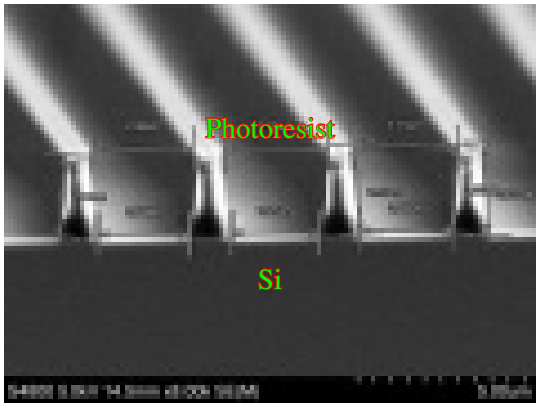
Based on these results, a spin speed of 3000 rpm was selected for further experiments. This speed produced a thicker film, which, according to the ellipsometer mapping, demonstrated high uniformity across the sample. High uniformity was more important than absolute thickness, as this will result in a more uniform etch. From this point forward, 3000 rpm was used consistently throughout the remaining work.

4.2.2 Deciding Development Solution

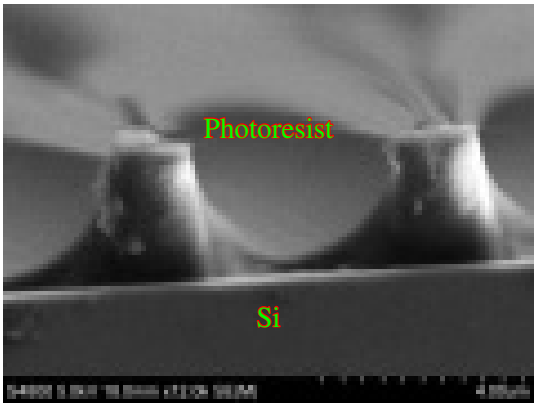
After establishing the optimal spin speed for the photoresist, the next stage was to select an appropriate development solution. Three developer solutions were tested: (A) a baseline sample exposed to 210 $mJ \cdot cm^{-2}$ and developed in a 1:1 ratio of AZ Developer to DI water, (B) a sample exposed to 210 $mJ \cdot cm^{-2}$ and developed in a 1:2 ratio of AZ Developer to DI water, and (C) a sample developed in a 1:1 solution of AZ 726 to DI water.

Throughout this trial, the UV dose was kept constant at 210 mJ $\cdot$ cm^{-2}. SEM images of the resulting development, shown in Figure 4.3, indicated that the solution of AZ 726 displayed the most promising results and was thus selected for further use.

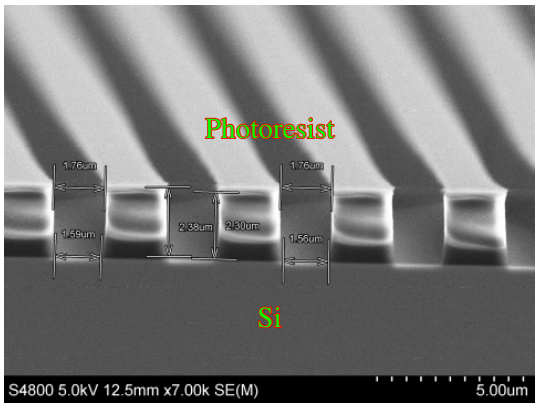
This outcome aligned with expectations, as AZ 726 is one of the developers recommended by Micro-Chemicals for ECI 3024, as noted in the technical data sheet. AZ Developer is a metal ion-containing (MIC) developer formulated with disodium metasilicate and trisodium phosphate, while AZ 726 is a metal ion-free (MIF) developer based on TMAH. Although TMAH can etch Al_2O_3 and β-Ga_2O_3 at a slow rate, its potential impact on the final result was unknown, prompting the initial consideration of AZ Developer. TMAH dose, however, etch a-Ga_2O_3 at a considerable rate [244]. As a result that AZ 726 was the developer solution which was continued to be used.



(A)
1:1 AZ Developer:DI water
Reasonable definition



(B)
1:2 AZ Developer:DI water
Poor definition



(C)
1:1 AZ 726:DI water
Good definition

Figure 4.3: Different developments on Si using ECI 3024. These were based on variants of the protocol outlined. Only soft contact was used for the photolithography step, with a dose of 210 mJ $\cdot$ cm^{-2}. **(A)** developed with a 1:1 ratio of AZ Developer. **(B)** changed the developer to a 1:2 ratio. **(C)**, was developed with 1:1 AZ 726:DI water solution. The sample developed (C) had the features most resolved. Further development would in no doubt optimise AZ Developer, however, going forward, AZ 726 was used.

4.2.3 Photolithography - Mask to Sample Contact

To further improve feature resolution, the type of contact used for mask alignment was investigated. When a mask is brought down onto a sample, it is held in physical contact with the photoresist layer. Higher contact pressure presses the Cr on the mask more firmly into the photoresist, reducing air gaps and enabling a more ideal transfer of UV light into the photoresist. These gaps can allow more of the UV dose to diffuse into the photoresist, which is undesirable as it reduces the definition of the features. As a result, reducing these air gaps improves feature resolution.

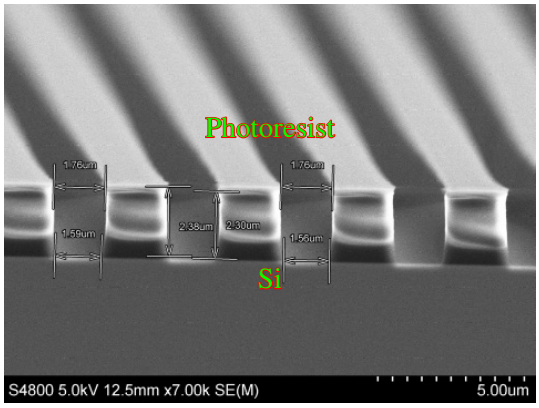
The tool used in this development process offers three contact types: soft, hard, and vacuum con-

tact, each applying increasing pressure to the sample. Soft contact is preferred when high resolution is not a priority, as it minimizes potential damage to both the mask and sample. Higher pressure options, such as hard and vacuum contact, can increase resolution but also pose a greater risk of mechanical damage to the sample and accelerated wear on the mask.

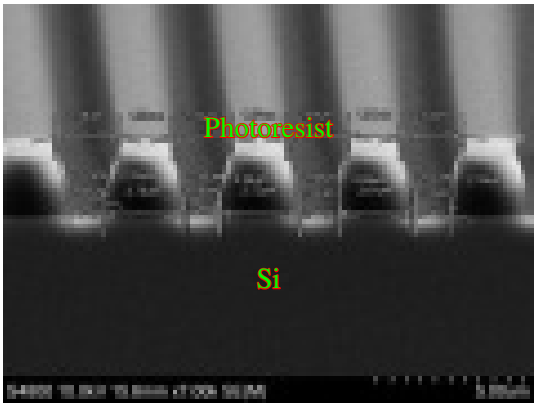
SEM images obtained on Si using the ECI protocol are shown in Figure 4.4, comparing soft, hard, and vacuum contacts. The trenches patterned in the photoresist appeared to be more defined under hard contact mode, however, the difference between hard and vacuum contact was not noticeable from the SEM imaging. For this reason, hard contact was selected for further use, as the additional stress and potential damage from vacuum contact did not justify its use in this context.

It is important to note that SEM imaging in this study may be subject to misleading artefacts due to various factors, including damage from cleaving across the cross-section, cleaving angle relative to trench orientation, handling-related damage, and the angle at which the exposed cross-section is held to the SEM beam. Additionally, the charging effect of the photoresist can complicate interpretation, making the justification for chosen process parameters difficult to fully quantify. The issues that arise from imaging like this means that it's not necessarily knowing the dimensions that are expected, for example if the spacing measured is 3 μm, if the same was supposed to be 2 or 4 μm. This could be due to over or under development, which in turn could be developer solution/times, UV dose or heat/lack of heat treatment. The angle that the sample is also effects the measurement, the choice of image used was from what section of the sample could be focused on, with a clear definable profile of the trench pattern. This means there is a lack of consistently in the image quality as well as the nature of the trenches being imaged and the magnification used.

While efforts were made to collect samples from the centre of the wafer, with little time post development to reduce changes of damage so leading to misleading SEM imaging. It is acknowledged that the images in Figure 4.4 may not fully represent the process quality and, in some cases, could appear contradictory to the described observations. This is due to the quality of the images which was obtained, this is because of the conditions and sample preparation prior to imaging. Rather than exclude these images, the author acknowledges this limitation and notes that greater care should be taken to reduce such inconsistencies.



(A)
Soft contact
Poor



(B)
Hard Contact
Noticeably better than soft contact.

(C)
Vacuum contact
Noticeably better than soft contact.

Figure 4.4: Samples of the trench patterned using different developments on Si with ECI 3024, the trench was designed to be 2 µm. Illustrating the effects of different contacts on the sample. **(A)** is under soft contact. **(B)** is under hard contact, and **(C)** is under vacuum contact. Improvement was observed from soft contact to hard. However, the transition from hard to vacuum did not show as much improvement, so hard contact was chosen for the future development of this process. It should be noted that the SEM imaging shows the hard and vacuum contact here, it is believed to be due to the perceptive of the imaging.

4.2.4 Edge Bead Removal

At this stage, it became apparent that the edge bead was significantly impacting the process, as seen when comparing trench profiles from the wafer's central regions to those at the outer edges. The edge bead is a thicker ring of photoresist that forms around the edges of a sample after spinning, primarily due to the dynamics of the spinning process, with irregular shapes and smaller samples there is more of an impact. Since the spin speed used was relatively low to achieve a thicker photoresist film, this also increased the size of the edge bead, resulting in thicker photoresist at the sample edges than at the centre.

Ultimately, the process was be transferred onto a 2" (001) β-Ga_2O_3 with SiN_x epilayer. Due to the small size and slow spin speed, this would lead to large edge beads that interfered with the mask's contact with the photoresist on the sample surface. When the mask is pressed against the sample, it contacts the thicker edge areas first, which reduces pressure and contact quality toward the sample's centre. For similar reasons as noted in 4.2.3, the UV dose diffuses through air gaps created by the edge bead, reducing pattern accuracy. Edge beads particularly affect non-circular samples due to Bernoulli effects [487]. As a result, it is advantageous to remove the edge bead, which allows the mask to achieve better contact with the sample's central region, similar to the improvements seen with increased contact pressure.

To mitigate the impact of edge beads, a manual edge bead removal method was applied to the samples. This involved using cotton swabs doused with acetone to lightly wipe along the wafer's outer edge, removing the excess photoresist build-up. While more systematic methods exist, such as dispensing solvent blends during spinning, this simpler method was adopted due to resource constraints. Manual edge bead removal has been used effectively in similar work [488], although alternative approaches, such as applying a solvent mixture such as AZ EBR from Microchemicals [489], could offer more consistent results. While this manual approach provided some improvement, it was not systematic, which is one reason why direct before-and-after comparisons are not included.

4.2.5 Transfer To Si/SiN_x

The ECI photoresist process developed on Si was subsequently applied to SiN_x/Si to determine if the addition of a thin SiN_x layer would affect the protocol, as shown in Figure 4.5. The SiN_x was deposited by KLA, this was using the SPTS Delta PECVD, the process is proprietary. While thin, the SiN_x layer could potentially influence UV light reflection, refraction, or thermal conductivity, which might alter photoresist performance. However, Figure 4.5 indicates that the SiN_x layer had no noticeable impact on the process.

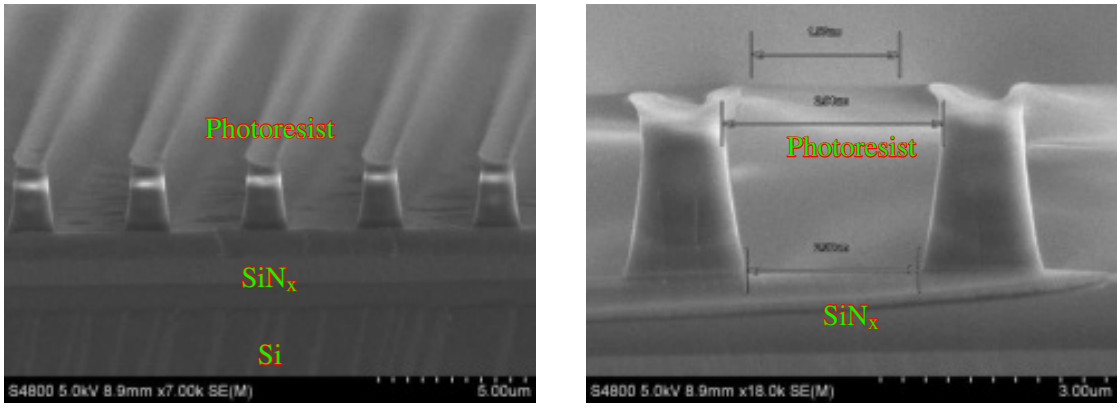


Figure 4.5: SEM images of the photoresist/SiN_x/Si ECI resist development, the spacing is 4 µm. This was translated process developed on Si transferred onto SiN_x/Si. The process seems directly translatable without requiring further development.

4.2.6 Conclusion to Si process

This initial stage established parameters for patterning trenches on SiN_x/β-Ga_2O_3. The process was first developed on Si, given the availability of material and a pre-existing protocol in Swansea. Starting with basic process confirmation, adjustments were made to enhance resolution and development quality, including optimising contact pressure and performing edge bead removal. After confirming these parameters, the protocol was successfully transferred to SiN_x/Si. The developed region, measuring 2.3 µm compared to the target of 2 µm, was also deemed acceptable.

4.3 SiN_x/Al_2O_3 Transfer

The ECI 3024 protocol developed so far was first optimised on Si and then transferred to SiN_x/Si. Before applying this process to β-Ga_2O_3, which differs significantly from Si, it was decided to first transfer the protocol to Al_2O_3, a more similar material. Due to limited availability of β-Ga_2O_3, direct testing on this material was not feasible.

This subsection is structured to include an introduction to the work on Al_2O_3, testing a range of UV doses, confirming the development solution's compatibility, and concluding the process development on SiN_x/Al_2O_3.

4.3.1 Introduction for photoresist transfer to SiN_x/Al_2O_3

Since β-Ga_2O_3 is a transparent material, the protocol was transferred onto SiN_x/α-Al_2O_3 to optimise the process. SiN_x/α-Al_2O_3 was chosen due to its accessibility, with Al_2O_3 sourced from Inseto and SiN_x deposited by KLA. The α-Al_2O_3 were purchased from Inseto and can be seen in Section 3.2.10.

ECI 3024 photoresist is sensitive to i-line UV light (365 nm). Si has a refractive index of approximately 6.5 [490], compared to β-Ga_2O_3 at around 2 [491]. The refractive index for α-Al_2O_3 closer at 1.7 [490], it was selected as an appropriate substitute. Although α-Al_2O_3 is not an exact match for β-Ga_2O_3, it was chosen as the refractive index more closely match than Si.

4.3.2 Determine UV dose for Al_2O_3/SiN_x

Building on the process developed for SiN_x/Si, a UV dose range from 150 to 350 mJ · cm^{-2} was tested on SiN_x/α-Al_2O_3. A dose of 210 mJ · cm^{-2} was selected as optimal, with examples shown in Figure 4.6 and the full dose range detailed in Appendix A.3.

It is important to note that the transparent nature of β-Ga_2O_3 may influence UV dose requirements in photolithography.

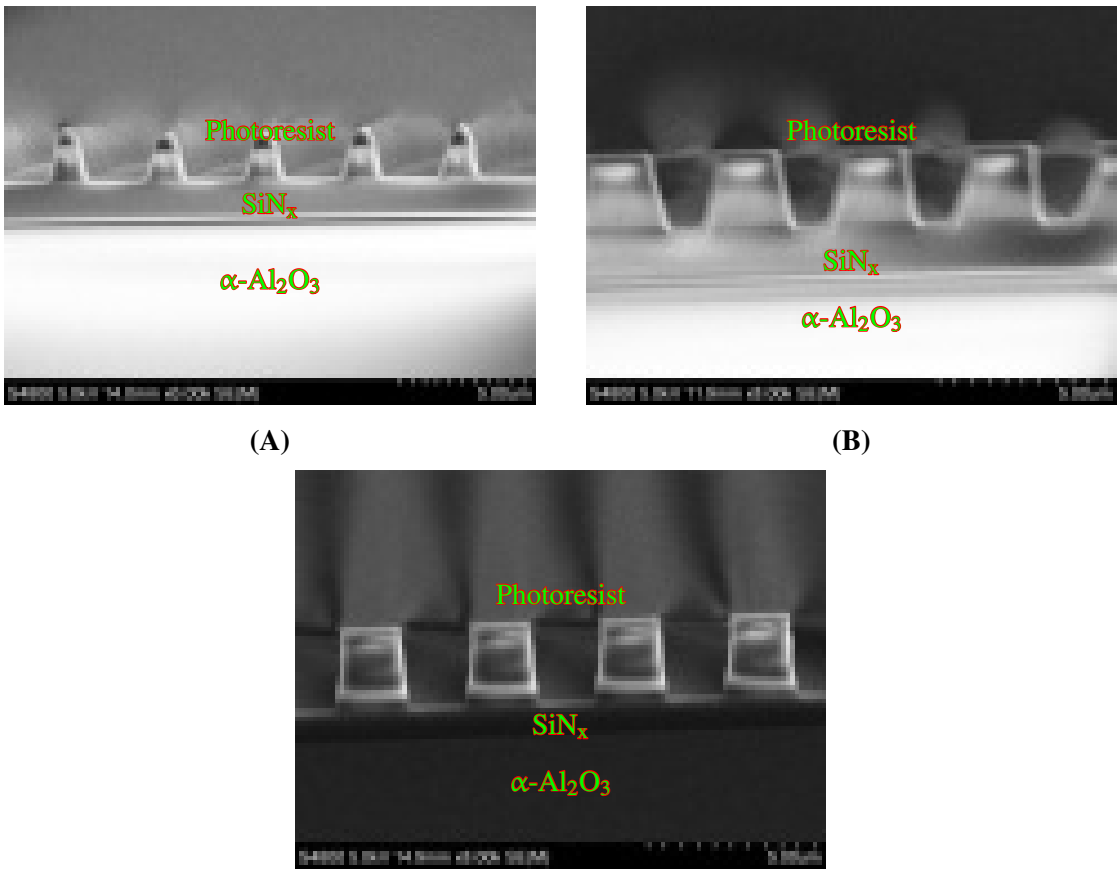
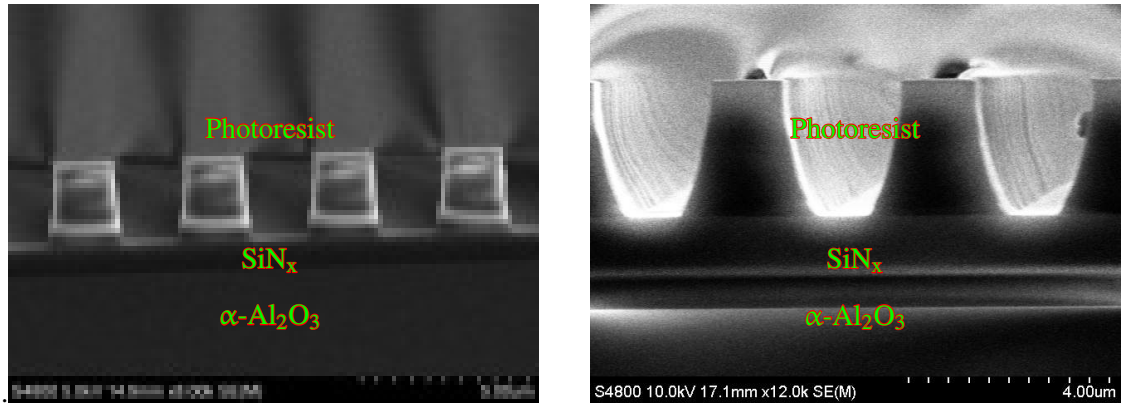


Figure 4.6: SEM imaging of SiN_x/α-Al_2O_3, **(A)** dosed at 350 mJ · cm^{-2}, **(B)** dosed at 150 mJ · cm^{-2} and **(C)** 210 mJ · cm^{-2}. The full dosing range can be seen in the Appendix A.3.

4.3.3 Development test on Al_2O_3

AZ 726 and AZ Developer were compared again on α-Al_2O_3, as shown in Figure 4.7. The results indicate that AZ 726 outperformed AZ Developer and is suitable for use with Al_2O_3. Since TMAH based developers can etch Al_2O_3, this test was necessary to confirm compatibility with Al_2O_3 substrates. There was no obvious etching into the Al_2O_3, indicating a negligible etch rate for this initial work.



(A) **(B)**

Figure 4.7: SEM images of the cross section of the SiN_x/α-Al_2O_3 after trenches were patterned using ECI 3024 protocol developed. **(A)** were developed with AZ 726 a TMAH-based Developer, where as **(B)** were developed with AZ-Developer a MIC Developer.

4.3.4 Conclusion to SiN_x/α-Al_2O_3 Development

One reason for using SiN_x/α-Al_2O_3 to optimise the protocol from Si was that the substrate affects the optimal UV dose [492].

This substrate change impacts the exposed area, influencing both the trench or mesa size and the sidewall angle. Sidewall angle is critical for device performance, so a wide dose range was tested to identify a dose that consistently produced low-angle sidewalls, with the ideal aim to be vertical with no deviation at the moment. Examples of the dose effects are shown in Figure 4.6, with the full dose range detailed in Appendix A.3. The difference between the lowest and highest doses tested (150–350 $mJ \cdot cm^{-2}$) was significant.

A dose of 210 $mJ \cdot cm^{-2}$ produced the straightest sidewalls, though consistency issues suggested that factors other than dose may be influencing the sidewall angle. For this reason, 210 $mJ \cdot cm^{-2}$ was retained as the working dose until these other issues could be further investigated.

4.4 Transfer to β-Ga_2O_3/SiN_x

Following the protocol developed on α-Al_2O_3, the process was ready to be transferred to β-Ga_2O_3. This transfer utilised the established protocol on Al_2O_3/SiN_x, with the AZ 726 developer solution and a UV dose of 210 mJ · cm^{-2}. Due to limited availability of β-Ga_2O_3 substrates, iterating this process presented additional challenges.

4.4.1 Initial Process on β-Ga_2O_3/SiN_x

In the initial processing attempt, a 2" (001) β-Ga_2O_3 wafer was used, sourced from Novel Crystal Technologies. Three additional 2" Si wafers with SiN_x layers deposited by the KLA division were processed alongside the β-Ga_2O_3 wafer using the ECI protocol developed in this work as spectator wafers.

The SiN_x/Si wafers were measured with an ellipsometer to confirm the thickness of the SiN_x layer, targeting 1 μm and achieving a measured result of 990 nm, as detailed in Appendix A.2. It became evident that the edge bead remained problematic and that, given the cleave planes of β-Ga_2O_3 (001), (100), and (201), precise dicing would be required. Cross-sectional SEM imaging wasn't collected due to these issues.

To proceed with etch development, KLA requires that the samples were diced into smaller die for cross-sectional trench inspection. Additionally, it was determined that rotating the mask by 90° would better align the trenches for inspection, facilitating the cleaving process. The process parameters were retained for the next iteration

4.4.2 Second iteration

in the second attempt three 4" (001) β-Ga_2O_3 wafers were purchased from Novel Crystal Technology, with SiN_x deposited on two wafers to compare hard and soft mask effects, as per KLA's requirements. The offcut was not considered in this work. While it should have been measured the offcut and surface roughness was not investigated prior to the SiN_x deposition. The initial surface would change the etch rate and end roughness, however, it was deemed that the priority is to get an initial etch process. Using larger wafers mitigates the effect of the edge bead, as there is a larger central region that remains relatively unaffected by the edge bead.

Following photolithography, the samples were diced by DISCO Corporation into 10 mm die and sent to KLA for etching, though etching details were proprietary. The etching process was based on B/Cl chemistry, using the SPTS Synapse etching tool, the etch process is propitery.

Pre-etch photolithography profiles, shown in Figure 4.8, reveal successful transfer of the photoresist pattern for etching, with trench widths from 1.5 to 2 μm compared to the 2 μm mask design. The samples imaged here were unsuitable for the etching trial due to handling-related damage, but they were still valuable for evaluating photolithography results. It is important to note that these observations represent the most damaged samples.

Post-etch profiles can be seen in Figure 4.9, these images were provided by KLA SPTS division. These figures demonstrate that the photoresist patterning onto the SiN_x hard mask was successful, effectively patterning the underlying β-Ga_2O_3. The SEM cross-sectional imaging, suitable for ImageJ analysis, provided data summarised in Table 4.2. As SEM cross-sectional imaging can be affected by charging effects, cleave angle, and trench profile angle, quantification remains challenging.

In this work, the etch profile angle ranged between 72° and 77° with β-Ga_2O_3 etch depths measured at 700 nm and 1130 nm for samples (A) and (B), respectively. The initial SiN_x thickness on these samples was approximately 1000 nm, measured on a spectator Si wafer, and was reduced to 700 nm and 847 nm, resulting in a selectivity range of 0.40 to 0.13 (SiN_x/β-Ga_2O_3). These values, obtained through pixel comparisons with SEM scale bars, showed some expected variability due to quantification challenges. Overall, the results suggest that SiN_x is a suitable hard mask with favourable selectivity for β-Ga_2O_3 etching.

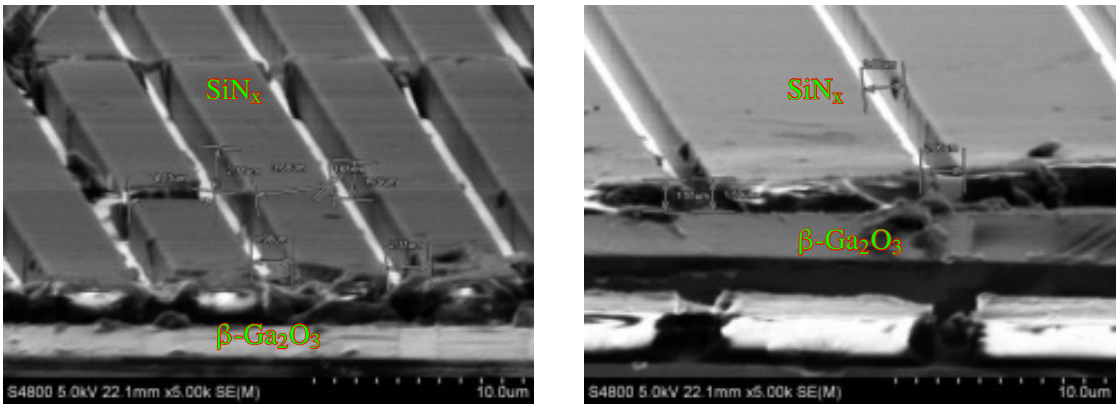
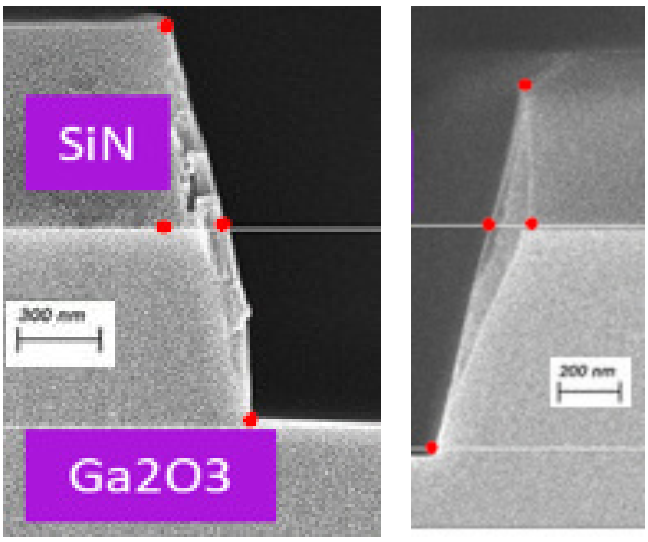


Figure 4.8: SEM images of the SiN_x/β-Ga_2O_3 post development, these samples were from the second round of etch trails on 4" β-Ga_2O_3 wafers. The dimensions of the trenches can be seen and compared to those on the mask shown in Figure 4.1. The smallest trench size on the mask was 2 μm and observed this seems to range from 1.7-2 μm.



(A) **(B)**

Figure 4.9: The etch profiles of the first **(A)** and second **(B)** etch developments on SiN_x/β-Ga_2O_3 are shown. KLA performed two different etch processes, however, they did not disclose these to me. This etch was performed by KLA division. It can be seen that the selectivity of SIN_x to β-Ga_2O_3 appears favourable, as a trench profile has been successfully etched. The angle of the etch is 80-75°. The red Dots indicates where pixel measurements were taken/

Scale (pixels)	25.725	Scale (pixels)	21.50
Pixel to nm	11.661	Pixel to nm	13.95
β-Ga_2O_3 (pixels)	63	β-Ga_2O_3 (pixels)	81
β-Ga_2O_3 (nm)	737	β-Ga_2O_3 (nm)	1130
SiN_x (pixels)	60	SiN_x (pixels)	61
SiN_x (nm)	700	SiN_x (nm)	848
Removed SiN_x (nm)	300	Removed SiN_x (nm)	152
Selectivity	0.4	Selectivity	0.14
Angle (°)	73	Angle (°)	76
(A)		(B)	

Table 4.2: The Raw and processed image-J data for SiN_x/β-Ga_2O_3 etched in Figure 4.9 (A) and (B) respectively. The scale was taken from the scale bar and the pixels for β-Ga_2O_3 and SiN_x were taken from the image and scaled to nm. From this pixel measurement from the images the angle was calculated, it should be noted as this is an angle from the pixel measurement there isn't a standard deviation as this is a snapshot and any given error would be misleading. It is unclear if there was any redeposition during the etch process.

4.5 Conclusion

In this work, a protocol to pattern photoresist onto β-Ga_2O_3 for use with a KLA dry etch process was developed, this demonstrated successful trench etching. This process was implemented using ECI 3024 photoresist patterned and developed over SiN_x which acted as a hard mask. Post etching achieving trench profiles with angles between 72° and 77°, It is unclear if there was any redeposition during the etch process. SiN_x proved to be a suitable hard mask, and ECI 3024 was effective for patterning this hard mask. Accurate cross-sectional SEM images prior to etching could have provided further insight into the influence of patterning on the etch profile, but degradation of the patterned photoresist limited these observations.

The protocol, outlined in Section A.4, enables the formation of various geometries on β-Ga_2O_3, a valuable feature for device design and fabrication. This process could be further refined, and it appears that optimisation on α-Al_2O_3 was unnecessary. This finding suggests that the limitations observed were influenced by factors other than UV dose, possibly related to the thin film of SiN_x affecting optical properties more significantly than the substrate.

It is likely that edge bead formation played a major role in these limitations, though the baking stages might also have had an effect. The baking stage of this process was not optimised in this work, and is a factor which could be considered going forward. Additionally, ECI 3024, being a DNQ-based photoresist, relies on H_2O for development, so the absence of a rehydration step could have affected results and could be investigated. Rehydration, which allows the photoresist to absorb moisture, might have optimised reaction conditions [464]. Differences in polishing (double-sided for β-Ga_2O_3 and single-sided for α-Al_2O_3) may also have affected UV light interaction with the substrates, contributing to the varied outcomes.

AFM could be used to investigate the surface roughness, to see if this has an issue on the etch, and profilometer can be used to look height of the trench profile. This should be performed both pre and post etching, to see the profile of the photoresist and the resultant etch. To conserve resources, this optimisation could begin on glass, which has a refractive index (1.45) closer to β-Ga_2O_3 (2) than Si (6) [490] [491]. Depositing Cr on glass using PVD would improve SEM imaging by mitigating charging effects, which have complicated imaging of insulating substrates like α-Al_2O_3 and β-Ga_2O_3. Alternative imaging the samples under a low vacuum conditions can help improve image insulate materials which would also be a potential solution.

Optimising this protocol on 4" wafers at faster spin speeds may reduce edge bead effects and produce more consistent trench profiles. This process could involve profiling trenches with a profilometer rather than cleaving for SEM, allowing for a more efficient cycle: 1) Apply photoresist with varying parameters, 2) Characterise trench profiles with a profilometer, 3) Strip the photoresist mask and clean the sample with piranha solution.

Such iterative cycles would reduce the need for cleaving and SEM analysis, conserving both time and resources. Further process refinements could also allow expansion of design features beyond trenches.

The next phase of this work would involve optimising feature sizes and sidewall profiles, which are crucial for device applications. As in this development process this was not addressed, so it is unknown how well the post development features match the design on on β-Ga_2O_3 or to the post etch samples. Additionally, the approach developed here could be adapted to assess MIS interface characteristics, as described in Chapter 5, where a dielectric layer is deposited and the MIS interface characteristics are explored. The following chapter will delve into these aspects in greater detail.

CHAPTER 5

GATE DIELECTRIC DEVELOPMENT

In this chapter MIS capacitors were fabricated with (001) β-Ga_2O_3, the dielectric layers used were ALD deposited Al_2O_3 and PECVD deposited SiO_2. The density of interface traps (D_{it}) and the effects of prolonged post metallisation annealing on the dielectric-semiconductor interface was investigated. This means that D_{it}, as well as other sources of charge affects the turn on/off voltage of a MISFET as well as the degree of enhancement or depletion of the channel at a given voltage. An increased trap concentration also increases gate leakage though trap assistance tunnelling, lowering the mobility near the interface affecting the on-state resistance of the device. MIS capacitors were used as simple test structures to facilitate this investigation into dielectric-semiconductor properties. The MIS structure acts as the channel in power devices like the MISFET, which is an important part of these devices. The D_{it} affects the devices channel would conduct, and how it interacts with applied potential, to turn it on or off. While post deposition and post metallisation anneals have been investigated the effect of prolonged annealing is rarely investigated.

This chapter is structured to give an introduction to the topic, the fabrication process for the MIS capacitors, followed by results and analysis,finally the conclusion on the work which was performed is given.

5.1 Introduction

Dielectric materials are used to fabricate semiconductor devices, serving as insulating layers to block the current flow or to have a voltage applied to polarise them [493]. They are widely employed to isolate sections of a device, protect surfaces from external disruptions (passivation and termination), or function as gate dielectrics to control the on/off states of devices by manipulating the electric field in the semiconductor material [494]. In particular, the dielectric layer(s) used in MIS structures play a crucial role in power electronic devices such as MISFETs, as discussed.

Due to the difficulty in realising p-type β-Ga_2O_3, the fabrication of FET structures so far relies on either MIS based structures, or hetero-junctions. Hetero-junctions, however, have their challenges, such as maintaining purity during growth, achieving high-quality interfaces, and addressing lattice mismatch issues. Unlike some other semiconductors, β-Ga_2O_3 lacks a native dielectric layer, such as Si/SiO_2 or GaN/Ga_2O_3. this necessitating the deposition of dielectrics. The quality and dielectric constant of these deposited layers are critical factors influencing device performance.

To study the dielectric-semiconductor interface, MIS capacitors are often fabricated as test structures. These devices simplify the analysis by minimising complexities associated with full-device operation, such as in MISFETs. Given the inherent limitations of β-Ga_2O_3, which require dielectric layers for device functionality, the dielectric-semiconductor interface becomes a key factor in determining the on/off behaviour of such devices.

In this work, MIS capacitors were fabricated to investigate the dielectric-semiconductor interface of β-Ga_2O_3. MIS capacitors were selected due to their simplicity and ease of fabrication. By employing an approximation described later, these structures do not require ohmic contacts for characterisation. Capacitance-voltage (CV) measurements were conducted, utilising the Terman method to evaluate the D_{it}. The advantage of not requiring ohmic contacts allows the interface to be investigated without additional processing steps such as etching or annealing, relying only on a single metal deposition process. This simplified fabrication approach was adopted to minimise complexity, establishing an initial baseline for dielectric deposition at Swansea University to optimise in future work. The disadvantage of this approach is that there is not an ohmic contact, which can be characterised, to build a full model. It is very reliant on the approximations holding true without the ability to separate the different contributing factors into the device circuit.

Al_2O_3/SiO_2 are widely used dielectrics, as high/low k dielectrics, respectively, which are common in the semiconductor industry. Previous studies have used MIS devices to investigate the effects of annealing on CVD-deposited SiO_2 layers, demonstrating improved CV characteristics. For example, Zarchi et al. [495] reported enhanced performance after annealing at 450 °C for 15 minutes, though their work was conducted on Si substrates rather than β-Ga_2O_3. Kita et al. [496] studied evaporated SiO_2 on (001) β-Ga_2O_3, applying prolonged post-deposition anneals (PDAs) at temperatures ranging from 600 to 1000 °C. Their findings indicated that higher temperature anneals reduced the D_{it} at the dielectric-semiconductor interface, prolonging the anneals up to an hour in O_2 was reducing the hysteresis and shifting V_{FB} towards ideal values. In contrast, annealing in N_2 led to a negative shift in V_{FB}, however, did reduce the D_{it}, this highlights the influence of annealing conditions.

Al_2O_3 is a widely used high-k dielectric for fabricating MIS devices with β-Ga_2O_3 due to the ultra-wide-bandgap. MIS capacitors have been employed to characterise the dielectric-semiconductor interface, the Terman method has been used to determine D_{it} [258], [407], [497]. PDAs have been shown to improve the quality of Al_2O_3 layers deposited via ALD. For example, ALD-deposited films annealed in N_2 or O_2 at 500°C for 2 minutes exhibited enhanced dielectric properties [258]. Similarly, Su et al. [407] employed the Terman method to evaluate Al_2O_3 deposited by ALD and observed improvements following a 2-minute O_2 anneal at 500°C. Zhang et al. [257] investigated Al_2O_3 deposited by ALD at 300°C onto (001) β-Ga_2O_3 surfaces pre-treated with piranha solution, achieving D_{it} values of 10^{11} $eV^{-1} \cdot cm^{-2}$. In contrast, Jayawardena et al. [406] studied (001) β-Ga_2O_3 Al_2O_3 interfaces and achieved significantly lower D_{it} values (10^{10} $eV^{-1} \cdot cm^{-2}$) using the conductance method.

Although significant research has been conducted on (001) β-Ga_2O_3 MIS capacitors with short PDA and post-metalisation anneals (PMA), the effects of prolonged annealing durations is not explored to the same degree. Although limited to a small range, the Terman method is a suitable approach for investigating the dielectric-semiconductor interface in these structures. In this work, the effects of extended PMA durations were examined, commonly, post PDA and combined PDA and PMA are investigated, rather than purely PMAs. By isolating the effects of PMAs, this study aims to provide insights into the long-term thermal stability and interface quality of dielectric-semiconductor systems, which are often confounded in studies combining PDA and PMA treatments.

5.1.1 Metal-Insulator-Semiconductor Layout

In this study, lateral MIS devices were fabricated, in the initial design stages, a mask was created using KLayout and procured from Photonics Ltd. The mask design, shown in Figure 5.1, was intended to be a single-layer mask, minimising the steps required for the fabrication process. The mask was designed to measure capacitance for small circular contacts with diameters ranging from 400 to 1000 μm. The contacts increased in steps of 200 μm, organised in rows of 20 contacts, with 5 rows for each contact diameter. These small circular contacts were spaced 200 μm apart from a larger grid contact that covered most of the wafer. The CV measurements were performed, the wafers were annealed. After which CV measurements were re-taken on fresh contacts on the wafer. New contacts were used to avoid repeated damage to contacts by repeated probing. It is essential that the grid contact was significantly larger in comparison to the smaller contacts. The reason behind this is discussed in Section 5.1.2. When this approximation hold true then the, MIS capacitor CV measurements would require an ohmic contact. This step would introduce further process steps, as well as the choice of the exact process order, which would also introduce new problems.

It is in the authors opinion that PDA are often investigated, however, PMA appears to be overlooked. The most cited ohmic contact to β-Ga_2O_3, Ti/Au, often degrades as a result of Ti oxidising at the metal-semiconductor interface. The contact resistance would likely change, assuming it continued to perform like an ohmic contact. The contact could also start to be rectifying again, adding more complexity to the situation.

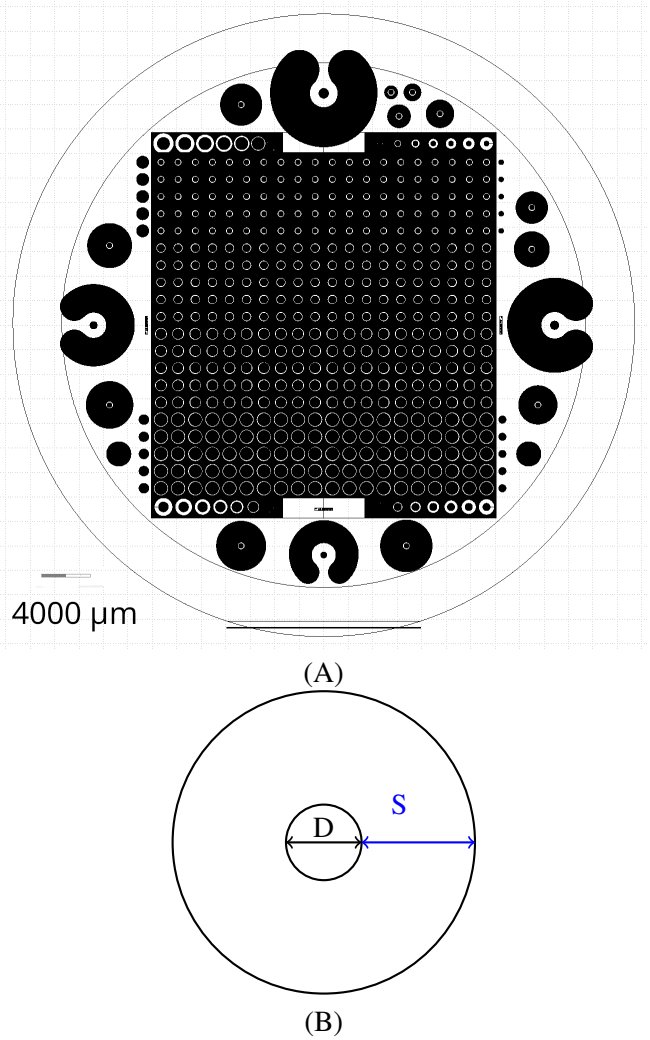


Figure 5.1: In sub-figure (A) the mask design of the mask which was used in this work, this was made in KLayout. The outer and inner rings were not present on the mask, rather marking the size of the wafer and an 2 mm exclusion zone for the outer/inner respectively. There is a series of small circular contacts with diameters of 400-1000 µm, sown as D on (B). These are separated by 200 µm from a large single contact, shown as S on (B).

5.1.2 Total Capacitance Approximation in Series

At this point, it is critical to set aside time to discuss a vital approximation introduced in this work at the design stage. As stated before, lateral MIS capacitance was used without ohmic contacts. While the ideal scenario would have the large grid contact as an ohmic contact, in this instance, it was designed with the same contact metallization, deviating from the norm. It is separated from the semiconductor by the dielectric. This design is a large grid with a hole in the middle and relatively small contacts.

The total capacitance (C_T) of the MIS structure fabricated in this work should be calculated by,

$$\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2} \tag{5.1}$$

where C_1 is the capacitance of the smaller contact and C_2 is the capacitance of the larger contact. To consider the large contact,

$$C_1 = \frac{\epsilon_0 \epsilon_I A_1}{T}, \tag{5.2}$$

and,

$$C_2 = \frac{\epsilon_0 \epsilon_I A_2}{T}. \tag{5.3}$$

Where ϵ_0 is the permittivity of free space, ϵ_I the relative dielectric constant of the insulator layer, the relative dielectric constant of semiconductor, A_2 is the area of the large grid contact, T is the thickness of the dielectric layer. The small contact has the same variables except for the contact area, so A_1. This is the ideal calculation, however, in this case, the large grid contact is much larger, so

$$A_2 \gg A_1, \tag{5.4}$$

is true, hence,

$$C_2 \gg C_1, \tag{5.5}$$

therefore we can make the following approximation,

$$\frac{1}{C_T} \approx \frac{1}{C_1} \tag{5.6}$$

This is why lateral CV measurements do not require a back ohmic contact with the samples, so long as this approximation holds true.

5.2 Fabrication Process

The fabrication process for the MIS capacitors is detailed in this section. The process began with the deposition of dielectric layers onto two separate (001) β-Ga_2O_3 wafers, this was followed by a metal lift-off process to deposit metal contacts. A step-by-step process flow is provided in Appendix B.1.

The β-Ga_2O_3 material used in this study was purchased from Novel Crystal Technologies Ltd. These were Sn-doped substrates which had a measured carrier concentration of 3×10^{18} cm^{-3}, this was determined as part of this work and the material described in Section 3.2.10. Additionally, Si spectator wafers were employed as conditioning substrates to confirm the correct operation of the dielectric deposition tool and process. This was to infer the deposition on the samples of interest.

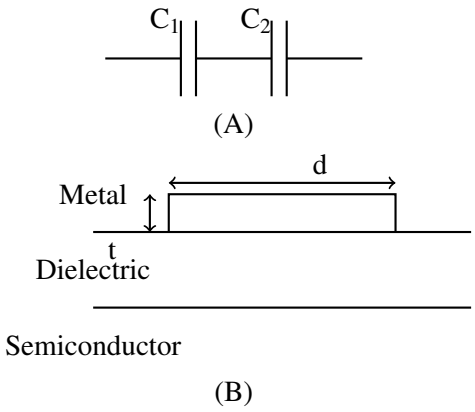


Figure 5.2: A diagram describing the setup for the assumptions in Equations 5.1) to 5.6. Where (A) is the effective circuit diagram required, and (B) the separate capacitors. In (B) t is the thickness of the dielectric layer and d is the diameter of the contact. In this case the contacts are circular so the area used in the equations is determined from the diameter.

5.2.1 Dielectric Deposition

The first step in the fabrication process for the MIS capacitors was the deposition of the dielectric layers. This stared by solvent cleaning, using acetone and IPA, in retrospect a piranha clean would have been beneficial. The dielectric layer separates the semiconductor from the metal contacts and must be deposited before fabricating the metal contacts.

The thickness and dielectric constant of the insulating layer are both critical parameters, as they directly determine the accumulation capacitance (C_A) of the capacitor. The thickness of the dielectric layers was estimated using spectator Si wafers, which were measured on an ellipsometer and the dielectric constant from the accumulation capacitance was estimated by measuring the capacitance and apparent thickness. This step was performed on Si wafers instead of β-Ga_2O_3 due to challenges in modelling the optical properties of β-Ga_2O_3 on the ellipsometer. The ellipsometer provided a fast, non-destructive method to verify the deposition tool's performance and to estimate the deposited dielectric thickness accurately.

Silicon Dioxide Deposition

SiO_2 was deposited onto β-Ga_2O_3 using the PECVD system described in Section 3.1.7. Due to practical constraints with the PECVD system, a carrier wafer has to be used. A specific carrier wafer had to be fabricated to process the 2" β-Ga_2O_3 wafer safely and effectively. The PECVD system utilises a load lock system, making it unsuitable to directly place the β-Ga_2O_3 wafer without risking damage during vacuum transfer.

This carrier wafer was fabricated, using a 6" Si wafer, SiO_2 was deposited and a 2" hole was etched into the wafer. This was to create an inlay for the 2" β-Ga_2O_3 wafer.

Using this carrier wafer was critical for several reasons. During vacuum transfer, the β-Ga_2O_3 wafer, if simply balanced on a flat surface, could become dislodged or damaged. While the sample could be secured with glass slides, this method introduces significant edge effects, causing a non-conformal deposition. Edge effects arise from the interaction of the plasma, precursor, carrier gas, electromagnetic field and geometry of the deposition zone. This leads to a non-uniform deposition across the wafer. The fabricated carrier wafer mitigated these issues by securely holding the β-Ga_2O_3 in place while minimising edge effects during deposition.

5.2.2 Aluminum Oxide Deposition

The deposition of Al_2O_3 was carried out using the MVD tool, as described in Section 3.1.7. Since the MVD system is not designed to accommodate 2" wafers directly, a 2" wafer holder originally repurposed from the PVD system was utilised. This holder featured a slight lip to securely hold the 2" wafers during the deposition process. The alternative method of placing the wafer directly on the chamber floor was avoided to ensure the sample was in similar conditions to a normal deposition, minimising potential deviation from the expected deposition.

Repurposing the holder allowed both sides of the β-Ga_2O_3 wafer to be exposed to the ALD process in the middle of the chamber. This was intended to promote uniform deposition in terms of thickness and composition. The holder designed for the MVD is defined for 4" and 6" wafers, making its adaptation necessary for processing the smaller 2" wafer.

The MVD system supports the simultaneous processing of multiple wafers, which is distinct from the PECVD process where Si spectator wafers were used separately before and after each deposition. In this process, Si spectator wafers were included during the ALD deposition as controls to confirm tool performance and validate the uniformity of the deposited Al_2O_3. The deposition was performed a colleague in CNH.

5.2.3 Confirming Dielectric Deposition

Determining whether the deposited process operated correctly is crucial, as this information will be needed in a later analysis. This was achieved by measuring the dielectric layer on spectator Si wafers using ellipsometry, as described in Section 3.1.10 All Si spectator wafers had the native oxide measured before processing and then remeasured post-deposition. This was to build a model of the two layers on the spectator wafers (native oxide and deposited layer) to confirm the deposition, β-Ga_2O_3 does not have additional native oxide (or dielectric layer) so only the deposited layer was needed to be determined.

	Layer Thickness (nm)		
Wafer	Pre-Deposited	Post-Deposited	Native/Deposited
Si_{12}	1.38	50.41	1.38/49.03
Si_{13}	1.38	51.51	1.38/50.13
Si_{14}	1.38	51.05	1.38/49.67
Si_{15}	1.38	50.06	1.38/48.68
Si_{16}	1.39	50.50	1.39/49.11
Si_{17}	1.38	51.19	1.38/49.81

Table 5.1: The Si wafers measured on the ellipsometer, the subscript refers to the wafer number. 13, 14, 16 and 17 were PECVD SiO_2 performed before and after depositions on β-Ga_2O_3, wafers 12 and 15 are Al_2O_3 deposited at the same time in the MVD. 50 nm was chosen as the process was well know to work in Swansea, in retrospect a choice of 20 nm would have been more suitable for a gate in power electronics. These were fitted using as Cauchy Films, the parameters are in the appendix in Section B.3.

Measurements were not taken directly on β-Ga_2O_3. This is because ellipsometry measurements on β-Ga_2O_3 are challenging because of its transparent nature, which means it would require transmission mode measurements and the development of a new optical model. Creating these models would require calibration using known materials and independent verification of the dielectric properties and thickness of the β-Ga_2O_3 and dielectric materials. Without performing this, the transpose measurement would not be useful. In contrast, Si is an opaque substrate with well-established optical properties, making the models reliable for serving as an alternative for measuring film thickness deposited.

Ellipsometry was chosen because it is an accurate, quick, and non-destructive method. For PECVD-deposited SiO_2, Si spectator wafers were measured on the ellipsometer before and after each deposition onto β-Ga_2O_3 to confirm the process was functioning as expected. Similarly, for Al_2O_3 deposited with MVD, Si wafers were measured before and after deposition to establish a reliable model for estimating the thickness of Al_2O_3 films. The measured thicknesses are presented in Table 5.1, with fitting parameters detailed in Appendix B.3.

5.2.4 Contact Fabrication

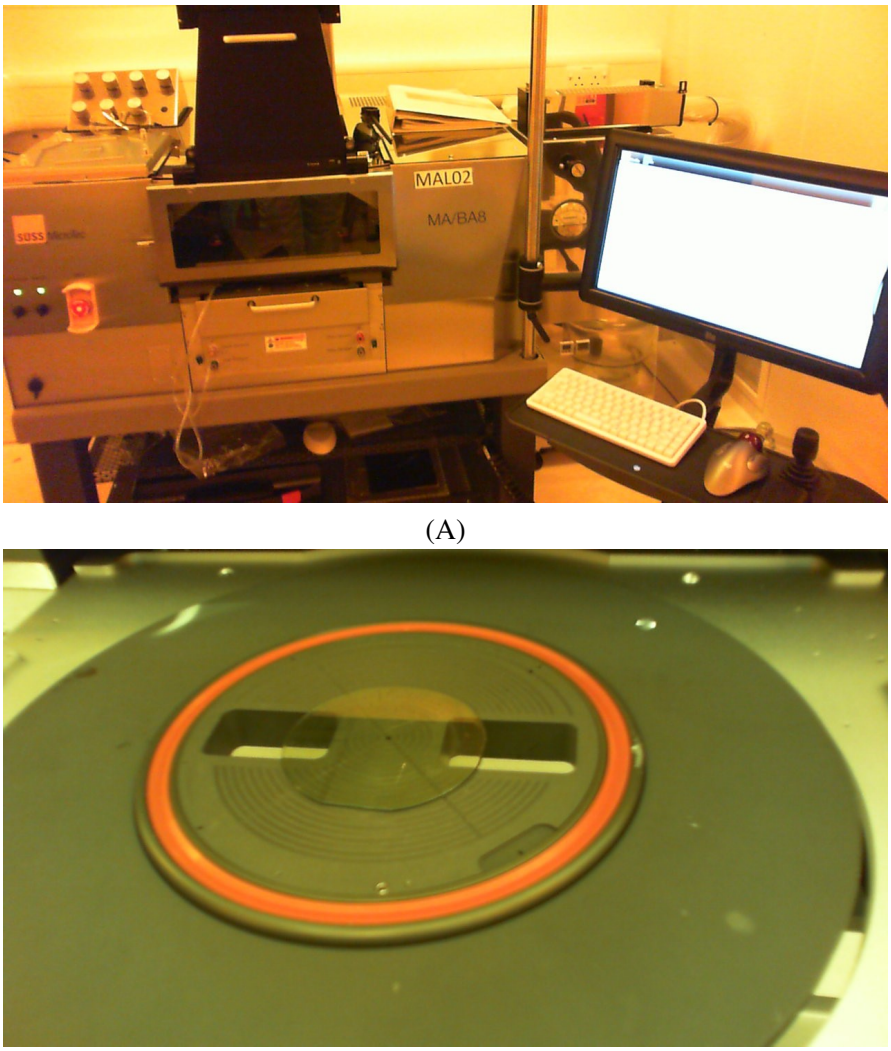
Samples were solvent-cleaned following the procedure described in Section 3.1.2. Due to the fragility of β-Ga_2O_3, cleaning was performed in a beaker with acetone and IPA instead of using a sonicator. These were bulk β-Ga_2O_3 prior to any dielectric layer deposited. To pattern the metal contacts a metal lift off process using a single layer of negative photoresist was used to pattern the sample. As adopted from Chapter 4, attempts were made to remove the edge bead. While tools and chemicals for removing the edge bead are available, the edge bead was manually removed in this work for the same reason. This was by using a swab and acetone touching the edge of the sample to try to remove some, a photo of this can be seen in Figure 5.3. This process was discussed in Chapter 4.

The cleaning and patterning process were:

(1) The samples were submerged in acetone for 10 minutes, followed by IPA for 5 minutes, and then dried with a N_2 gun. (2) The samples were dehydrated by baking at 120°C for 10 minutes. (3) Ti prime was applied to improve photoresist adhesion and spun at 4000 rpm with 1000 rpm acceleration for 30 seconds. (4) The Ti prime layer was baked at 120°C for 120 seconds. (5) AZ LNR-003 photoresist was applied to the samples. The photoresist was stored overnight in a syringe, this was to reduce impurities and trapped air in the syringe, as discussed in Section 3.4. (6) At this point manual removal was performed using a swab dipped in acetone to remove/reduce the edge bead formation, as illustrated in Figure 5.3 and discussed in Chapter 4. (7) After the edge bead was manually reduced, the samples were baked at 110°C for 60 seconds to reduce the solvent in the photoresist. (8) Finally, the samples were transferred to the mask aligner for pattern curing.

Figure 5.3: Manual removal of the edge bead. This was done with a swab dabbed in acetone and then lightly brushed around the edge of the sample.

The mask was loaded into the mask aligner, and the samples were aligned and exposed to UV light at 130 mJ $\cdot$ cm^{-2}. Following exposure, the samples were rested for two minutes to allow for out gassing and rehydration. The samples before exposure are shown in Figure 5.4, and the mask design is illustrated in Figure 5.1. After resting, the samples were baked at 110°C for 80 seconds to stabilise the photoresist and complete the patterning process.



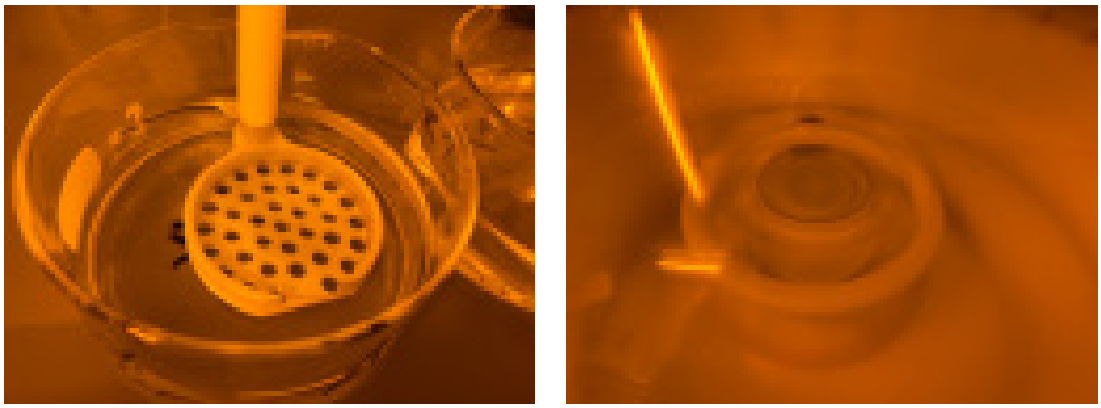
(A)

(B)

Figure 5.4: (A) the mask aligner used to expose the photoresist to the UV light and (B) the β-Ga_2O_3 sample loaded onto the mask aligner about to be patterned.

The samples were then developed using a solution of AZ-developer and DI-water 2:1 for 230 s, then rinsed in a weaker solution 1:2 for 15 s. This was intentional over development, leading to a larger undercut the single photoresist layer which significantly enhances the effectiveness of metal lift-off procedures. This is because a metal lift-off process uses an undercut to let the solvent seep in and dissolve the remaining photoresist later. This breaks the metal apart, leaving behind the contacts. The

samples were then washed in DI water for 10 s each, and then they were dried using a spin dryer. This can be seen in Figure 5.5.



(A) (B)

Figure 5.5: Fabrication of the samples, (A) β-Ga_2O_3 during development, (B) being dried in the spin dryer.

The metal deposition for the MIS capacitors was performed with the Lesker 75 PVD system, as described in Section 3.1.6. The samples were loaded into a 2" wafer chuck. The PVD was pumped down to a base pressure of approximately 10^{-7} mTorr, with the pump operating at 50% capacity.

The next day, once the system reached the desired pressure, the sample was set to rotate, and the turbo pump speed was increased to 100% for the duration of the deposition. Ar gas was introduced at a flow rate of 100 sccm, stabilising the pressure between 4.61 and 4.7 mTorr. A DC potential was applied to the Ti gun to ignite the plasma, starting at 30 W and increasing in 5 W increments up to 60 W. At this setting, the deposition rate was measured at 0.07 $nm \cdot s^{-1}$, with a voltage-to-current ratio of 305 V/0.95 A. An initial 100 nm of Ti was deposited into the chamber with the shutter shut, so that the sample is not coated. This was to clean contaminants from the target surface and create a getter layer, reducing residual oxygen and improving vacuum conditions. Following this, an additional 44.6 nm of Ti was deposited onto the samples.

The DC power supply was then switched to the Al target, maintaining similar conditions for pressure and argon flow. The power was gradually increased from 30 W to 150 W in 5 W increments, achieving a deposition rate of 0.08 $nm \cdot s^{-1}$, with a voltage-to-current ratio of 335 V/0.45 A. After predepositing 50 nm, a total of 145.5 nm of Al was deposited. The system was subsequently switched back to Ti for a final deposition step, under the same conditions as the initial deposition of Ti, depositing an additional 66.6 nm of Ti.

Finally, Au was deposited as the capping layer. The argon flow rate was increased to 139 sccm, with a stabilised pressure of 6.6 mTorr and a deposition rate of 0.05 $nm \cdot s^{-1}$. A pre-deposition of 500 nm. The resulting metal stack consisted of Ti/Al/Ti/Au layers with thicknesses of 20/100/20/25 nm, respectively. Ti was chosen as the contact metal as it is an adhering metal, then Al was used as metal which could be deposited fast to create a thick layer, the second Ti layer was to adhere to the Al with a capping layer of Au to stop it oxidising. In retrospect Ni should have been used at it is also an adhering metal, is often used as a barrier layer to limit diffusion and has a higher work function to β-Ga_2O_3 which is beneficial for a gate contact. The only real drawback to using Ni is the slower deposition rate due to it being a ferrous metal, requiring an RF source.

Post-deposition, the samples were submerged in D350 solution overnight to strip the remaining photoresist and facilitate the metal lift-off process. This left the metal pattern behind. It should be restated that no ohmic contacts were present on these devices, as explained in Appendix 5.1.2. This means that no ohmic contacts were needed before and after the fabrication of the gate, which means there is no chance for these metal contacts to be degraded or affected by that fabrication process. This metal deposition and lift-off were repeated on both sides of the β-Ga_2O_3 wafer and on a single Si wafer for SiO_2 and Al_2O_3 deposition. The Si wafers were fabricated to act as a checked that the process was operating correctly, which could be investigated on the ellipsometer.

5.3 Experimental Process and Analysis

After fabricating the MIS capacitors, CV measurements were conducted. Following each set of measurements, the samples were subsequently annealed in a furnace under a N_2 atmosphere at 100°C, then 200°C, and finally at 300°C for one hour. Fresh contacts were used for each set of CV measurements to ensure accuracy. The old contacts remained on the wafer. This iterative process allowed the effects of annealing on the dielectric-semiconductor interface to be investigated.

The samples were inspected under a microscope to determine the contact area of the MIS capacitors, which is essential for later analysis, including the modelling of CV measurements and the Terman method used to investigate D_{it}. FIB-TEM analysis was performed on the Al_2O_3/β-Ga_2O_3 MIS capacitor after the final annealing stage. This analysis provided critical information about the dielectric layer's thickness and interface characteristics, necessary for subsequent D_{it} calculations. However, FIB-TEM and Terman analyses were not performed on the SiO_2-based MIS capacitor, as will be explained when discussing the CV measurements for SiO_2.

This section is organised as follows. First, the optical inspection is presented before any CV measurements or annealing. A discussion of the FIB-TEM results follows this, as the thickness data is crucial for interpreting D_{it} in later sections. Finally, the CV measurements are presented and analysed, leading into the next section, which develops a model to determine D_{it} with the Terman method.

5.3.1 Optical Inspection

After the metal lift-off process, the samples were inspected under the Keyence microscope (as described in Section B.2). This was to verify the contact area, confirm the metal liftoff process was successful, and ensure the contacts were separated to avoid shorting, making the measurements meaningless. Determining the contact area and being confident about the size was critical, as this plays a significant role in the C_A and, therefore, the analysis.

To ensure confidence in measurement size, the samples were compared to a known reference sample from MSC co with known dimensions to calibrate the microscope measurements. After calibration, compared to the mask design the largest discrepancy was 20 μm. Most deviations, however, were within the range of 5 to 10 μm smaller than the mask design. These differences should be accounted for by adding 5 to 10 μm to the microscope measurements. Images of the inspected samples and calibration comparisons are presented in the Appendix B.2.

The observed feature sizes were consistently smaller than their counterparts on the mask design, this was determined after calibrating the microscope with the known reference sample. These deviations ranged from 10 to 25 μm in diameter, translating to a typical reduction of 5 to 15 μm compared to the mask size. These deviations are negligible for larger devices, but for smaller devices, they could introduce up to 7% uncertainty, decreasing to approximately 3% for larger devices. Measurements were averaged across multiple tests rather than determining individual contact sizes to minimise measurement errors. This is likely due to some over development in the patterning process, leading to the removal of more photoresist then intended due to dark erosion.

5.3.2 Metal-Al_2O_3-β-Ga_2O_3 MIS FIB-TEM-EDX Analysis

The Metal-Al_2O_3-β-Ga_2O_3 structure underwent more extensive analysis than the Metal-SiO_2-β-Ga_2O_3, primarily because ALD-deposited Al_2O_3 is widely used as a gate dielectric, whereas PECVD-deposited SiO_2 is typically employed for passivation and isolation. This distinction made the Al_2O_3-based structure of greater interest in this study. It should be noted that while the deposition here was performed with a MVD, the process was an ALD one to deposit Al_2O_3. To investigate the D_{it} accurate information about the layer thickness to generate an ideal model to compare to the CV measurement.

The Al_2O_3/β-Ga_2O_3 structure was analysed using FIB-TEM and EDX, as detailed in Appendix B.4. This was performed by Institut Catalá de Nanociéncia Nanotecnologia (ICN2) in Spain. The measured dielectric thickness from FIB-TEM was 46.8 ± 1.7 nm, slightly lower than the thickness measured via ellipsometry. It is important to note that these measurements were performed on different samples, which could explain the discrepancy. This difference is likely due to unreacted reagents being removed during the annealing process, that is excess precursor chemicals which were in the layer were removed by the annealing process which caused the decrease in layer thickness. However, this could be the result of densification, which is where the dielectric densifies. A scanning EDX analysis across the structure is shown in Figure 5.6, highlighting the distribution of elements such as O, Ga, Al, and Ti. These signals, presented in arbitrary units, indicate the relative presence of elements along the cross-section. The signal in EDX is not comparable to other signals, i.e. the response of O and Ga, so

the units are in arbitrary signal strength for that element compared to its other points in the measurement.

The EDX scan revealed a Ti peak at approximately 30 nm, corresponding to the Ti contact layer. There is overlap between the Ti and Al layers was observed, with substantial overlap at around 20 nm. Beyond 30 nm, the Ti signal diminished sharply, indicating minimal diffusion into the dielectric layer. The Al content was highest between 30 and 50 nm, representing the Al_2O_3 layer. This signal gradually decreased until approximately 70 nm, where the Ga signal from the β-Ga_2O_3 layer became dominant. Minor variations in the Ga signal within the metal contact region could be attributed to impurities or noise in the measurement. Alloying the Ti/Al could affect the contact's work function.

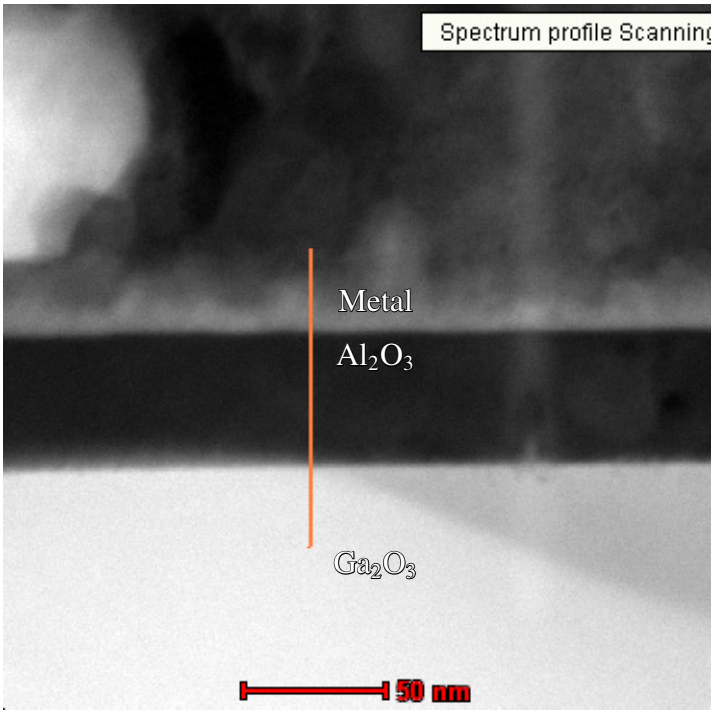
The oxygen signal displayed notable diffusion trends, with a peak in the β-Ga_2O_3 layer and a gradual decline through the Al_2O3 layer, falling off steeply at the metal interface. This distribution suggests that the metal contact layer may include TiO_x due to oxygen diffusion into the Ti layer. If the Ti is fully oxidised, this layer may contribute to the dielectric layers.

Interestingly, the Al_2O_3 layer exhibited two distinct regions of Al content, a higher concentration near the Ti interface and a lower concentration further into the dielectric. The underlying cause of this bilayer structure is unclear. Possible explanations include deposition-related effects, densification during annealing, impurity removal, or diffusion through the Ti layer. Unfortunately as their is only EDX data post annealing the change in composition due to the annealing cannot be identified. It should be noted that this is scan is close to the dielectric layer and not across the entire metal layer, so it is unknown how the metal layers have interrelated post annealing. While the colour change past annealing indicates that the Au has diffused into the metal contact, this is something which should be confirmed,

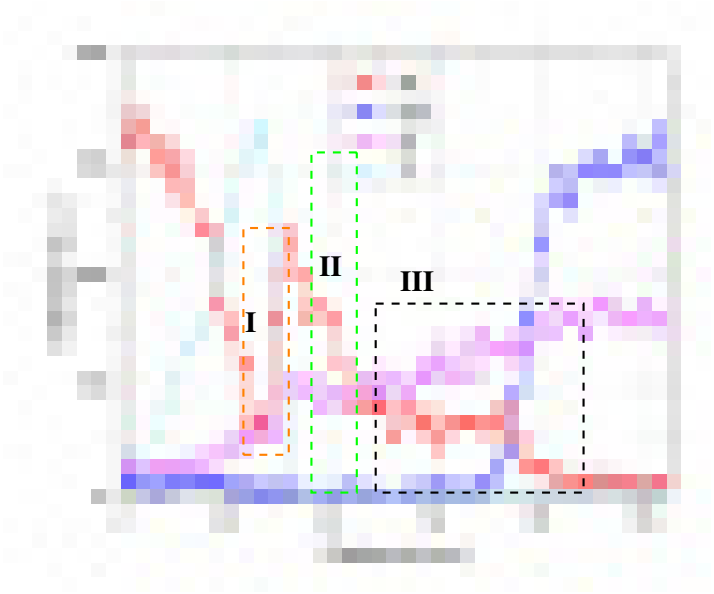
The placement of the layers and their relative thicknesses were verified using pixel measurements in ImageJ software [498], which confirmed alignment with the observed EDX data. Overall, the FIB-TEM and EDX analyses provide critical insights into the structure, composition, and potential diffusion processes occurring within the MIS stack.

EDX was performed on the metal portion of the contact, and these can be seen in Figures 5.7 and 5.8. In these, the metal contacts are predominantly Ti, Al, and Au, which is to be expected. The carbon signal is likely residual carbon, however, some of this could be from the organic material used in the Al_2O_3 deposition. The signal due to O is not unexpected as some diffusion of O from the β-Ga_2O_3/Al_2O_3 is shown in the scanning EDX in Figure 5.6. The small Ga signal also agrees with the scanning EDX in Figure 5.6, indicating either diffusion or impurity in the metal deposited.

As a final note, it's worth reiterating that given the prevalence of Cu in TEM holders, this remains the most plausible source of the Cu observed in the sample. The Cu signal observed in Figures 5.7 and 5.8 can reasonably be attributed to the TEM holder or lamination process rather than impurities or contamination in the sample itself.

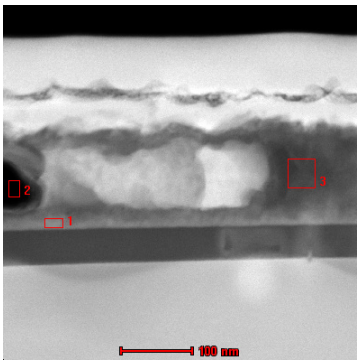


(**A**)

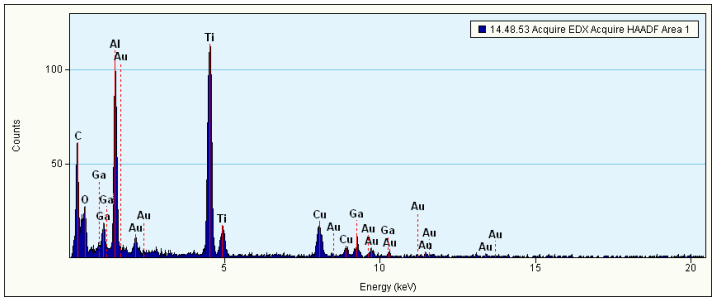


(C)

Figure 5.6: The FIB-SEM and EDX across the whole MIS interface, with the red cut line marked **i**, used for the EDX in **B**. The metal contact is Ti/Al/Ti/Au, however, only metal near the surface was included in this measurement. In **B** the intensity (arbitrary units) for O, Ti, Al and Ga as red ■, purple ▲, dark blue ● and light blue ★ respectively. There are also three regions of interest, **I** overlap of the Ti and O signals, **II** a large build up of Al signal in contrast to **III**.



(A)



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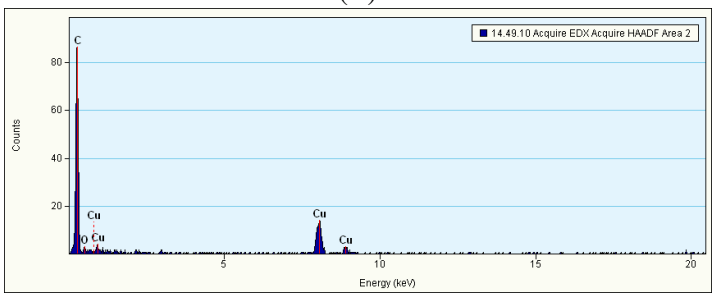
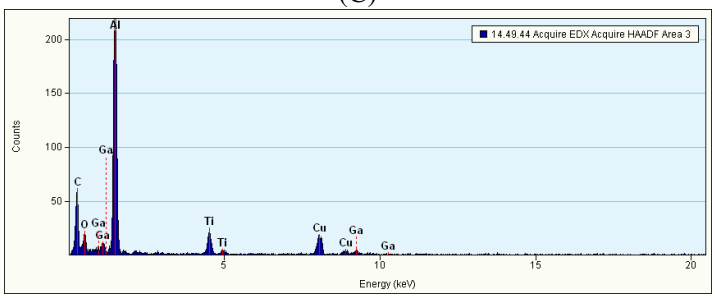
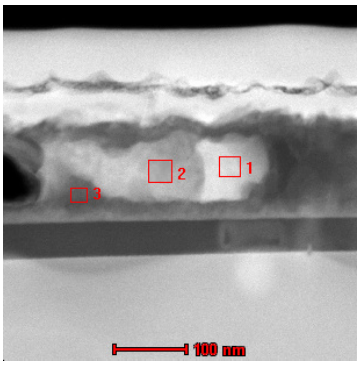


(C)

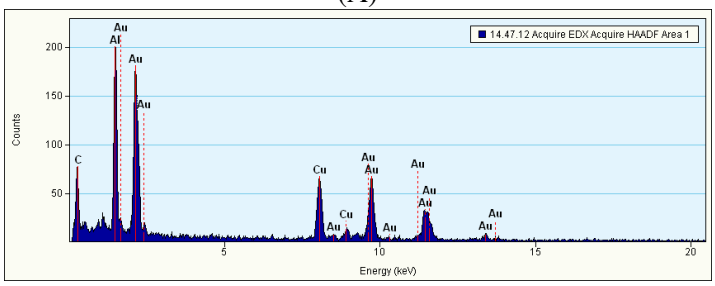


(D)

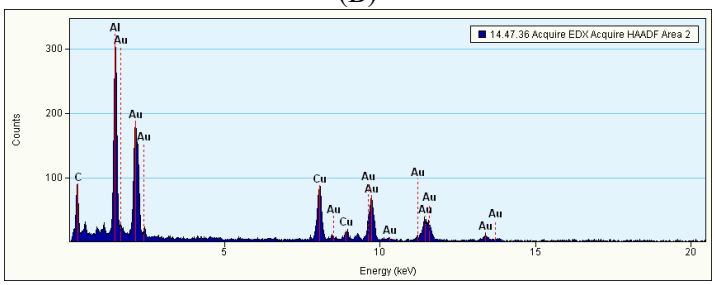
Figure 5.7: SEM image (A) which had EDX performed on subsections (1), (2) and (3) shown in sub figures in (B), (C) and (D) respectively. This was looking at the elements in the metal contact, this does seem to show the metals as expected of Al, Au and Ti. There seems to be a signal for Cu, this seems to be some contamination in the metal contact. It is unclear where this originated from however as it is only seen in the metal film it is most likely from the metal deposition.



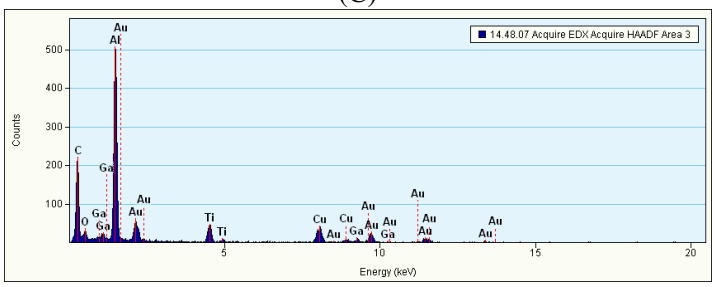
(A)



(B)



(C)



(D)

Figure 5.8: SEM image (A) which had EDX in performed on subsections (1), (2) and (3) shown in sub figures in (B), (C) and (D) respectively. This was looking at the elements in the metal contact, this does seem to show the metals as expected of Al, Au and Ti. There seems to be a signal for Cu, this seems to be some contamination in the metal contact. It is unclear where this originated from however as it is only seen in the metal film it is most likely from the metal deposition.

5.3.3 Capacitance-Voltage Measurements

The CV measurements were performed using a Wentworth probe station and a Keysight analyser, as shown in Figure 3.37 and described in Section 3.6. This setup is a semi-automated system which was intended to be able to take measurements across a wafer testing of multiple devices. This is based on a wafer map set up on the Wentworth probe station and controlled by the Keysight analysis. Only a subsection consisted of 10 contacts for each diameter size (1000 μm, 800 μm, 600 μm, and 400 μm), rather than the full set of 50.

New sets of measurements were performed on new contacts after each anneal to avoid potential damage from repeated probing, however, some measurements did not make proper contact, resulting in noise being recorded. To mitigate this, when analysing the data, care was taken to select measurements that made contact and could take a full measurement. This was to remove failed measurements to remove unnecessary noise.

The measurements were conducted at 30°C to keep the temperature constant. After dry runs of the processing with Si-based MIS capacitors, the measurement frequency was set to 1 MHz. For the Metal-SiO_2-β-Ga_2O_3 capacitors, a voltage range of ∓15 V was selected. The measurements were performed by sweeping the voltage from depletion into accumulation and back to depletion. That is negative to positive and back to negative, ensuring a depletion to accumulation and back to depletion. This method typically yields capacitance values closer to the true capacitance [262]. However, either direction can introduce a distortion to the true CV curve by injecting charge or mobile ions.

However, when applying the same voltage range to the Metal-Al_2O_3-β-Ga_2O_3 capacitors, they were destroyed, see Figure B.8 for an example. This behaviour was unexpected, particularly because no such breakdown was observed in Si/Al_2O_3 capacitors. To prevent further sample destruction, the voltage range was reduced to −15 V to +9 V, this does mean that the samples were not driven into deep accumulation, which caused concerns during the analysis and will be addressed later.

The breakdown behaviour discrepancy is unknown due to the material differences between the substrates is difficult to determine as they are quite different. Possible contributing factors include variations in dielectric thickness, interface quality, or defect density. Additionally, the ALD Al_2O_3 process was originally optimised for Si substrates and may not produce equivalent film properties on β-Ga_2O_3. Differences in the reaction during the ALD process could result in different stress in the deposited layer, the morphology or defect density, which could be responsible for the breakdown occurring on one and not the other.

Further investigation is necessary to identify the root cause of this breakdown. Suggested approaches include FIB-TEM analysis to compare the deposited films on Si and β-Ga_2O_3, ideally with equivalent doping concentrations. Complementary CV measurements would also help analyse interface trap densities and correlate them with the breakdown behaviour. The breakdown observed in the Al_2O_3/β-Ga_2O_3 MIS capacitors is unlikely to be attributed to damage from the metal deposition method. Both Si/Al_2O_3 and β-Ga_2O_3/Al_2O_3 structures underwent identical metal deposition using PVD sputtering, which did not induce similar breakdown behaviour in the Si-based devices. Furthermore, the thermal ALD process used for Al_2O_3 deposition was performed simultaneously in the same environment for all substrates, ruling out damage caused during the deposition process as a cause.

This leaves the substrate properties as a plausible factor. The breakdown could arise from differences in doping concentration, the specific interaction of the Al_2O_3 layer with the (001) β-Ga_2O_3 surface, or residues present on the β-Ga_2O_3 that were not removed during cleaning. However, since both Al_2O_3/β-Ga_2O_3 and SiO_2/β-Ga_2O_3 were cleaned using the same procedure and are highly doped, substrate residues alone are unlikely to explain the breakdown behaviour fully, however, cleaning both samples with piranha solution could improve the certainty of this.

Notably, the breakdown occurred as the devices were swept from depletion into accumulation. During this process, charge injection into the dielectric layer is a plausible explanation for the failure. The high carrier concentration in the β-Ga_2O_3 could explain a higher rate of charge being injected into the dielectric layer in general, which could further be amplified if the interface has a high level of interface traps. The band offsets between β-Ga_2O_3 and Al_2O_3 are also lower than Si and Al_2O_3 which could offer an explanation for this. Further analysis, such as interface trap characterisation or band alignment studies, would be necessary to isolate the root cause of this behaviour.

In this work, it was not possible to drive the β-Ga_2O_3/Al_2O_3 MIS capacitors into strong accumulation. This limitation arose from capacitor breakdown, meaning the true maximum capacitance C_A could not be measured. To deal with this, a technique proposed by Samares Kar [261] was used to estimate C_A.

This technique states that, (1) the surface charge and interface trap density D_{it} are exponential functions of the surface potential while in the accumulation region, (2) the measurements are performed in the accumulation region, and (3) the capacitance gradient (β) remains constant so that,

$$C_{sc} = a_1 e^{\beta\phi_S}, \tag{5.7}$$

and

$$C_{it} = a_2 e^{\beta\phi_S}, \tag{5.8}$$

are true.

Using this approach, C_A was estimated with the function (G),

$$G(c) = C^{-\frac{1}{2}} \cdot \sqrt{\frac{dC}{dV}} \tag{5.9}$$

by plotting this in the accumulation region. The method produced reasonable results for regions approaching medium to strong accumulation. This introduces a degree of inaccuracy, as C_A was not directly measured. See Figure 5.9 for Al_2O_3/β-Ga_2O_3 based capacitors for example and Figure 5.10 for SiO_2/β-Ga_2O_3 capacitors.

The inability to drive the metalAl_2O_3/β-Ga_2O_3 capacitors into strong accumulation contrasts with the behaviour of Si-based capacitors, where both Al_2O_3/Si and SiO_2/Si systems showed clear saturation in strong accumulation and deep depletion. This inability means C_A is an estimation which adds a level of uncertainty.

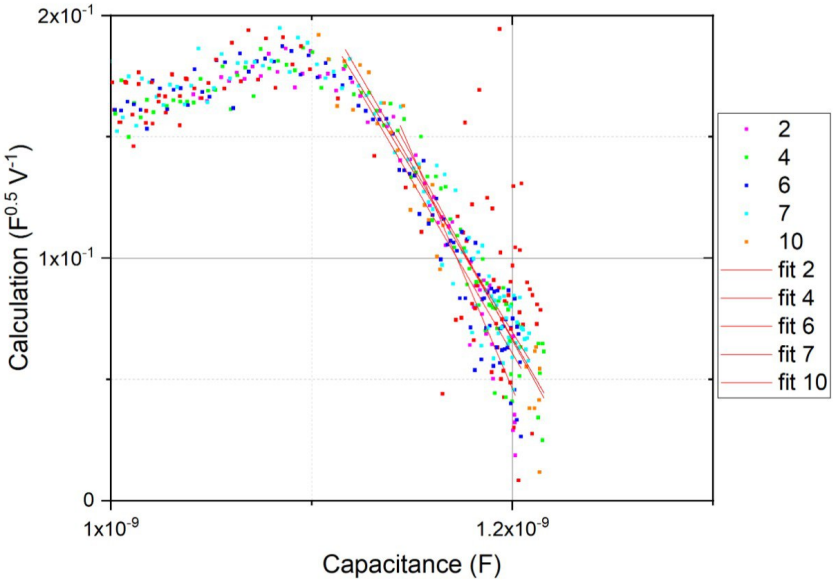
For the β-Ga_2O_3/SiO_2 capacitors, strong accumulation and deep depletion were observed in the as-deposited state. However, annealing at 200°C caused the capacitance to decrease significantly, leading to transitional behaviour in the CV curves.

The CV characteristics of the SiO_2/β-Ga_2O_3 sample changed significantly after the final anneal at 300°C. See Figure 5.10. Specifically, the hysteresis was reduced, and deep depletion was no longer identifiable. In comparison, the Si/SiO_2 sample exhibited two distinct plateaus as the device was driven into strong accumulation.

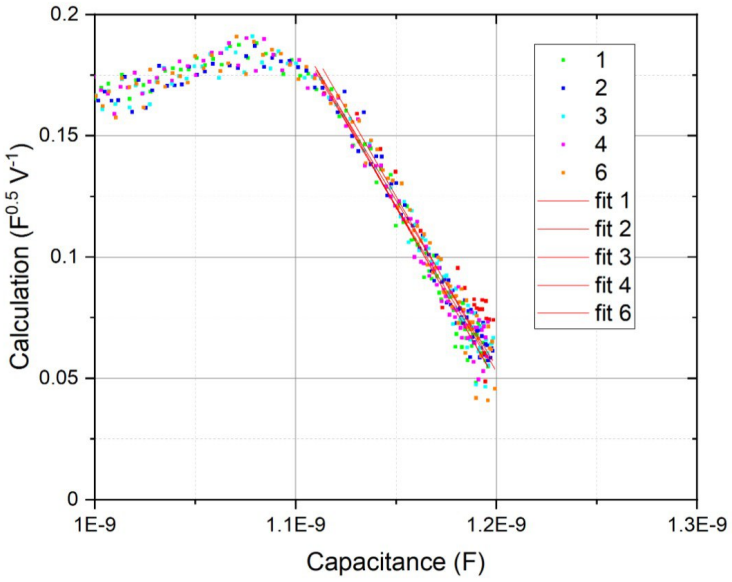
However, this plateau behaviour was not observed in the β-Ga_2O_3/SiO_2 sample. It is plausible that the higher doping concentration and elevated D_{it} stretched the CV curve to such an extent that these plateaus became indistinguishable. An example of this breakdown can be seen in the Appendix B.8.

This masking behaviour highlights the challenges faced in determining strong accumulation for Al_2O_3/β-Ga_2O_3 capacitors. It was not possible to confirm whether the capacitance reached a maximum as it could not be driven to higher voltages. This introduces a degree of uncertainty in determining the C_A so a potential error in the analysis and characterisation of the samples. While the approach used to estimate C_A should be valid, it is important to acknowledge this limitation, and it is an estimation.

This should be done by taking measurements before and after annealing, as well as adding other measurements techniques such as AFM and XPS. Building a model on the ellipsometer to incorporate β-Ga_2O_3 to then include Al_2O_3. This will allow better optimisation for the deposition conditions and pre and post deposition.

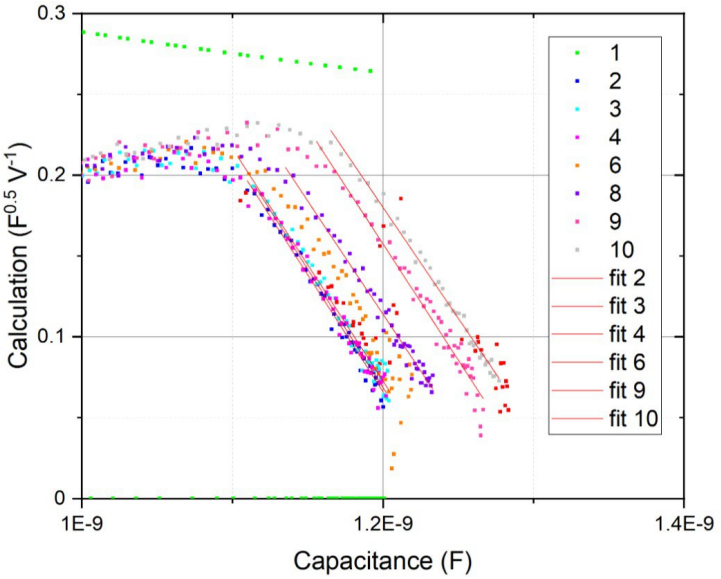


(A)

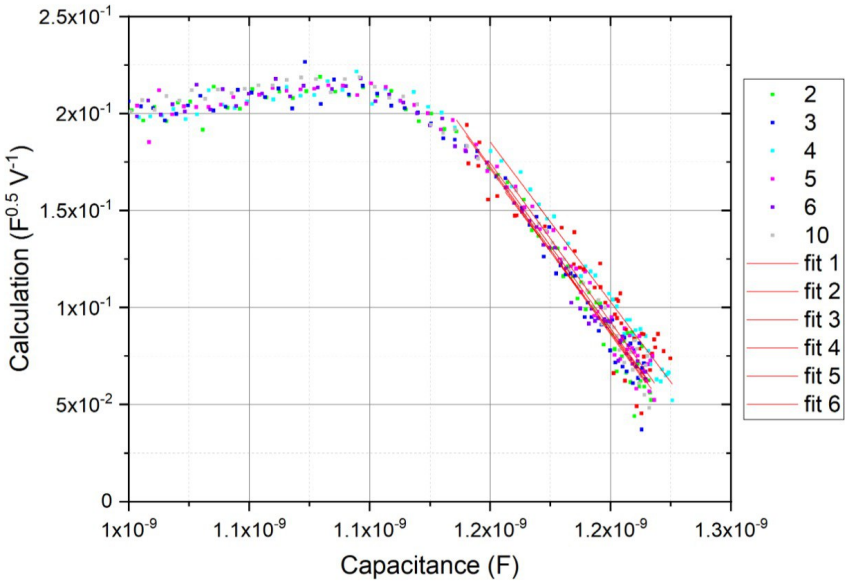


(B)

Figure 5.9: The plots used to determine the C_A for the Metal-Al_2O_3-β-Ga_2O_3, these are for the contacts with diameter of 1000 μm. This is As deposited (A), and annealing at 100°C (B), 200°C (C) and 300°C (D) respectively. In each plot, the number in the legend refers to the contact position within that set of ten measurements. The intercepts for the individual fittings can be seen in Table B.8. The CV plots are shown in Figure 5.11. The calculation is from equation 5.9, the fitted intercept on the x-axis gives an approximation to the C_A.

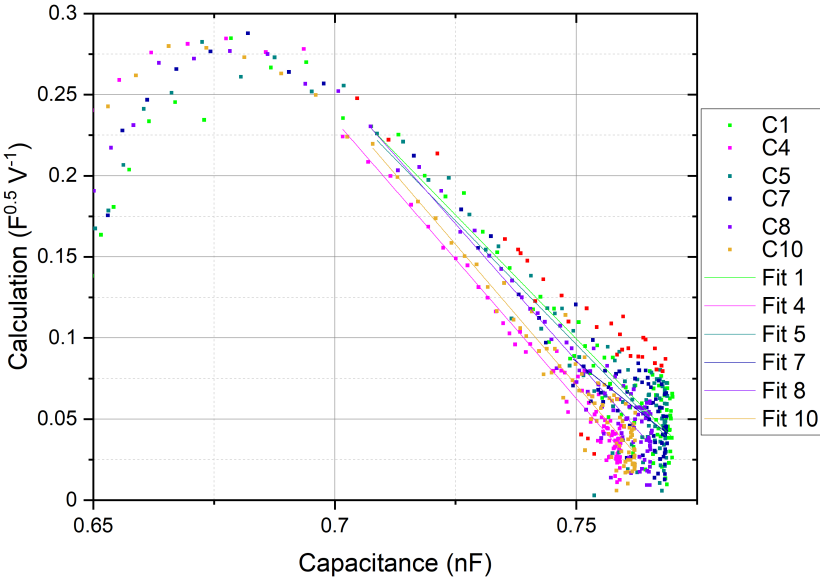


(C)

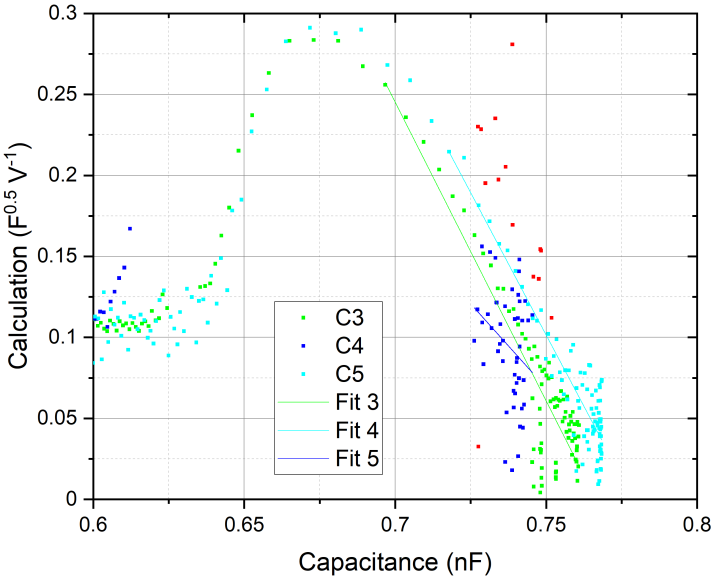


(D)

Figure 5.9: The plots used to determine the C_A for the Metal-Al_2O_3-β-Ga_2O_3, these are for the contacts with diameter of 1000 μm. This is As deposited (A), and annealing at 100°C (B), 200°C (C) and 300°C (D) respectively. In each plot, the number in the legend refers to the contact position within that set of ten measurements. The intercepts for the individual fittings can be seen in Table B.8. The CV plots are shown in Figure 5.11. The calculation is from equation 5.9, the fitted intercept on the x-axis gives an approximation to the C_A.

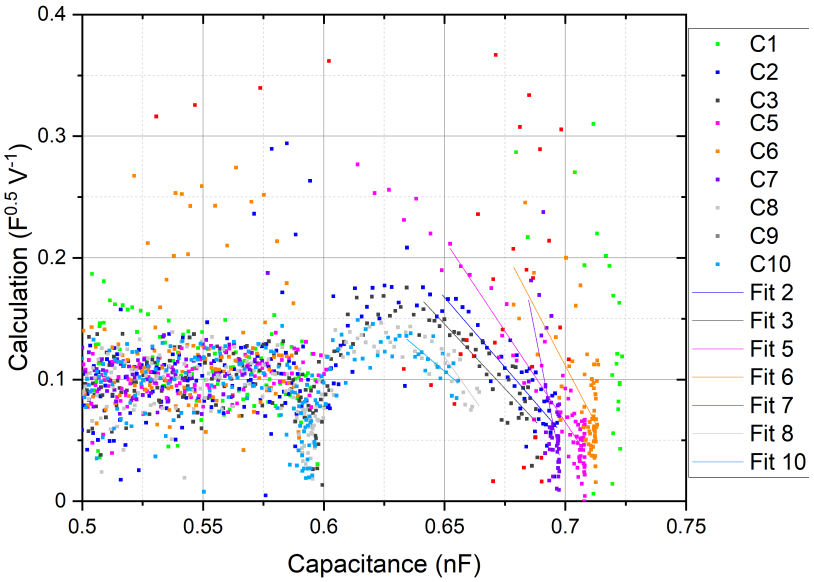


(A)

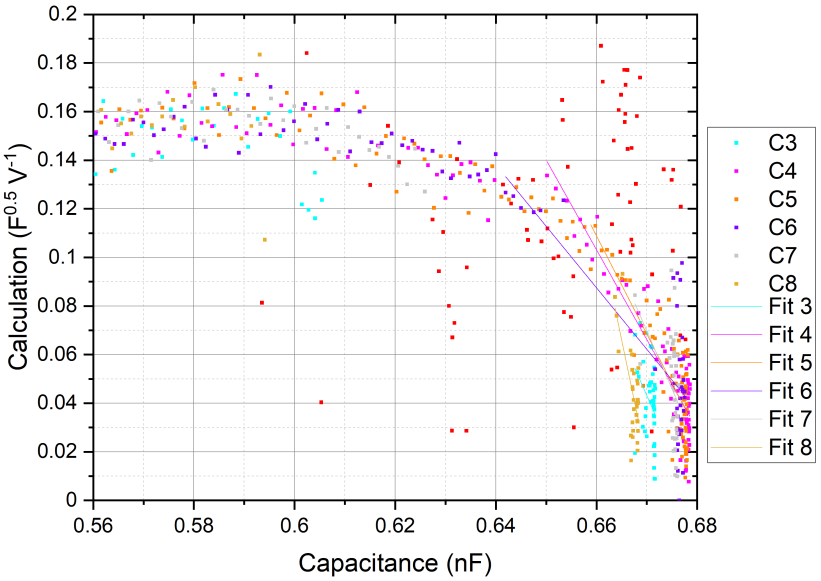


(B)

Figure 5.10: The plots used to determine the C_A for the Metal-SiO_2-β-Ga_2O_3, these are for the contacts with diameter of 1000 μm. This is As deposited (A), and annealing at 100°C (B), 200°C (C) and 300°C (D) respectively. In each plot, the number in the legend refers to the contact position within that set of ten measurements. The calculation is from equation 5.9, the fitted intercept on the x-axis gives an approximation to the C_A.

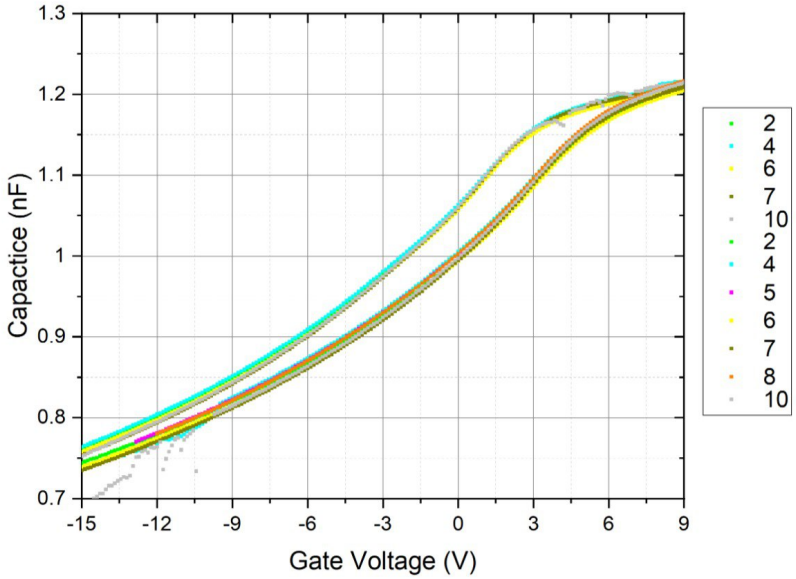


(C)

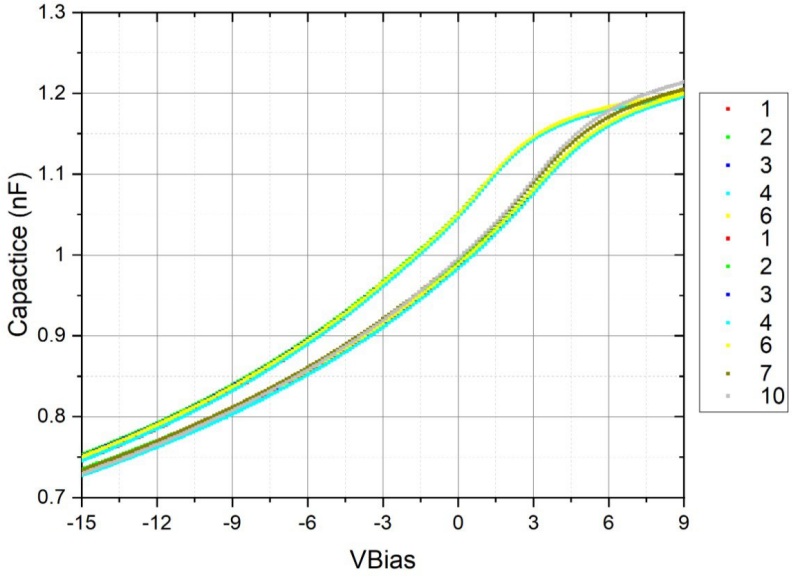


(D)

Figure 5.10: The plots used to determine the C_A for the Metal-SiO_2-β-Ga_2O_3, these are for the contacts with diameter of 1000 μm. This is As deposited (A), and annealing at 100°C (B), 200°C (C) and 300°C (D) respectively. In each plot, the number in the legend refers to the contact position within that set of ten measurements. The calculation is from equation 5.9, the fitted intercept on the x-axis gives an approximation to the C_A.

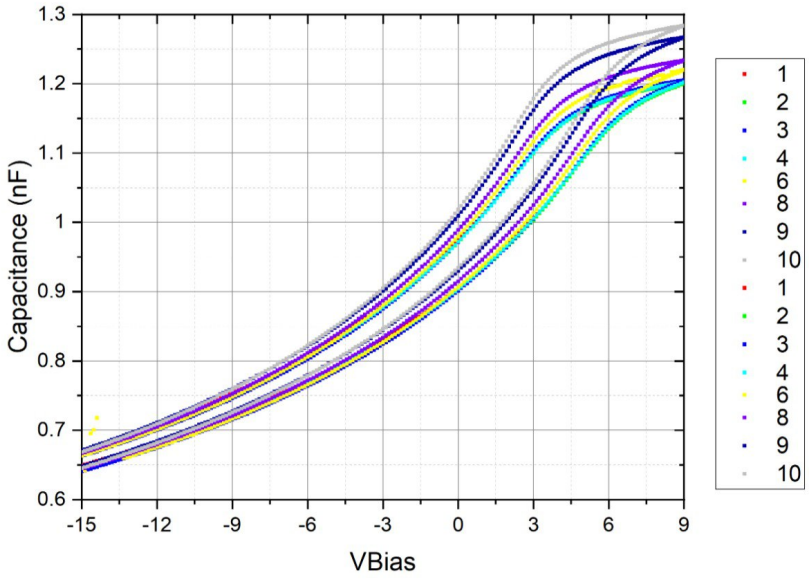


(A)

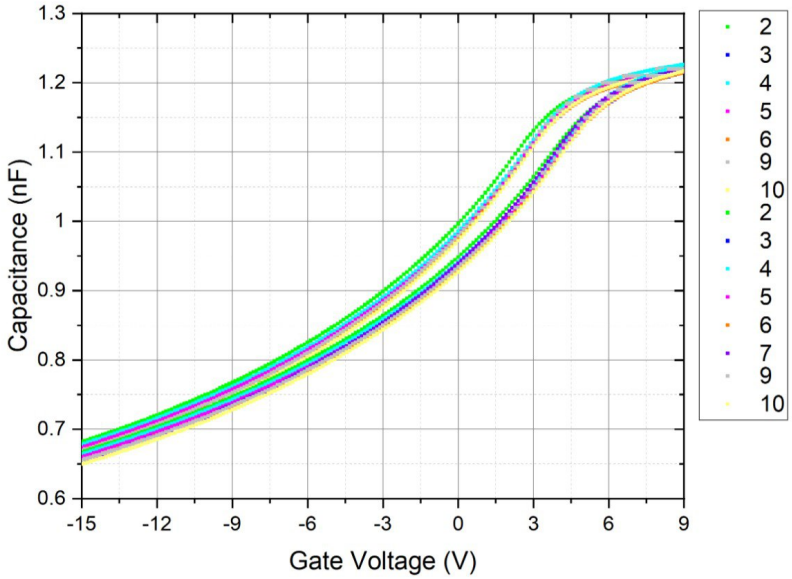


(B)

Figure 5.11: The CV plots for the Metal-Al_2O_3-β-Ga_2O_3, these are for the contacts with diameter of 1000 μm. This is As deposited (A), and annealing at 100°C (B), 200°C (C) and 300°C (D) respectively. In each plot, the number in the legend refers to the contact position within that set of ten measurements. Measurements which failed were removed from the plot.



(C)



(D)

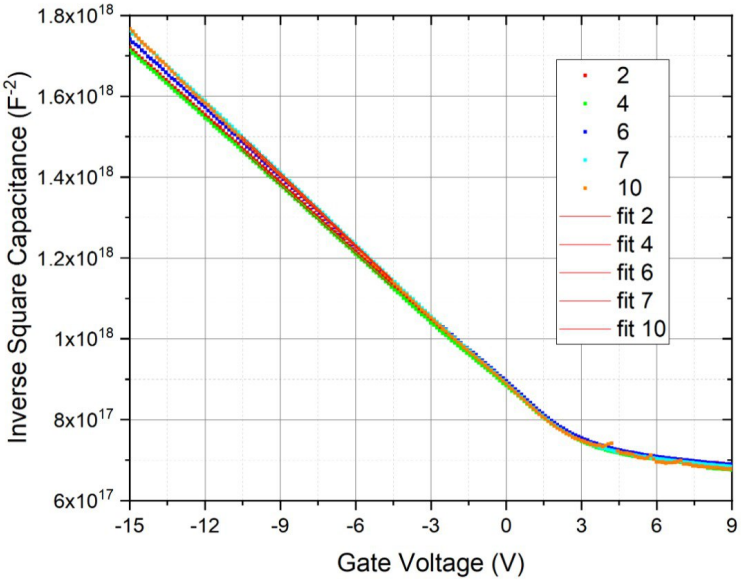
Figure 5.11: The CV plots for the Metal-Al_2O_3-β-Ga_2O_3, these are for the contacts with diameter of 1000 μm. This is As deposited (A), and annealing at 100°C (B), 200°C (C) and 300°C (D) respectively. In each plot, the number in the legend refers to the contact position within that set of ten measurements. Measurements which failed were removed from the plot.

In this work, the effective carrier concentration was calculated using the method described in Section 3.4.3. The carrier concentration was calculated from the $\frac{dC^{-2}}{dV_G}$ from the linear fit of the C^{-2} vs V_G plot, an example of which is shown in Figure 5.12. The calculated doping concentrations using this method are presented in Table B.10 with corresponding gradients from the plots. These concentrations were found to be $4.08 \pm 0.086 \times 10^{18}$ cm^{-3}, $4.78 \pm 0.958 \times 10^{18}$ cm^{-3}, $2.87 \pm 0.050 \times 10^{18}$ cm^{-3}, and $3.01 \pm 0.066 \times 10^{18}$ cm^{-3} for as-deposited, and after sequential annealing at 100°C, 200°C, and 300°C, respectively.

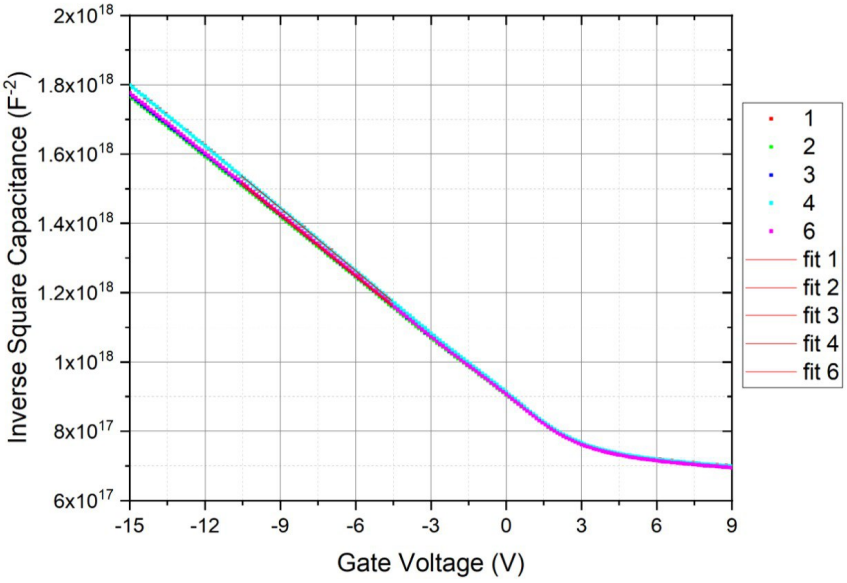
The errors were derived from the standard deviation of the gradients used in the C^{-2} vs.V_G plots. Given the influence of D_{it} on the CV curve, and thus on the C^{-2} vs V_G plot, it was assumed that annealing would reduce D_{it}, leading to more accurate carrier concentration estimates. Therefore, the final estimate of $3.01 \pm 0.066 \times 10^{18}$ cm^{-3} is considered the most reliable value.

A notable discrepancy was observed between the calculated doping concentrations and the manufacturer's specified concentration of 1.1×10^{19} cm^{-3}. This deviation is likely attributable to the high D_{it}, which stretches the CV curve and impacts the doping calculation's accuracy. A comparison using Hall effect measurements could help clarify this discrepancy. At the time this was not pursued as a process for ohmic contacts had not yet been developed in Swansea, this was later addressed in Chapter 6. It is also important to not that this was on bulk material, which Hall measurement requires a thin film.

Finally, it is important to highlight the role of C_A in this calculation. The accuracy of C_A is crucial not only for determining the carrier concentration but also subsequent analyses, as potential errors in C_A can propagate throughout the characterisation process.

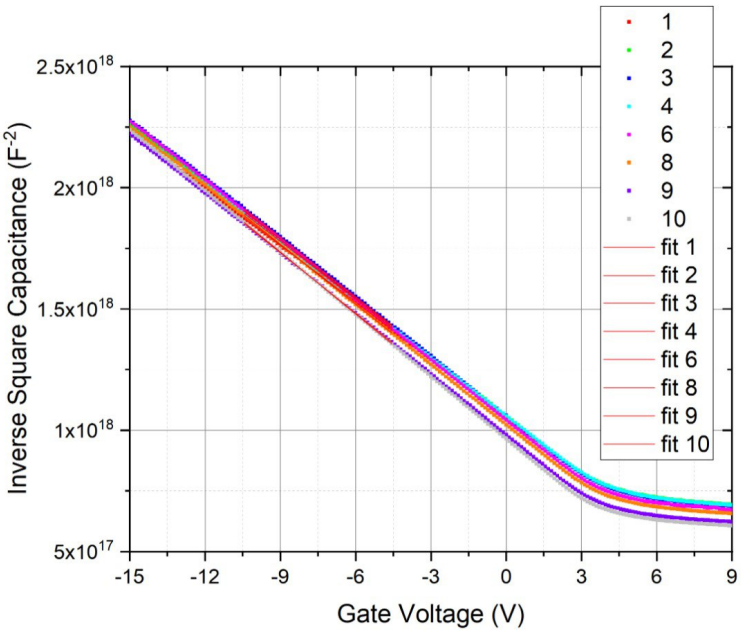


(A)

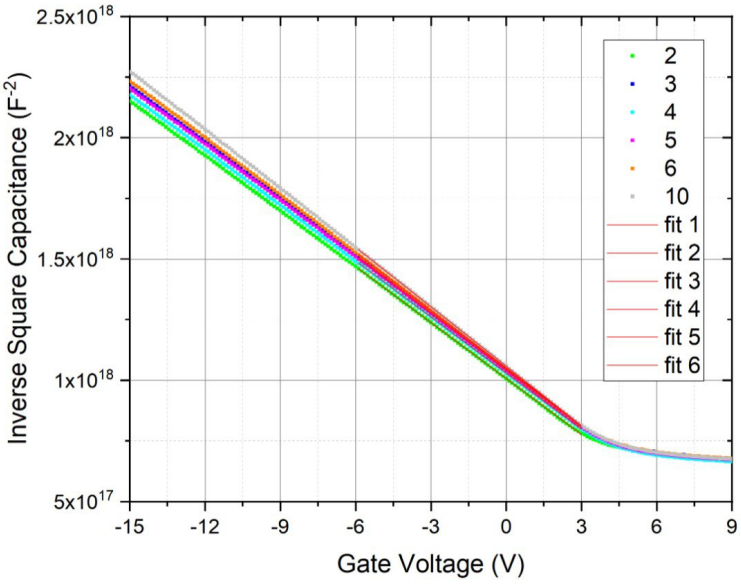


(B)

Figure 5.12: The inverse squared capacitance as a function of gate voltage, a linear fit to the depletion region of the curve, used to calculate the doping concentration. These are as deposited, and after annealing at 100°C, 200°C and 300°C (A), (B), (C) and (D) respectively.

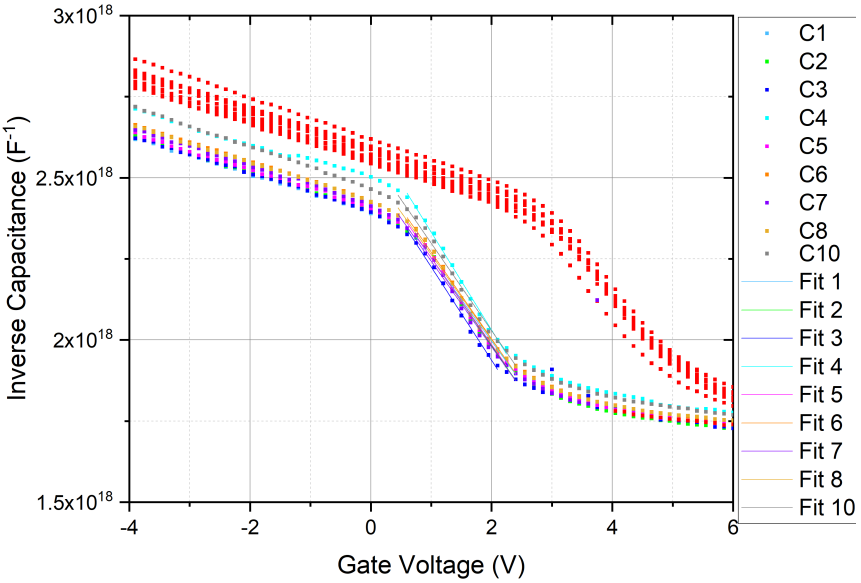


(C)

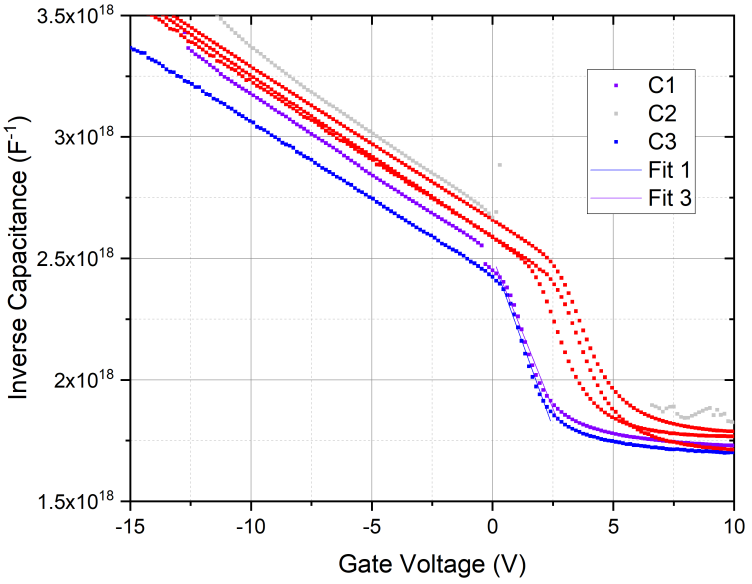


(D)

Figure 5.12: The inverse squared capacitance as a function of gate voltage, a linear fit to the depletion region of the curve, used to calculate the doping concentration. These are as deposited, and after annealing at 100°C, 200°C and 300°C (A), (B), (C) and (D) respectively.

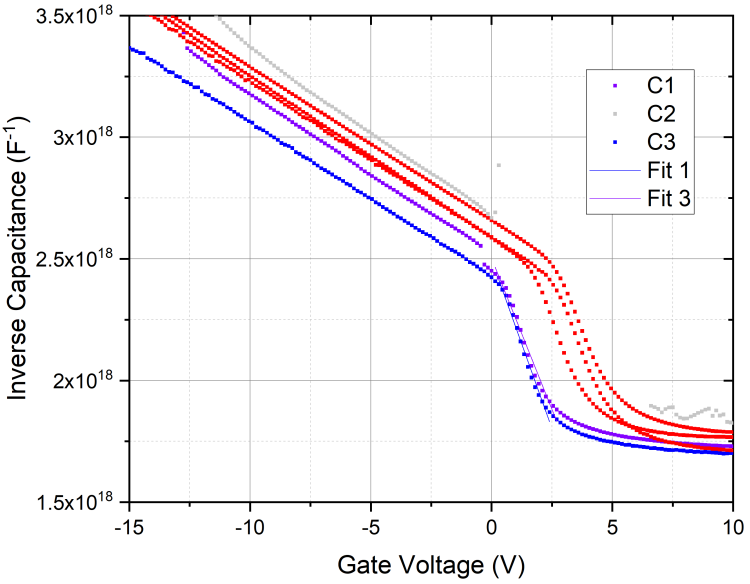


(A)

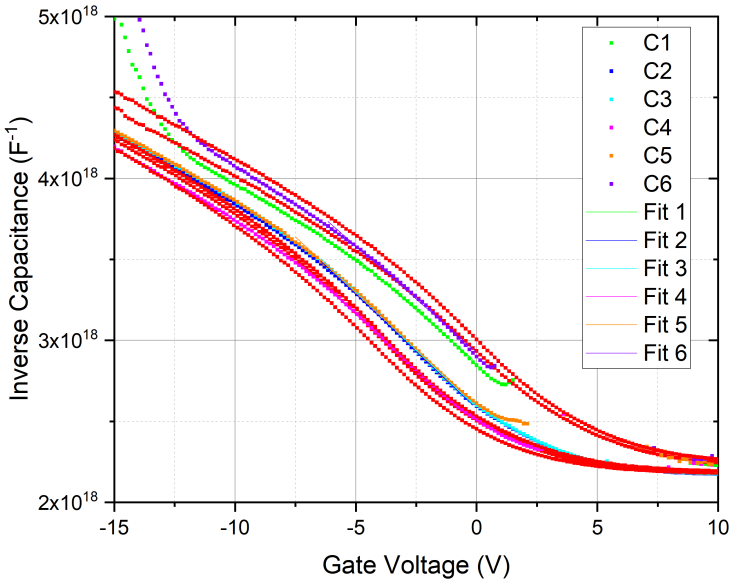


(B)

Figure 5.13: The inverse squared capacitance as a function of gate voltage, a linear fit to the depletion region of the curve, this was used to calculate the doping concentration. These are as deposited, and after annealing at 100°C, 200°C and 300°C (A), (B), (C) and (D) respectively.



(C)



(D)

Figure 5.13: The inverse squared capacitance as a function of gate voltage, a linear fit to the depletion region of the curve, this was used to calculate the doping concentration. These are as deposited, and after annealing at 100°C, 200°C and 300°C (A), (B), (C) and (D) respectively.

The Terman method [477] was used to calulate D_{it}. This is where an ideal CV curve was used to characterise the devices, it was used to determination the flat band voltage (V_{FB}), which in turn was used to characterise the D_{it} of the MIS structure. The ideal curve was compared to the experimental results to perform this. This is why the previous values determined such as carrier concentration and C_A were so important, any error is propagated into the ideal curve and so the analysis going forward.

V_{FB} was calculated by determining the flat band capacitance (C_{FB}) the point where the theoretical surface potential is zero, as shown in Equation 3.4. In the ideal case, with no metal-semiconductor work function difference (ϕ_{MS}) or additional charge, the V_{FB} would be 0 V. However, experimentally, V_{FB} is influenced by various factors, including D_{it}, D_O, D_M and D_F. By comparing the experimental CV curve to the ideal one, the location of V_{FB} on the experimental curve can be identified. Interpolation of experimental data was used to accurately determine V_{FB}, linear interpolation was used as the experimental capacities measured do not directly match the C_{FB}, the ratio between points was used to estimate the V_{FB} for a value more representative of the true V_{FB}. The V_{FB} theoretically is,

$$V_{FB} = \phi_{MS} - \frac{Q_{it}(\phi_s)}{C_A} - \frac{Q_M}{C_A} - \frac{Q_O}{C_A} - \frac{Q_F}{C_A} \tag{5.10}$$

where ϕ_{MS} is the metal-semiconductor work function and where Q is the total charge related to the density by,

$$D_x = \frac{Q_x}{C_A} \tag{5.11}$$

where the subscript x is to denote between fixed (F), interface traps (it), mobile (m) or oxide (o) charges (Q), density of charge (D_x), related to the shift in voltage (v). In the ideal case, V_{FB} is equal to ϕ_{MS}. The additional charges can be combined (Q_{TC}). Without further work, it is impossible to disentangle these components entirely. Given that the observed hysteresis shift was negative, it was specifically attributed to charge injection into the dielectric layer (Q_O), this is an inference as these values are grouped and separating them is not possible with the work performed here. It is also possible that Q_M and Q_O were also present in the DA sweep.

In conclusion, while an ideal CV curve provides valuable insights into the MIS structure, the experimental limitations and presence of non-idealities necessitate careful interpretation of results. These limitations, particularly those related to hysteresis and charge injection, should be considered when analysing the interface and dielectric properties. This indicates that in the next iterations of this work, tests should be done to experimentally separate these values as much as possible, relying on inferences and grouped values, which limit how useful this information is.

5.3.4 Terman Method

$D_{it}(\phi)$ can be determined in several ways L.M. Terman first developed the Terman method reported in 1962 [477]. The method utilises high-frequency CV measurements, it is shown in Appendix B.6. At sufficiently high frequencies, the contribution of D_{it} to the total capacitance is negligible because the AC signal switches too quickly for the D_{it} states to respond. Thus, only the DC signal contributes to the observed D_{it}.

The Terman method is sensitive to both slow and fast traps, meaning the absolute position of the CV curve will be distorted based on D_{it} as a function of the DC voltage. These traps stretch out the CV measurement. While the Terman method has known limitations, it is widely used as a quick and effective method to determine D_{it} in the order of 10^{10} and above [262].

The D_{it} is calculated by comparing the experimental and ideal CV curves. At the same capacitance value, the respective experimental and ideal gate voltages are compared, with their difference related to the charge due to D_{it} at a given surface potential ϕ. The relationship is expressed as,

$$D_{it}(\phi) = \frac{Q_{it}(\phi)}{qA} = \frac{C_A}{q^2 A}\frac{d}{d\phi}\Big(V_g - V_{g,i}\Big) = \frac{C_A}{q^2 A}\frac{td\Delta V_g}{d\phi} \tag{5.12}$$

Here, ϕ is the surface potential, A is the area of the gate contact, q is the electron charge, V_g is the experimental gate voltage, and $V_{g,i}$ is the ideal gate voltage.

The difference between the experimental and ideal gate voltages is given by,

$$\Delta V_g = Vg - Vg, i \tag{5.13}$$

The ideal CV curve is generated using previously calculated values, such as C_A, carrier concentration, and V_{FB}. Any errors in these parameters propagate into the ideal CV curve and subsequently into the calculated D_{it}, underscoring the importance of accurate earlier calculations.

The $V_{g,i}$ is derived from an ideal surface potential ϕ, which by definition at the flat-band condition is,

$$\phi = U = V_i = 0 \tag{5.14}$$

This is shifted by the experimentally determined V_{FB}, aligning the ideal curve to the experimental flat-band capacitance C_{FB}. Divergence beyond this point is attributed to D_{it}. The resulting D_{it} value from Equation 5.12 is located ϕ below the conduction band edge ($E_C - E_T$) as $-q\phi$.

The Terman method is most accurate for mid-gap states but tends to overestimate D_{it} near the band edges. States may not be visible because they require electron-hole generation to populate and depop-

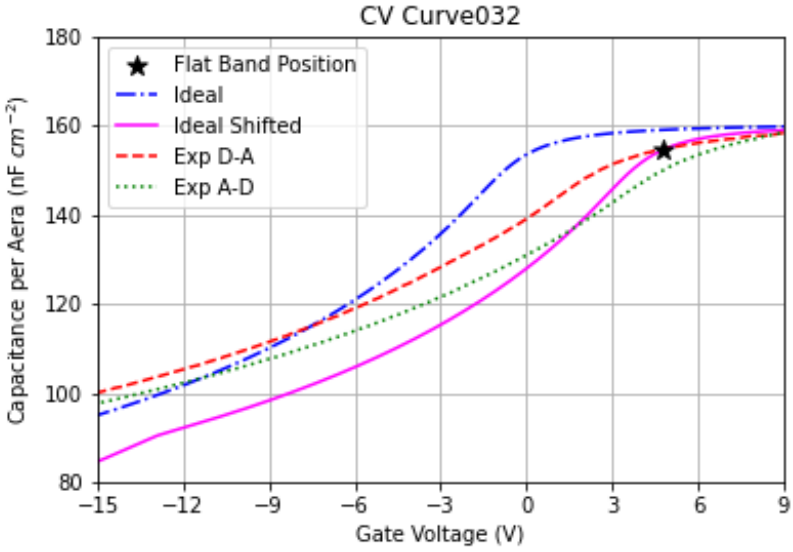
ulate. For wide bandgap materials like β-Ga_2O_3, this limits the observable range to states within 1 eV of the conduction band edge [478] [479]. UV- or thermal-assisted CV methods could be employed to extend this range.

In this work, D_{it} was calculated using the Terman method for as-deposited samples and after each annealing stage. The method is limited to a range near the conduction band edge, typically 0.2–0.6 eV below, where it may overestimate D_{it} when closer to the conduction band and underestimate as it goes further into the band gap. In this range, D_{it} values of up to 10^{14} $eV^{-1} \cdot cm^{-2}$ were observed.

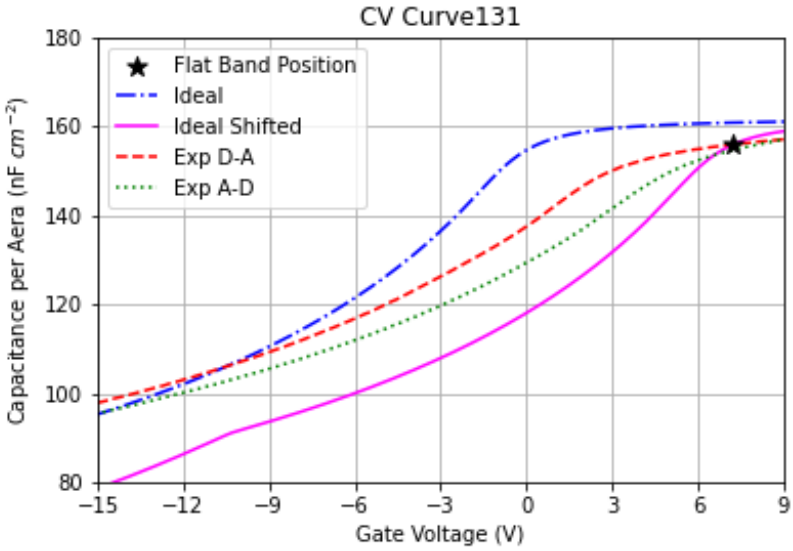
The mean of D_{it} calculated in this work can be seen in Table 5.2, as well as the accumulation capacitance and carrier concentration. The initial D_{it} was found to be $3.11 \pm 0.22 \times 10^{12}$ $eV \cdot cm^{-2}$, after annealing at 200°C it reduced to $2.89 \pm 1.01 \times 10^{11}$ without significant change after annealing at 300°C

Sample	C_A nF	Carrier Concentration cm^{-3}	Effective Oxide Thickness nm	D_{it} $eV^{-1} \cdot cm^{-2}$
As Deposited	1.25 ± 0.0042	$3.96 \pm 0.00923 \times 10^{18}$	21.84187 ± 0.18917	$3.11 \pm 0.22 \times 10^{12}$
100°C	1.24 ± 0.0026	$3.86 \pm 0.00528 \times 10^{18}$	21.93573 ± 0.04688	$2.69 \pm 0.12 \times 10^{12}$
200°C	1.25 ± 0.0026	$2.80 \pm 0.00770 \times 10^{18}$	21.2424 ± 0.59762	$2.89 \pm 1.01 \times 10^{11}$
300°C	1.25 ± 0.0044	$2.91 \pm 0.00642 \times 10^{18}$	21.6313 ± 0.0748	$2.89 \pm 0.09 \times 10^{11}$

Table 5.2: The tabulated data for samples Al_2O_3/β-Ga_2O_3 MIS capacitor, as deposited and annealed from the CV measurements and processed to determine C_A, effective carrier concentration, effective oxide thickness and D_{it} between 0.2-0.6 eV. This range was chosen as above 0.6 eV more of the D_{it} decreases due to charge carrier generation rate which means the system isn't in equilibrium and below 0.2 eV it can be effected by band bending effects.

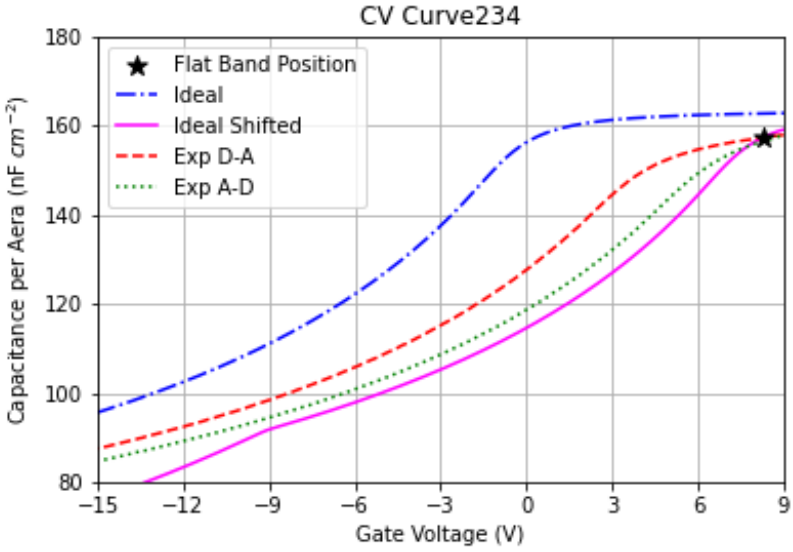


(A)



(B)

Figure 5.14: Example Ideal and experimental CV for β-Ga_2O_3/Al_2O_3 MIS capacitors (A) as deposited and after annealing at 100°C (B), 200°C (C) and 300°D for an hour at each temperature consecutively. These are example graphs with the remaining in the appendix B.27, B.28, B.29 and B.30. For each ideal and experimental CV curve the Terman method was used to calculate the D_{it}.



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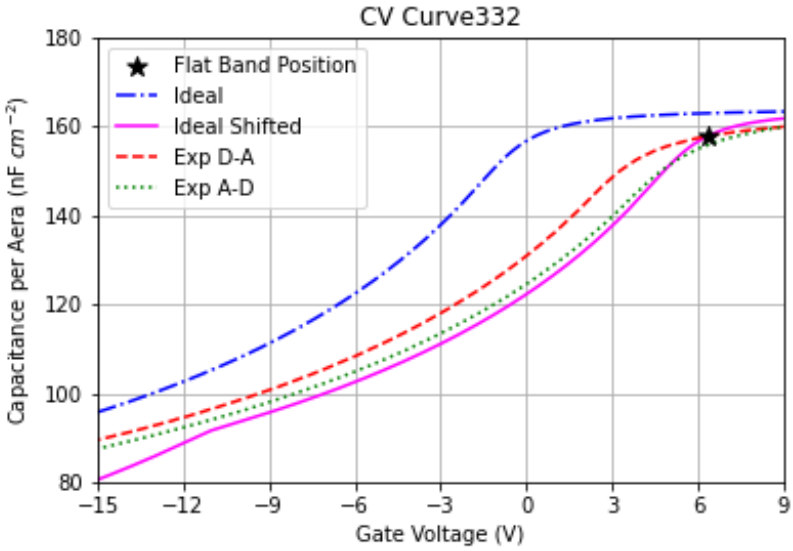
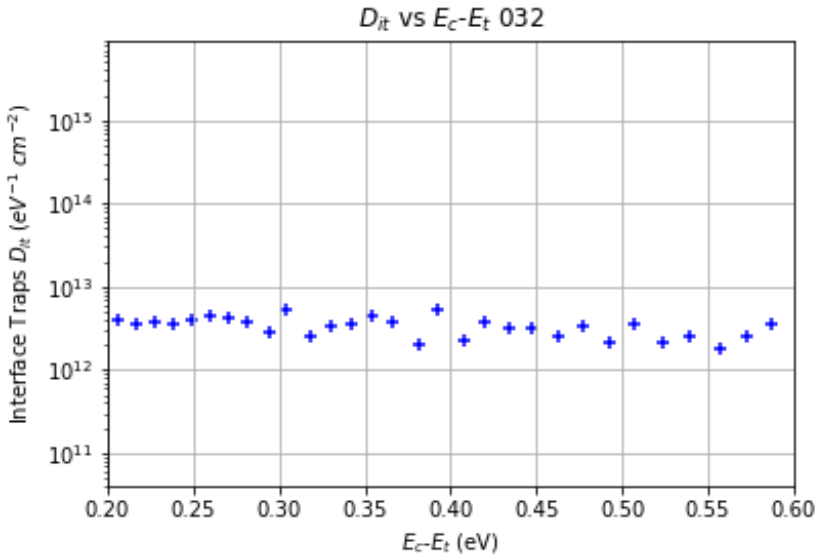
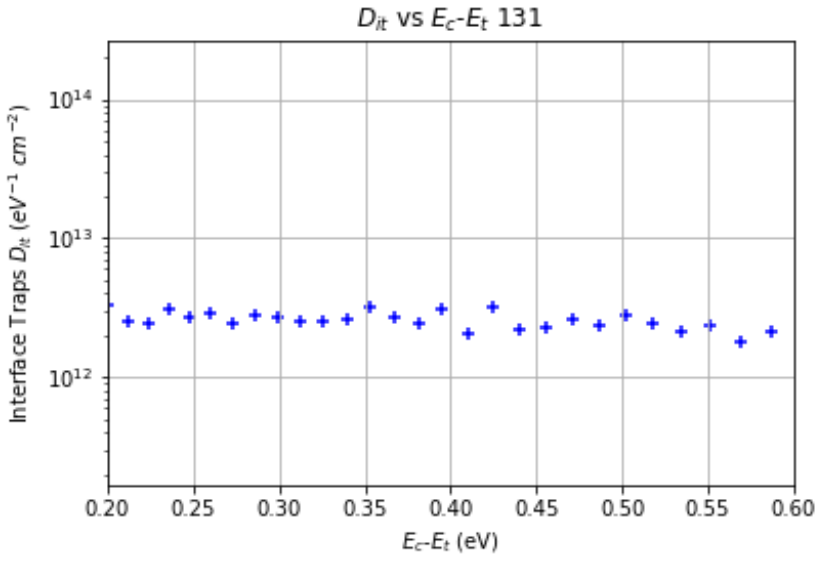


(D)

Figure 5.14: Example Ideal and experimental CV for β-Ga_2O_3/Al_2O_3 MIS capacitors (A) as deposited and after annealing at 100°C (B), 200°C (C) and 300°D for an hour at each temperature consecutively. These are example graphs with the remaining in the appendix B.27, B.28, B.29 and B.30. For each ideal and experimental CV curve the Terman method was used to calculate the D_{it}.

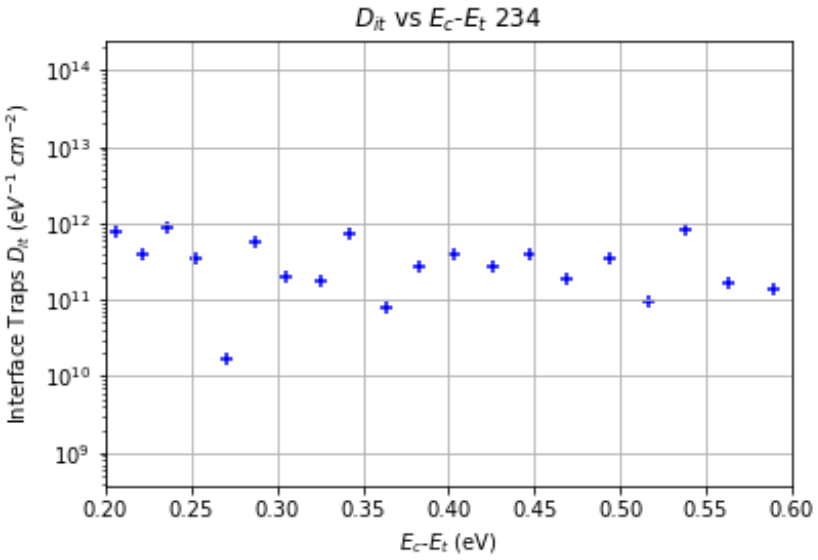


(A)

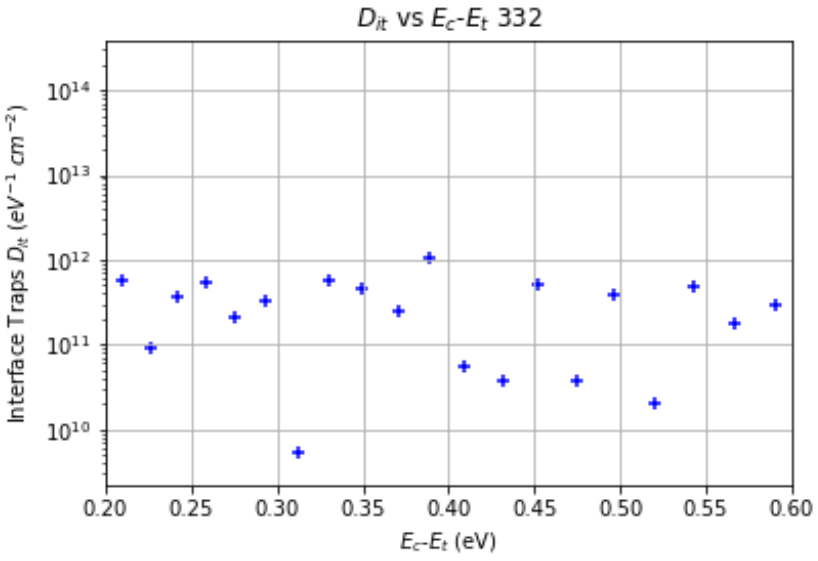


(B)

Figure 5.15: Example D_{it} between 0.2-0.6 eV from the conduction band for the β-Ga_2O_3/Al_2O_3 MIS capacitors (A) as deposited and after annealing at 100°°C (B), 200°°C (C) and 300°C (D) for an hour at each temperature progressively. These are example graphs with the remaining in the appendix B.23, B.24, B.25 and B.26. Plot (E) shows a comparison of these plots plotted on a single graph.

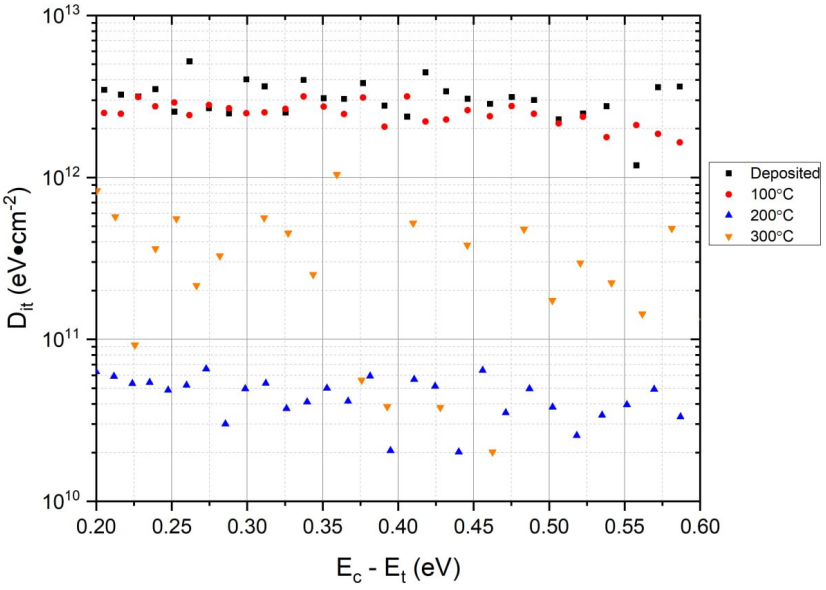


(C)



(D)

Figure 5.15: Example D_{it} between 0.2-0.6 eV from the conduction band for the β-Ga_2O_3/Al_2O_3 MIS capacitors (A) as deposited and after annealing at 100°°C (B), 200°°C (C) and 300°C (D) for an hour at each temperature progressively. These are example graphs with the remaining in the appendix B.23, B.24, B.25 and B.26. Plot (E) shows a comparison of these plots plotted on a single graph.



(E)

Figure 5.15: Example D_{it} between 0.2-0.6 eV from the conduction band for the β-Ga_2O_3/Al_2O_3 MIS capacitors (A) as deposited and after annealing at 100°°C (B), 200°°C (C) and 300°C (D) for an hour at each temperature progressively. These are example graphs with the remaining in the appendix B.23, B.24, B.25 and B.26. Plot (E) shows a comparison of these plots plotted on a single graph.

5.4 Conclusion

In this chapter, MIS capacitors based on bulk Ga_2O_3 were fabricated and characterised. The metal layer stack consisted of Ti/Al/Ti/Au (20/80/20/20 nm), while the dielectric layers were ALD-deposited Al_2O_3 and PECVD-deposited SiO_2. The targeted dielectric layer thickness was 50 nm. The actual thickness of the dielectric layers was determined using ellipsometry on spectator Si wafers.

CV measurements were conducted on the MIS capacitors in their as-deposited state and after sequential annealing at 100°C, 200°C, and 300°C for one hour in an N_2 environment. The SiO_2 samples exhibited unexpected CV profiles, the cause of which remains unclear. Consequently, further analysis of these samples was not pursued. In contrast, the Al_2O_3 samples were further investigated using FIB-TEM to inspect the semiconductor-dielectric interface.

Carrier concentration, V_{FB}, and C_A were calculated for the Al_2O_3-based MIS capacitors based on data from CV measurements, ellipsometry, and FIB-TEM. This information was used to construct ideal CV profiles, which were then compared to the experimental profiles to estimate the D_{it} using the Terman method. The D_{it} values decreased significantly after annealing at 200°C, indicating improved interface quality.

In the β-Ga_2O_3/SiO_2, as-deposited it can be seen that the sample dose go into deep depletion. This changes dramatically after the final anneal, as there is not a clear transition from depletion into the deep depletion, there was also an issue in accumulation when the measured capacitance would drop. The Si/SiO_2 sample was quite different, while sharing the issue seen in the final anneal of β-Ga_2O_3/SiO_2, this occurred throughout the Si/SiO_2 operation. It also suffered from what appears almost two accumulation regions, where there seems to be a local plateau between accumulation and depletion, this became more pronounced with progressive annealing. The carrier concentration distorts the CV profile, it is uncertain if this is also present on the β-Ga_2O_3 substrate or if this feature is only present on the Si substrate. In terms of the Si/SiO_2 sample, this means that there is uncertainty for the C_A, the C_{FB} and V_{FB}, as a result, any determination of the D_{it} is likely erroneous as the Terman method uses an idealised model to compare to the experimental data.

This idealised model is only as good as the data which is being used to develop it. This could be an indication that the deposition of the SiO_2 onto the substrates might have introduced impurities or was poor quality. Compare this to the Al_2O_3 samples, both Si and β-Ga_2O_3, the CV profiles do not share this characteristic. The D_{it} of these samples were calculated for these as the C_A can be trusted hence the values for C_{FB} and V_{FB} are more accurate, the model can be more accurately generated and the D_{it} are less likely to be erroneous. This means that there is more uncertainty in the Si/Al_2O_3 then the β-Ga_2O_3/Al_2O_3 sample. The D_{it} seemed to decrease with the progressive annealing, after the annealing stage of 200°C.

Annealing increased the C_A, based on the initial and final thickness, as implied by the ellipsometry reading and observed by the FIB-TEM measurements. This is due to an apparent reduction in the volume of the dielectric with the calculated ϵ decreasing towards the accepted value range for Al_2O_3. The reduction in volume and decrease in dielectric value can be described by Atsushi et al. [499], where they investigated Al_2O_3 films on Si. It was attributed that removing methyl groups was responsible for both of these. The EDX noticed a significant Al spike near the surface. As stated before, it is unknown when it occurred. Separate measurements as the dielectric is deposited, the metal is deposited, and after annealing would reveal more information about both thickness and whether any diffusion is occurring.

It was expected to have more Al diffuse into the β-Ga_2O_3 which was observed by Klingshirn et al. [500], therefore some diffusion of Al into Ga_2O_3 was expected. It should be noted that this was on a different orientation (201) and annealing temperature 500°C. This would not be expected on SiO_2, as the diffusion of Al is lower then that of Al_2O_3 [501], [502]. This densification and diffusion could explain the changes to the shapes and magnitude of C_A, which seem to primarily occur in the 100-200°C annealing range for both samples. Looking at Figure 5.11, it can be seen that the plots for, as-deposited and 100°C are similar to one another, which is also the case for 200°C-300°C. This appears to be an important point, as both curves appear to change at this point, marginal for Al_2O_3 but dramatic for SiO_2. This indicates that the system becomes more stable at this point, indicating that the densification and The CV curve was also seen to be more unstable in the PECVD SiO_2 than the ALD Al_2O_3. These factors show that the nature of PECVD does not produce interfaces which are as suitable as ALD [503].

There was a decrease in the hysteresis observed between the forward and reverse CV measurements after annealing. There was significant variation in the hysteresis as deposited, but this decreased after annealing. This would correspond to a reduction of shifted voltage from mobile and oxide charge, while here it cannot be determined which or what ratio of this is occurring. This could mean the density of mobile charge, or mobility of this charge, as it is the shift in voltage in the time that the CV measurement is taken. Alternatively this could be less charge being introduced into the dielectric layer during operation, this could also be charge due to charge already being introduced into the dielectric layer during annealing.

D_{it} was reduced after annealing at 200°C, with little change after 300°C. While an improvement compared to rapid PMA, which has been shown to reduce D_{it} significantly more effectively. It should be noted that in this work, D_{it} was measured with the Terman method, which overestimates D_{it}, whereas Hirose et al. [504] used the conduction method and piranha treatment both of which achieve more accurate results, however, at the cost of more measurement time.

While issues exist with the Terman technique for evaluating D_{it} in wide band-gap semiconductors, this method offers a relative comparison between similar interfaces following PDA [505]. The calculated D_{it} plots are shown in Figure 5.15, and the values for D_{it} presented in Table 5.2. The Q_H is believed to be related to injected charge, and in this case, it causes the C_{FB} to shift negatively, indicating that the mobile charge is positive and is reduced after annealing. For Al_2O3, it can be seen that annealing affects the nature of the curve. Until it stabilises after a 200°C anneal, however, it can be seen that between 200°C and 300°C, the accumulation to depletion curve ΔV_H is consistent, showing that the sweep is not affected by the mobile charge. This indicates that the Q_H is negative, and it can be seen that this is reduced by annealing. D_{it} was approximately 10^{12} $eV^{-1} \cdot cm^{-2}$ as deposited, reducing to 10^{11} $eV^{-1} \cdot cm^{-2}$. D_{it} could have been introduced during the depositions involving organic compounds, carbon content is often present, affecting the optical and electrical properties.

Matsubara et al. [256], investigated the $Al/GeO_2/Ge$ MIS structure, where they incorporated PDA and PMA over an extended time period. It was found that an extended PMA could be relevant to this work as the PMA performed were 200-400°C for 30 minutes, it was found that in the range 300-400°C in forming gas H^+ or N_2 increased the D_{it}. This showed it was a thermal effect which was believed to be an effect on the Al electrodes rather then the GeO_2/Ge portion of the structure as PDA did not have the same effect. This conclusion seems to disagree with what was found in this work, where an increase of D_{it} was observed, believing to be a result of some degradation of the gate electrode. As the gate electrodes were different here, Al compared to Ti this could explain the difference or perhaps the capping and overlayers employed in this work adequately resisted the degradation which could have occurred.

Zhang et al. [257], investigated MIS capacitors on (001) β-Ga_2O_3 , with thermal ALD Al_2O_3. In this work the Al_2O_3 was deposited at 300°C where the precursors were tri-methyl-aluminum (TMA) and H_2O. In the worked performed by Zhang et al. [257], the gate electrode was formed by evaporating Ni on the topside, and the ohmic contact by evaporating Al onto the backside. The β-Ga_2O_3 was pretreated by piranha cleaning and PDA, the piranha clean was believed to introduce hydroxyl groups onto the surface of the β-Ga_2O_3. This promotes the initial growth of Al_2O_3 layers due to the mechanism described in Section 3.1.7. The piranha cleaning may also remove valence defects which can act as trapped charge. Zhou et al. [258], decreased D_{it} down to 2.3×10^{11} $cm^{-2} \cdot eV^{-1}$. This was on (-201) β-Ga_2O_3, with a combination of PDA and piranha cleaning. Piranha cleaning was shown to smooth the surface of the β-Ga_2O_3, reducing the RMS of the surface $0.26 \rightarrow 0.17$ nm. This reduced the hysteresis $0.45 \rightarrow 0.1$ V, after a PDA of 500°C, which was observed in both N_2 or O_2 atmosphere, this PDA was for period of 2 minutes. They found that the O_2 anneal was more effective at reducing the D_{it}, 3.3×10^{11} $cm^{-2} \cdot eV^{-1}$ to 2.3×10^{11} $cm^{-2} \cdot eV^{-1}$ N_2/O_2. It has been demonstrated by Shibata et al. [259], that a small change in carbon contamination can lead to a significant optoelectronic effect increasing the D_{it}. This makes quantifying the percentage of carbon responsible for these

changes challenging. The D_{it} appeared to lower with annealing for both samples with Al_2O_3 having a lower D_{it} then SiO_2. This improvement was unexpected as MIS capacitors Hiroshi et al. [256], found that for GeO_2Ge an increase in D_{it} was seen after post mentalisation anneal, this was attributed to the degradation of the metal contact. This was because it was observed after a 300°C annealing post-metallisation but not observed post-deposition anneal.

To summarise the work performed in this chapter investigating dielectrics onto (001) β-Ga_2O_3, MIS structures employing ALD Al_2O_3 and PECVD SiO_2 were compared using CV measurements. Following PMA, substantial changes were found to both types of MIS capacitors. In both cases, accumulation capacitance reduced, which could correlate with the formation of suboxide interlayers at the metal-dielectric identified using TEM-EDX. A reduction in Q_H was attributed to a decrease in the density of mobile charges in the dielectrics following PDA. This occurred in both dielectrics but was most pronounced in the SiO_2, where the charge switched.

In the case of Al_2O_3, a more ideal CV profile was observed compared with the SiO_2 counterpart, where the character of the CV curve changed. The observed changes indicate that neither of these dielectrics should be exposed to these temperatures and expected to operate as-deposited. They should be kept below certain operating conditions or annealed so that their characteristics do not change during the operation of the device. While Al_2O_3 would be suitable for a gate dielectric, reducing significantly after annealing at 200°C (from $3.11 \pm 0.22 \times 10^{12}$ to $2.89 \pm 1.01 \times 10^{11}$ $eV^{-1} \cdot cm^{-2}$). remaining stable at 300°C. Further work could be done to investigate higher deposition temperatures to assess if it is more resistant to change. It was observed that Al_2O_3 had lower D_{it} and higher C_A then SiO_2. It is also important that the CV curve was also unrecognisable after the annealing. It also is clear from the CV curves that low-temperature ALD Al_2O_3 appears more stable than PECVD SiO_2. This, alongside the low-k dielectric, means it is unsuitable as a gate dielectric, however, it may be suitable for passivation. Further work would be required to determine whether the diffusion of the metals across the interface was an issue for Al_2O_3.

PECVD SiO_2 and Al_2O_3 deposited at 100°C have been demonstrated, and electrical measurements taken after exposure to temperatures up to 300°C for an hour. This has shown that without further treatments, these are not suitable dielectrics for Ga_2O_3 at temperatures above 200°C and further work should be undertaken to establish their operating conditions and possible treatments to extend this range.

CHAPTER 6

β-GA_2O_3 OHMIC CONTACT DEVELOPMENT

Ohmic contacts are a crucial step in device fabrication, as outlined in Chapter 2. Although various metallisation processes have been developed and are discussed in Chapter 2, a suitable protocol was developed in Swansea. In this chapter, four metallisation schemes Ti/Al, Ti/Au, Ti/Ag, and Ti/W, were investigated over three development cycles. Ti/W was introduced in the second cycle, and Ti/Ag and Ti/Au were tested in the third and final cycle. The experiments were conducted on bulk (001) β-Ga_2O_3 and epitaxial (-201) Ga_2O_3 substrates, with photoresist application protocols optimised for each metal contact. The goal was to use circular transmission line models (CTLMs) to measure contact resistance, however, to be characterised the IV measurement on the CTLM structures require thin film geometry and such treatment is not valid on bulk substrates. An attempt was subsequently made on thin films of β-Ga_2O_3, proved challenging due to, the low doping levels in the material.

6.1 Introduction

Ohmic contacts are essential for fabricating functional semiconductor devices, as discussed in Chapter 2. Numerous factors affect the formation of ohmic contacts on β-Ga_2O_3, including the material's phase, orientation, doping level, and surface states. Additionally, the deposition technique, such as sputtering or evaporation, influences the contact properties. The metal stack configuration and deposition methods play a significant role in the formation of ohmic contacts, as discussed in Chapter 2. While the contact layer is the most critical, interactions between layers within the stack also impacts performance. Other influential factors include pre- and post-metallisation treatments, such as chemical cleaning, plasma treatment, and annealing under different conditions.

Most reported ohmic contacts for β-Ga_2O_3 use Ti as the contact layer, paired with various capping and overlayers. Ti is highly adhesive and has a work function close to the electron affinity of β-Ga_2O_3, which ideally requires a work function near 4.8 eV based on the Schottky-Mott rule. With a work function of approximately 4.33 eV [506], Ti forms a contact compatible with β-Ga_2O_3. However, Ti can oxidise upon annealing, forming an interfacial TiO_2 layer, similar to silicide formation in Si-metal contacts. The thickness and composition of the contact layer and the growth of TiO_x oxides play crucial roles in the thermal stability and conductivity of the contact.

Alternative ohmic contact methods include using degenerate semiconductors such as ITO or AZO as the contact layer, but these typically require high-temperature (over a 1000°C) anneals, making them less practical for device applications.

In work by Callahan et al. [283], ultra-thin Ti layers (5–10 nm) were evaporated onto (001) β-Ga_2O_3 doped at 4×10^{18} cm^{-3}. It was observed that limiting the Ti contact layer to 5 nm restricted TiO_2 growth, significantly improving thermal stability, particularly when paired with a thick Au capping layer (100 nm).

This work explores multiple metallisations and capping layers for β-Ga_2O_3, with Ti/Au being the most commonly reported and thus the benchmark contact for comparison. However, as Au is costly and inert, it is incompatible with CMOS processing, creating a need for Au-free contacts. This issue, common in GaN-based technology [507], may also affect β-Ga_2O_3 device integration. While Au certainly is adventitious due to its high chemical stability, meaning that the contact is resistance to oxidation meaning the contact is less likely to deregulate. The high electrical conductivity of Au is beneficial for using Au as a capping layer.

To address this, Au-free alternatives, such as Ti/Al, Ti/W, and Ti/Ag, were evaluated alongside Ti/Au. Ti/Al contacts have been previously demonstrated [297], making them suitable candidates for this study. Ti/W contacts were also considered, drawing on work by Tetzner et al. [284], who found that sputtering Ti/W alloy onto β-Ga_2O_3 created stable ohmic contacts. In our study, Ti and W were deposited as separate layers, with Ti acting as the contact layer and W as the capping layer. Finally, Ti/Ag was investigated, as Ag can form pseudo-ohmic contacts [276], though dewetting observed after annealing posed challenges, raising questions about the role of pre- or post-treatment processes.

This study represents the first phase of developing ohmic contacts for β-Ga_2O_3 in Swansea, where Ti/Au, Ti/Ag, Ti/Al, and Ti/W configurations were explored, with a particular interest in Au-free contacts. The initial development was conducted on (-201) β-Ga_2O_3 epilayers with unknown doping levels, which proved unsuccessful. Subsequent work used bulk (001) β-Ga_2O_3, employing CTLM patterns for contact characterisation.

Even though thin layers of Ti has been demonstrated the layer was kept at 20 nm in this work, this was because the most commonly cited contacts use 20 nm. Significant time was spent developing photoresist protocols, initially using AZ 5214E, which was discontinued, necessitating a shift to AZ LNR 726. Significant edge bead formation on die-sized samples rather than full wafers was observed, which remained a challenge throughout the work.

6.2 Development Cycle

The process of developing and characterising ohmic contacts was conducted in three distinct development cycles, each building on findings from the previous cycle. These cycles were further shaped the next iteration of the process development with each adapting to new issues and transition to CISM.

Each development cycle informed the approach taken in the following cycle, with specific insights and challenges discussed at the end of each stage.

6.2.1 Development Cycle One

This first development cycle is structured to address initial challenges and outline the foundational steps taken to fabricate and evaluate ohmic contacts. This subsection begins with an introduction to the overall approach, followed by a discussion of contamination issues that were identified and resolved to allow for reliable measurements. Subsequent sections detail the contact fabrication method, the IV measurement procedure, and a discussion of the results obtained.

Introduction

This represents the initial development of ohmic contacts for this work in Swansea. As previously discussed, ohmic contacts are essential for any practical device, serving as source and drain contacts on n^+ bulk or thin layers, depending on device geometry. For this initial cycle, Ti/Au contacts were selected based on extensive prior use, with Ti/Al also chosen as it has demonstrated ohmic behaviour. Since Ti serves as the primary contact layer and Ag has shown pseudo-ohmic properties, so Ti/Ag was investigated, with Ag as the capping layer.

The primary aim of this cycle was to establish and test potential ohmic contacts to guide future work.

Initial investigations were conducted on heterostructure samples obtained from Kymer in 2017, consisting of 500 nm of epitaxial (-201) β-Ga_2O_3 grown on p-type Si. These layers were either Sn-doped to be n-type or unintentionally doped (UID). Sample details, as well as a view of these materials, are provided in Figure 3.30 and were discussed in Section 3.2.9.

One major issue encountered was the unknown carrier concentration, which influences ohmic contact formation. While the manufacturer estimated mid 10^{18} cm^{-3} for the doped epilayers, this could not be confirmed in early measurements.

The equipment posed an additional challenge, as most available tools were designed for 4" wafers, leading to processing issues on smaller die. These included significant edge bead formation and difficulty achieving consistent contact between the mask and sample during photolithography.

Attempts to measure the carrier concentration using a Hg probe were unsuccessful, likely due to the small contact between the Hg contact and sample. Though the probe was recalibrated and the acrylic plate resurfaced, reliable contact could not be maintained.

Using a Schottky contact, a CV measurement could provide a non-destructive means of determining carrier concentration on small die, as described in Chapters 3 and 5.

Si die (10 mm) were cleaved from 4" and 6" wafers sourced from Inseto and Pi-KEM, to identify processing issues before using actual samples. Potential problems included photoresist protocol challenges due to the pronounced edge bead on smaller samples. These Si trials, conducted prior to the work in Chapter 4, revealed further difficulties with edge bead management. Uneven pressure during mask alignment was another issue, Si die were used to balance the applied pressure and improve contact consistency during photolithography.

(A) (B)

Figure 6.1: One of the 6" Si wafers used in this work to create Si die for testing processes on small sample sizes (A), then cleaved into a selection in (B).

Fabrication

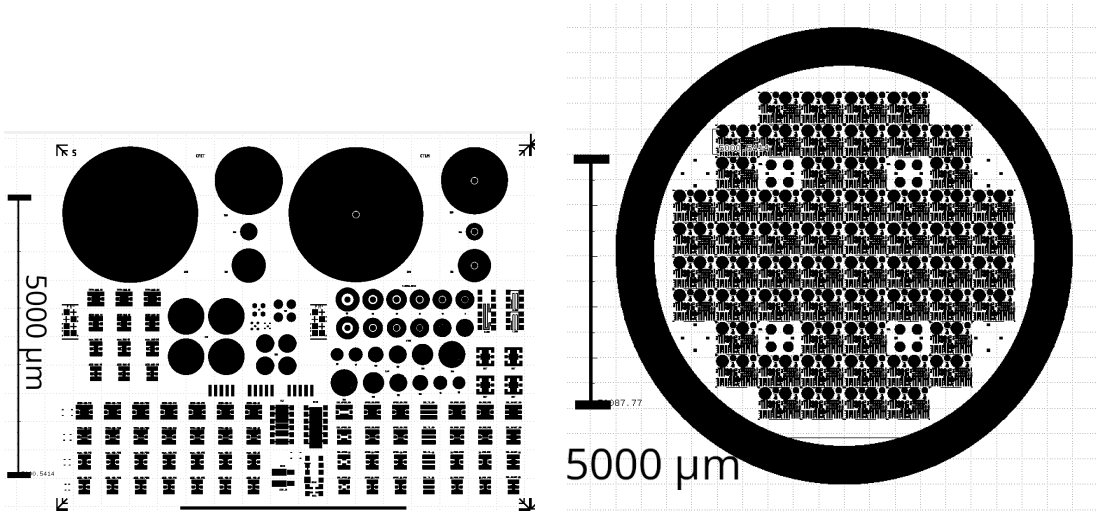
Before processing any β-Ga_2O_3 samples, Si wafers were cleaved to match the dimensions of the actual die to serve as representative test samples in the following process. These Si wafers acted as spectators to verify the consistency of the UV patterning and development stages. (1) Both Si and epi-β-Ga_2O_3/Si samples were solvent-cleaned by submerging in acetone for 10 minutes, followed by IPA for 5 minutes, and then dried with an N_2 gun. (2) The samples were dehydrated on a hot plate at 100°C for 10 minutes to remove moisture, improving the reliability of photoresist layer adhesion. (3) Ti-prime was then applied as an adhesive agent, spun at 4000 rpm with an acceleration of 1000 for 30 s. (4) After this, the samples were baked for 120 s at 110°C. (5) AZ 5214E photoresist was spun onto the samples at 3000 rpm, 1000 acceleration for 45 s. (6) Subsequently this was baked at 110°C for 60 s. (7) The samples were then exposed to 45 $mJ \cdot cm^{-2}$ UV light using the mask shown in Figure 6.2. (8) This was followed by baking for 120 s at 120°C and a blanket flood exposure of 300 $mJ \cdot cm^{-2}$. (9) Development was performed in a solution of 2:3, AZ Developer to DI water for 60–90 s, followed by a rinse in a 1:3 AZ Developer to DI water solution for 10 s, and two final rinses in DI water for 10 s each.

After preparation, the samples were loaded into the PVD K.Lesker system for metal deposition, detailed in Section 3.1.6. Three metallisations were applied, these were Ti/Al, Ti/Au, and Ti/Ag. Each followed the same Ti deposition process, with variations in the capping layer.

The deposition system was pumped down overnight with the turbo pump set to 50%, then increased to 100% to achieve a pressure in the 10^{-7} mTorr range. Ar was introduced at 100 sccm, and 50 W power was applied to the Ti target, with a V/I ratio of 260/0.220 V/A. A getter layer of Ti was deposited to reduce O_2 levels and limit outgassing from previous depositions.

For the Au deposition, Ar was introduced at 120 sccm, with a chamber pressure of 6×10^{-3} mTorr. Ag deposition was performed with 75 sccm Ar flow, a potential of 30 W, and a chamber pressure of 4.5×10^{-3} mTorr, yielding a deposition rate of 1.6 Å $\cdot$ s^{-1}. Al was deposited with 100 sccm Ar flow, starting at 50 W and increasing incrementally to 150 W, with a chamber pressure of 3.5×10^{-3} mTorr.

Following deposition, lift-off was conducted in D350, producing a final layer thickness of 20/80 nm for each metal stack. The fabricated samples are shown in Figure 6.3.



(A) (B)

Figure 6.2: The mask used in the initial ohmic study of this work, (A) is the subsection used and (B) is the total mask.

A generic process flow for the metal-lift-off process used in this work can be seen in Appendix C.1.

Results Initial Ohmic contact

IV measurements were taken before annealing and subsequently after annealing at 300°C, 400°C, and 500°C for two minutes each, under an inert atmosphere. Examples of the IV measurements for Ti/Ag, Ti/Au, and Ti/Al contacts are shown in Figures 6.4, 6.6, and 6.5, respectively. None of the samples exhibited ohmic behaviour.

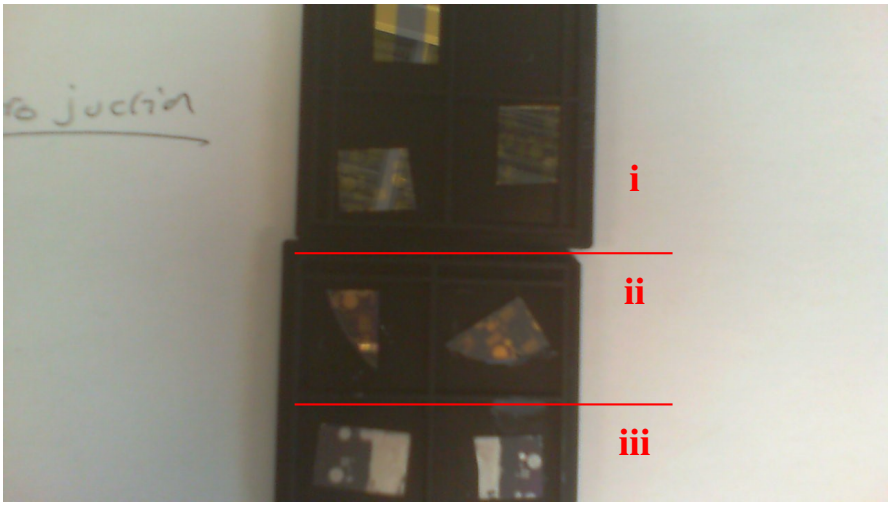
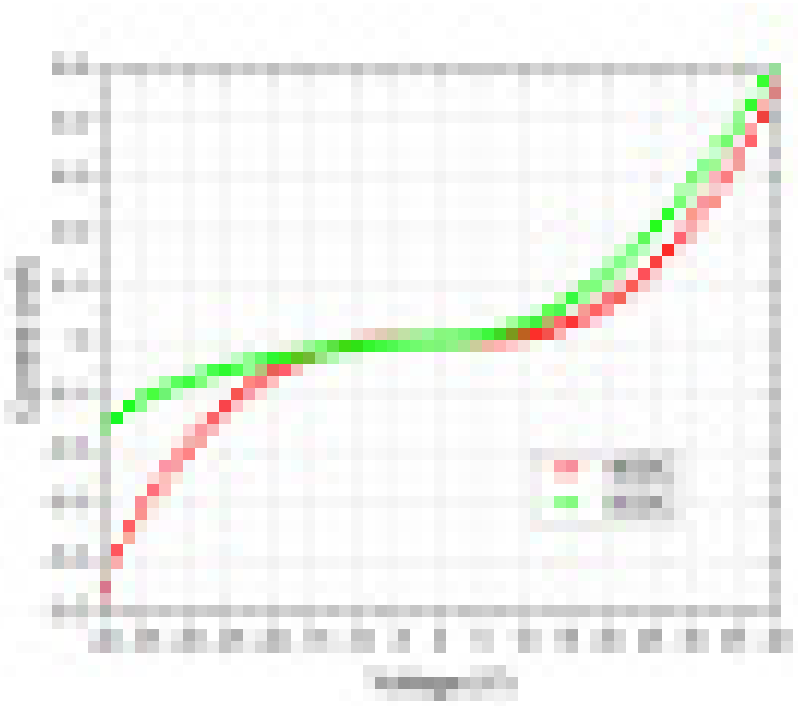


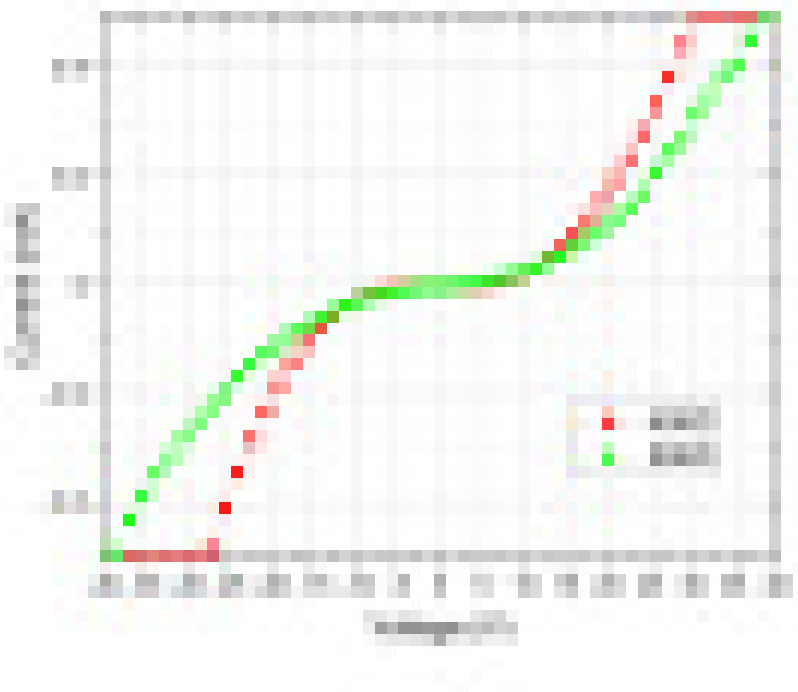
Figure 6.3: The β-Ga_2O_3/Si heterostructure samples after the metal deposition metal lifted off. The metalisations were Ti/Au (i), Ti/Ag (ii) and Ti/Al (iii).

In all IV curves, the measured current remained low, likely due to the high resistance, particularly affecting the Ti/Al contacts, which may have obscured the Schottky nature of the contacts. The low current levels observed, even at high applied voltages, further suggest that sheet resistance was a dominant factor.

This initial attempt did not use a dedicated mask, and not all contacts were consistently formed across samples. This inconsistency may have contributed to the varying measurements, with some unintentionally doped (UID) samples appearing more conductive than their intentionally doped counterparts. Ti/Al contacts showed the most potential for ohmic behaviour, although they remained the least conductive among the three metal stacks tested. This is a further indication that the resistance of the β-Ga_2O_3 is dominating the IV plot, rather than Ti/Al being pseudo-ohmic.

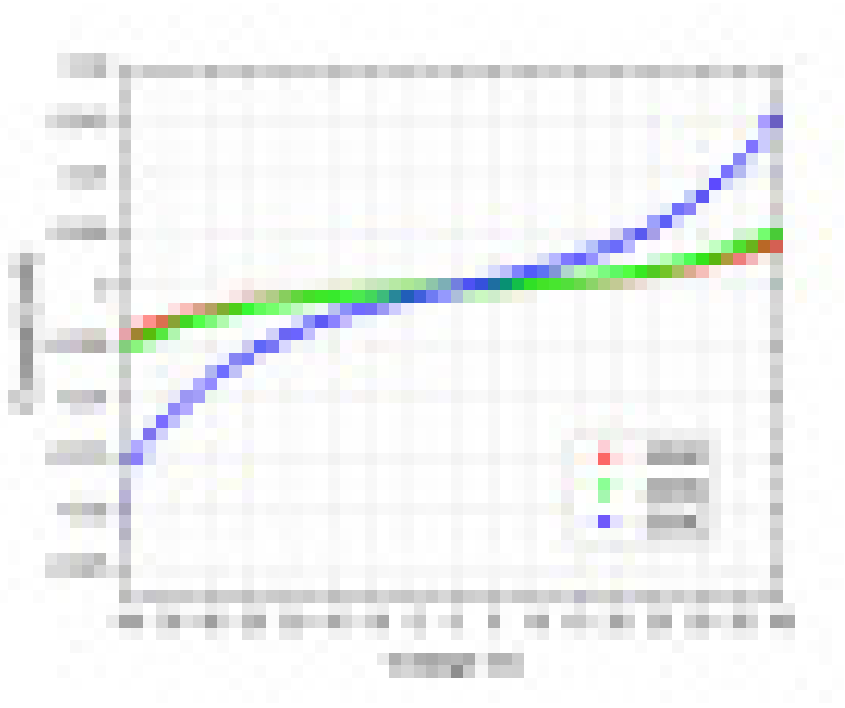


(A)

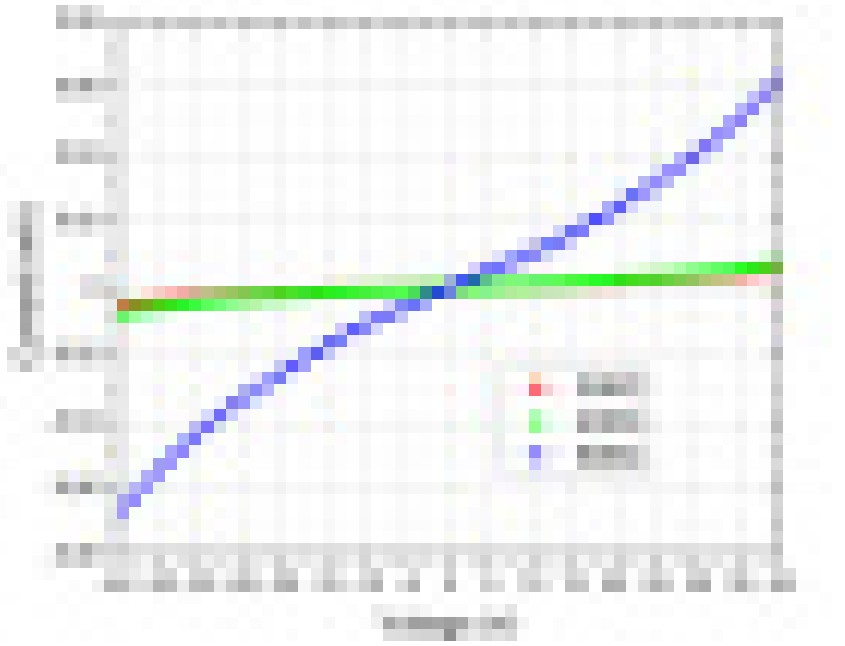


(B)

Figure 6.4: Example IV measurements from Ti/Ag contacts on (A) n-type Sn and (B) unintentionally doped (−201) β-Ga_2O_3.

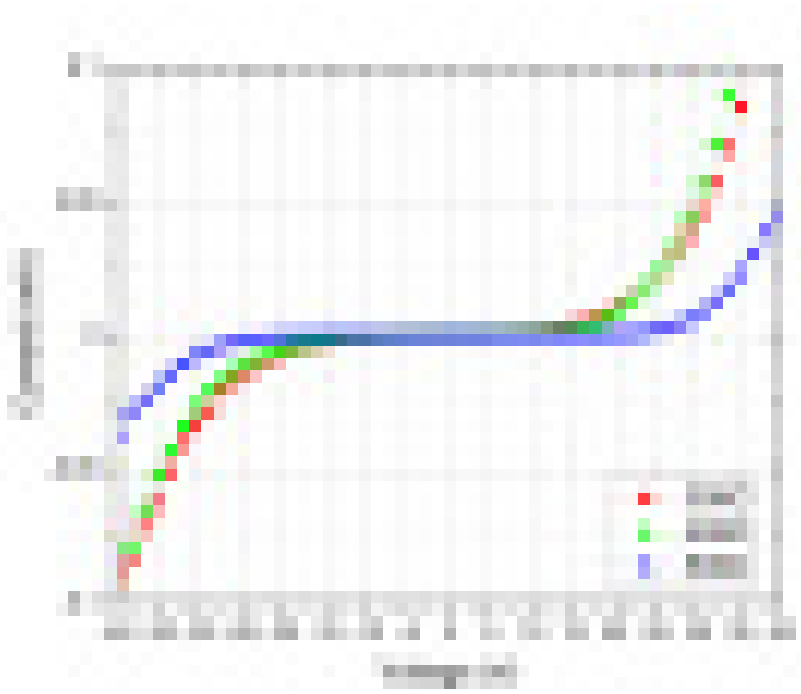


(A)

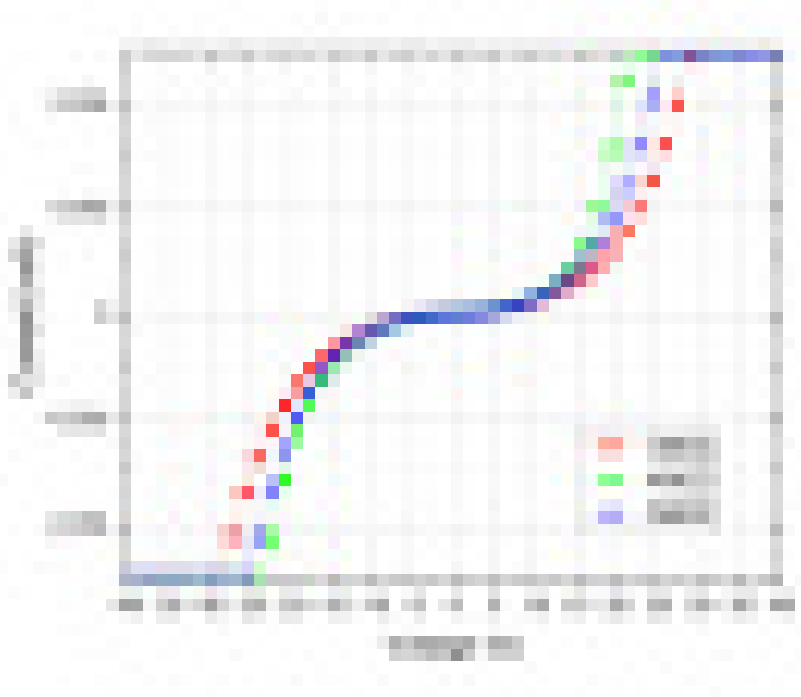


(B)

Figure 6.5: Example IV measurements from Ti/Al contacts on n-type (A) n-type Sn and (B) unintentionally doped (−201) β-Ga_2O_3



(A)



(B)

Figure 6.6: Example IV measurements from TiAu contacts on n-type (A) n-type Sn and (B) unintentionally doped (−201) β-Ga_2O_3

Conclusion on the Initial Ohmic contact

The initial development cycle provided insights into the metallisation processes and highlighted several critical considerations for subsequent cycles. Additionally, findings from Chapter 4 offered valuable guidance for refining the current approach.

This was the impracticality of cleaving β-Ga_2O_3 against the cleave plane, indicating that samples should be diced into 10 mm die before cleaving to appropriate dimensions. This cycle also underscored the need for a dedicated mask designed for 10 mm die and a compatible fixture on the mask aligner to securely hold smaller samples during photolithography.

Another critical issue identified was the lack of carrier concentration data for the β-Ga_2O_3 samples. With undetermined doping levels and a likely high degree of lattice mismatch between β-Ga_2O_3 and Si causing issues. In fact, to mitigate lattice mismatch between β-Ga_2O_3, Si, and SiC, Al_2O_3 can be used as an interlayer to help adhesion and lattice mismatching [508] [376] [509] [510]. These challenges indicate that the current samples may not be suitable for developing reliable ohmic contacts. To address this, β-Ga_2O_3 which is known to be highly doped and in bulk form, to avoid growth-related issues, will be used in the next cycle to improve the likelihood of achieving ohmic behaviour. Although bulk β-Ga_2O_3 introduces certain challenges, which will be explored in later sections, it is expected to provide an adequate basis for initial contact validation.

Due to these limitations, including the lack of an appropriate mask, uncertainties around the photoresist, and the undefined carrier concentration, it was decided to discontinue the ohmic development on these heterostructures temporarily. Moving forward, a new photoresist will be used, necessitating a new protocol, and a mask tailored for 10 mm die will be designed to allow for CV measurements if Schottky behaviour is observed. A precise determination of the carrier concentration will confirm the ability to achieve ohmic contacts or explain why it was not possible.

These adjustments are intended to establish a robust foundation for achieving reliable ohmic contacts on β-Ga_2O_3, addressing the limitations encountered during the initial development cycle and improving reproducibility in subsequent experiments. Further details regarding the challenges posed by bulk β-Ga_2O_3 will be discussed in the subsequent sections, providing context for the adjustments made in the next development cycle.

6.2.2 Process Development of new lift-off process AZ LNR-003

As stated before, the photoresist AZ 51245 E was discontinued, so a new lift-off protocol using a different photoresist was needed. This would remove concerns that the out of date photoresist was a potential issue, it is also needed as the amount of AZ 51245E was dwindling as the stock was slowly being used up and not really appropriate to be used for a new development process. The replacement was AZ LNR-003, which needed a new protocol to be developed before the ohmic work could continue.

Initial Conditions

The photoresist selected to replace AZ 5214E was AZ LNR-003 by MicroChemicals, the recommended alternative lift-off photoresist. MicroChemicals provides a matrix of recommended variables and resulting photoresist profiles for AZ LNR-003 on their website [511] [512]. This matrix served as a basis for creating an initial process, which was then systematically optimized to establish a reliable protocol.

To develop this protocol, variables were optimized individually in an iterative process, while other conditions were held constant to isolate the effect of each change. This approach was crucial to prevent overwhelming variability, which could obscure the impact of individual adjustments, and mirrors the systematic optimization method described in Chapter 4. The process for solvent cleaning and adhesive agents were the same as previously used.

The following steps outline the initial conditions for the AZ LNR-003 protocol: (1) The sample was solvent-cleaned, submersion in acetone for 10 minutes, followed by IPA for 5 minutes, and then dried with an N_2 gun. (2) Adhesive agent was applied to the sample. Sample is dehydrated on a hot plate at 150°C for 10 minutes. The adhesive agent (Ti-Prime) was applied by spin coating at 4000 rpm with 1000 rpm acceleration for 30 s, followed by baking at 120°C for 120 s. (3) AZ LNR-003 was applied by spin coating at 3000 rpm with 1000 rpm acceleration for 30 s. (4) The sample was soft-baked at 120°C for 120 s. (5) The sample was then exposed to UV light, with the exposure dose varied during optimization. (6) A post-exposure bake was conducted at 110°C for 90 s. (7) Finally, development was performed in an AZ Developer:DI water solution, with varying ratios used throughout this work to refine the process.

Spin Speed Confirmation

The initial spin speed for the AZ LNR-003 photoresist was selected based on the manufacturer's data sheet [511]. Tests were conducted on Si wafers with a spin speed of 3000 rpm, which is expected to yield a film thickness of approximately 3 µm according to the technical data sheet (Figure 6.7) [511].

To confirm this, ellipsometry measurements were performed on the samples, with the results shown in Table 6.1. A visual thickness map of the sample is available in Figure C.7 in Appendix C.3.

Parameter	Average	Min.	Max.	Std. Dev.
MSE	48.682	43.818	223.38	18.635
Thickness Å	30348.54	18565.21	30855.95	1249.29
A	1.6085	1.5886	2.3356	0.0767
B	0.0104	0.0095	0.0131	0.0003
C	0.0008	0.0006	0.002	0.0001
n of Cauchy Film 632.8 nm	1.639	1.6185	2.3808	0.0783

Table 6.1: The fitting parameters generated fitting a Cauchy model to AZ LNR 003 spun onto a Si wafer at 3000 rpm. The measurement confirmed the manufacturing protocol hence, this spin speed was used in the development of this protocol.

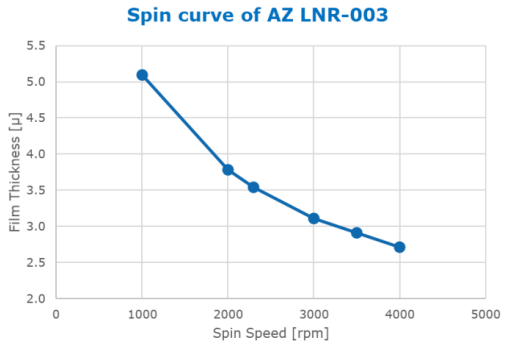


Figure 6.7: The film thickness of AZ LNR 003, after spinning at different speeds accordingly to the manufactures technical data sheet. This figure is available online at [511] and was produced by MicroChemicals.

Development Process Optimization

The data sheet from MicroChemicals recommends TMAH-based developers, so initial development protocols were based on these recommendations. However, this work aimed to transition to AZ Developer, an MIC-based developer, requiring an iterative approach to determine an appropriate development time. The switch from a TMAH-based developer was motivated by two key factors, TMAH is known to etch a-Ga_2O_3 while β-Ga_2O_3 is much more resistant [247], which could interfere with processing, and it is a known carcinogen, posing health risks during handling.

For initial testing, an exposure dose of 100 $mJ \cdot cm^{-2}$ was used with an existing development recipe to assess the development endpoint. Larger features were selected in these tests to approximate development times by eye, followed by detailed inspection under a microscope to confirm development completion. The initial development protocol was, develop in a 1:1.5 ratio of AZ Developer to DI water, rinse in a 1:3 AZ Developer to DI water solution, then rinse twice in DI water. This protocol required over 10 minutes for development, so the dilution ratio was increased to reduce development time. The modified development solution increased the concentration of AZ Developer in the first stage. Develop in a 1:1 AZ Developer to DI water solution, rinse in a 1:3 AZ Developer to DI water solution, then rinse twice in DI water. This adjustment reduced development time to 6-8 minutes. However, inconsistencies were observed, attributed to minor variations in solution mixing. To address this, the solution was further simplified by using pure AZ Developer in the development stage to minimize human error in mixing and reduce development time variability. Develop in pure AZ Developer, rinse in a 1:3 AZ Developer to DI water solution, and rinse twice in DI water.

This approach resulted in a consistent development time of approximately 50 seconds, with improved uniformity. Notably, development was observed to proceed more consistently and efficiently in larger solution volumes relative to the sample size, as illustrated in Figure 6.8.

Figure 6.8: The development set-up used in the developer optimization, this was one of the experiments made as part of the developer trial. It was found that the development in larger beakers out performed those in smaller beakers.

Exposure Dose Optimisation

The next variable optimized was the UV dose, tested in increments from 100 mJ·cm^{-2} to 275 mJ·cm^{-2} in steps of 25 mJ · cm^{-2}. These tests were performed on 2" Si wafers, each scribed with Greek letters α, θ, β, ϕ, γ, μ, ϵ, and ν to represent doses of 100, 125, 150, 175, 200, 225, 250, and 275 mJ · cm^{-2}, respectively. An unexposed and undeveloped wafer was also included for reference, shown in Figure 6.9, which revealed particles on the surface. This observation indicated that the contamination was inherent to the photoresist itself, rather than a result of the UV exposure or development process. As such, initial optimization was conducted with a contaminated bottle of photoresist, and fresh chemicals were subsequently used once the protocol was established.

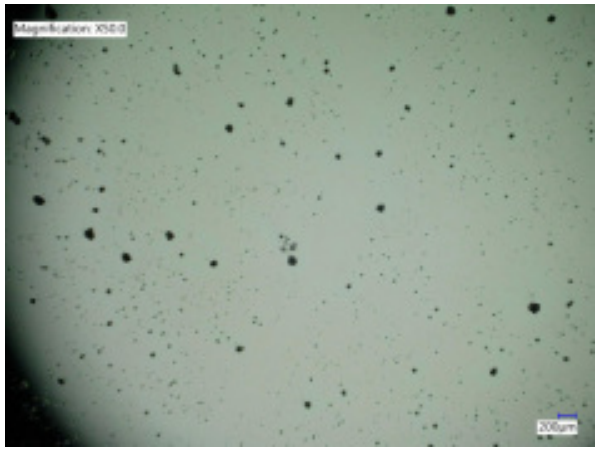


Figure 6.9: AZ LNR-003 spun on a 2" Si wafer with no dose or development. It can be seen that there were particles in the resist, this confirmed that the partials seen in the rest of the batch were unrelated to the development optimisation. This could have been a result of the pipettes that were being used at the time, as this was a simple way to control the pipettes being changed

This shows that the contamination of the other samples was not a result of optimisation but rather contamination in the photoresist. For this reason, the protocol was developed using a contaminated bottle, once it had been established, fresh chemicals were used. This is shown in Table 6.10 for reference, these wafers after the post-exposure bake are shown in Figure 6.11.

Table 6.10 summarizes the doses used, and post-exposure bake results are shown in Figure 6.11. To optimize development time, samples were cleaved after going through the preliminary protocol and then submerged in developer solution for varying durations: 50 s, 60 s, 70 s, and 80 s. Following cleaving, metal contacts of Ti/Al (20/80 nm) were deposited with the K. Lesker PVD system (see Section 3.1.6).

After metalization, samples were cleaved again, and a lift-off process was performed using D350 solution, as described in Section 3.2.8. Images of these samples are included in Appendix C.4. The UV dose range of 150-200 mJ · cm^{-2} yielded the most consistent results, and 175 mJ · cm^{-2} was selected as the optimal UV dose. In some tests, residual photoresist remained at 50 s development, so a 60 s development time was selected to ensure complete removal.

Dose mJ · cm^{-1}	100	125	150	175	200	225	250	275
Letter	α	θ	β	ϕ	γ	μ	ϵ	ν

Figure 6.10: The Greek letters and the respective UV dose in mJ · cm^{-1}, this easy reference to the reader.

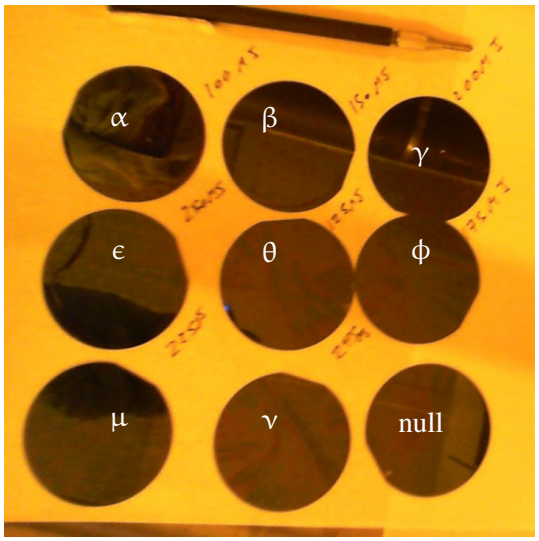


Figure 6.11: The samples used in the LNR-003 protocol development, are with different exposures as described in 6.2.2. These samples are the post-exposure bake and their relative positions with respects to their UV where α, θ, β, ϕ, γ, μ, ϵ and ν to represent 100, 125, 150, 175, 200, 225, 250 and 275 mJ · cm^{-2} respectively.

Process Development Conclusion

After testing and the refinement performed here, the final protocol was established as follows:

(1) The sample is solvent-cleaned by submersion in acetone for 10 minutes, followed by IPA for 5 minutes, and then dried with an N_2 gun. (2) The sample is dehydrated by baking at 150°C for 10 minutes. (3) Ti-prime, an adhesive agent, is spun onto the sample at 4000 rpm with 1000 rpm acceleration for 30 s, followed by baking at 120°C for 120 s. (4) AZ LNR-003 is then spin-coated at 3000 rpm with 1000 rpm acceleration for 30 s. (5) The sample is soft-baked at 120°C for 120 s. (6) UV exposure is applied at 175 mJ · cm^{-2}. (7) A post-exposure bake is conducted at 110°C for 90 s. (8) The sample is developed in pure AZ Developer for 60 s, followed by a rinse in a 1:1 AZ Developer:DI water solution, then rinsed twice in DI water, and dried with N_2 gun.

This protocol closely aligns with the recommendations in the AZ LNR-003 data sheet, which suggests a similar process for achieving a high degree of undercut. MicroChemicals' data sheet indicates a critical exposure plateau for AZ LNR-003 at doses between 150 and 200 mJ·cm^{-2}, with a target critical dimension near 6 μm [512]. Given that the data sheet recommends exposure intervals in 50 mJ $\cdot$ cm^{-2} steps, the chosen value of 175 mJ $\cdot$ cm^{-2} likely provides an optimal balance between the recommended values. The protocol presented here represents the foundation for subsequent refinements, which continues in the next section.

Change of protocol for AZ LNR-003

The transition into the new facility provided by CISM the opportunity to develop the process further was available to colleagues at CISM, so the process was further optimised and modifications to the protocol were made.

These modifications developed collaboratively with colleagues at CISM, lead to the updated protocol:

(1) The sample is solvent-cleaned by submersion in acetone for 10 minutes, followed by IPA for 5 minutes, and then dried with an N_2 gun. (2) The sample is dehydrated by baking at 150°C for 10 minutes. It should be noted that this is time is non critical, so long as the wafer is dehydrated prior to continuing. (3) Ti-prime, an adhesive agent, is spun onto the sample at 4000 rpm with 1000 rpm $\cdot$ s^{-1} acceleration for 30 s, followed by baking at 120°C for 120 s. (4) AZ LNR-003 is then spin-coated at 4000 rpm with 1000 rpm·s^{-1} acceleration for 30 s. (5) The sample is soft-baked at 120°C for 120 s. (6) UV exposure is applied at 150 mJ $\cdot$ cm^{-2}. This was changed from the previous value of 175 mJ $\cdot$ cm^{-2}, this process was optimised by the technical team in the transition from CNH to CISM. (7) A post-exposure bake is conducted at 105°C for 120 s. (8) The sample is developed in pure AZ Developer for 60 s, rinsed in a 1:1 AZ Developer:DI water solution, then rinsed twice in DI water, and dried in N_2.

These modifications represent a clear divergence from the initial work to develop the protocol, delineating between work performed by colleagues and work performed as part of this thesis.

6.2.3 Development Cycle Two

This is the second development cycle in the process to achieve ohmic contacts, this was performed after the transition to the CISM facility. This allowed the acquisition of material, β-Ga_2O_3 as well as a mask. This subsection is broken down into an introduction to this cycle, the mask design used in this cycle, the fabrication process the results and finally the conclusion to this cycle.

Introduction to Development Cycle Two

As noted at the conclusion of the first development cycle, the doping concentration was a primary concern in forming ohmic contacts and was therefore addressed in this stage. Following the relocation, the development process resumed with highly doped bulk (001) β-Ga_2O_3, acquired from Novel Crystal Technologies. The material specifications, detailed in Section 3.2.10, include a nominal doping concentration of 7×10^{18} cm^{-3}, though this has not been independently verified in this work.

The wafer was diced into 10 mm die, this was performed by DISCO HI-TEC EUROPE GmbH, see their website [513]. Care was taken when removing the die, to avoid damage. Since preliminary results showed potential with certain metal contacts, it was determined that these contacts merited further investigation. Both Ti/Au and Ti/Al have previously demonstrated ohmic behaviour, as discussed in Chapter 2.

Additionally, Ti/Ag was selected due to Ag's pseudo-ohmic behaviour and Ti's suitability as a contact layer, as previously demonstrated. Ag's work function is closer to that of β-Ga_2O_3, it was considered a potentially effective capping layer when combined with Ti, with the expectation that this configuration could enhance the contact properties. Although further studies are required to understand the specific interactions between Ti and Ag, this combination was included for its promising characteristics observed in previous works. Based on findings by Tetzner et al. [284], which reported that Ti/W alloys form ohmic contacts by Ti coalescence at the interface with W as a capping layer, this cycle also explored Ti/W as separate layers to investigate the potential for independent ohmic behaviour.

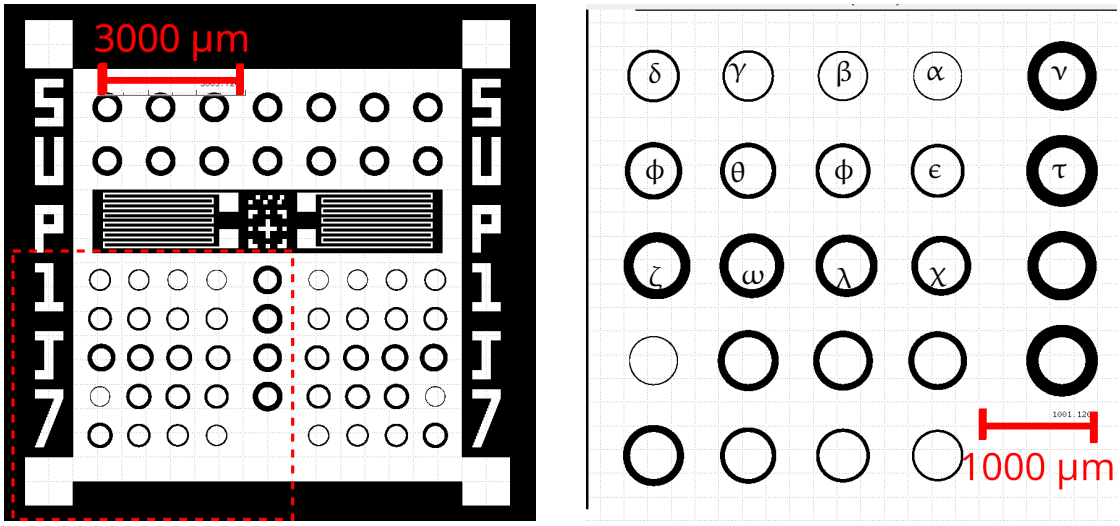
CTLM Mask Design

As established in the first development cycle, a specific mask was required to process 10 mm die, in order to characterise the contacts formed. The mask was designed to form CTLM structures for this second development cycle to accurate measure contact resistance and sheet resistance. This was also designed so if Schottky contacts were formed CV measurements could be taken in a similar matter to those used in Chapter 5 This mask design can be seen in Figure 6.12.

The mask design incorporated spacings ranging from 5 to 100 μm, a deliberate choice due to uncertainties about the fabrication limits for feature sizes during the transition to the new lab. By using a broad range of spacings, it was possible to adapt the process based on achievable resolutions in order to avoid further optimisation. CTLM patterns are more accurate with smaller spacing so ideally a range so as spacings of 5 μm were possible then a spacing range going from 4-20 μm would have been more appropriate in hindsight.

For reliable CTLM measurements, the inner contact needed to be sufficiently large relative to the spacing between contacts. Therefore, a 200 µm diameter was chosen for the internal contact, a size that has been shown to be effective and is commonly used in similar CTLM applications [474] [514] [282]. This dimension also facilitates easier contact and measurement. The inner contact pattern was mirrored to enable repeat measurements when required.

Additionally, the mask was designed with both positive and negative layouts, along with alignment marks, to accommodate potential future use of a bi-layer photoresist protocol.



(A) (B)

Figure 6.12: Mask design used in the development of ohmic contacts on 10 mm samples. (A) shows the full subsection mask layout designed for 10 mm samples, with a 2 mm edge exclusion zone to account for edge beads and handling damage. Both "positive" and "negative" polarities were included to support different lithography processes. (B) highlights the specific region of the mask containing the CTLM test structures. The CTLM contacts are identified by their spacing (d), with each contact having a radius of 200 µm. This mask was used with a 10 mm chuck on the mask aligner for precise alignment and processing. The spaceing of the contacts are 5, 10, 15, 20, 25, 30, 35, 40, 50, 60, 70, 80, 90 and 100 µm marked as $\alpha, \beta\gamma, \delta, \epsilon, \phi, \theta, \psi, \chi, \lambda, \omega, \zeta, \nu$ and τ.

Fabrication Process

The fabrication followed the protocol outlined in Section 6.2.2, utilising a negative resist for a metal lift-off process.

(1) The samples were solvent-cleaned by submersion in acetone for 10 minutes, followed by IPA for 5 minutes, and then dried with a N_2 gun. (2) The samples were dehydrated by baking at 150°C for 10 minutes. (3) Ti-prime was spin-coated onto the samples at 4000 rpm with 1000 rpm acceleration for 20 s, followed by baking at 120°C for 120 s. (4) AZ LNR-003 was spin-coated onto the samples at 4000 rpm with 1000 rpm acceleration for 30 s, followed by baking at 120°C for 120 s. (5) The

samples were exposed to UV does of 150 mJ $\cdot$ cm^{-2} in the mask aligner, then post exposure, baked at 105°C for 120 s. (6) The patterned photoresist was developed in pure AZ Developer for 60 s, rinsed in a 1:1 AZ Developer:DI water solution for 10 s, then rinsed twice in DI water, and dried with N_2. Then, metal was deposited with two different tools, the Moorefield PVD and Moorefield Evaporation systems, discussed in Sections 3.1.6, 3.1.6. Ti/Al and Ti/W were deposited using Moorefield PVD sputter shown in Figure 3.11, Ti/Ag and Ti/Au were deposited using a Moorefield electron evaporation shown in Figure 3.12. All these metal depositions were in a ratio of 20/80 nm.

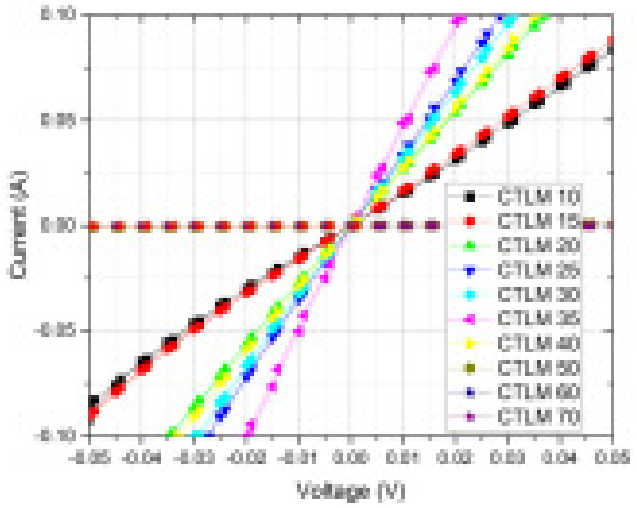
The final stage of the fabrication process was to strip the remaining photoresist and lift off the excess metal in D350. Metal deposited from the sputter system required additional sonicating in D350. The process flow can be seen in Section C.1, this is a generic process flow for a lift-off process.

Following metallisation, the Ti/Al, Ti/Ag, and Ti/Au contacts were annealed at 400°C for 2 minutes in a nitrogen atmosphere. The annealing temperature of 400°C was chosen as most ohmic contacts to β-Ga_2O_3 are annealed between 400-500°C, the lower end of this was used as the starting annealing point. This annealing process was performed using the AnnealSYS AS Master RTP system, which utilised a graphite-coated SiC susceptor, as described in the corresponding section. The annealing in a susceptor means that the heating is more uniform, and higher levels of certainty of the temperature profile exposed to the sample. This is because the susceptor is a constant material which is being heated by the lamps, which is being measured in consistent manor by the thermocouples and pyrometer measurements. This removes any need to calibrate for a new material. This is ignoring the physical constricts, that the system is not designed for 10 mm samples to be annealed individually, meaning that even if it was possible to balance the sample on their thermocouple, there is no guarantee that after pumped down to a vacuum and a gases introduced it would remain in contact, limiting consistently.

6.2.4 Results And Discussion on Second Development Cycle

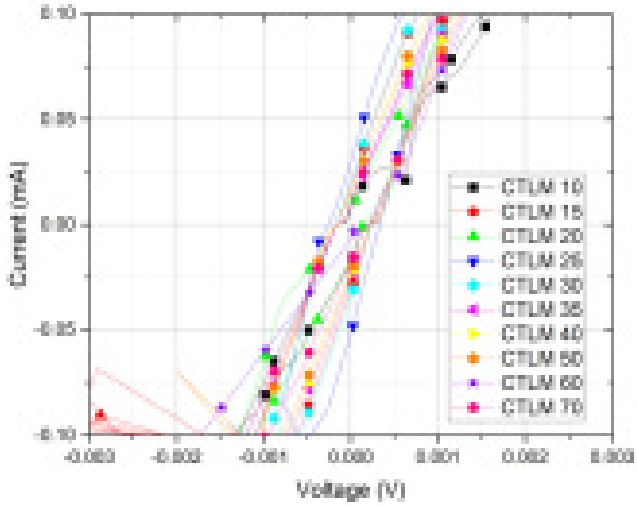
After annealing Ti/Al, Ti/Au and Ti/Ag at 400°C for two minutes, in a N_2 atmosphere, IV measurements were performed on Ti/W, Ti/Al, Ti/Au and Ti/Ag with the Keithly 4200A-SCS Parameter Analyser 3.5. To explain why Ti/W sample was not annealed, it appeared ohmic as deposited, the other contacts required annealing to achieve an ohmic contact. After annealing all four contacts exhibited ohmic behaviour, however, IV measurements for the different samples reached compliance at different voltages indicating that the different capping layers were affecting the conductivity, these can be seen in Figure 6.13. The IV measurements were performed between ±1 V, with a compliance at 5 mA, on CTLM test structures described in Section 3.3. The resistance was calculated from a linear fit to the IV plot, and the values averaged with the standard error calculated. Subsequently, the necessary CTLM corrections required from the change of TLM to CTLM were applied, discussed in Section 3.3. The inner fitting to the CTLM can be seen in Figure C.32, and the tabulated results can be seen in Table C.1.

Ti/Al



(A)

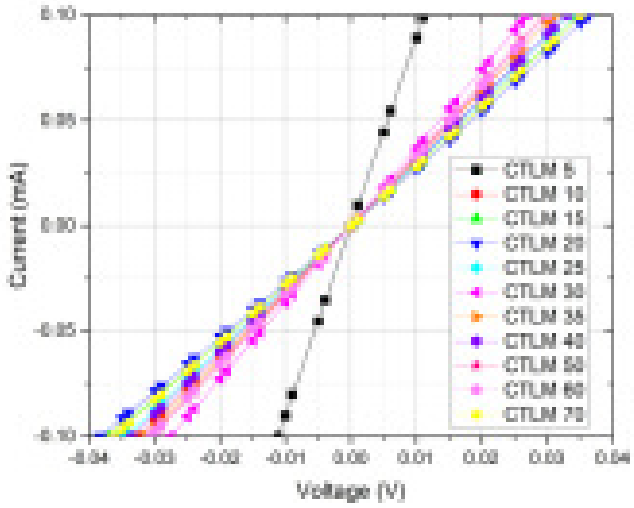
Ti/W



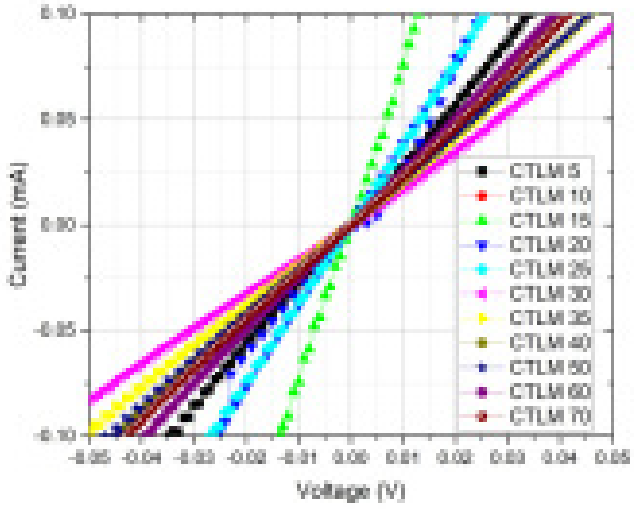
(B)

Figure 6.13: The IV plots on bulk (001) Ga_2O_3 the metal contacts, (A) Al/Ti after annealing at 400°C, (B) W/Ti as deposited, (C) Ag/Ti after annealing at 400°C and (D) Au/Ti after annealing at 400°C. These IV measurements were on CTLM. It can be seen that the samples appear to have an ohmic nature as the IV results appear to be linear. As expected the resistance of these contacts increased with increased CTLM spacing. The compliance was set to 0.1 mA, hence the scale and limited voltage range. These all appear to be linear with the increased spacing increase the resistance of each contact. This linear nature was unexpected on bulk material, as the current spreading is not limited. The only difference between these is the geometry of the structures.

Ti/Ag



(C)
Ti/Au



(D)

Figure 6.13: The IV plots on bulk (001) Ga_2O_3 the metal contacts, (A) Al/Ti after annealing at 400°C, (B) W/Ti as deposited, (C) Ag/Ti after annealing at 400°C and (D) Au/Ti after annealing at 400°C. These IV measurements were on CTLM. It can be seen that the samples appear to have an ohmic nature as the IV results appear to be linear. As expected the resistance of these contacts increased with increased CTLM spacing. The compliance was set to 0.1 mA, hence the scale and limited voltage range. These all appear to be linear with the increased spacing increase the resistance of each contact. This linear nature was unexpected on bulk material, as the current spreading is not limited. The only difference between these is the geometry of the structures.

These measurements were performed on bulk (001) β-Ga_2O_3, and while this does not satisfy the thin film condition required for CTLM measurements,

$$\rho_C > 0.2 R_{Sh} t^2, \tag{6.1}$$

the results were clearly ohmic and while it is expected that as the spacing increases, the CTLM correction fit becomes more erroneous, as the current path goes through more of the bulk material. However, this correction was still performed, as when spacing, less of the current passes through the bulk and so the deviation is not as impactful. Hence it was used as an approximation in this work.

Which is required for the TLM and, therefore, the CTLM test structures as stated in Chapter 3. The effect of this is that the current paths are not restricted, hence, resistance should be reduced as the current passes through more of the bulk. This is why CTLM theory does not work on bulk material. This is believed to be a reason why these values are erroneous, however, they still had the CTLM adjustment and an attempt to fit to them was made. These can be seen in Figure C.32, and the fitting parameters and calculated values can be seen in Table C.1. It is clear that these are invalid both from the values acquired and the underlying theory. Therefore they are included as the contact resistance did show an indication, however, the values and treatment should not be mistaken for being valid.

While Ti/W is erroneous with a negative gradient, even within the significant error associated with it, according to this, there is no transfer length. While Ti/Au and Ti/Al have transfer lengths, these are of the order of 231 and 186 μm respectively. This transfer length and low or negative sheet resistance seem high. However, the contact resistance calculated for Ti/Au and Ti/Ag were of the order of 10^{-5} $\Omega \cdot cm^2$, this is of the standard order of magnitude. Ti/Au contacts normally of the order 10^{-4} $\Omega \cdot cm^2$, Interestingly in work performed by Tetzner et al. [284], where TiW contacts were used, found ρ_C to be 5×10^{-5} going to 10^{-5} $\Omega \cdot cm^2$ after annealing at 700°C. In that work CTLMs with contact diameter as 100 μm, CTLM spacing of 4, 8, 12, 16, 20, and 24 μm, thickness of 30 nm and doping 10^{19} cm^{-3}. This indicates that even though there are issues with this, as can be seen from the unphysical sheet resistance, gradient, and transfer lengths, the specific contact resistances are remarkably close to the literature. However, the errors associated with these indicate that the CTLM measurements are not completely erroneous, however, these measurements have underlying issues. Lee et al. [515] found that increasing spacing increases the effective thickness of the current path, in the range 9.65-4.78 $\Omega \cdot \square$ between spacing 20-50 μm.

Berger et al. [516] performed simulations into SiC CTLM measurements, contact resistivity and thickness. By holding the contact resistance constant with varying thickness, they found that it would overestimate the contact resistance for thickness over 10 μm, the authors believe the same effect is occurring here. These are often after pretreatments, such as acid cleans or implantation, in other work without such treatments ρ_C on the order of 10^{-4} $\Omega \cdot cm^2$ have been demonstrated, 2.7 and 5 $\times 10^{-4}$ $\Omega \cdot cm^2$ [517] and [518]. Lee et al on bulk wide spacing found ρ_C 5×10^{-3} $\Omega \cdot cm^2$. This explains the high errors found here, if the real equivalent thickness of the channel is changing then it would be expected that the TLM approximation does not hold. Hence, the CTLM contacts are going out of agreement as the spacing increases.

Conclusion To the Second Development Cycle

To conclude, the development of ohmic contacts was successfully demonstrated through a series of trials using various metal contacts on highly doped bulk (001) β-Ga_2O_3. All four contacts, Ti/Au, Ti/Al, Ti/Ag and Ti/W all formed ohmic contacts. Metal stacks such as Ti/Au and Ti/Al, which are widely reported in the literature, were evaluated alongside Ti/Ag, where Ag has previously reported as pseudo-ohmic behaviour, and Ti/W, an unreported contact configuration near identical to TiW alloy which has formed a ohmic contact. This work established that Ti/Ag, following an annealing step, and Ti/W, as deposited, form ohmic contacts to (001) β-Ga_2O_3. The absence of an annealing requirement for Ti/W is of interest and is different from TiW which required annealing,

While the development cycle successfully demonstrated the formation of ohmic contacts, due to the substrates used which possibly introduce errors when used with CTLM measurements. However, it is clear that the contacts were ohmic, low resistance contacts to (001) β-Ga_2O_3 were achieved. The CTLM corrections do introduce an error as the measurements were performed on bulk material rather than thin film material, which means that the current can flow through the volume rather then being confined to the thin layer required for CTLM. This leads to a lowered measured resistance compared to the thin film.

In this study, Ti/Ag and Ti/W exhibited higher conductivity than Ti/Au and Ti/Al, as evidenced by consistently reaching compliance voltages before the other contacts. The resistance contribution from the β-Ga_2O_3 substrate should theoretically remain constant for contacts with identical spacing. Assuming the substrate is uniformly doped, the expected difference in total resistance between the CTLM spacings of the same size would be due to the metal-β-Ga_2O_3 contacts. In reality there will be slight variations which can occur due to factors such as discrepancies in spacing accuracy, differences in photoresist development time, lift-off resolution, and non-uniformities in the doping (carrier concentration) of the sample. While simulations have been performed by Lee et al. [514] in an attempt to match CTLM measurements to Slivarco (TCAD) models. It was found to grow in error as the material thickness was increased. Without knowing the exact dimensions of the bulk material and carrier concentration, therefore an attempt to demonstrate this with simulation would likely be invalid.

In the next iteration of this work, it is essential to address the errors, previously discussed. Therefore the CTLM structures should be fabricated on thin films of highly doped β-Ga_2O_3, on some insulating or n^- substrate. The Ti/W appeared to have more noise compared to other contacts, the high conductivity without the need for annealing means that it should be considered going forward. The ohmic behaviour of Ti/W is unsurprising, as it closely resembles TiW, where Ti reacts with the β-Ga_2O_3. Ti/Ag and Ti/W both exhibited higher conductivity than Ti/Al and Ti/Au, also warrants further exploration. Unlike Ti/W, Ti/Ag did not require sonication during the lift-off process and has not previously been reported as an ohmic contact. These contacts should be benchmarked against Ti/Au, as it remains the most commonly used ohmic contact configuration.

6.2.5 Development Cycle Three

This marks the third and final development cycle in this work to achieve and characterise ohmic contacts on β-Ga_2O_3. In the second development cycle, ohmic contacts were successfully achieved, in this cycle the aim was to build upon this. So the CTLM devices are appropriate fabricating ohmic contacts on thin film material. This cycle is organised as follows: an introduction, the photolithography process employed, an additional cleaning stage, the fabrication process, the results, and a conclusion to the third development cycle.

Introduction to the Third Development Cycle

The third development cycle aimed to address the limitations identified during the second cycle, and utilising metallisation methods which successfully formed ohmic contacts to β-Ga_2O_3 in the previous iteration. This cycle used a similar material, incorporating an epitaxial layer with specifications akin to those employed in the initial stages of this study.

It is anticipated that Schottky contacts, rather than ohmic contacts, may form due to the expected carrier concentration in the epilayer being considerably lower. As similar material failed to form ohmic contacts in cycle one and the lower concentration from the manufacture it is predicted that the doping is insufficient for ohmic behaviour. Nonetheless, the metallisation approaches and CTLM test structures established in the second cycle remain applicable, and the thin-film nature of the epilayer satisfies the prerequisites for CTLM measurements.

Given the challenges encountered in the initial cycle attempting to form contacts on β-Ga_2O_3/Si, a range of annealing conditions was explored in this cycle to accommodate potential variations. This time individual anneals rather than consecutive annealing. Additionally, findings from the second cycle revealed that Ag and W capping layers demonstrated lower resistance than Au. Due to the availability of materials and avoiding consecutive annealing, Ti/Ag was selected for this development cycle and compared against Ti/Au, with the plan to compare contact resistivity if ohmic contacts were

formed. Ti/Ag is deposited with e-beam evaporation, in cycle two this did not require a sonic bath during the lift-off process, which was one reason Ti/Ag was chosen over Ti/W. It is worth noting that Ti/Ag also provided an IV measurement which had less noise than Ti/W.

A critical enhancement in this cycle was the introduction of a plasma cleaning (descum) step to remove residual photoresist from patterned samples. This process is expected to improve the likelihood of forming ohmic contacts amy introduce dangling bonds. While ideally, substrates such as semi-insulating β-Ga_2O_3 with a thin n^+ layer would be preferred, these were not available within the project's time frame. Pre-existing epitaxial material, β-Ga_2O_3/4H-SiC, similar to that used in the initial cycle was used because the thin film is needed CTLM measurements. This is despite limited information about their doping concentrations, which was a concern found in the initial work.

A refined photolithography protocol was adopted to improve the resolution of the CTLM structures at smaller spacings.

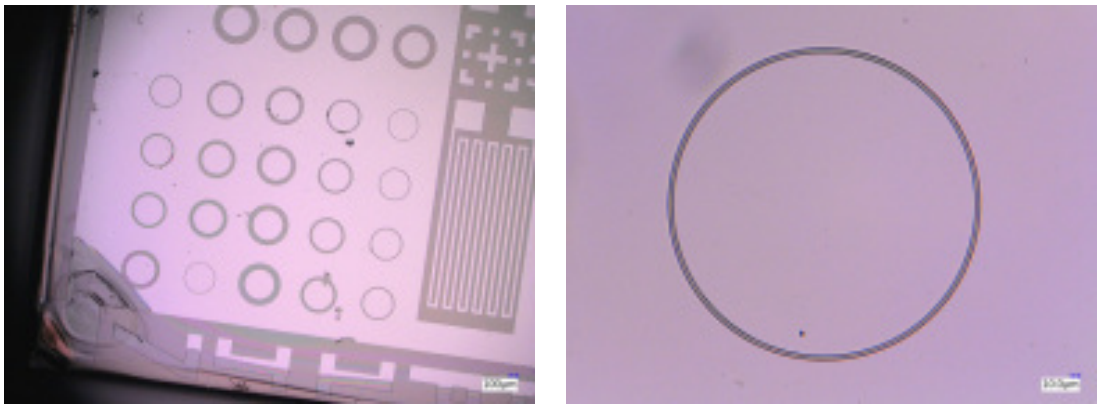
Bi-Layer Protocol

A bi-layer process was used in this cycle, this was developed in CISM and transferred this process due to it previously being used to achieve features down to a micron. It was used to improve the resolution of the features being developed.

The process perform was: (1) The sample was pre-baked at 120°C for 120 s, this is to dehydrate the sample. (2) after this Ti prime, an adhesive agent was spun at 4000 rpm, 1000 acceleration for 20 s. (3) After this the sample was baked again at 120°C for 120 s. This process used a photoresist LOR B, a positive photoresist, which is used as an under layer in the bi-layer protocol. (4) This is spun at 3000 rpm, 1000 acceleration for 30 s. (5) then baked at 180°C for 180 s. As this is a positive photoresist, which is the under layer, the etch rate of the LOR B is determined by heat treatments rather then UV. (6) After the baking stage then AZ 1512 HB was spun onto the surface, this was at 4000 rpm, 1000 acceleration for 30 s. (7) then was then baked at 100°C for 90 s.

As mentioned in the materials section, however, it should also be noted that AZ 1512 HB is a positive photoresist. After both the LOR B and AZ 1512 HB were spun onto the surface, the process to remove edge bead as performed in previous sections was used, a cotton swab was used to try to remove and attempt to mitigate the edge bead of the layers of photoresist. Then to pattern the sample the sample is placed into the a mask aligner and is exposed to 70 $mJ \cdot cm^{-2}$. This was then developed in solutions of 1:1 AZ Developer to DI water, this was for 55 s, then rinse in 1:2 AZ Developer to DI water for 10 s. Then the sample was rinsed twice in DI water.

After this, the sample was cleaned with a plasma asher, this was 150 W, 5 sccm of O, for 60 s, this process was determined in Section 6.2.5. An 10 mm die was used to confirm that the development, this can be seen in Figure 6.14, the edge bead can be seen in this Figure indicating this is an issue for this protocol.



(A) (B)

Figure 6.14: A 10 mm Si die which was used to test the bi-layer protocol, this was using the CTLM mask which was used in the second development cycle. Where sub-figure (A) is the CTLM patterns and (B) is the smallest feature size resolved.

Plasma Asher Etch Rate

The PE-50 plasma asher was used to clean and descum the sample, with the added potential to roughen the surface to create dangling bonds. Before this could be performed it was important to determine the etch rate of the plasma asher on the top layer photoresist, this layer is AZ 1512 HB. This was performed by spinning the top layer photoresist onto four 10 mm die of Si, this was then measured on the ellipsometer, in order to calculate the deposited thickness of the layer. Then the sample was exposed to the plasma asher, for set times at 150 W with 5 sccm of oxygen, after which the samples where remeasured on the ellipsometer.

The optical parameters for the Cauchy model were taken from the technical data sheet, then the thickness was estimated based off the spin speed according to the technical data sheet these are shown in Table 6.2 and Figure 6.15.

Parameters	Value
Cauchy A	1.5996
Cauchy B	0.013498
Cauchy B	0.000194
n	1.63447
k	0

Table 6.2: The Cauchy model parameters which were taken from the technical data sheet in order to model and fit to the photoresist AZ 1512 HB, provided by MicroChemicals.

These were plotted to get an approximate etch rate, however, it should be clear that the difference in the samples was similar to the difference in the etching. This is likely because the samples were small, so were affected by the relatively large edge bead, which can be seen in the Si example here, after it was developed. The rates were calculated for different times and the data points and rate can be seen in Figure 6.16. The etch rate was found to be 1.7 ± 0.1 nm $\cdot$ s^{-1}. From this it was decided that a time of 60 s would be safe to use as a cleaning stage for this photoresist.

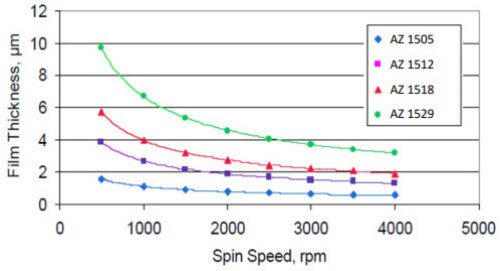


Figure 6.15: The thickness of films of spun AZ 1500 series photoresist at different spin speeds according to the technical data sheet from the manufacture MicroChemicals [468]. The spin speed used in this work matches the approximate thickness which is given by this plot, below 2 µm. The thickness is predominately determined by the spin speed rather then duration, it is not known how long these were spun for, however, it is likely in the order of 60 s.

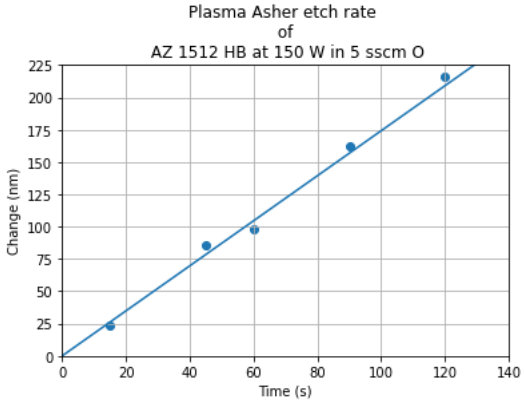


Figure 6.16: The plasma asher etch rate of AZ 1512 HB, at 150 W, in 5 sccm of O. This was using the PE-50 Plasma asher sold by Plasma Etch tool. This was on 10 mm Si die.

The approach used in this has two issues. The first is that spinning on a 10 mm die would create a large, effective edge bead and non-uniformity. This non-uniformity means that the measured photoresist thickness before and after plasma treatment may be inaccurate between measurements. The other issue is when applying this information to real usage When really using the photoresist protocol, it is devoted, so even if the photoresist, which is supposed to remain, still suffers from dark erosion, lowering the thickness. Both the dark erosions and reduction due to ashing should be measured and accounted for when considering whether the plasma clean is appropriate, as the combined total reduction in the photoresist is vital to ensure that the pattern remains intact.

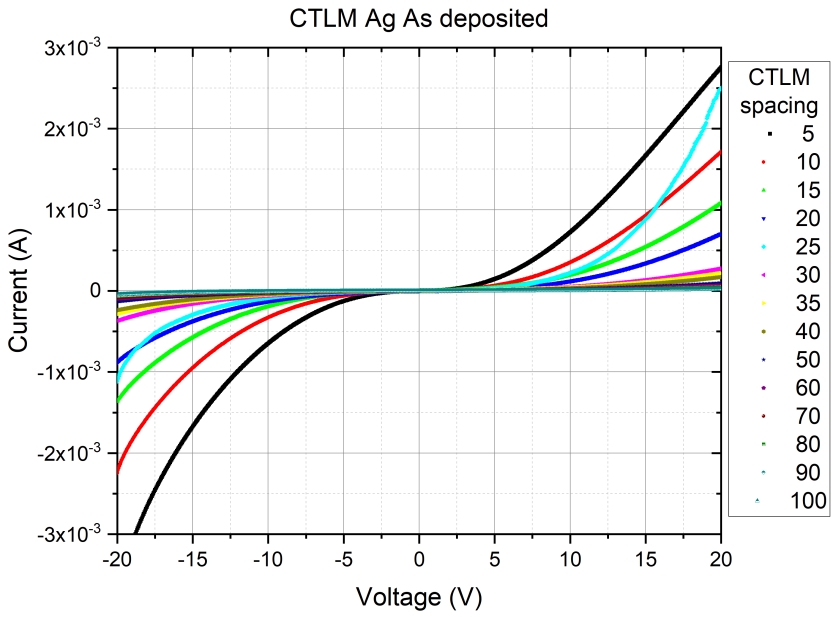
Processing

0.5 μm (-201) β-Ga_2O_3 epi-layer grown on 6H-SiC was used, these were purchased from Kymer with the same specifications on the epi-layer as in the initial development stage. It was not known if the SiC was doped. According to the manufacture the epi-layer was doped mid 10^{18} cm^{-3}, the substrates in this case were nominally n-type, however, not specifically doped. The samples were first cleaned with a solvent clean, 10 minutes of acetone, 10 minutes of IPA, then dried with a N_2 gun. Following this, the bilayer protocol outlined previously was used to pattern the die, post development these samples were then cleaned in an oxygen plasma, again outlined earlier. These samples then had metal deposited onto them using the Moorfeild evaporator system, this was used to deposit (20/80) nm of Ti/Au and Ti/AG. This was then lifted-off in D350, in this case some of these samples required sonication in order to lift off the metal, examples can be seen in Figure 6.19. Post-metal deposition, the samples were annealed using the Annealsys AS Master RTP system at three temperatures: 300°C, 400°C, and 500°C. Each annealing step was performed for 2 minutes in a N_2 atmosphere. For both Ti/Au and Ti/Ag, this left three annealed samples and one as-deposited sample for subsequent characterisation.

Results, Current Voltage

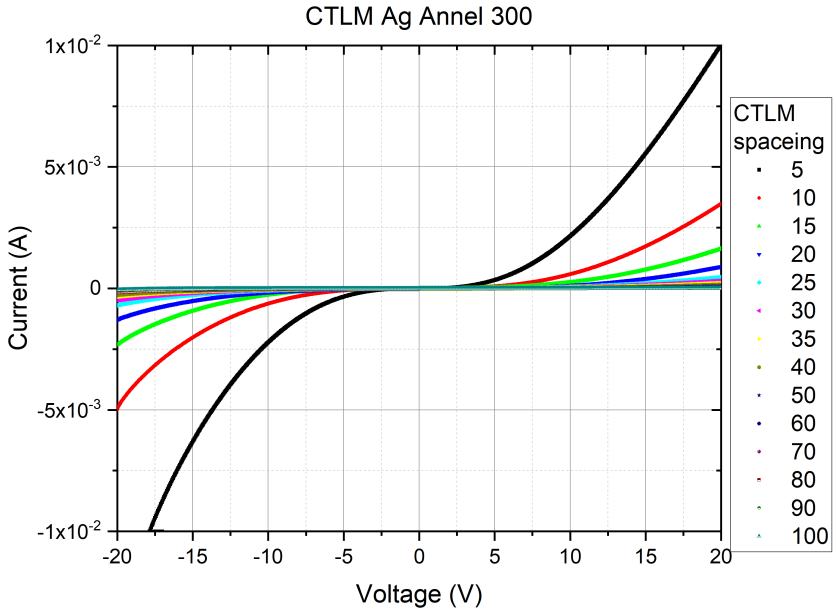
The IV measurements for the CTLM structures with different annealing conditions are shown in Figures 6.17 and 6.18. The plots exhibit non-linear behaviour, indicating that the contacts are not ohmic or, at best, exhibit very poor ohmic characteristics.

As Deposited



(A)

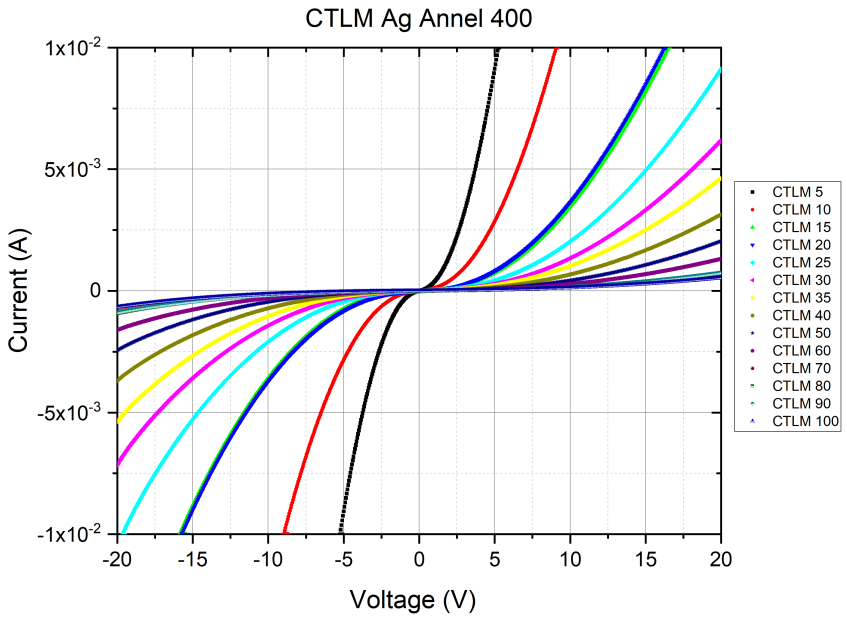
Annealing 300°C



(B)

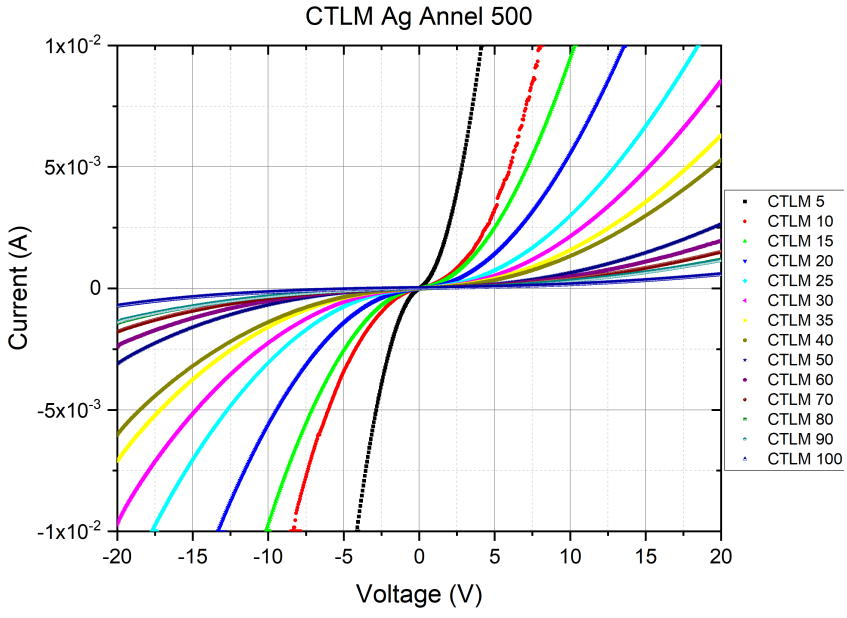
Figure 6.17: IV plots of the different CTLM structures for Ti/Ag, (A) as deposited, (B) after annealing at 100°C, (C) 200°C and (D) 500°C.

400°C



(C)

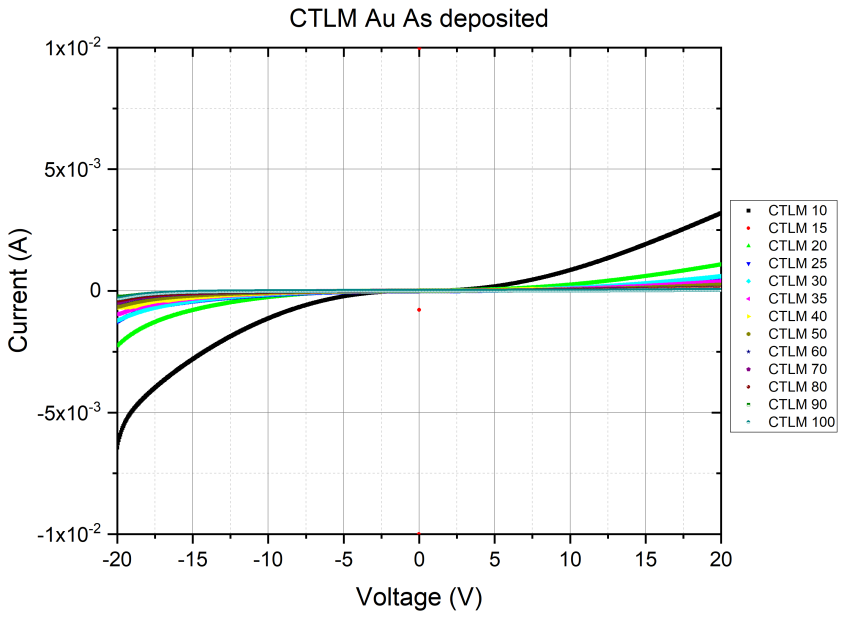
500°C



(D)

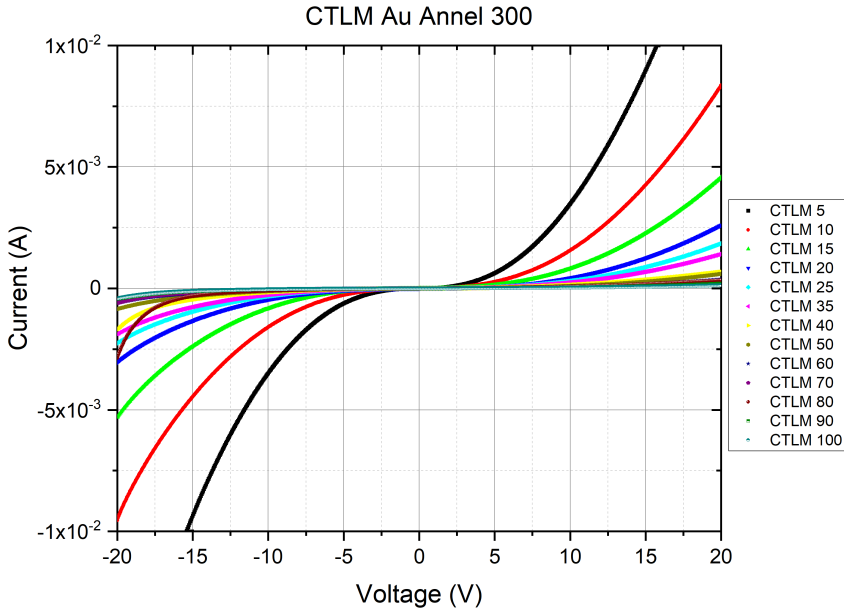
Figure 6.17: IV plots of the different CTLM structures for Ti/Ag, (A) as deposited, (B) after annealing at 100°C, (C) 200°C and (D) 500°C.

As deposited



(A)

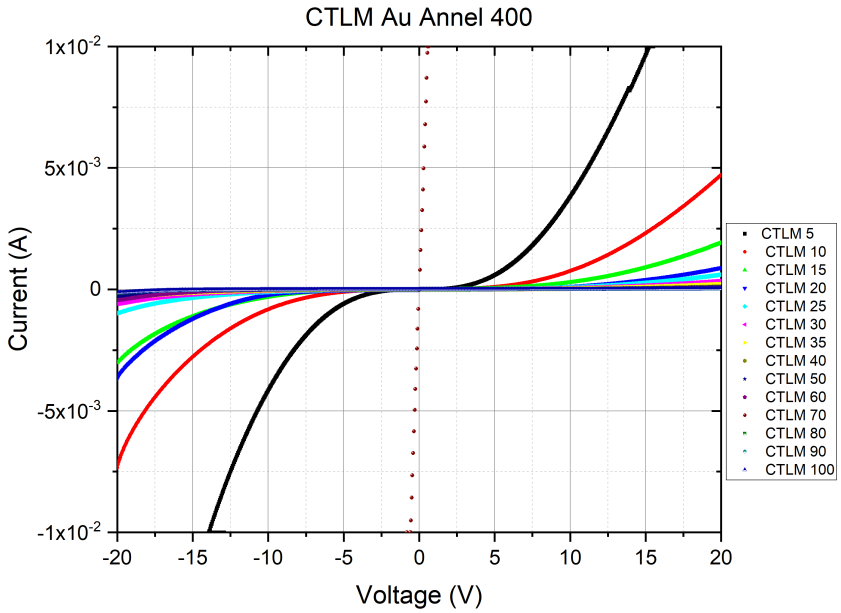
300°C



(B)

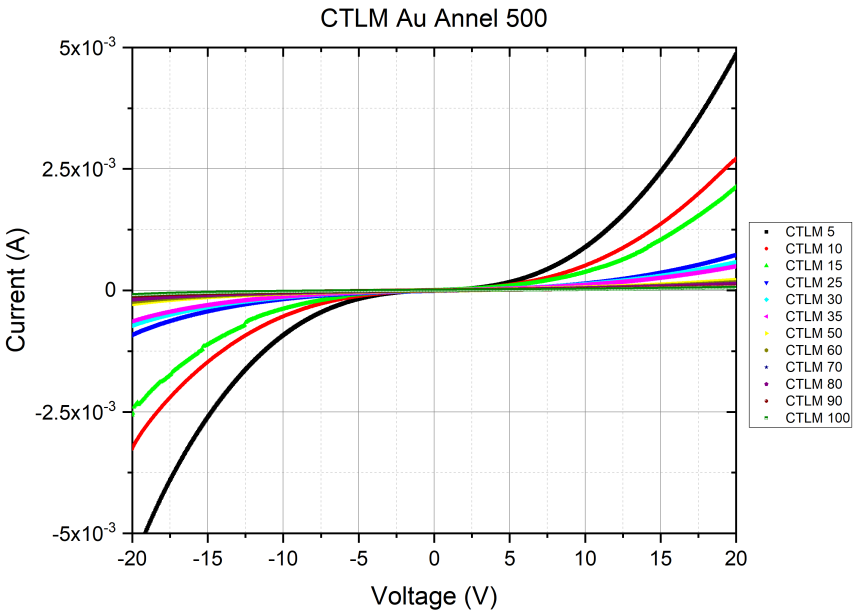
Figure 6.18: IV plots of the different CTLM structures for Ti/Au, (A) as deposited, (B) after annealing at 100°C, (C) 200°C and (D) 500°C.

400°C



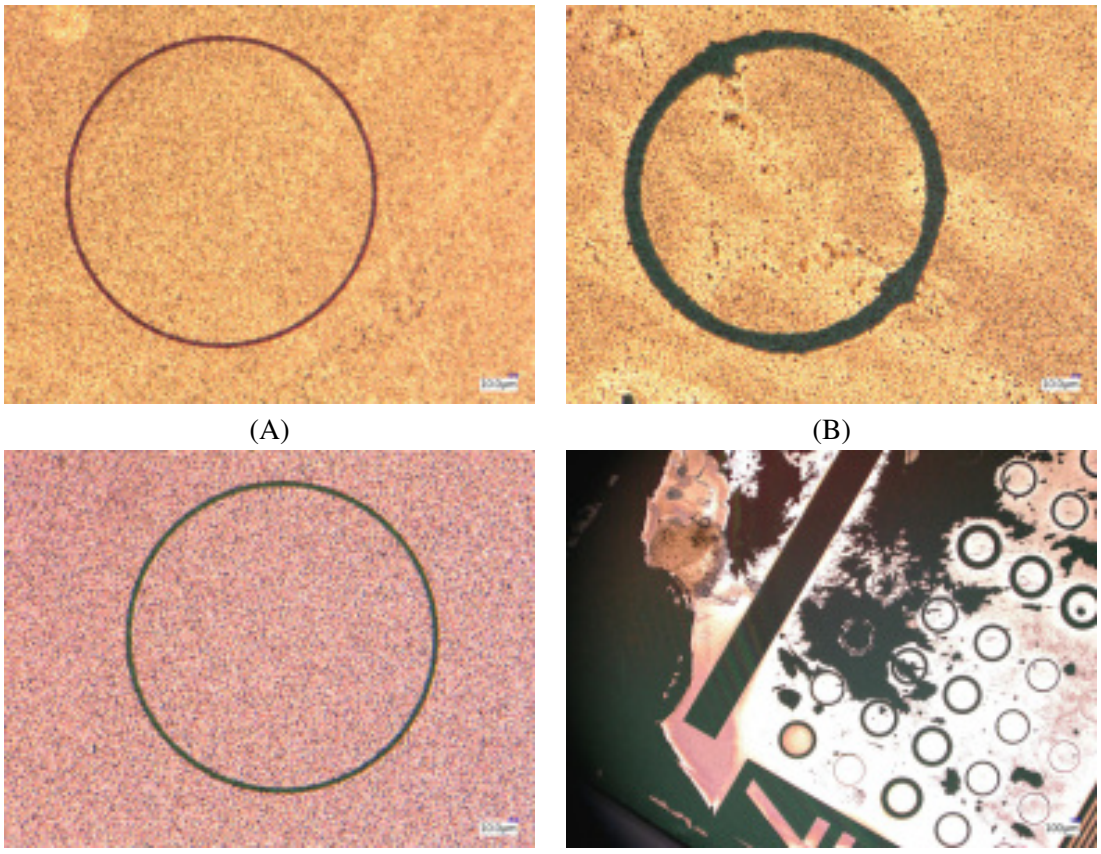
(C)

500°C



(D)

Figure 6.18: IV plots of the different CTLM structures for Ti/Au, (A) as deposited, (B) after annealing at 100°C, (C) 200°C and (D) 500°C.



(A) (B)

(C) (D)

Figure 6.19: Examples of the samples post lift off (A) and (B) Ti/Au and (C) and (D) Ti/Ag, where (A) and (C) are examples where the sample lifted off well, and (B) and (D) are examples were it did not. This was believed to be due to the edge bead which seems to be very impactful with this protocol and with the curved samples which were patterned and processed.

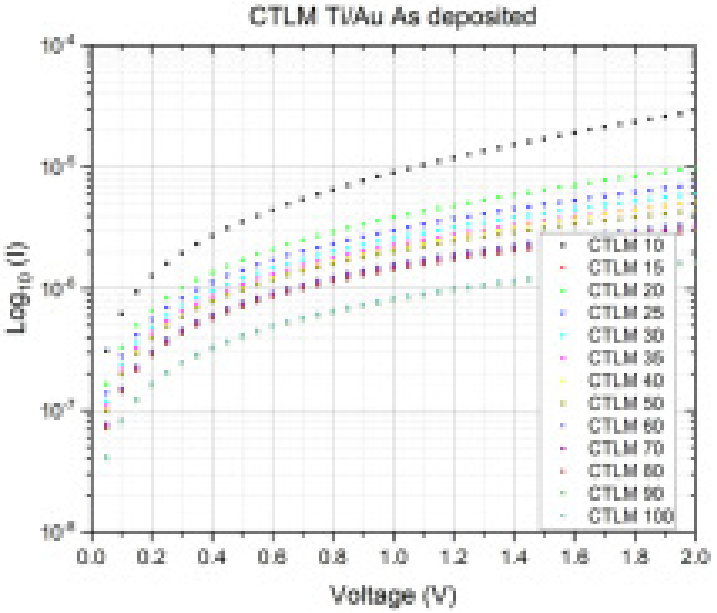
If the two contacts were both Schottky contacts then it could be modelled as two Schottky diodes opposing one another, however, with the second contact being much larger it was possible that that the leakage current would be significant to be able to modelled this setup as a single diode with a resistor in series [262]. The difference between each set of contacts should then be a result of the resistance of this resistor increasing. If this was the case then it could be modelled by the equation,

$$I = I_0\left(e^{\frac{q}{nK_bT}-IR} - 1\right) \tag{6.2}$$

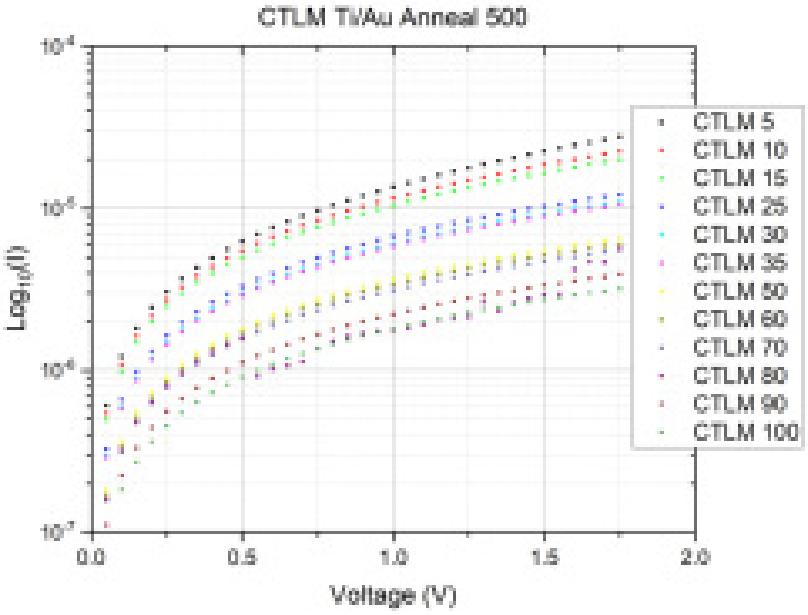
is the more appropriate in this case as the CTLM spacing increases the resistance of the thin film becomes more dominant. An attempt was made to consider this as a single diode dominated by the smaller contact. If the diode could be modelled to Equation 6.2, then the resistance can be treated in the same manner as CTLM as this resistance has the same cause. Plotting $\log_{10}$(I) vs voltage the ideality factor n of a diode can be found from the linear portion of this plot, where the gradient m is given by,

$$m = \frac{q}{2.3nK_bT}, \tag{6.3}$$

where the factor 2.3 is to account from the translation from the natural logarithm to base 10. In this case a linear portion was not found, however, the shape of the plot, this could be if the contacts are poor ohmic contacts, the leakage might not be high enough to make the approximation that the system would act like a diode, as well as the resistance in series might be high and obfuscates the linear portion. The plots can be seen in Figures 6.20, an example plot showing a diode and a diode with a significant resistor in series in Figure 6.21.



(A)



(B)

Figure 6.20: Example plot of $Log_{10}(I)$ as a function of voltage, this was for Ti/Au as deposited and after annealing at 500°C. It can be seen that there is not a linear portion of the plot. The curved nature of it indicates that if it is following Schottky diode, there is a high resistance in series.

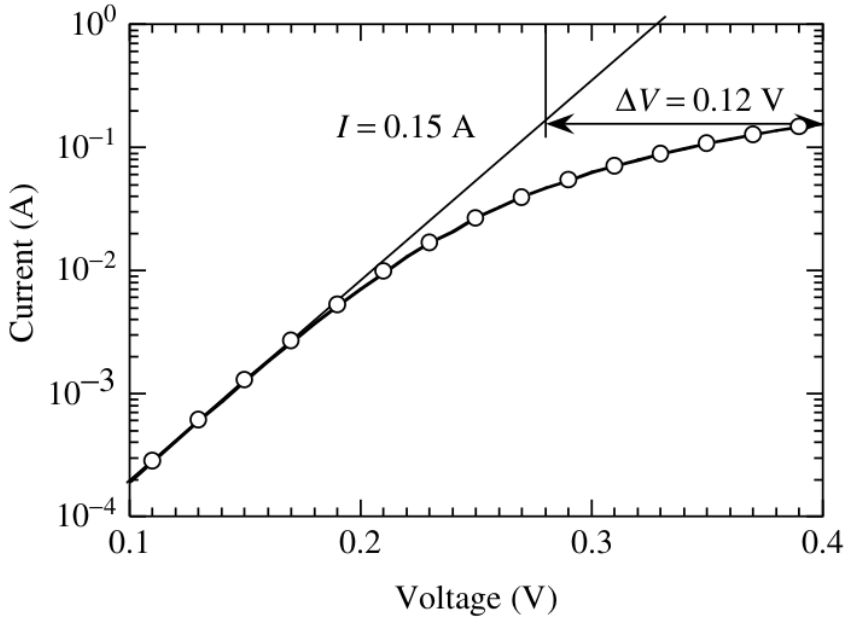
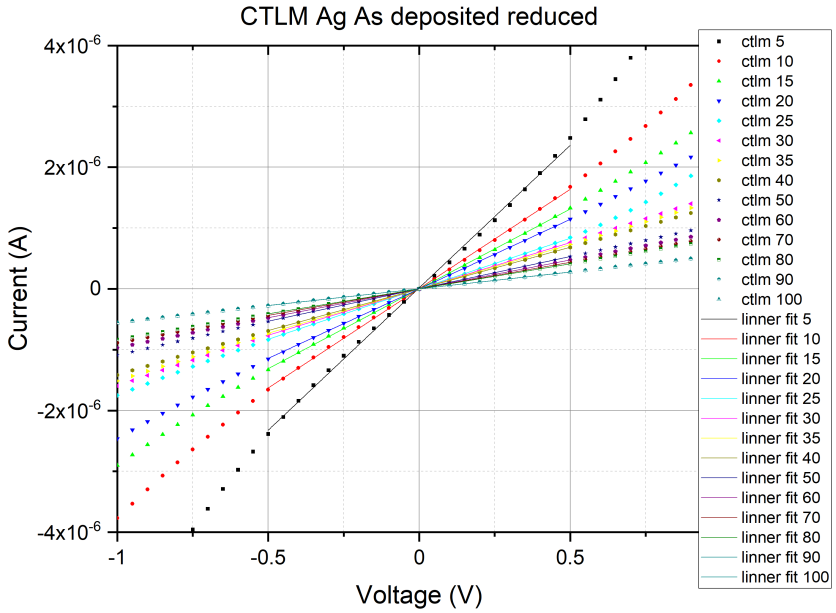
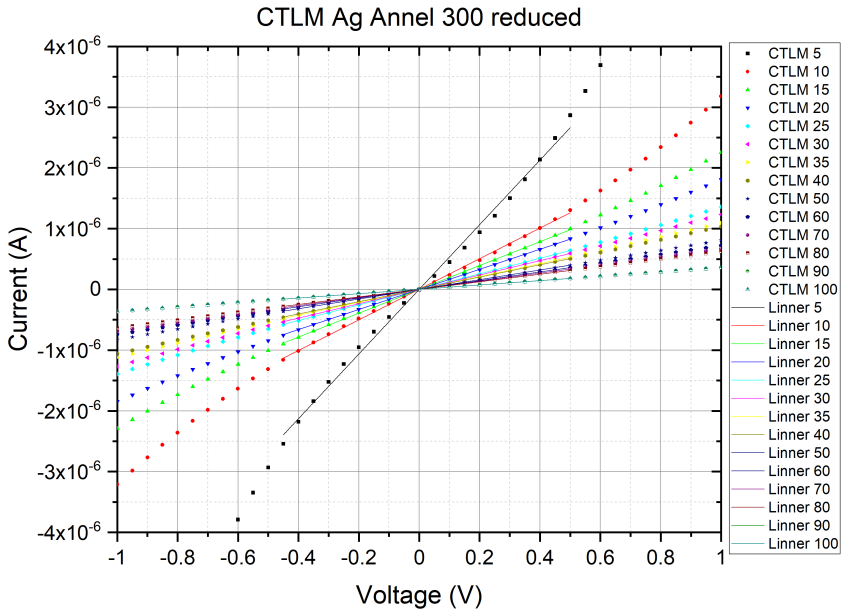


Figure 6.21: An example Log_{10} vs V plot showing a diode and one with a significant resistor in series, where the ΔV is due to this resistance. Comparing the shape of this plot with increasing spacing in CTLM measurements in Figure 6.20, therefore increasing the resistance. This follows a similar pattern. This was taken from [262].

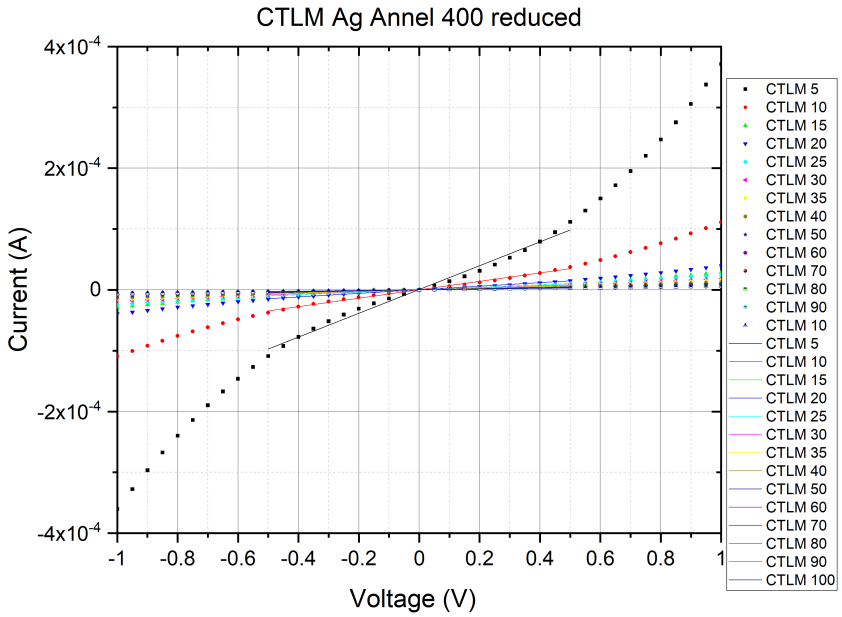


(A)

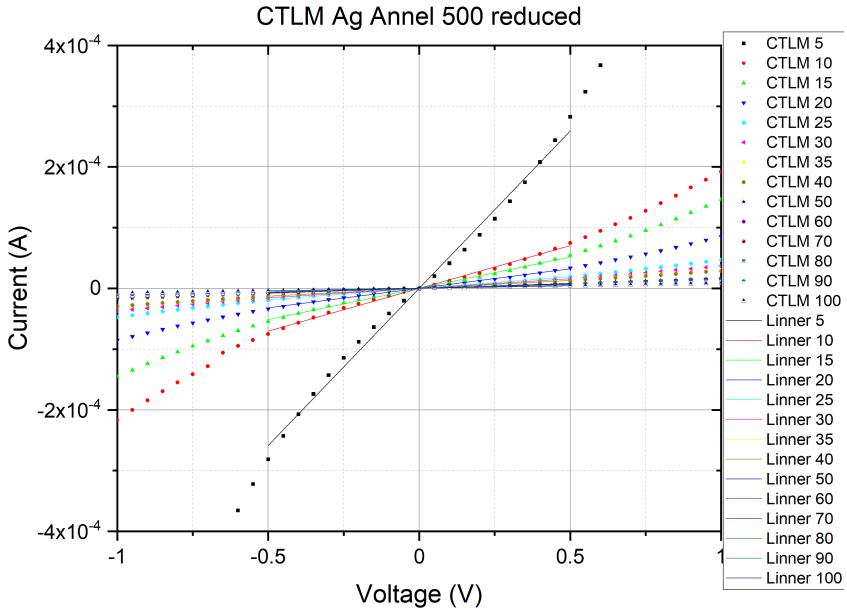


(B)

Figure 6.22: IV plot of the CTLM contact at a reduced voltage range, and the fitting between ±0.5 V. This was for the Ti/Ag samples. As deposited, and after annealing at 300, 400 and 500°C for (A), (B), (C) and (D) respectively. This was performed for each metalisation with the gradients tabulated in the Appendix in Table C.2, in this region the IV appears ohmic. This could be leakage current for a Schottky contact or this could be a poor ohmic contact.

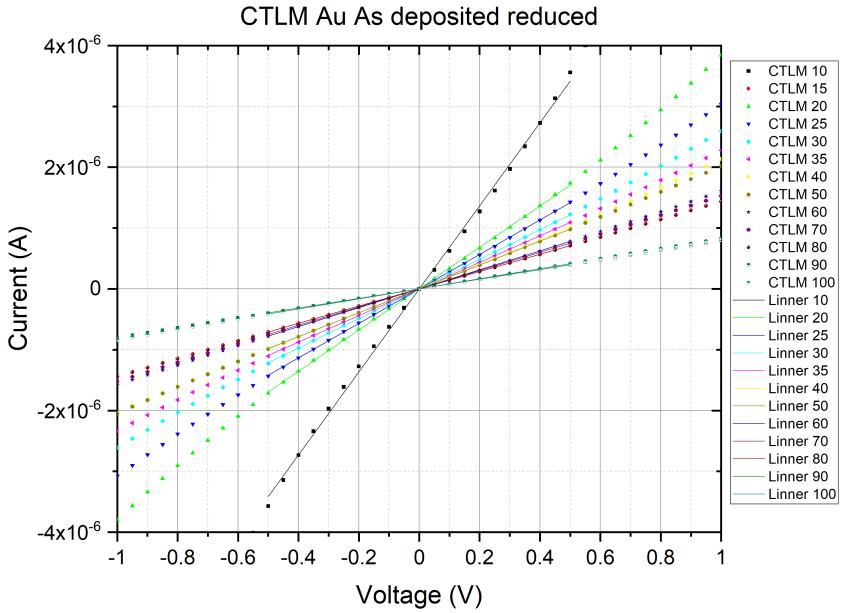


(C)

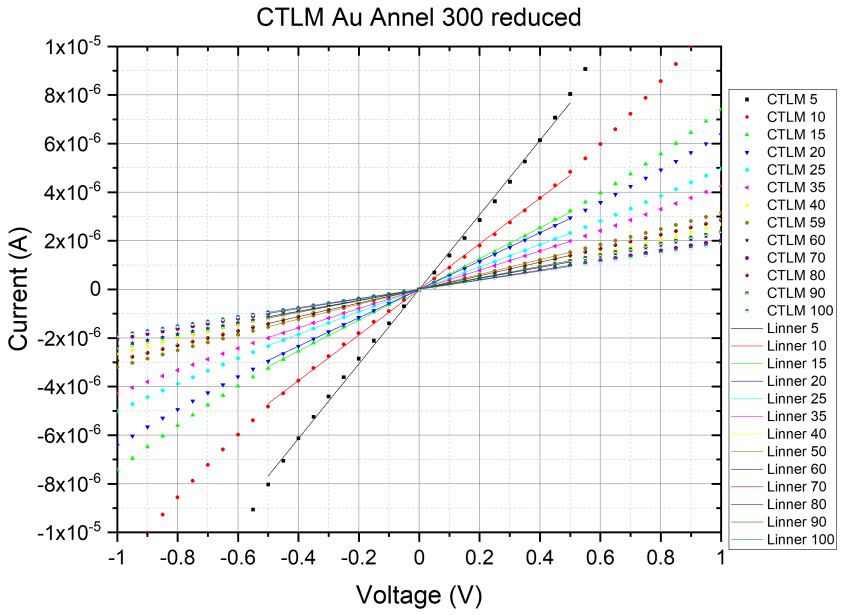


(D)

Figure 6.22: IV plot of the CTLM contact at a reduced voltage range, and the fitting between ±0.5 V. This was for the Ti/Ag samples. As deposited, and after annealing at 300, 400 and 500°C for (A), (B), (C) and (D) respectively. This was performed for each metalisation with the gradients tabulated in the Appendix in Table C.2, in this region the IV appears ohmic. This could be leakage current for a Schottky contact or this could be a poor ohmic contact.

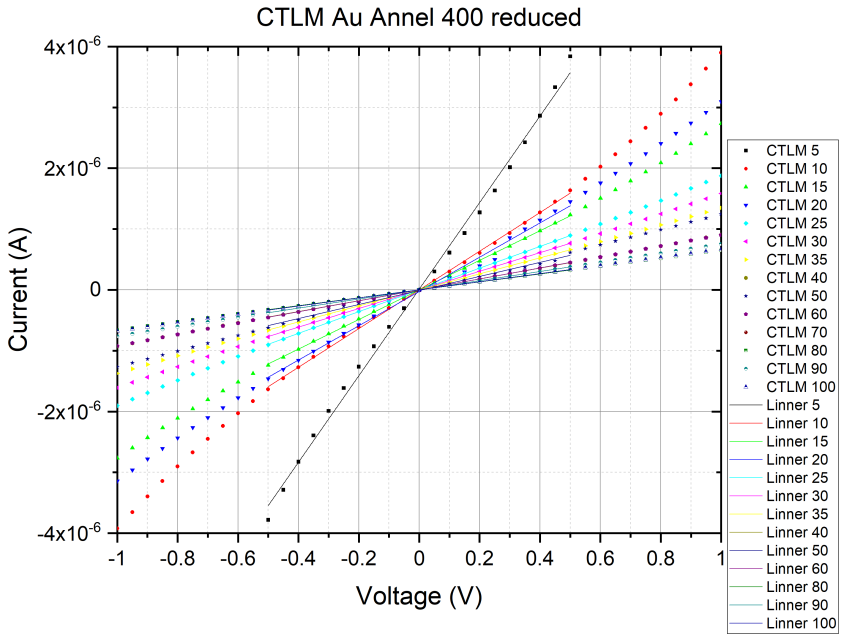


(A)

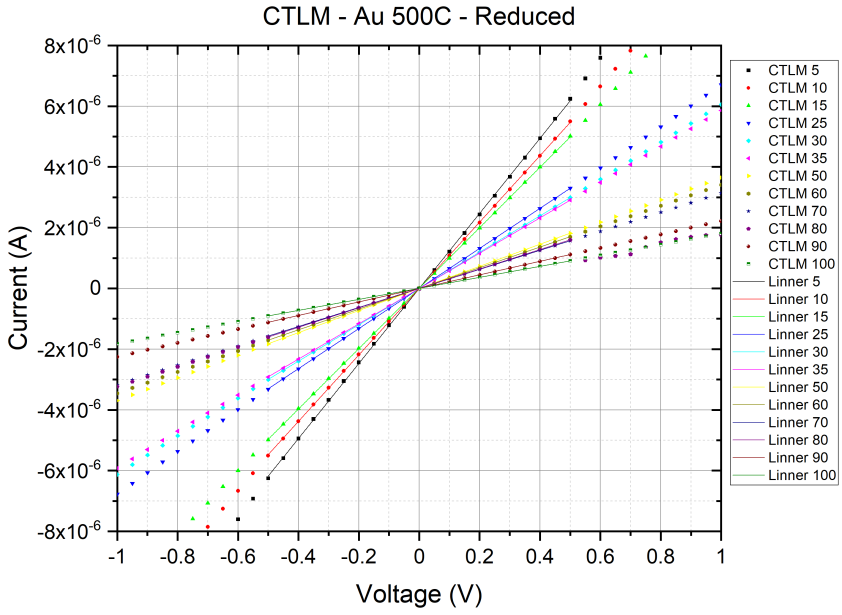


(B)

Figure 6.23: An example IV plot of the CTLM contact at a reduced voltage range, and the fitting between ±0.5 V. As deposited, and after annealing at 300, 400 and 500°C for (A), (B), (C) and (D) respectively. This was for the Ti/Au samples. This was performed for each metalisation with the gradients tabulated in the Appendix in Table C.2, in this region the IV appears ohmic. This could be leakage current for a Schottky contact or this could be a poor ohmic contact.



(C)



(D)

Figure 6.23: An example IV plot of the CTLM contact at a reduced voltage range, and the fitting between ±0.5 V. As deposited, and after annealing at 300, 400 and 500°C for (A), (B), (C) and (D) respectively. This was for the Ti/Au samples. This was performed for each metalisation with the gradients tabulated in the Appendix in Table C.2, in this region the IV appears ohmic. This could be leakage current for a Schottky contact or this could be a poor ohmic contact.

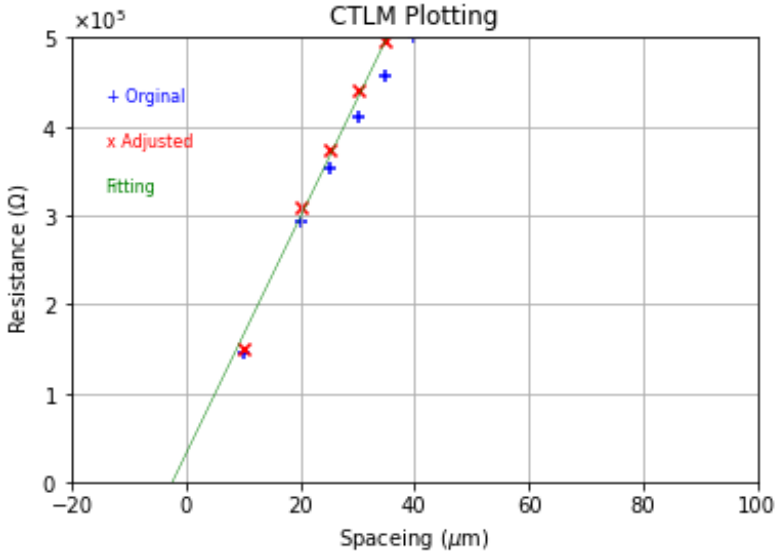
Results, CTLM

The contacts exhibited either poorly ohmic behaviour or Schottky characteristics with low barrier heights. To analyse the IV measurements, fittings were performed on the low-current region, specifically between ±0.5 V. The fitted plots for this reduced voltage range are shown in Figures 6.22 and 6.23, with the corresponding gradients summarised in Table C.2 in the Appendix. The resistance was calculated from the gradient obtained from these fits.

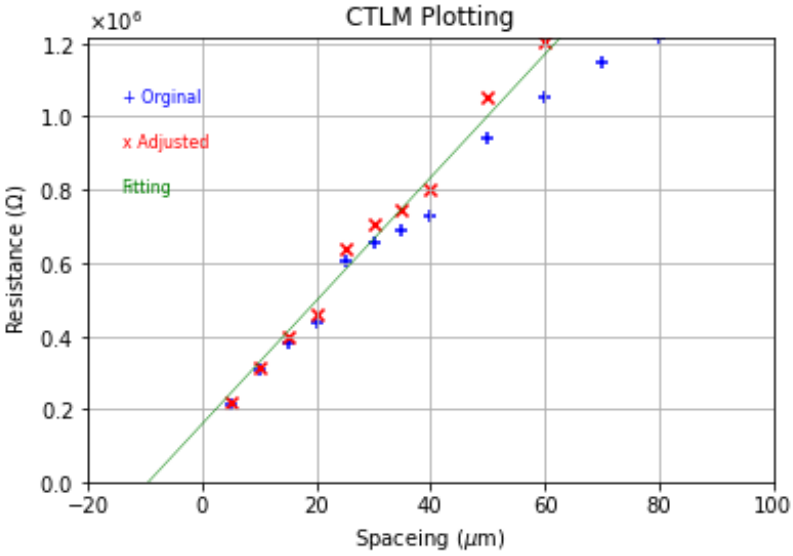
Using the CTLM corrections for resistance-, the resistance values were adjusted to account for the geometry of the test structures, and a linear fit was applied to the adjusted data, excluding outliers. These CTLM plots and their fittings are presented in Figure 6.24, with the calculated sheet resistance (R_{Sh}) and contact resistance (R_C) detailed in Table 6.3.

The results indicate high R_{Sh}, with significant variability observed between different metallisation stacks. As all samples were fabricated on the same wafer, this variability is unexpected and may suggest either a highly defective epitaxial layer or non-uniform doping across the wafer.

The calculated contact resistance (R_C) values were exceedingly high, with some samples yielding negative R_C values, which are physically implausible. This further supports the conclusion that the fitting methodology and the CTLM treatment are not suitable for this dataset, even within the restricted voltage range. Due to this a different approach was used to see if the contact could be characterised in another way.

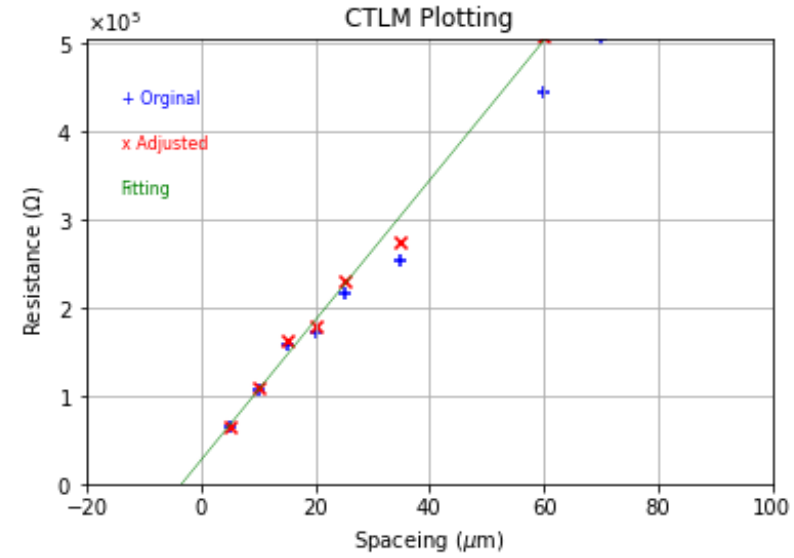


(A)

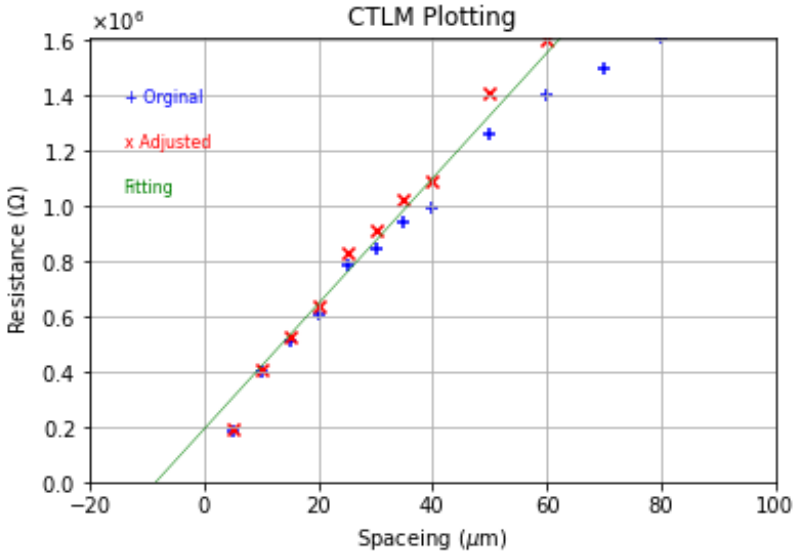


(B)

Figure 6.24: The CTLM plots from the IV measurements in the reduced voltage range, this was for Au (A), (C), (E) and (G) and Ag (B), (D), (F) and (H) respectively, as deposited (A) and (B), at 300°C (C) and (D), 400°C (E) and (F) and 500°C. The original data is shown in blue +, the adjusted data in red x and green line. The results from these are tabulated in Table 6.3.

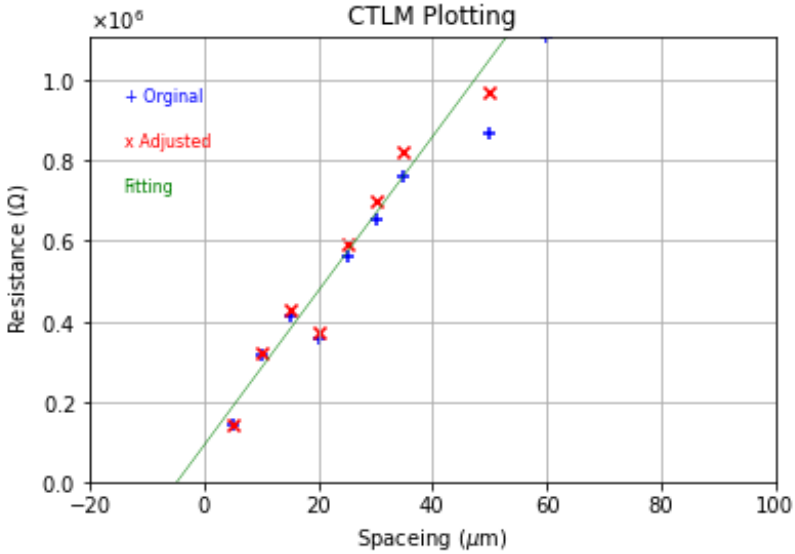


(C)

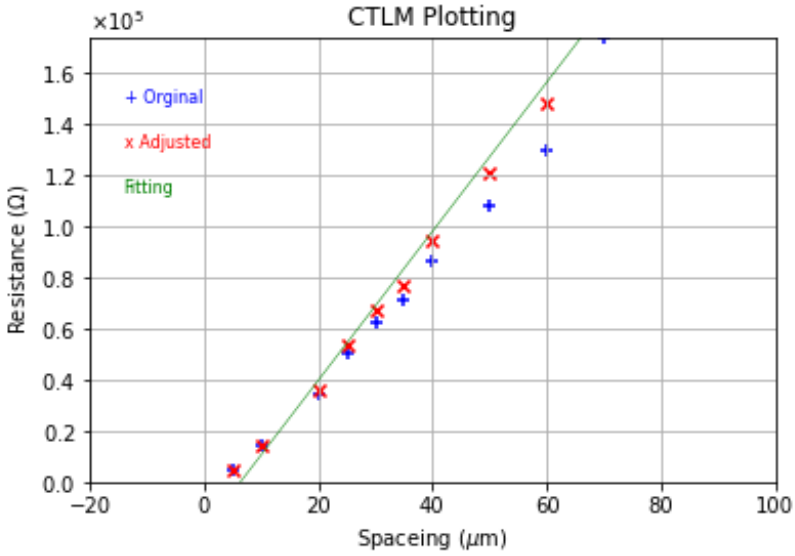


(D)

Figure 6.24: The CTLM plots from the IV measurements in the reduced voltage range, this was for Au (A), (C), (E) and (G) and Ag (B), (D), (F) and (H) respectively, as deposited (A) and (B), at 300°C (C) and (D), 400°C (E) and (F) and 500°C. The original data is shown in blue +, the adjusted data in red x and green line. The results from these are tabulated in Table 6.3.

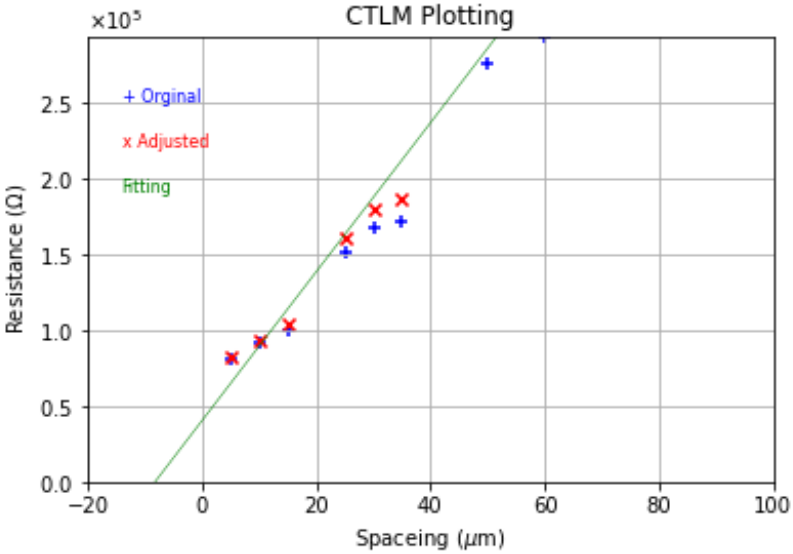


(E)

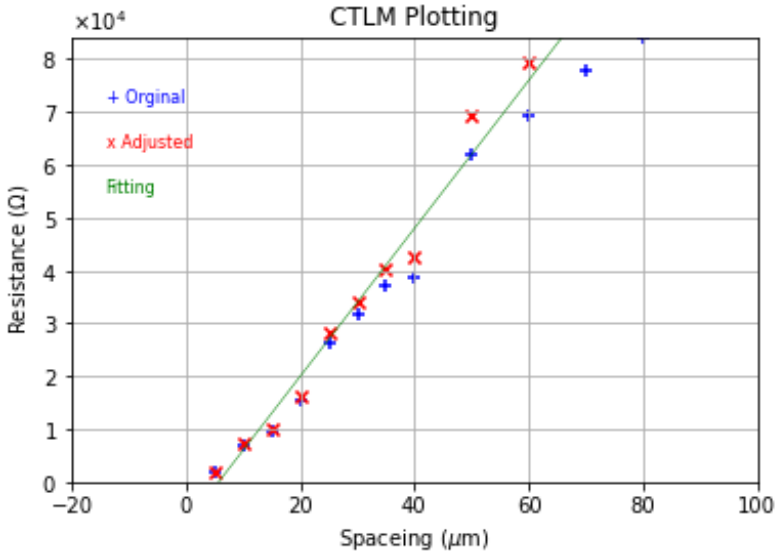


(F)

Figure 6.24: The CTLM plots from the IV measurements in the reduced voltage range, this was for Au (A), (C), (E) and (G) and Ag (B), (D), (F) and (H) respectively, as deposited (A) and (B), at 300°C (C) and (D), 400°C (E) and (F) and 500°C. The original data is shown in blue +, the adjusted data in red x and green line. The results from these are tabulated in Table 6.3.



(G)



(H)

Figure 6.24: The CTLM plots from the IV measurements in the reduced voltage range, this was for Au (A), (C), (E) and (G) and Ag (B), (D), (F) and (H) respectively, as deposited (A) and (B), at 300°C (C) and (D), 400°C (E) and (F) and 500°C. The original data is shown in blue +, the adjusted data in red x and green line. The results from these are tabulated in Table 6.3.

Sample	R_{Sh} (Ω)	R_C (Ω)	L_C (μm)
Ag, As deposited	21200000	79300	4.71
Ag 300°C	28500000	957000	4.22
Ag, 400°C	3660000	−9230	−3.17
Ag, 500°C	1760000	−3970	−2.84
Au, As deposited	16740000	15900	1.19
Au, 300°C	9960000	13500	1.71
Au, 400°C	24100000	45600	2.37
Au, 500°C	6160000	20200	4.12

Table 6.3: The calculated sheet resistance (R_{Sh}), contact resistance (R_C) and the transfer length (L_c), with Ti/Ag and Ti/Au contacts on β-Ga_2O_3. These were calculated using IV measurements from the reduced voltage range.

Results, Voltage Capacitance Measurements

The contacts exhibited either Schottky or poorly ohmic behaviour, as evidenced by IV measurements in the prior section. To further investigate their nature, CV measurements were conducted under the assumption that both contacts were Schottky, functioning as two capacitors in series. In should be noted that these models are not entirely valid. As there is a current passing across the Schottky contact in the voltage ranges used in this work, this dose change the underling assumptions of how the circuit is modelled. Rather then the normal model which is a resistor and capacitor in series, whereas in this case it should be a capacitor and resistor in parallel, however, the value of this resistor is unknown as well as the point at which it is conducting. While CV measurements typically require one contact to be ohmic, the approximation used here mirrors the approach described in Chapter 5 for MIS capacitors. The total capacitance (C_T) of this is,

$$\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2} = \frac{C_1 + C_2}{C_1 C_2} \tag{6.4}$$

That is for capacitance 1 and 2 (C_1 and C_2) , with areas A_1 and A_2 respective the following is valid,

$$A_1 \gg A_2 \tag{6.5}$$

As a result the capacitance values are,

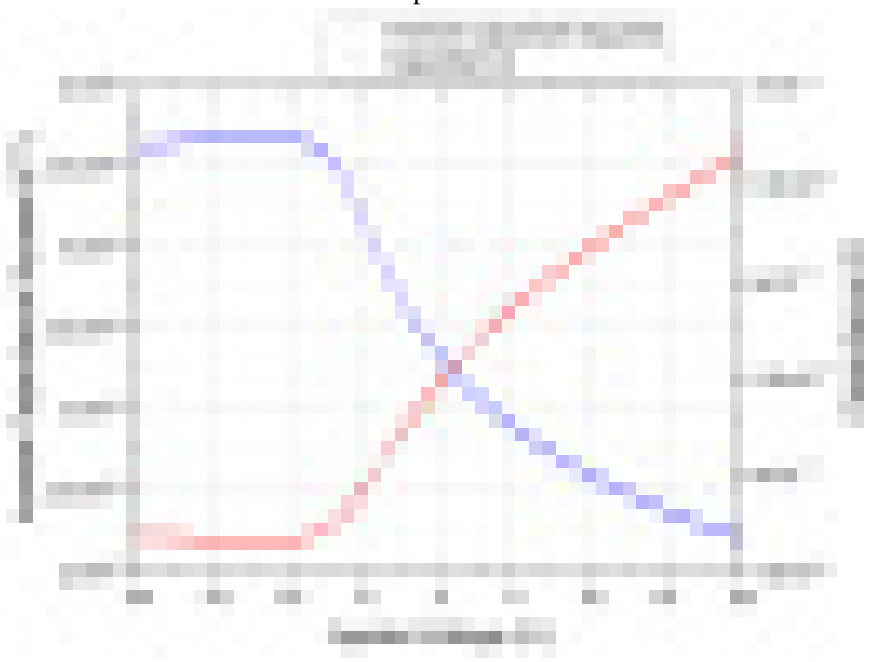
$$C_1 \gg C_2 \tag{6.6}$$

Then Equation 6.4 can be approximated as,

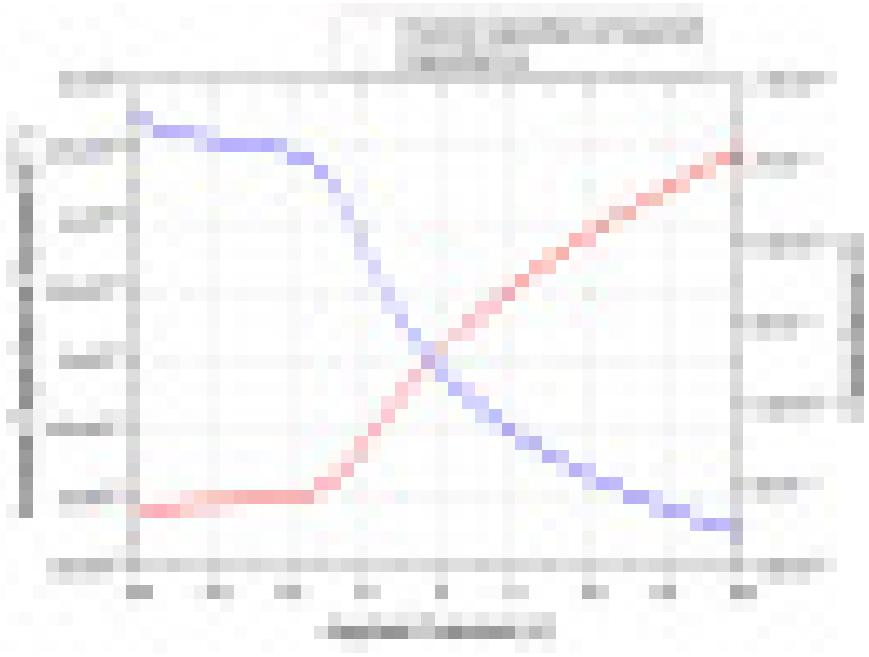
$$\frac{1}{C_T} \approx \frac{C_1}{C_1 C_2} = \frac{1}{C_2} \tag{6.7}$$

As a result it can be approximated that the larger second contact area ensures the smaller contact dominates the total capacitance, validating this approximation near zero bias. Unlike MIS structures, the CV characteristics observed lack an accumulation region, as there is no oxide layer.

As deposited



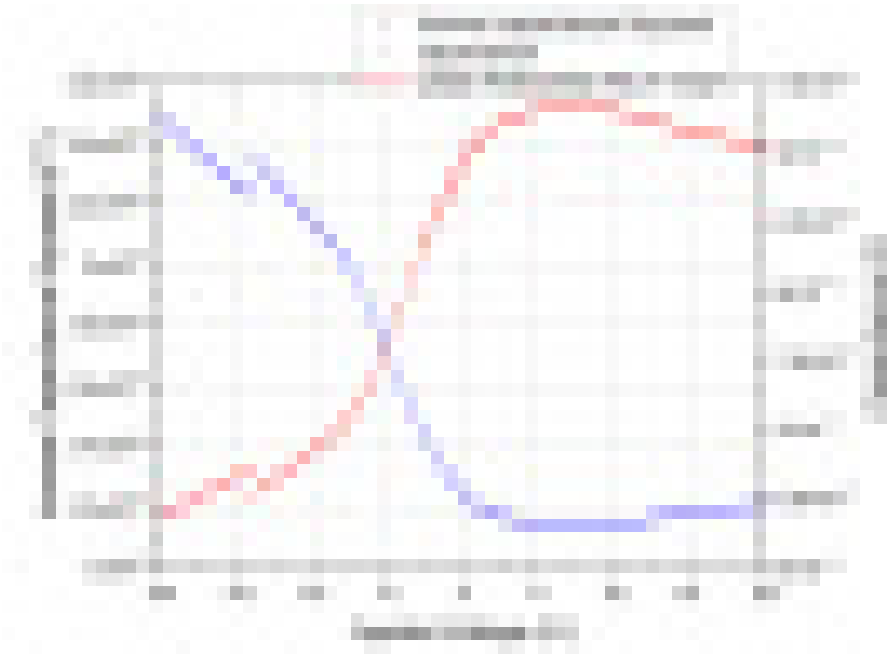
(A)
300°C



(B)

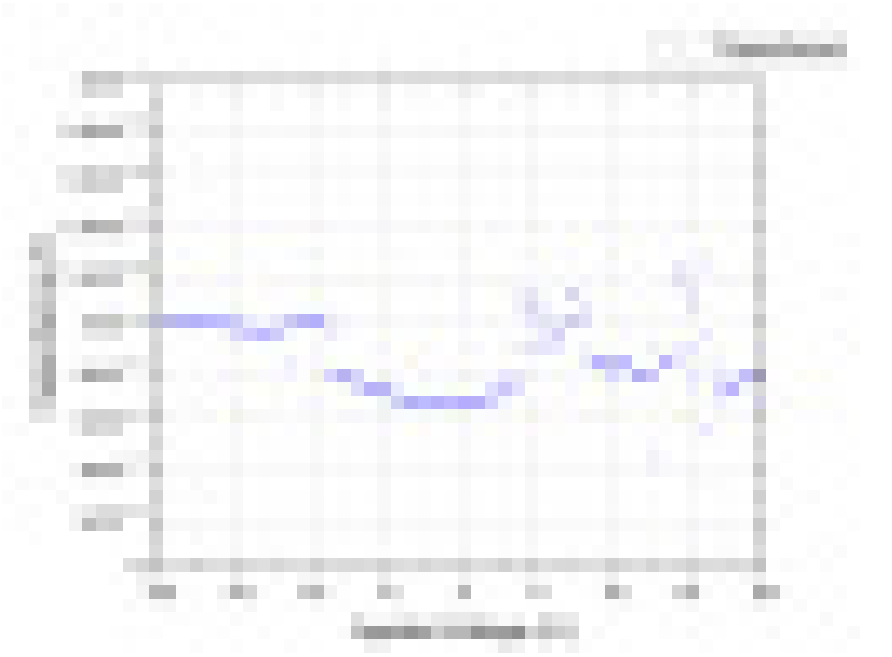
Figure 6.25: The CV (red) and C^{-2} (blue) vs V plots for the Ti/Ag contacts, these used a contact with a separation of 100 µm. The CV plot for the contact annealed at 500°C, (A) as deposited, and after annealing at (B) 300°C, (C) at 400°C and (D) 500°C. The CV measurement for 500°C failed as such there is no C^{-2} as this measurement would be meaningless. It should be noted that compare these to Figure 6.17, at the voltages in this range there is a current passing though.

400°C



(C)

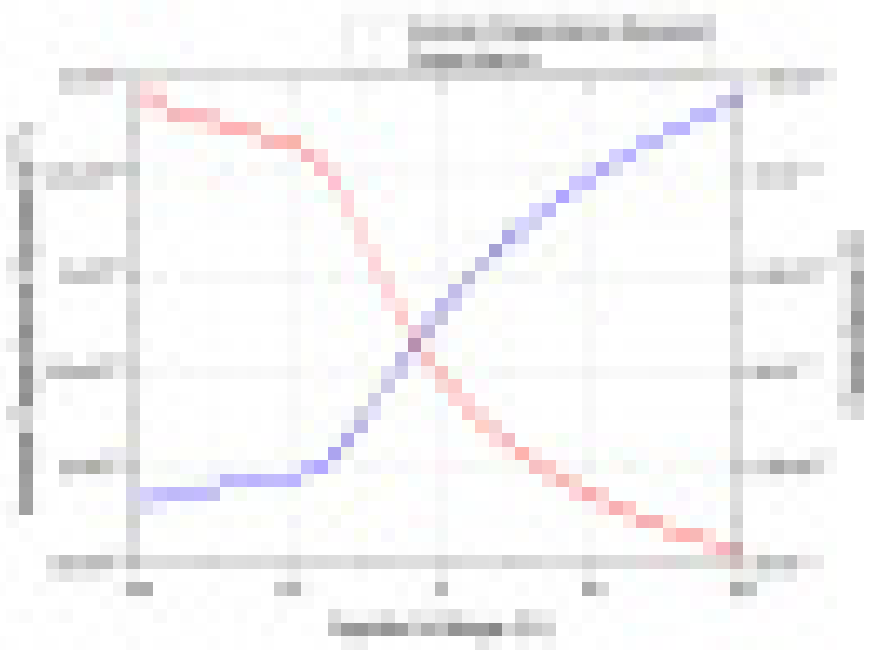
500°C



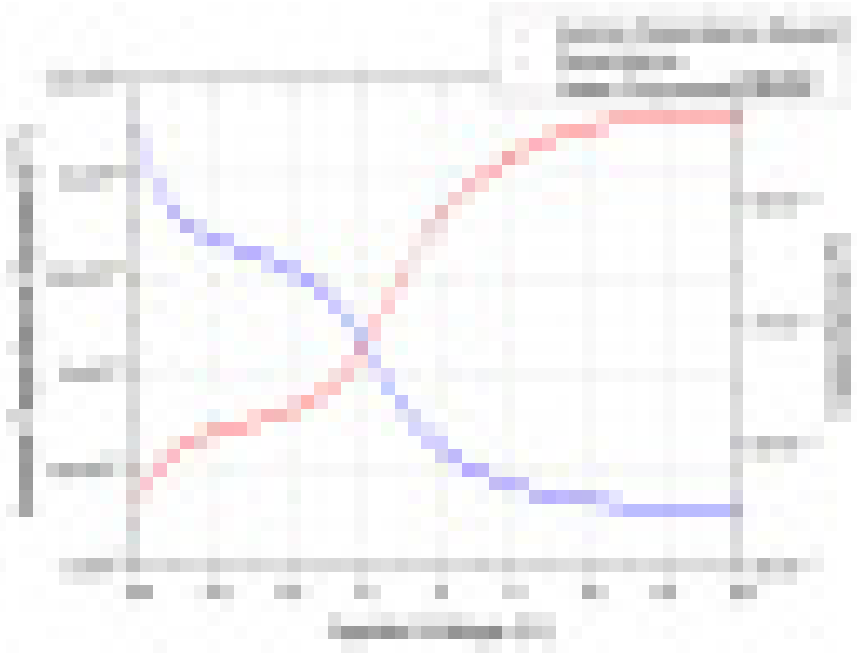
(D)

Figure 6.25: The CV (red) and C^{-2} (blue) vs V plots for the Ti/Ag contacts, these used a contact with a separation of 100 μm. The CV plot for the contact annealed at 500°C, (A) as deposited, and after annealing at (B) 300°C, (C) at 400°C and (D) 500°C. The CV measurement for 500°C failed as such there is no C^{-2} as this measurement would be meaningless. It should be noted that compare these to Figure 6.17, at the voltages in this range there is a current passing though.

As deposited



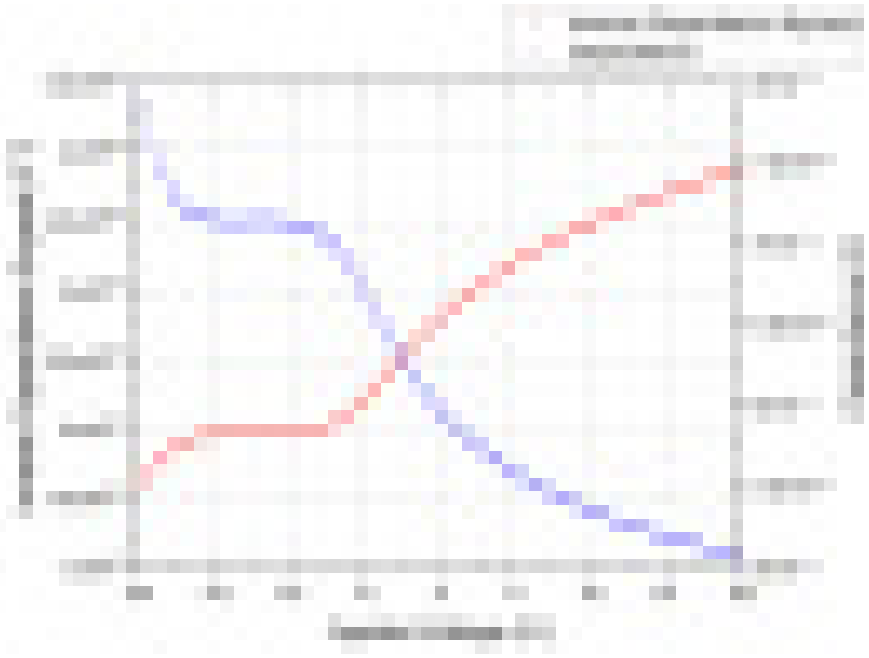
(A)
300°C



(B)

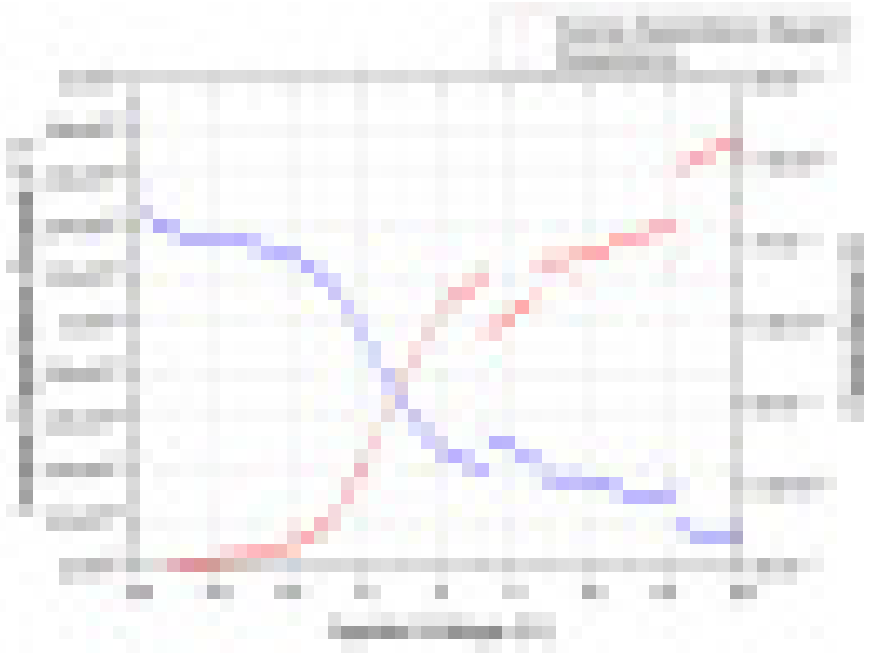
Figure 6.26: The CV (red) and C^{-2} (blue) vs V plots for the Ti/Au contacts, (A) as deposited, and after annealing at (B) 300°C, (C) at 400°C and (D) 500°C. It should be noted that compare these to Figure 6.18, at the voltages in this range there is a current passing though.

400°C



(C)

500°C



(D)

Figure 6.26: The CV (red) and C^{-2} (blue) vs V plots for the Ti/Au contacts, (A) as deposited, and after annealing at (B) 300°C, (C) at 400°C and (D) 500°C. It should be noted that compare these to Figure 6.18, at the voltages in this range there is a current passing though.

The carrier concentration was derived from the C^{-2} versus V plots using,

$$N = \frac{2}{A^2 \epsilon_0 \epsilon_S \frac{dC^{-2}}{dV}}. \tag{6.8}$$

The calculated carrier concentration, was calculated for each CV measurement and the average was approximately 7×10^{17} cm^{-3}. The set of results cam be seen in Table 6.4. This carrier concentration is significantly lower than the manufacturer's specification of mid-10^{18} cm^{-3}, it should be noted that this is the effective carrier concentration and a high density of interface states could be distorting the CV measurement [519], effecting the calculated carrier concentration.

This low carrier concentration likely explains the difficulty and failure to form ohmic contacts with the material in this cycle, as this affects the metal-semiconductor work function. The metallization process was proven, in cycle two, however, this on a highly doped substrate, and the material here appears to be a lowly doped, heteroepitaxial layer. Using the calculated carrier concentration the built-in voltage (V_0) and effective barrier height (ϕ_B^{CV}) for this Schottky contact were calculated by using,

$$V_0 = \frac{K_b T}{q} \log \frac{N_C}{N}, \tag{6.9}$$

where N_C, the effective density of states in the conduction band, is given by:

$$N_C = 2M_c \left(\frac{2\pi {m_e}^* K_b T}{h^2} \right)^{\frac{3}{2}}. \tag{6.10}$$

The barrier height ϕ_B was calculated by using,

$$\phi_B = V_i - V_0 - \frac{K_b T}{q}, \tag{6.11}$$

where V_i is found from the intercept of the $\frac{A}{C^2}$ versus V plot. The calculated barrier height was $\phi_B = 0.46 \pm 0.002$ eV, which falls not too far from the expected range for Ti on lowly doped β-Ga_2O_3. Based on the Schottky-Mott rule the barrier height ideally is 0.33 eV. Yao et al. [300] suggest that work function alone does not determine Schottky behaviour, factors such as pre- and post-treatments can significantly modify contact properties.

The results suggest that the contacts are Schottky with a low ϕ_B, influenced by high defect density and non-uniformity across the surface. The IV method, which relies on the Richardson constant (A^{**}), is highly sensitive to these variations, leading to inconsistent results. In contrast, CV measurements are less affected by surface defects, providing more reliable estimations of carrier concentration and barrier height [262]. This highlights the importance of addressing material defects and doping uniformity in future studies. It should be noted that this analysis is based off the idea that the contact is acting like a capacitor, however, it should be noted that there is likely a large leakage current. This is indicated by the IV plots of the same contacts. This changes the model which should be used to a capacitor with a resistor in parallel circuit. This dose bring into question the validity of the analysis used, however, it was still used to estimate the carrier concentration and barrier height.

Sample	Carrier Concentration (cm^{-3})	Error (cm^{-3})
Au, As deposited	9.05064×10^{17}	9.1×10^{15}
Au, 300°C	8.6×10^{17}	2.4×10^{16}
Au, 400°C	8.9×10^{17}	1.0×10^{16}
Au, 500°C	7.5×10^{17}	6.8×10^{15}
Ag, As deposited	7.6×10^{17}	7.5×10^{15}
Ag, 300°C	8.1×10^{17}	6.3×10^{15}
Ag, 400°C	8.8×10^{17}	2.0×10^{16}
Ag, 500°C	-	-
Mean	8.4×10^{17}	6.3×10^{16}

Table 6.4: The calculated carrier concentration and built in voltage from the Schottky contacts, this was calculated from inverse capacitance squared verse gate voltage gradient and the built in voltage from the voltage intercept. This was with lateral contacts, with a spacing of 100 µm. The metal contacts were Ti/Au and Ti/Ag in a ratio of 20/80 nm. This was calculated gradient change near zero, as both contacts are Schottky capacitors, both should be in depletion at this gate bias and the smaller contact should dominate. The plots these are derived from can be seen in Figures 6.26 and 6.25, Ag 500°C was not measured as a stable CV curve was not measured. It can be seen that the doping concentration appears to be high 10^{17} cm^{-3}. It should be noted that the carrier concentration should not be changing, the change is an indication that it is inaccurate and the change is due to the effect on the CV measurements. It is worth remembering figures 6.17 and 6.18. This means that current is passing though the contact in the same voltage range that the CV measurements are being taken, this adds an inaccuracy to this method. This is likely the reason the carrier concentration is not consistent.

Sample	V_i (V)	Error (V)	ϕ_B (eV)	Error (eV)
Au, As deposited	−28.0	0.3	0.466	8.16063×10^{-4}
Au, 300°C	−26.8	0.7	0.465	1.19×10^{-4}
Au, 400°C	−27.7	0.3	0.466	8.48×10^{-4}
Au, 500°C	−25.5	0.2	0.463	7.82×10^{-4}
Ag, As deposited	−26.6	0.3	0.464	8.06×10^{-4}
Ag, 300°C	−27.5	0.2	0.465	7.89×10^{-4}
Ag, 400°C	−22.9	0.5	0.459	9.75×10^{-4}
Ag, 500°C	-	-	-	-
Mean	−26.4	1.7	0.464	0.0022

Table 6.5: The V_i from the plots of C^{-2} verse V, this is for Ti/Au and Ti/Ag samples as deposited and after annealing at 300°C, 400°C and 500°C. These plots can be seen in Figures 6.25 and 6.26. The ${\phi_B}^{CV}$ were calculated using the mean carrier concentration show in in Table 6.4, 8.36504×10^{17} cm^{-3}. As Ag annealed at 500°C did not have a successful CV curve this result was disregard. As these are determined from Figures 6.26 and 6.25, which are related to Figures 6.17 and 6.18, the same inaccuracy apply as a current is passing though.

Conclusion To Third Development Cycle

To conclude the third development cycle, the metallisation used in this cycle, which was proven to work in cycle two on bulk substrates, was unsuccessful in forming ohmic contacts on the hetro-epitaxial-grown thin film. This outcome is attributed to the material's lower carrier concentration, measured from CV measurements taken on the structure using the apparent Schottky contacts. This carrier concentration calculated deviates significantly from the manufacturer's specifications, however, as noted, there are issues based on the interface states with this method of determining the carrier concentration.

The behaviour of the contacts, whether as Schottky with a low barrier height or as poorly ohmic, is difficult to categorise due to the inability of IV plots to conform to either model. This could be due to two Schottky contacts being back-to-back, so a Schottky diode model could not be fitted to the IV measurements. CV measurements suggest a low-barrier Schottky contact, consistent with the behaviour of two Schottky diodes in series. The significant reduction in current with increasing CTLM spacing supports the conclusion that the material is lowly doped and highly resistive, which aligns with the failure to achieve ohmic behaviour. This also distorts the Log_{10}I versus V plots, preventing the determination of key Schottky diode parameters, such as the saturation current, as no linear region is observable.

A major limitation of IV measurements with Schottky contacts is their sensitivity to defects, which can significantly alter the Richardson constant. Given that this material was grown hetero-epitaxially, it is likely to have a higher density of defects due to lattice mismatching, though this has not been explicitly proven in this work. These defects impact IV measurements more than CV measurements, which are less sensitive to surface inhomogeneities.

These metallisations successfully formed ohmic contacts in the second development cycle, suggesting that the process can form ohmic contacts on suitably doped material. If future work was performed using similar material, further iterations could include surface treatments. These could be HF cleaning or Si implantation, to increase the carrier concentration near the surface, enabling ohmic behaviour.

While increased annealing temperatures appeared to improve conductivity, ohmic contacts were not found with this third cycle. This is believed to be because of the low doping in the material. This means the next stage of work should focus on obtaining more suitable material, ideally highly doped thin-film β-Ga_2O_3 with carrier concentrations in the high 10^{18}-10^{19} cm^{-3} range. This material should ideally be grown homoepitaxially on semi-insulating or UID β-Ga_2O_3 substrates to minimise defects. While heteroepitaxial growth could also provide valuable insights into metallisation behaviour, it is more prone to defects caused by lattice mismatching, potentially complicating measurements and analysis.

6.3 Chapter Conclusion

Ultimately in this chapter Ti-based contacts were explored in order to form ohmic contacts, these were in a ratio of 20/80 nm of Ti to capping metal. The metals used were, Ti/Au, the predominate ohmic contact cited in the literature, Ti/Al which has also been reported as being able to form ohmic contacts. The other two contacts explored were Ti/W, which was based off a reported ohmic contact from a TiW alloy, the other was Ti/Ag, while not reported previously Ag has been reported to from pseudo-ohmic behaviour, dewetting after annealing. For this reason Ti/Ag was pursued as a possible candidate for ohmic contacts, as Ag showed potential ohmic contact and with a suitable contact layer dewetting may be avoided While not much can be learned from cycles one and three, apart from the issue that carrier concentration is vital, confirming that this should be adopted to know if ohmic contacts are possible from the onset is necessary.

Efforts were made to use a Hg probe to characterise the thin-film material in cycle one, this was not possible, this is believed to be due to the sample size. Ultimately, the Schottky contacts formed in cycle three enabled an estimation of the carrier concentration. These results strongly suggest that the carrier concentration in the material did not match the manufacturer's specification, contributing to the failure to form ohmic contacts. It is important to note that a high density of interface traps (D_{it}) could have influenced these measurements, necessitating additional techniques such as Hall measurements to corroborate these findings. Using larger sample sizes for Hg-probe measurements would be preferable, as this non-destructive method allows samples to be processed afterwards. Potentialy this could involve characterising an entire wafer with the Hg probe, dicing the wafer, and then processing individual die.

MIS capacitors could also be used as a suitable alternative to calculating the carrier concentration rather than relying on forming a Schottky contact, this could have a better measurement due to the interface-trapped states in the CV measurement. However, they require the deposition of a dielectric layer, which itself might require post-deposition anneals, post-metalisation anneals and pre-cleaning processes. The same issues must be addressed regarding a second ohmic contact or an approximation based on the size of the contact. MIS capacitors could be integrated into the test structures as part of a larger device fabrication process. For example, in developing a MISFET, a sacrificial die could be used to measure carrier concentration in regions reserved for ohmic contacts and the channel.

The use of material in cycle three, similar to cycle one, was due to cost, availability and time constraints. The ideal material would be an n^+ epi-layer grown on a semi-insulating substrate doped with Fe. If such material is unavailable, n^- substrates could be used, though heteroepitaxial layers are more prone to defects due to lattice mismatching. These defects could affect results and should be carefully considered.

Cycle two demonstrated that the metallisations can form ohmic contacts on highly doped material, showing that it was a suitable process, this is to be expected as Ti is commonly used as a contact layer in ohmic contacts for β-Ga_2O_3. Of the metallisations performed in this chapter, Ti/Ag exhibited lower contact resistance than Ti/Au, indicating its potential as a superior contact. In cycle three, after annealing at 400°C, there was improved conductivity, with Ti/Ag samples showing lower calculated barrier heights compared to Ti/Au calculated using CV measurements. This is in agreement with the results from cycle two, where Ti/Ag contacts consistently reached compliance before Ti/Au contacts. To optimise contact performance, future experiments could explore metallisation stacks such as Ti/Ag/Ni/Au. Also, it would be of interest to draw in Ti/W and Ti/Al into the study for a full set of comparisons, as those metallizations were also successful in cycle two.

The work performed in this chapter demonstrated that all four metallisations, Ti/Ag, Ti/Au, Ti/Al, and Ti/W, can form ohmic contacts on (001) β-Ga_2O_3, providing that the material is highly doped. The results suggest that Ag and W may be superior capping layers or potentially overlayers in more complex metal contacts compared to Au, which is commonly used. Ag showing promise due to its lower barrier height (ϕ_B) of approximately 0.005 eV lower then Au. W seemed to more ready form an ohmic contact, the effect of annealing and other pre and post treatments may improve this. Future work should focus on refining these metallisation processes and providing there is a supply of highly doped thin-film substrates to enable further development of ohmic contacts to β-Ga_2O_3, which is required for device development.

CHAPTER 7

CONCLUSION

Prior chapters introduced β-Ga_2O_3, the issues which needed to be addressed and the specific aims of this thesis. The experimental methodology was explained, the results analysed and discussed. Here the key findings are presented, their relation to the objectives, and how the work can be progressed to develop β-Ga_2O_3 for power electronics.

7.1 Conclusions on β-Gallium Oxide Trench Etch Development Chapter 4

The aim for Chapter 4 was to develop a process to pattern photoresist on β-Ga_2O_3 with the purpose to transfer these patterns by etching β-Ga_2O_3. This was performed in an iterative process starting with Si to SiN_x/Si then onto SiN_x/α-Al_2O_3 and finally onto SiN_x / (001) β-Ga_2O_3. SiN_x was used as the hard mask, with the sample then successfully etched, with the pattern transferred across. The purpose for this etching is required to isolate regions and change the geometry of β-Ga_2O_3, which is a requirement for device fabrication. The etch was successfully conducted with the pattern transferred across to β-Ga_2O_3. While more work needs to be performed to transfer this into more useful etch patterns for device fabrication this chapter was ultimately successful in its aim.

In summary, a photoresist protocol with the etch chemistry required for β-Ga_2O_3 has been introduced to the power electronics community.

7.2 Conclusions Regarding β-Ga_2O_3 Gate Dielectrics Chapter 5

In this chapter MIS capacitors were fabricated and exposed to a series of consecutive PMA anneals. The MIS capacitors were fabricated on 2" (001) β-Ga_2O_3 wafers, with ALD Al_2O_3 and PECVD SiO_2, with Ti/Al/Ti/Au metal contacts. The annealing temperatures were, 100°C, 200°C and 300°C for each consecutive anneal. CV measurements were taken as deposited and after each annealing stage, and after the final annealing the samples were inspected under FIB-TEM and EDX.

Using ALD Al_2O_3/(001) β-Ga_2O_3, MIS capacitors, it was found that a long temperature anneal reduced D_{it} (as determined by the Terman method) and hysteresis was reduced. The reduction in the hysteresis meant that Q_M and Q_O was reduced due to annealing, meaning that some combination of less charge was being injected into or less mobile charges in the dielectric layer. The Terman method was used to extract the D_{it}, from β-Ga_2O_3 MIS capacitors to provide a valid comparison. This yields approximate values for of D_{it} between 0.2-0.6 eV below the conduction band. As deposited the D_{it} was 3.96×10^{12} $eV^{-1} \cdot cm^{-2}$ being reduced after 1.7×10^{12} $eV^{-1} \cdot cm^{-2}$ after annealing consecutively at 100°C and 200°C for an hour each. With a further anneal at 300°C the D_{it} increased back up to 2.17 $eV^{-1} \cdot cm^{-2}$ indicating inflection point. This implies that the annealing was improving the interface between β-Ga_2O_3 and Al_2O_3 up to 200°C then degrading after this position. A thickness reduction was inferred by comparing ellipsometry on 'spectator' Si wafers with cross-sectional FIB-TEM on β-Ga_2O_3 after the final anneal. PECVD SiO_2/β-Ga_2O_3 was also investigated, while improvements to the profile were seen.

Concerning ALD Al_2O_3/(001) β-Ga_2O_3 the chapter found that this was partially successful, the effect of successive prolonged PMA was investigated.

Regarding samples with PECVD SiO_2/(001) β-Ga_2O_3, the CV curve had a distorted shape with two plateaus. As a result the Terman method was not applied as the ideal CV model used to compare in the Terman method would be invalid, so the change in D_{it} and C_A is not known. This is not unexpected as PECVD SiO_2 rarely gate dielectric, it was in this work as SiO_2 can be used as a gate dielectric and at the time only had access to PECVD rather then ALD or other CVD deposition methods.

7.3 Conclusions on β-Ga_2O_3 Ohmic Contact Development Chapter 6

In Chapter 6 a series of ohmic contact trials were developed, the initial step on lightly doped β-Ga_2O_3. These were rectifying, which is believed to be due to low carrier concentration. This was then followed by successful fabrication onto highly doped (10^{19} cm^{-3}) bulk (001) β-Ga_2O_3. Metallisations utilising Ti/Al, Ti/Au, Ti/Ag and Ti/W, Ti/Al, Ti/Au, Ti/Ag were annealed at 400°C for two minutes. Notably, Ti/W, this contact proved to be ohmic contact without the need for annealing post deposition. This has an important aspect, as it reduces the processing steps required to form ohmic contacts, by decreasing the costs, increases throughput and lowering the thermal budget that the material is exposed to. This helps decrease the cost and increasing the economical viability of β-Ga_2O_3 material being realised.

Following this, on lightly doped (calculated at 7×10^{17}) on (-201) epi-β-Ga_2O_3, Ti/Ag and Ti/Au, the contacts were annealed at 300°C, 400°C and 500°C. Despite proven metalisations , going above the annealing temperatures the contacts remained rectifying. This final attempt had rectifying contacts. This is believed to be due to the low carrier concentration, as determined by CV measurements performed using the Schottky contacts. From these CV measurements, the ϕ_B was determined. It was observed that the ϕ_B was lower for Ti/Ag at 400°C 0.459 eV compared to 0.462 eV for Ti/Au annealed at 500°C. The CV for Ti/Ag annealed at500°C could not be found, however, if the trend continues which is observed for Ti/Au this could further reduced.

The main aim as described in Chapter 6 was to form ohmic contacts to β-Ga_2O_3, this was achieved. On the bulk β-Ga_2O_3 where the ohmic contacts were successful, with Ti/Ag, and Ti/Au having the lowest ρ_C, both about 7.3×10^{-5} $\Omega \cdot cm^2$, Ti/W appeared to have 1.1×10^{-3} $\Omega \cdot cm^2$, however, this was erroneous as the liner fit was not physical. This was due to the measurements performed on bulk, as well as difficulty On the lightly doped epi-β-Ga_2O_3 it was confirmed that the carrier concentration was too low to form ohmic contacts, Schottky contacts were formed.

7.4 Further Work

Each chapter has further work which can be associated with it, as well as further development which is not strictly associated with work in any chapter in particular.

7.4.1 Further Development regarding etching

The next stage of this work would be to remove the SiN_x hard mask, this should be performed with hot phosphoric acid. Following this an investigation into the surface roughness of the sidewall and etched region and profile of the etch post removal should be performed. Different post etch treatments could be performed to investigate what effects these have. Cleaning is part of the post etch treatments which can be used to repair and smooth the resultant etch, reduce the D_{it}, and improve electrical properties [520], [521]. As part of post etching treatment rounding of the trenching through the use of post-etch treatment would also be a desirable feature to build into future devices and hence an aspect for further development of this work.

Another aspect to look at would be the patterns which are being transferred. In this work trenches were patterned whereas smaller widths and different shaped features, could be explored, these features can be etched, as well as the profile of the etch. Another aspect is staggered or bevelled etching, which is commonly used for field plates and again for managing the electric field. These can be explored on β-Ga_2O_3 as well as other dielectrics, which are often used as part of this. A further aspect of this is also the deposition of dielectric layers onto these newly etched regions.

7.4.2 Further Work regarding Dielectrics

The first approach would be to address the issues raised regarding the comparisons, performing the same annealing ranges for Al_2O_3/Ga_2O_3 with RTA as opposed to the long thermal annealing used in this work. Another point is to perform PDA to compare to the PMA performed in this work. This is to provide a direct comparison to these more common annealing conditions allowing for a comparison to be made.

In the literature pre-deposition treatments have been shown to improve D_{it}, therefore further work could be done by repeating and comparing with one another. In this regard, introducing cleaning stages such as acid cleans, particularly piranha, has been shown to improve the interface. HF-buffer cleans as well as plasma cleaning also remains as options to determine if they reduce the amount of trapped charge.

There are other post-deposition treatments which are open for further work on this topic, in this work long furnace PMA whereas a comparison to RTA as well as PDA and PMA comparisons also can be made. Annealing conditions are also an aspect which can be developed, as the work here was performed in N_2, so opening this up to different environments is an aspect which can be developed. ALD

deposited Al_2O_3 have been the main focus, however, this can be expanded to compare other deposition methods.

An alternative route to develop is to use a different CV analysis to investigate the sample, as the Terman method is not the most accurate way to calculate the D_{it}. This is not to say that the Terman method is invalid, it is useful for comparisons for shallow D_{it}.

The High-Low method, is very similar to the Terman, whereas in the Terman an experimental high frequency curve is compared to an idealised curve, in the High/Low it is instead compared to low frequency, so that the interface traps have time to charge and be used instead of the ideal model. This is inherently more accurate to make no assumptions about the sample, that is being directly measured so the differences are because of D_{it} and not an inaccuracy of the model. This, while requiring more time, yields more accurate results for D_{it}. UV assisted CV has been used to probe wide bandgap semiconductors like SiC and GaN. UV can be used to generate electron-hole pairs, this enables trapped states throughout the band gap to react to the measurement. Purely high frequency techniques such as the Terman method underestimates the D_{it}, as these states are not filled during the sweep.

Because of the electron-hole generation rate in WBG semiconductors the inversion layer would take a long time to be filled with room temperature measurements. This time can be dramatically reduced to a experimental reasonable time by either high temperature measurements or illumination under UV. Therefore the hysteresis of illuminated and dark measurement can be used to determine the D_{it} of the deep level states. This is applicable to β-Ga_2O_3 where the low hole generation rate in n-type β-Ga_2O_3 limits the range which the bandgap can be probed to shallow energy levels.

7.4.3 Further Development regarding Ohmic contacts

The natural continuation of this work would be to continue the study, on Ohmic contacts, however, on an n^+ epitaxial layer with a doping of the order of 5×10^{18} cm^{-3} or higher. Ideally on semi-insulating or on an n^- so it was homo-epitaxial growth with the semi-insulating layer drift region with a doping of the order of 10^{16} cm^{-3}. This could be achieved by N^+ epitaxial layer onto semi-insulating or even a hetero-structure on a substrate such as sapphire α-Al_2O_3. The epi-layer should fulfil the conduction in Equation 3.17. This would allow for direct comparisons between Ti/Au, Ti/Ag, Ti/Al and Ti/W, as the contact resistances for each could be separated out. Alongside the CTLM test structures it would also be important to confirm the carrier concentration, this could be done by fabricating MIS test structures on die cut from the same wafer. Alternatively hall measurements could be used over MIS capacitors, another alternative is to use a Schottky CV measurement. This could be done with a Hg-probe before the wafer is diced, or deposit a Schottky contact onto a die after the formation of the ohmic contact, or two Schottky contacts where one contact is a much larger size to the other. This is in order to make sure that the layer of interest is highly doped, so that the current is confined with this layer.

LIST OF PUBLICATIONS

- Conference, "Ultra-wide bandgap oxides (UWO) 2023", Bristol, UK, Poster Presentation, "β-Ga_2O_3 Processing: An Investigation of Advanced Gate Dielectrics", Jacob Asher[1], Jacob Mitchel[1], Jon Evans[1], Dan Gillard[1], Stefan Zeiske[1], Antonio Martinez[1], Craig Fisher[1], Zeyu Chi[2], Ekaterine Chikoidze[2], Amador Perez-Tomas[3], Mike Jennings[1]

  1. Bay Campus, College of Engineering, Swansea University, Fabian Way, Crymlyn Burrows, Swansea SA1 8EN, UK,
  2. GEMaC, CNRS, Université Paris-Saclay, France,
  3. Catalan Institute of Nanoscience and Nanotechnology (ICN2), CSIC and The Barcelona Institute of Science and Technology, Barcelona, Spain

- Paper, "Ga_2O_3 and Related Ultra-Wide Bandgap Power Semiconductor Oxides: New Energy Electronics Solutions for CO_2 Emission Mitigation", Materials 2022, 15(3), 1164; https://doi.org/10.3390/ma15031164, by Zeyu Chi[1], Jacob J. Asher[2],Michael R. Jennings[2],Ekaterine Chikoidze[1] and Amador Pérez-Tomás[3].

  1. GEMaC, CNRS, Université Paris-Saclay, France,
  2. Bay Campus, College of Engineering, Swansea University, Fabian Way, Crymlyn Burrows, Swansea SA1 8EN, UK,
  3. Catalan Institute of Nanoscience and Nanotechnology (ICN2), CSIC and The Barcelona Institute of Science and Technology, Barcelona, Spain

Appendices

APPENDIX A

APPENDIX FOR CHAPTER 4

This is the appendix for Chapter 4, this chapter holds the ellipsometry mapping data and fitting parameters which were used to find the thicknessers of the ECI 3024 and SiN_x films. The entire set of SEM images used in the development of the protocol at different UV doses. Then some of the SEM images of the β-Ga_2O_3 cross-sections post development. A table of values generated from image-J to find estimate the etching results for the β-Ga_2O_3, as there were only two images these tables are not reliable. Finally there is the process flow diagram for the work performed in the Chapter 4.

A.1 Appendix ECI 3000 PR Spinning

In this work, ECI 3000 was spun at different speeds to determine the optimal speed for the desired thickness. Changing the spin speed has two main effects, the slower the speed the thicker the film. This comes at a cost of less uniformity and larger edge beads. In this work the photoresist was spun at 3000, 4000 and 5000 rpm. The samples were then measured using the ellipsometer described in Section 3.1.10. The samples then had a Cauchy film modelled to them to measure the thickness of the photoresist. The results can be seen in Tables A.1, A.2 A.3 and Figures A.1, A.2 A.3. From these results, it can be seen that the increase in spin speed did not result in much greater uniformity across the wafer and so the spin speed was chosen to be 4000 rpm.

Parameter	**Average**	**Min.**	**Max.**	**Std. Dev.**
MSE	13.4	11.98	16.93	1.541
Thickness # 1 (nm)	1996.6	1977.32	2020.99	13.39
A	1.6032	1.6008	1.6086	0.0023
B	0.014	0.0117	0.0146	0.0008
C	-0.0004	-0.0006	0.0002	0.0002
n of Cauchy Film @ 632.8 nm	1.6358	1.6333	1.642	0.0022

Table A.1: The fitting parameters for the Cauchy model used to measure the thickness of the ECI spun at 5000 rpm.

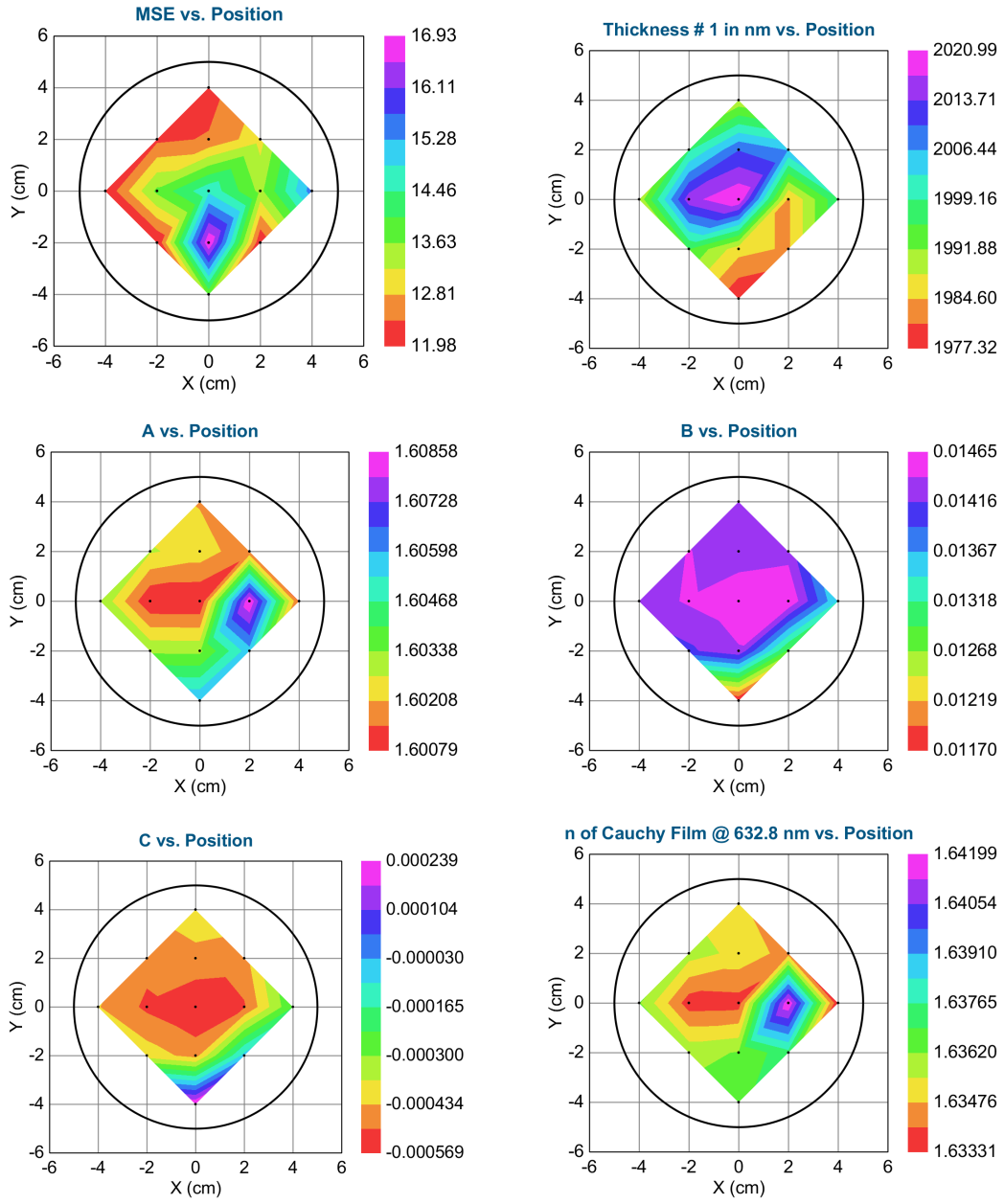


Figure A.1: The photoresist across the wafer after being spun at 5000 rpm. The film had a measured film thickness of 1977.32 nm. This was on Si.

Parameter	Average	Min.	Max.	Std. Dev.
MSE	35.708	11.662	175.131	53.936
Thickness # 1 (nm)	2249.42	1933.09	2310.26	130.72
A	1.6388	1.601	1.8312	0.0847
B	0.0149	0.0125	0.0191	0.0014
C	-0.0007	-0.0028	0.0008	0.0008
n of Cauchy Film @ 632.8 nm	1.6718	1.6338	1.8674	0.0848

Table A.2: The fitting parameters for the Cauchy model used to measure the thickness of the ECI spun at 4000 rpm.

Parameter	Average	Min.	Max.	Std. Dev.	% Range
MSE	202.219	202.032	202.727	0.194	0.344
Thickness # 2 (nm)	2601.93	2590.34	2611.46	7.13	0.8118
Thickness # 2 (nm)	2601.93	2590.34	2611.46	7.13	0.8118
A	1.6250	1.6228	1.6265	0.0011	0.2316
B	0.0137	0.0131	0.0142	0.0003	7.6344
C	0.0003	0.0002	0.0004	0.0001	67.5093
n of Cauchy @ 632.8 nm	1.4750	1.4750	1.4750	0.0000	0.0000

Table A.3: The fitting parameters for the Cauchy model used to measure the thickness of the ECI spun at 3000 rpm.

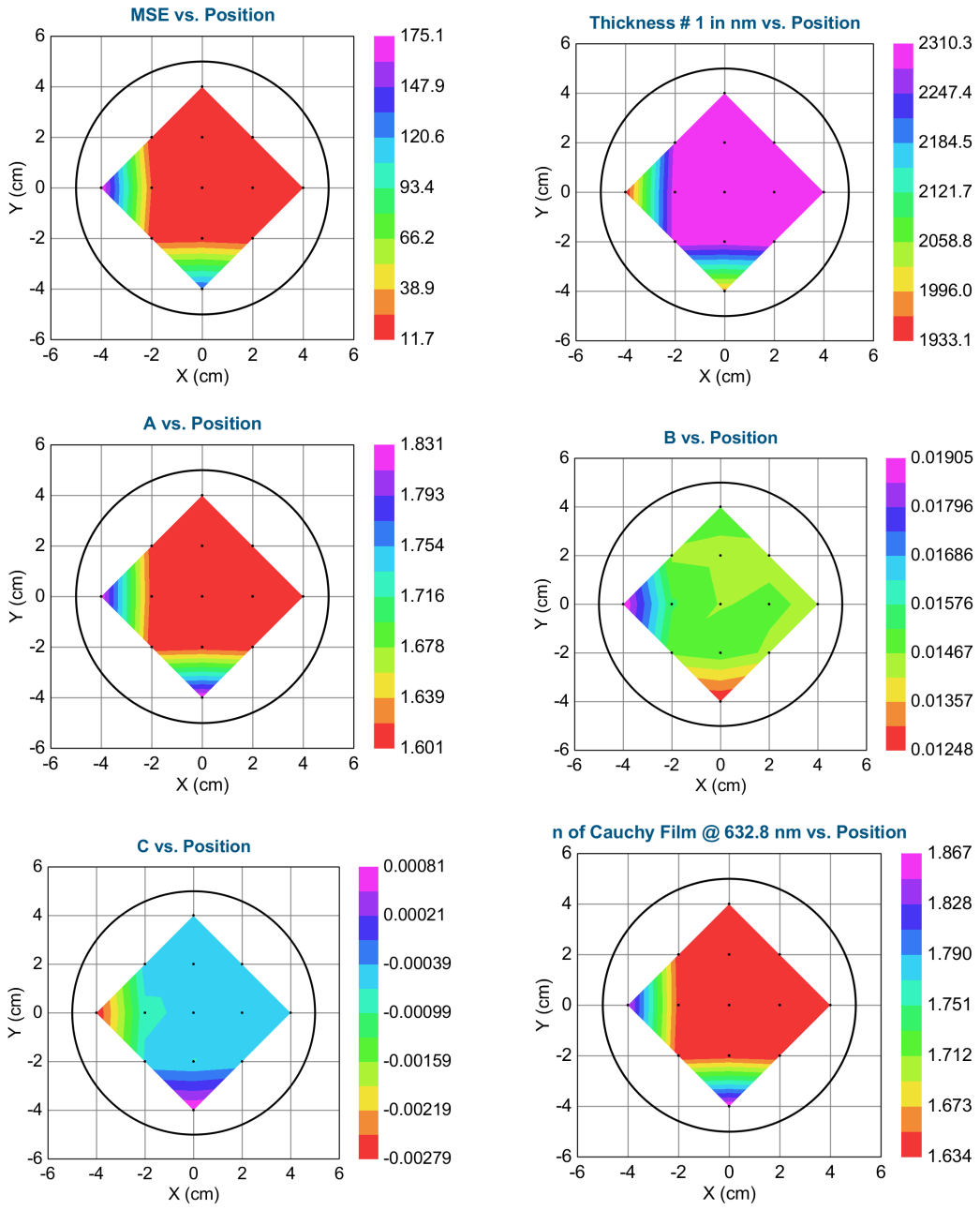


Figure A.2: The photoresist across the wafer after being spun at 4000 rpm. The film had a measured film thickness of 1978.84 nm. This was on Si.

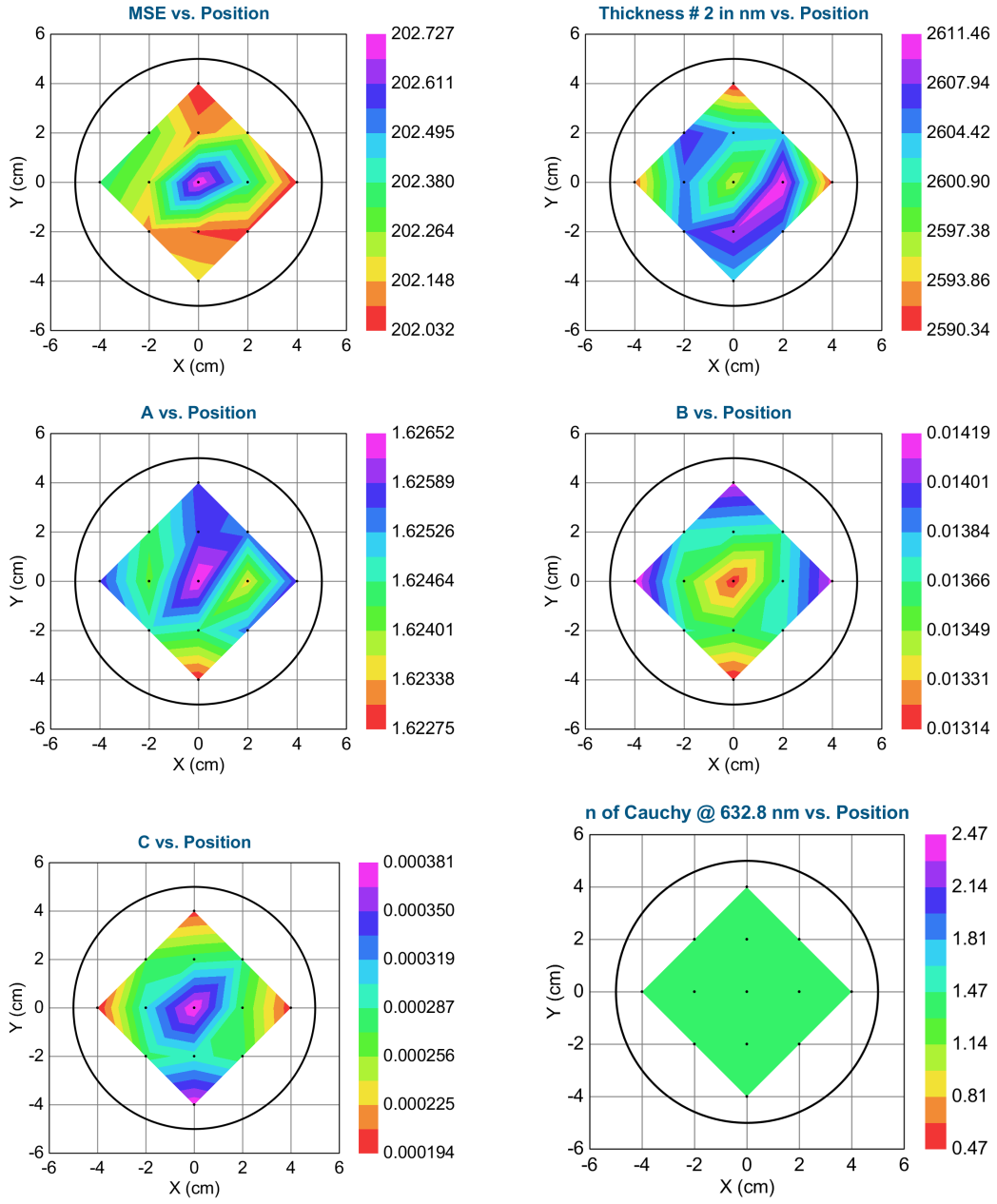


Figure A.3: The photoresist across the wafer after being spun at 3000 rpm. The film had a measured film thickness of 2600 nm. This was on Si.

A.2 Appendix SiN_x thickness

As part of the work in Chapter 4 in order to confirm the SiN deposited onto the sample the Si/SiN sample was measured on the ellipsometer as mentioned in Section 3.1.10. This was to confirm that the sample had 1 μm of SiN deposited onto the surface. The results and fitting parameters can be seen in Table A.4 and Figure A.4. It can be seen that the thickness of the deposited SiN_x layer was 990 nm.

Parameter	**Average**	**Min.**	**Max.**	**Std. Dev.**
MSE	11.183	10.364	16.519	1.135
Thickness (nm)	990.58	984.16	999.58	4.46
A	1.9502	1.9461	1.957	0.002
B	0.0311	0.0291	0.0316	0.0005
C	0.0004	0.0002	0.0008	0.0001
n of Cauchy Film @ 632.8 nm	2.0301	2.0253	2.0373	0.002

Table A.4: The fitting parameters used for measuring the SiN_x on Si, the Si sample was measured as a spectator wafer for β-Ga_2O_3. This is because of the difficulty in measuring on transparent substrates.

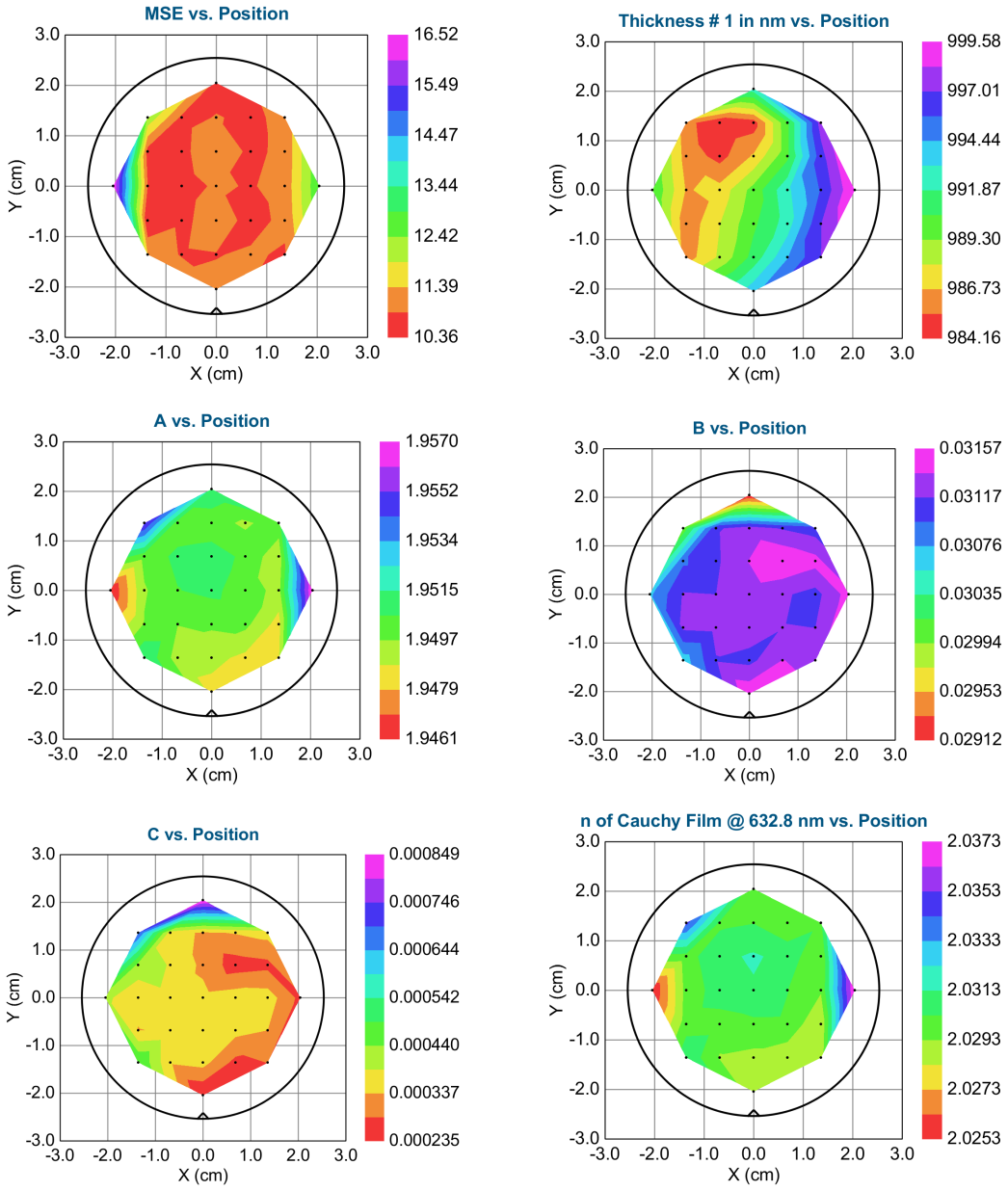


Figure A.4: The result of the ellipsometry measurement across the Si/SiN_x wafer. The measured thickness of the SiN can be seen across the wafer.

A.3 SEM images of Al_2O_3

The SEM images of the development for ECI 3024 on α-Al_2O_3, these are dosed with different UV light.

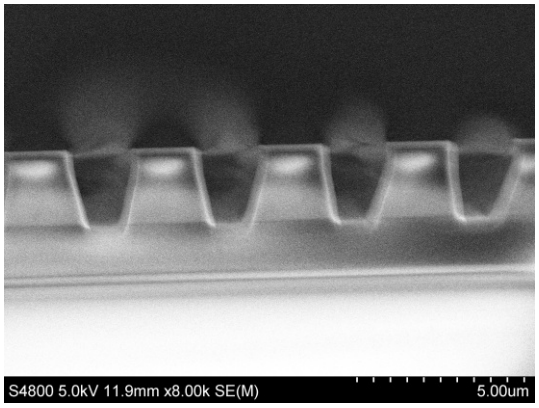


Figure A.5: SiN_x/α-Al_2O_3 trench profile, ECI 3024, UV dose 150 mJ $\cdot$ cm^{-2}.

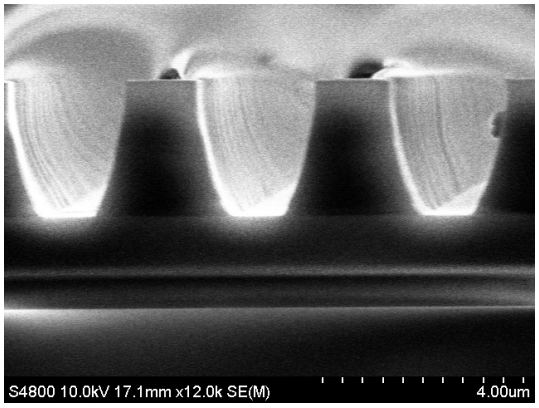
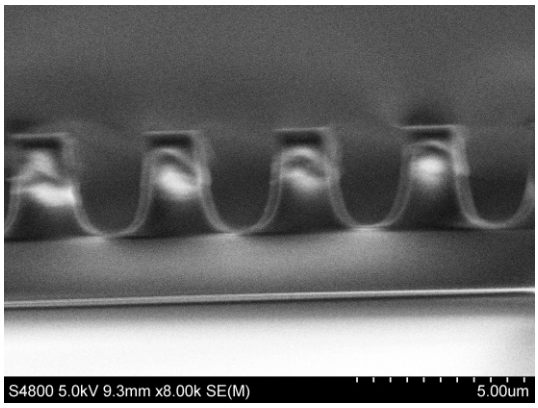


Figure A.6: SiN_x/α-Al_2O_3 trench profile, ECI 3024, UV dose 210 mJ $\cdot$ cm^{-2}.



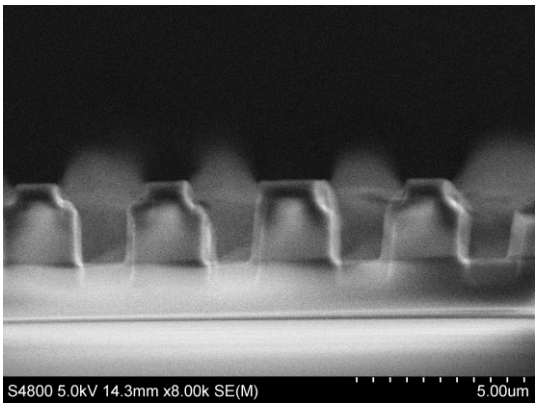


Figure A.7: SiN_x/α-Al_2O_3 trench profile, ECI 3024, both with a UV dose 220 mJ $\cdot$ cm^{-2}.

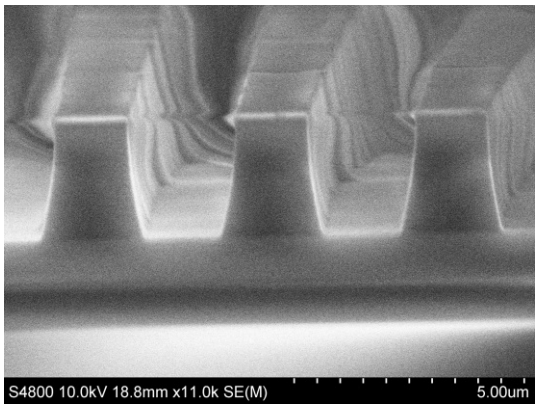


Figure A.8: SiN_x/α-Al_2O_3 trench profile, ECI 3024, UV dose 230 mJ $\cdot$ cm^{-2}.

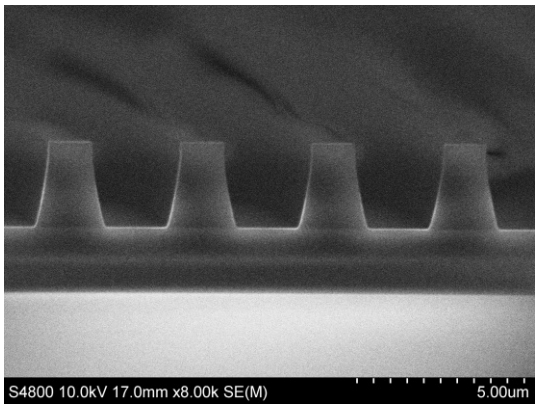


Figure A.9: SiN_x/α-Al_2O_3 trench profile, ECI 3024, UV dose 270 mJ $\cdot$ cm^{-2}.

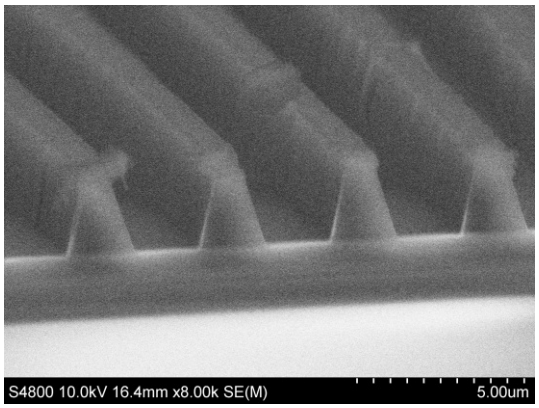


Figure A.10: SiN_x/α-Al_2O_3 trench profile, ECI 3024, UV dose 290 mJ $\cdot$ cm^{-2}.

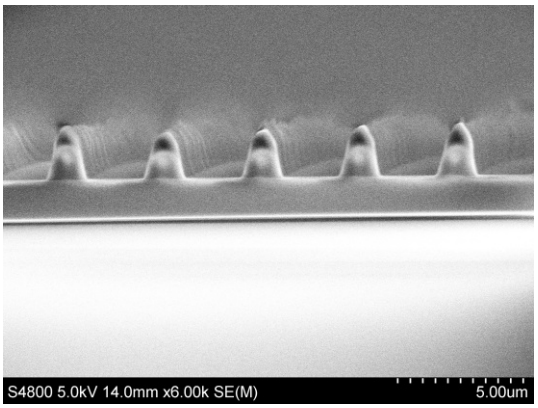
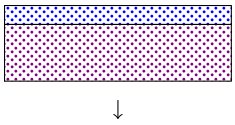


Figure A.11: SiN_x/α-Al_2O_3 trench profile, ECI 3024, UV dose 350 mJ $\cdot$ cm^{-2}.

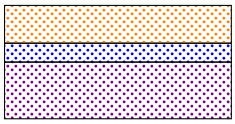
A.4 Etch Process Flow

The basic process flow used for process for etching in Chapter 4. This is just a photoresist process flow, this is assuming that the sample already has the hard mask SiN_x depositioned.

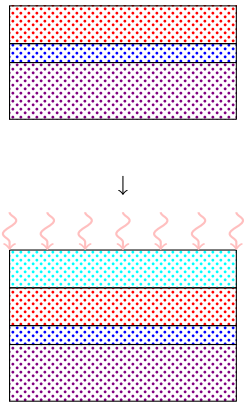
- The semiconductor substrate is solvent cleaned.
  - Submerged in acetone for 10 minutes.
  - Submerged in IPA for 5 minutes
  - Dry with N_2.



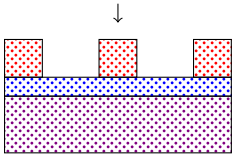
- Ti-prime is spun onto the sample, Ti-prime is an adhesive agent onto the sample.
- Baked at 120°C for 120 s.



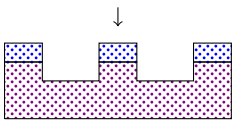
- ECI-3024 is spun onto the sample at: 3000 rpm, acceleration 1000 for 45 s.
- Baked at 100°C for 180 s.



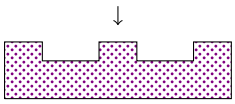
- Exposed to 210 mJ $\cdot$ cm^{-2} of UV i-line.
- Baked at 100°C for 180 s.



- Developed sample:
  - AZ 726 60 s.
  - AZ 726 : DI water (1:2) for 10 s.
  - DI water, two times for 10 s.
  - Dry with N_2



- Etch sample, KLA process.



- Remove the hard mask, SiN_x, hot phosphoric acid.

End of the Etch process

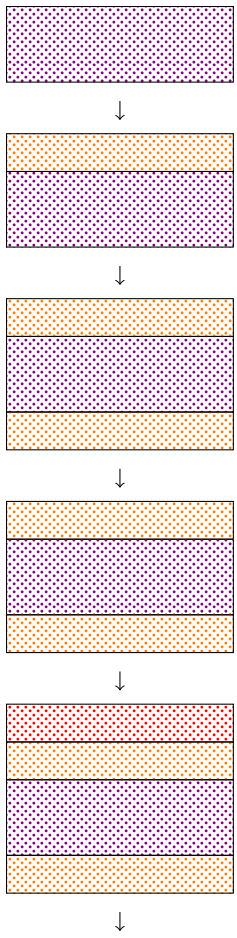
APPENDIX B

APPENDIX FOR CHAPTER 5

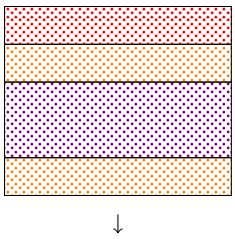
B.1 Appendix MIS Process Flow

The process flow used to fabricate MIS-capacitors, was use in this work. This is repeated for both sides of the wafer.

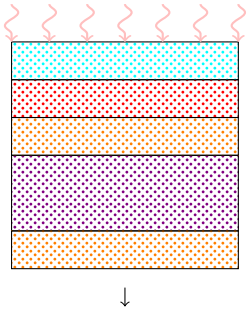
- The semiconductor substrate is solvent cleaned
- In the PECVD SiO_2 was deposited.
- The sample is flipped and in the PECVD SiO_2 was deposited.
- Solvent clean the sample & pre-bake the sample at 150°C for about 10 minutes.
- Spin Ti-prime, an adhesive agent onto the sample & bake at 120°C for 120s.



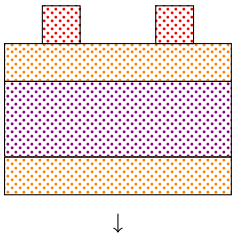
- Spin photoresist (AZ-LNR-003), onto the sample & bake at 110°C for 60s.



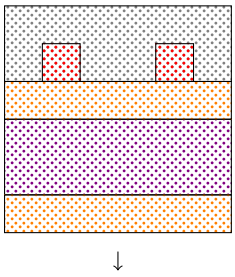
- On a mask aligner, expose to 130 mJ $\cdot$ cm^{-2} of UV, then bake at 110°C for 80s.



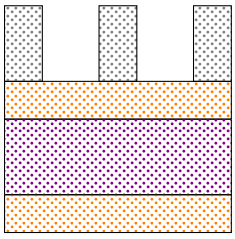
- Develop the photoresist in a solution of 2:1 AZ-developer:DI-water for 230 s. Then rinse in a solution of 1:2 AZ-developer:DI water for 15 s. Then rinse In DI-water twice.



- Deposit metal onto the sample using the PVD, in this case Ti/Al/Ti/Au at 25/100/25/20 nm.



- The metal is lifted off with D350, leaving behind the patterned metal contact.



B.2 Microscope Imaging

In this section are all the images used to determine the contact size of the MIS structure used in this work.

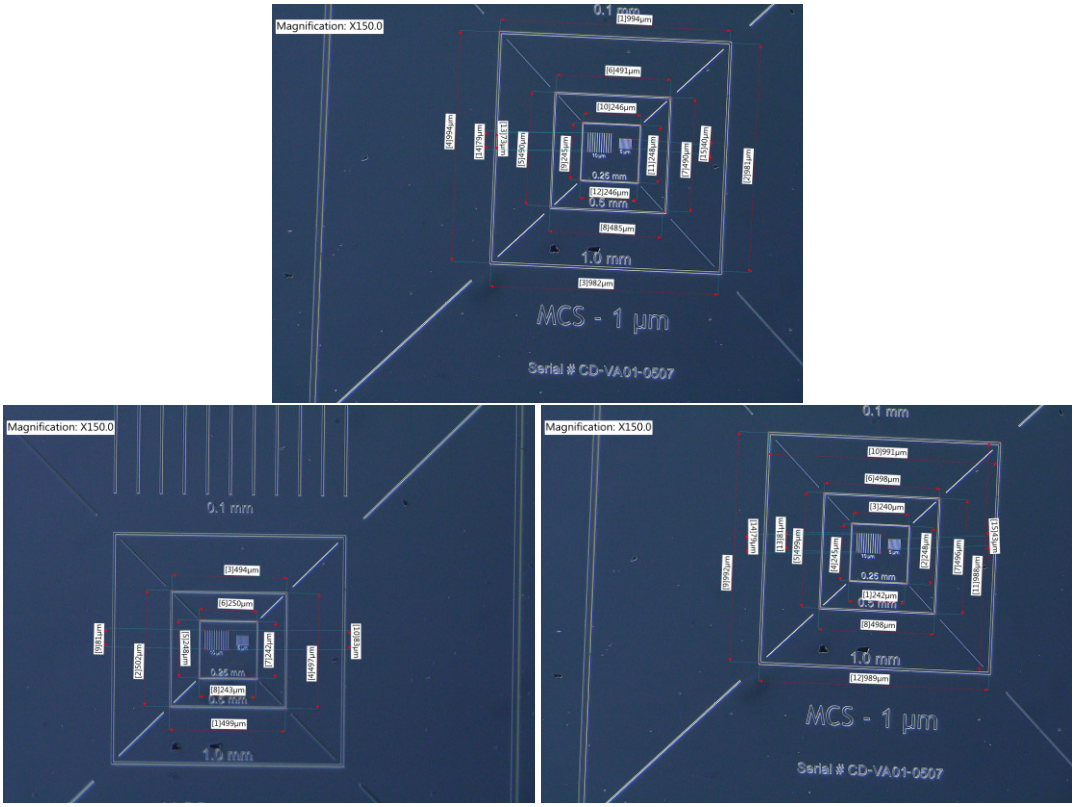


Figure B.1: This is a known piece of Si with known sizes measured on it, this means it is useful for determining the true size of features under the microscope. As you can see the measurements made on the Keynesk microscope and software closely match those of the known sample. As expected the smaller the feature the more inaccurate they become, however, it at most was around 20 µm and more commonly was 5 to 10 µm out.

B.3 Ellipsometry - Dielectric

The fitting parameters for the native oxide and deposited dielectrics on Si, this was used to calibrate that the dielectric deposition worked and the amount deposited. As β-Ga_2O_3 is opaque this was only performed on the Si wafers and not the β-Ga_2O_3. This deposited value was still used as it was a non-destructive test, this was performed on before the deposition and after however not after annealing the samples.

Wafer 12-pre-deposition					
Parameter	**Average**	**Min.**	**Max.**	**Std. Dev.**	**% Range**
MSE	0.629	0.614	0.659	0.014	7.159
Native Oxide (nm)	1.37	1.35	1.4	0.01	3.2114
Angle Offset	0.0333	0.0248	0.0498	0.0064	75.0439
MSE	0.629	0.614	0.659	0.014	7.159
Wafer 12-post-deposition					
Parameter	**Average**	**Min.**	**Max.**	**Std. Dev.**	**% Range**
MSE	1.256	1.182	1.392	0.071	16.675
Thickness 1 (nm)	50.2	49.87	50.41	0.15	1.0667
A	1.6235	1.6106	1.6339	0.0055	1.4303
B	0.0024	-0.0002	0.0058	0.0014	254.0249
C	0.0003	0.0001	0.0006	0.0001	144.2589
n of Cauchy Film @ 632.8 nm	1.6314	1.6255	1.6367	0.0027	0.6866

Table B.1: The fitting parameters for Si_{12}, pre and post deposition of Al_2O_3.

Wafer 13-pre-deposition					
Parameter	**Average**	**Min.**	**Max.**	**Std. Dev.**	**% Range**
MSE	0.615	0.605	0.638	0.009	5.33
Native Oxide (nm)	1.37	1.35	1.4	0.02	3.7373
Angle Offset	0.0338	0.0267	0.0481	0.0049	63.3097
Wafer 13-post-deposition					
Parameter	**Average**	**Min.**	**Max.**	**Std. Dev.**	**% Range**
MSE	1.29	1.235	1.356	0.028	9.348
Thickness # 1 (nm)	51.16	50.77	51.6	0.26	1.6347
A	1.4849	1.4769	1.4906	0.0031	0.9233
B	0.0029	0.0017	0.0045	0.0006	94.7046
C	0.0001	-0.0001	0.0002	0	373.745
n of Cauchy Film @ 632.8 nm	1.4926	1.4878	1.496	0.0019	0.5444

Table B.2: The fitting parameters for Si_{13}, pre and post deposition of SiO_2.

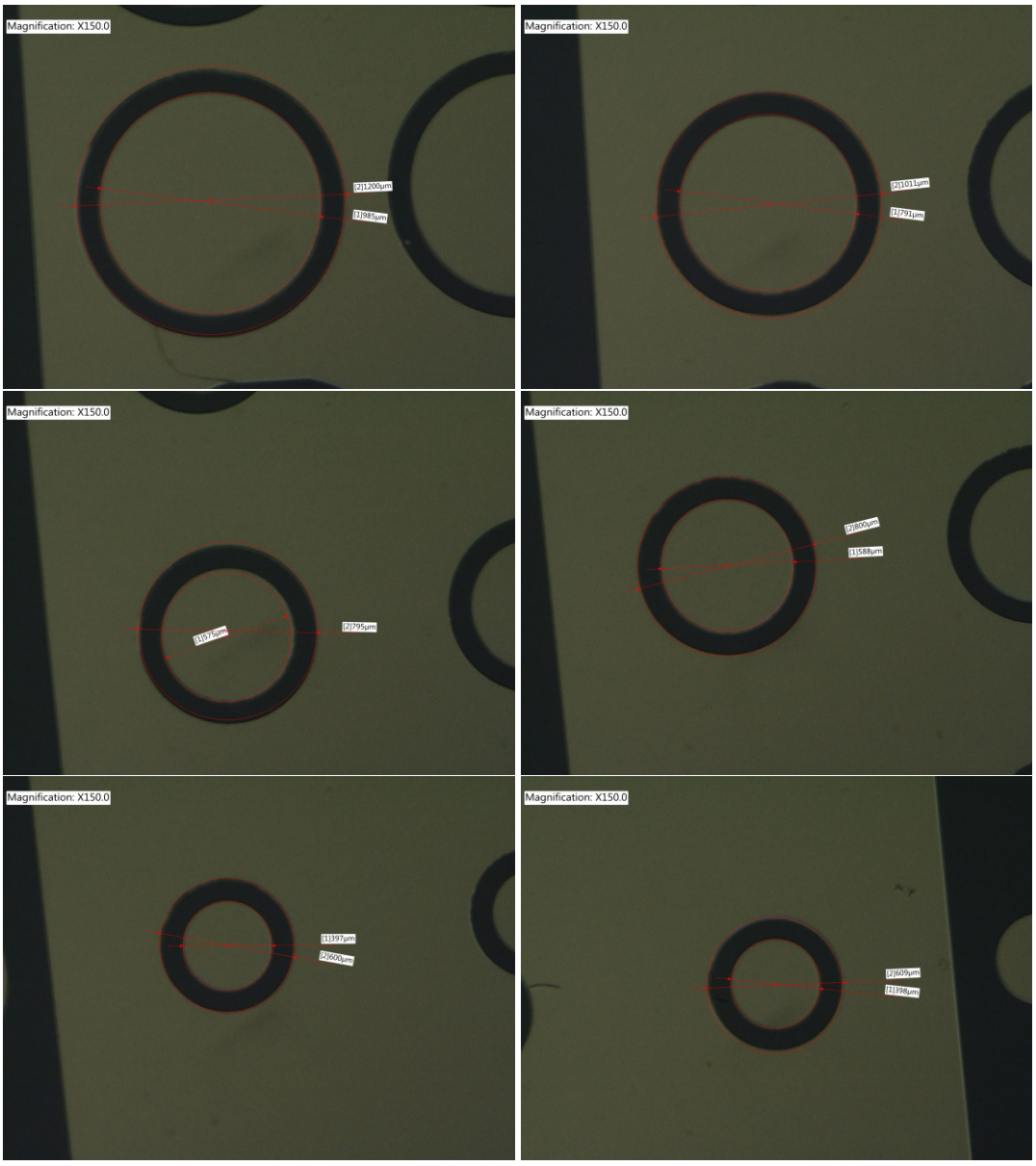


Figure B.2: These are images of different sized features Si-Al_2O_3 wafer, the spacing between the two should be 200 µm and the device sizes go from 600 to 1000 µm in steps of 200 µm. These were taken across the wafer to get an idea of the feature size. They seem to be around 10 µm smaller but does go up to 25 µm. This seems to be consistent with B.1.

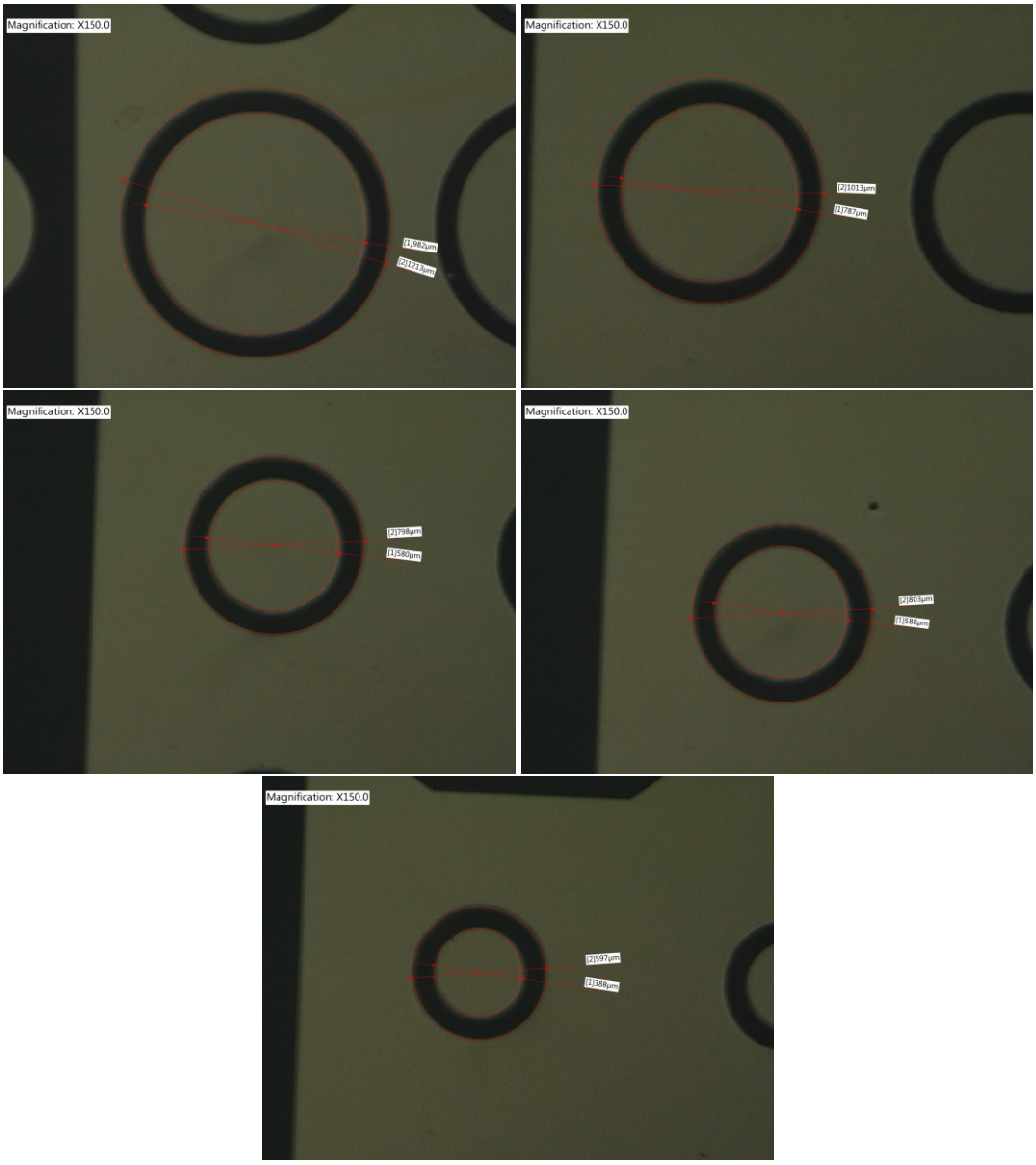


Figure B.3: These are images of different sized features Si-SiO_2 wafer, the spacing between the two should be 200 μm and the device sizes go from 600 to 1000 μm in steps of 200 μm. These were taken across the wafer to get an idea of the feature size. In this case the feature sizes seem to be generally 10 to 20 μm smaller, this is a slight difference between this and the calibration sample B.1 indicating these are slightly smaller.

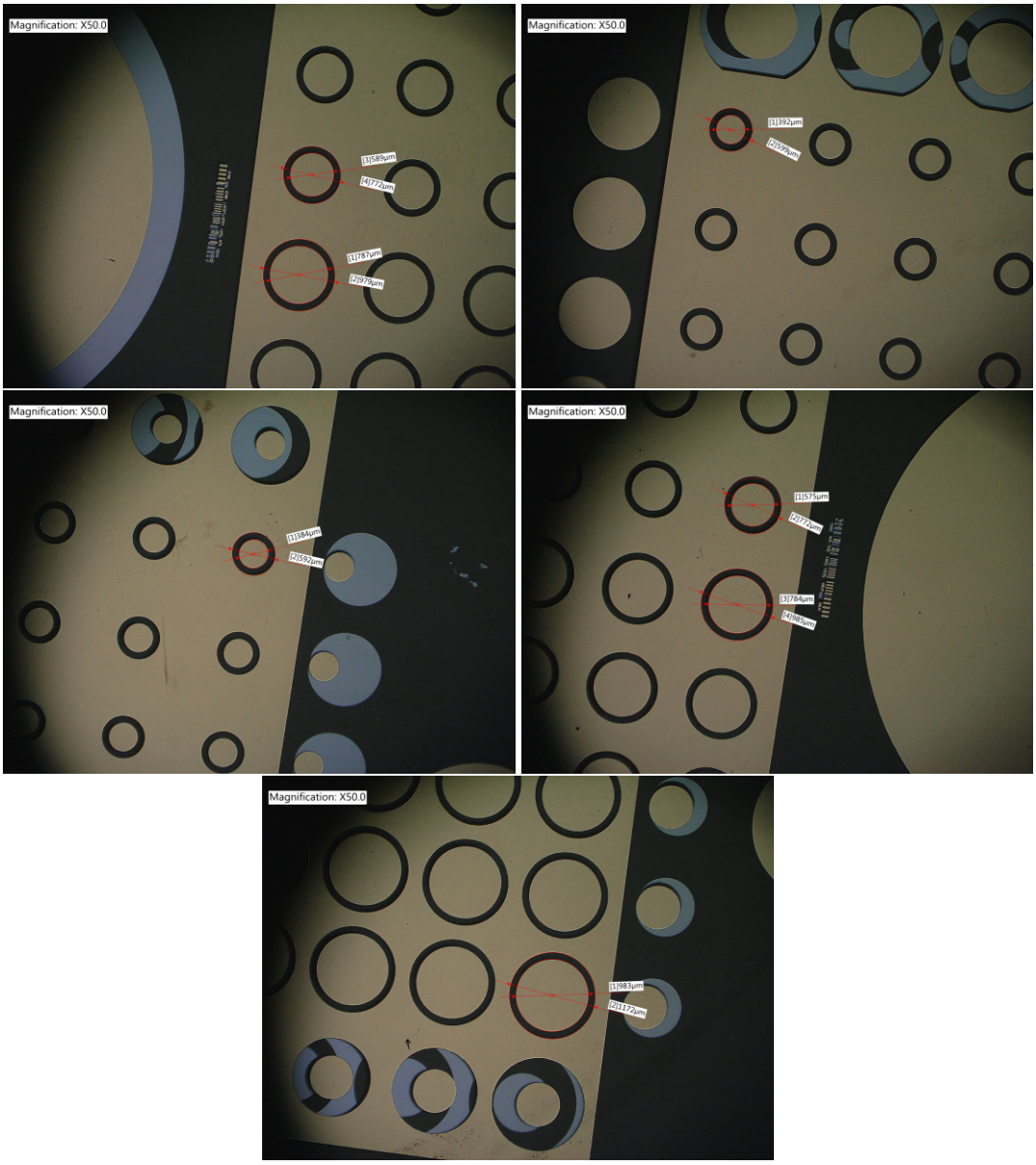


Figure B.4: These are images of different sized features on the top side of the β-Ga_2O_3-Al_2O_3 wafer, the spacing between the two should be 200 μm and the device sizes go from 600 to 1000 μm in steps of 200 μm. These were taken across the wafer to get an idea of the feature size. In this case the feature sizes seem to be generally 10 to 25 μm smaller, this is a slight difference between this and the calibration sample B.1 indicating these are slightly smaller.

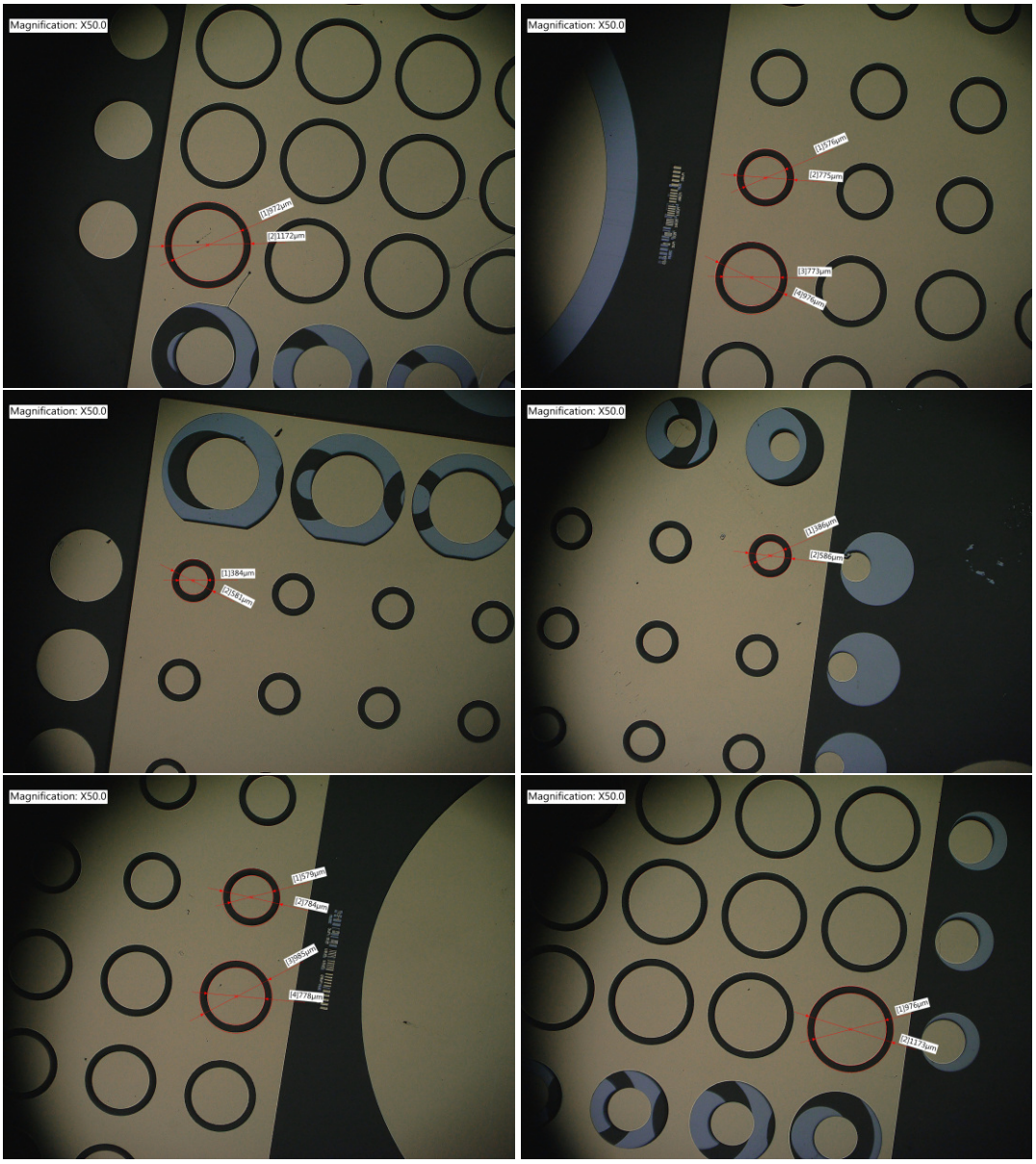


Figure B.5: These are images of different sized features on the bottom side of the β-Ga_2O_3-Al_2O_3 wafer, the spacing between the two should be 200 μm and the device sizes go from 600 to 1000 μm in steps of 200 μm. These were taken across the wafer to get an idea of the feature size. In this case the feature sizes seem to be generally 15 to 25 μm smaller, this is a slight difference between this and the calibration sample B.1 indicating these are slightly smaller.

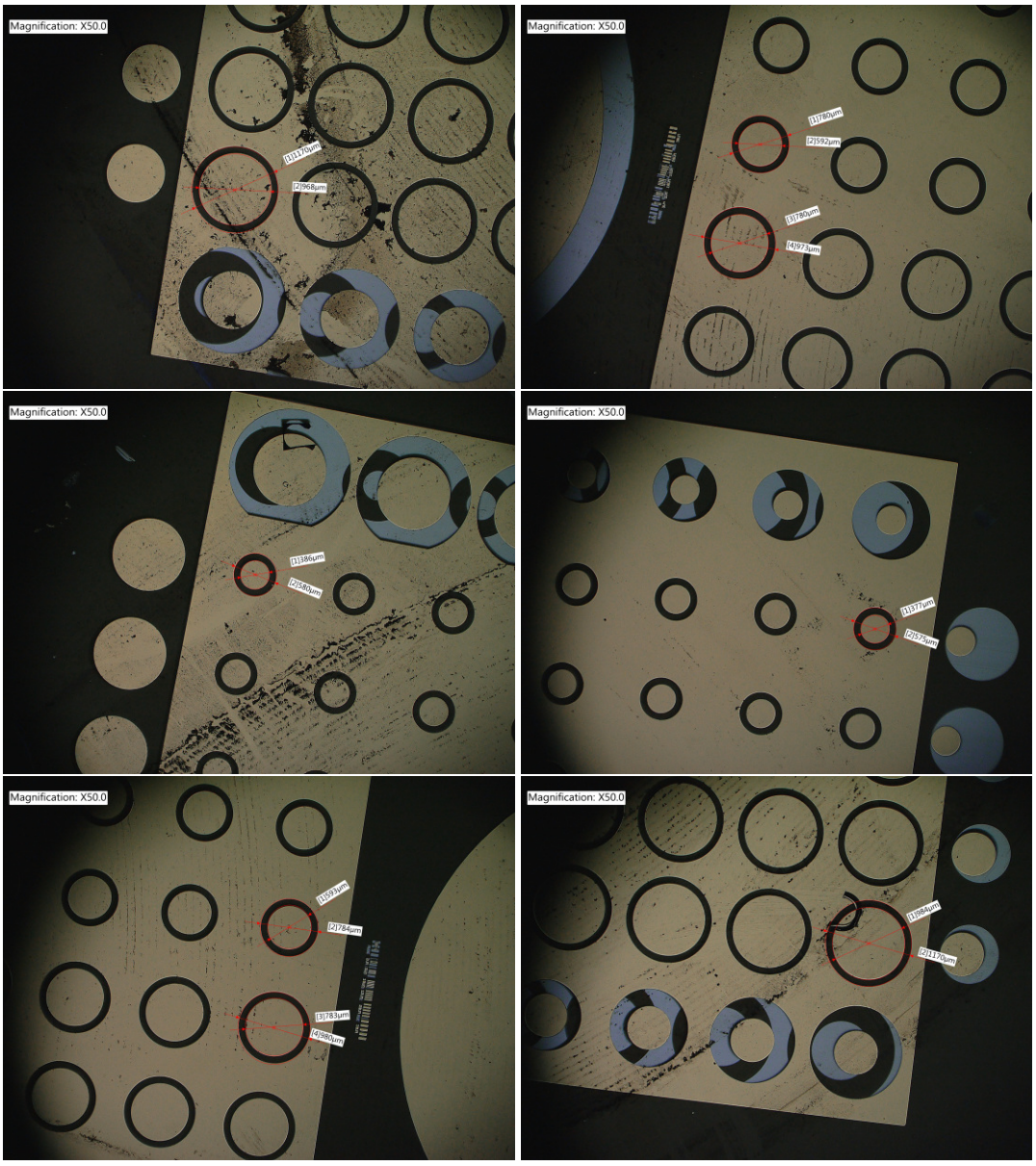


Figure B.6: These are images of different sized features on the top side of the β-Ga_2O_3-SiO_2 wafer, the spacing between the two should be 200 µm and the device sizes go from 600 to 1000 µm in steps of 200 µm. These were taken across the wafer to get an idea of the feature size. These were taken across the wafer to get an idea of the feature size. In this case the feature sizes seem to be generally 10 to 25 µm smaller, this is a slight difference between this and the calibration sample B.1 indicating these are slightly smaller. The black marks are likely burned photoresist.

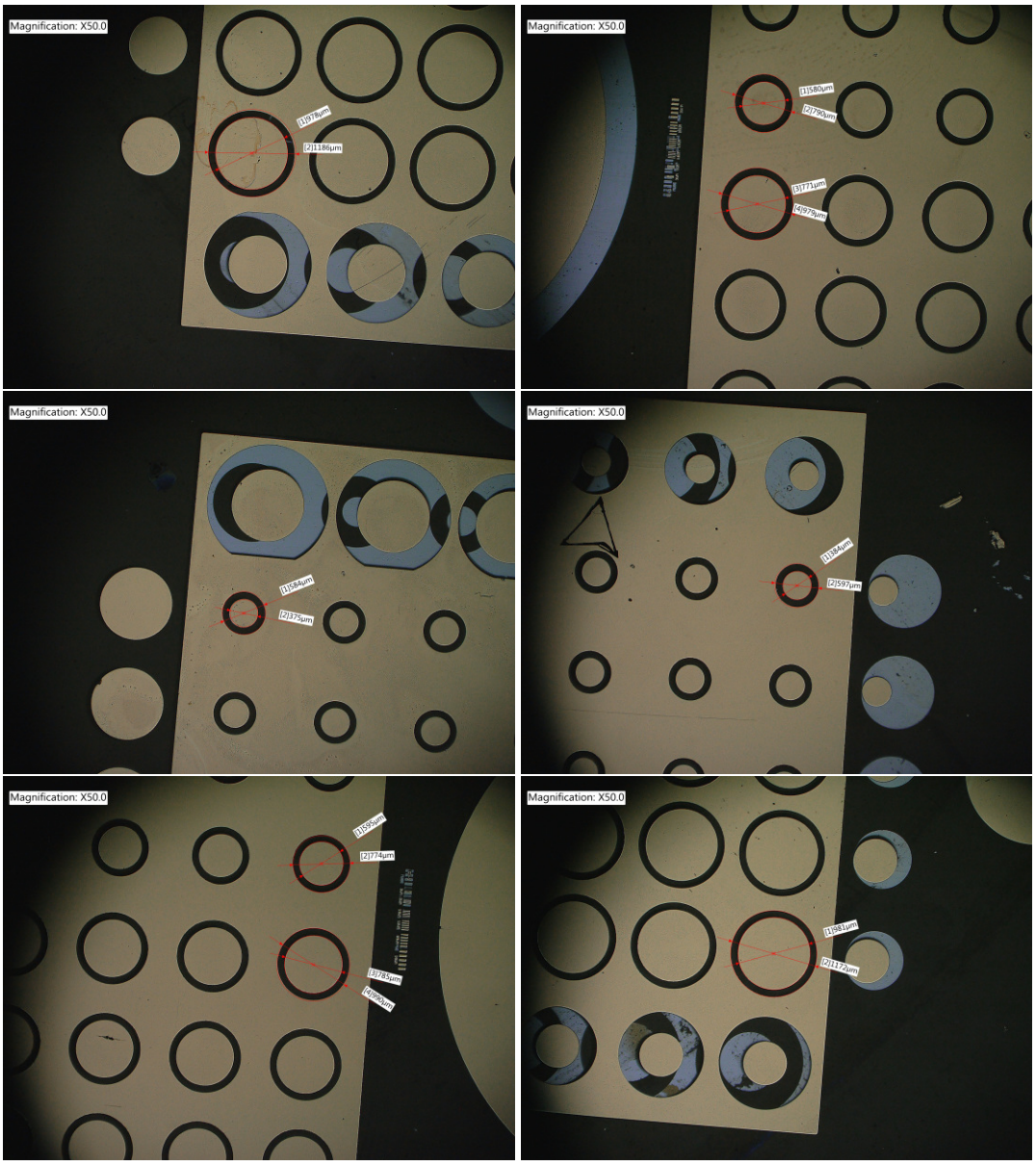


Figure B.7: These are images of different sized features on the bottom side of the β-Ga_2O_3-die wafer, the spacing between the two should be 200 µm and the device sizes go from 600 to 1000 µm in steps of 200 µm. These were taken across the wafer to get an idea of the feature size. These were taken across the wafer to get an idea of the feature size. In this case the feature sizes seem to be generally 10 to 20 µm smaller, this is a slight difference between this and the calibration sample B.1 indicating these are slightly smaller.

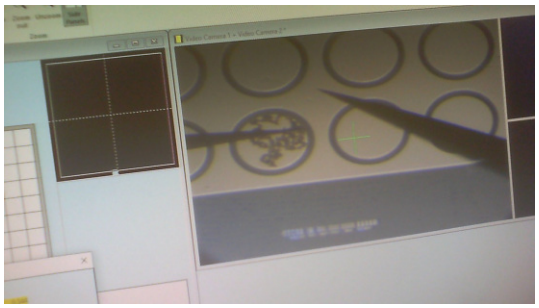


Figure B.8: An example contact on metal/Al_2O_3/β-Ga_2O_3 after too high of voltage applied and the contact subsequently broke down.

Wafer 14-pre-deposition					
Parameter	**Average**	**Min.**	**Max.**	**Std. Dev.**	**% Range**
MSE	0.616	0.596	0.644	0.014	7.686
Native Oxide (nm)	1.37	1.35	1.4	0.02	3.731
Angle Offset	0.0342	0.0267	0.0555	0.0071	84.1651
Wafer 14-post-deposition					
Parameter	**Average**	**Min.**	**Max.**	**Std. Dev.**	**% Range**
MSE	1.29	1.224	1.416	0.056	14.845
Thickness # 1 (nm)	50.67	50.28	51.08	0.26	1.5776
A	1.4857	1.4752	1.4931	0.0039	1.2106
B	0.0027	0.0011	0.005	0.0008	143.1067
C	0.0001	-0.0001	0.0002	0.0001	397.2207
n of Cauchy Film @ 632.8 nm	1.4931	1.487	1.4973	0.0022	0.6885

Table B.3: The fitting parameters for Si_{14}, pre and post deposition of SiO_2.

Wafer 15-pre-deposition					
Parameter	**Average**	**Min.**	**Max.**	**Std. Dev.**	**% Range**
MSE	0.616	0.605	0.645	0.013	6.622
Native Oxide (nm)	1.37	1.35	1.4	0.01	3.35
Angle Offset	0.0362	0.0287	0.0574	0.0068	79.2379
Wafer 15-post-deposition					
Parameter	**Average**	**Min.**	**Max.**	**Std. Dev.**	**% Range**
MSE	1.242	1.186	1.453	0.066	21.458
Thickness # 1 (nm)	49.94	49.61	50.19	0.14	1.1737
A	1.6242	1.6163	1.636	0.0042	1.2118
B	0.0022	-0.0009	0.0044	0.0011	236.7223
C	0.0003	0.0002	0.0006	0.0001	132.0376
n of Cauchy Film @ 632.8 nm	1.6319	1.6283	1.6377	0.002	0.5788

Table B.4: The fitting parameters for Si_{15}, pre and post deposition of Al_2O_3.

Wafer 16-pre-deposition					
Parameter	**Average**	**Min.**	**Max.**	**Std. Dev.**	**% Range**
MSE	0.696	0.616	1.269	0.173	93.801
Native Oxide (nm)	1.37	1.34	1.42	0.02	5.6244
Angle Offset	0.0624	0.023	0.0893	0.0152	106.3725
Wafer 16-post-deposition					
Parameter	**Average**	**Min.**	**Max.**	**Std. Dev.**	**% Range**
MSE	1.229	1.146	1.423	0.064	22.566
Thickness # 1 (nm)	50.2	49.96	50.59	0.19	1.26
A	1.4753	1.4663	1.483	0.0035	1.129
B	0.0026	0.001	0.0044	0.0007	135.3493
C	0.0001	0	0.0003	0.0001	292.3029
n of Cauchy Film @ 632.8 nm	1.4823	1.4771	1.4869	0.0021	0.662

Table B.5: The fitting parameters for Si_{16}, pre and post deposition of SiO_2.

Wafer 17-pre-deposition					
Parameter	**Average**	**Min.**	**Max.**	**Std. Dev.**	**% Range**
MSE	0.68	0.625	1.034	0.111	60.295
Native Oxide (nm)	1.37	1.35	1.41	0.02	4.4353
Angle Offset	0.0594	0.0291	0.0863	0.014	96.2151
Wafer 17-post-deposition					
Parameter	**Average**	**Min.**	**Max.**	**Std. Dev.**	**% Range**
MSE	1.277	1.222	1.485	0.065	20.604
Thickness # 1 (nm)	50.99	50.84	51.25	0.13	0.8061
A	1.4823	1.4742	1.4909	0.0036	1.1241
B	0.003	0.0012	0.0046	0.0008	116.8647
C	0.0001	-0.0001	0.0002	0.0001	564.729
n of Cauchy Film @ 632.8 nm	1.4901	1.4853	1.4952	0.0021	0.6599

Table B.6: The fitting parameters for Si_{17}, pre and post deposition of SiO_2.

B.4 TEM Al_2O_3

The Ga_2O_3/Al_2O_3 sample was then sent to Institut Catalá de Nanociéncia Nanotecnologia (ICN2) after the CV measurements were finished to be FIB-TEM and EDX. This was to investigate the thickness of the dielectric layer as well as the composition of the sample. It can be seen that the dielectric layer seems to have densification, of the dielectric layer. The samples were also had EDX performed on them these can be seen in figures 5.7 and 5.8. In these we can confirm that the metal deposited was Ti, Al and Au. There also appears to be a Cu single seen, this is believed to be from the TEM stage.

B.4.1 Tabulated TEM Data

Table B.7: Here are the tabulated values to calculate the thickness of the Al_2O_3. In this table the Position column the terms stand for where on the image it was taken. Where L, M or R stand for the left, middle or right side of the image, the term S is the scale bar. The scale bar is the size of the scale bar in nm. The Length is the calculated length (scale factor for S) in nm. From this data the average thickness was found to be 46.78 ± 1.69, this is excluding the lengths calculated in TEM images 4, 11 and 13. The TEM images are shown in the Appendix B.4.2.

TEM Image	**Position**	**Pixels**	Scale (nm)	**Length (nm)**
1	S	275.25	100	0.36
1	L	129.5	100	47.05
1	L	125.75	100	45.69
1	M	125.75	100	45.69
1	M	125	100	45.41
1	R	125.833	100	45.72
1	R	129.833	100	47.17
2	S	319	50	0.16
2	L	295	50	46.24
2	L	293	50	45.92
2	M	293	50	45.92
2	M	296	50	46.39
2	R	300	50	47.02
2	R	300	50	47.02
3	S	270.333	20	0.07
3	L	601	20	44.46
3	L	600	20	44.39
3	M	607	20	44.91
3	M	609	20	45.05
3	R	609	20	45.06
3	R	601	20	44.46
4	S	26.567	500	18.82
4	L	2.55	500	47.99
4	L	2.613	500	49.18
4	M	2.488	500	46.83
4	M	2.575	500	48.46
4	R	2.642	500	49.72

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Table B.7 – Continued From Previous Page

TEM Image	**Position**	**Pixels**	Scale	**Length (nm)**
4	R	2.583	500	48.61
5	S	14.867	100	6.72
5	L	7.367	100	49.55
5	L	7.367	100	49.55
5	M	6.95	100	46.75
5	M	7.033	100	47.31
5	R	7.1	100	47.76
5	R	7.333	100	49.32
6	S	41.7	50	1.20
6	L	39.1	50	46.88
6	L	34.8	50	41.73
6	M	38.4	50	46.04
6	M	37.7	50	45.20
6	R	38.7	50	46.40
6	R	38.8	50	46.52
7	S	20.95	50	2.39
7	L	19.333	50	46.14
7	L	20.033	50	47.81
7	M	19.133	50	45.66
7	M	19.133	50	45.66
7	R	19.2	50	45.82
7	R	19.2	50	45.82
8	S	23.85	20	0.83
8	L	57.8	20	48.47
8	L	57.5	20	48.22
8	M	56.4	20	47.30
8	M	55.3	20	46.37
8	R	56.8	20	47.63
8	R	56.7	20	47.55
9	S	20.85	50	2.40
9	L	20.45	50	49.04
9	L	20.65	50	49.52
9	M	19.567	50	46.92
9	M	19.367	50	46.44
9	R	18.767	50	45.00
9	R	18.933	50	45.40
10	S	82.333	100	1.22
10	L	39.375	100	47.82
10	L	40	100	48.58
10	M	37.688	100	45.78
10	M	37.938	100	46.08
10	R	36.688	100	44.56
10	R	38.375	100	46.61

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Table B.7 – Continued From Previous Page

TEM Image	**Position**	**Pixels**	Scale	**Length (nm)**
11	S	26.7	500	18.73
11	L	2.65	500	49.63
11	L	2.725	500	51.03
11	M	2.663	500	49.87
11	M	2.788	500	52.21
11	R	2.638	500	49.40
11	R	2.638	500	49.40
12	S	21.233	200	9.42
12	L	5.325	200	50.16
12	L	5.2	200	48.98
12	M	5.225	200	49.22
12	M	5.35	200	50.39
12	R	5.225	200	49.22
12	R	5.075	200	47.80
13	S	37.25	2000	53.69
13	L	1.006	2000	54.01
13	L	0.919	2000	49.34
13	M	0.9	2000	48.32
13	M	0.867	2000	46.55
13	R	0.988	2000	53.05
13	R	0.994	2000	53.37

B.4.2 TEM Images

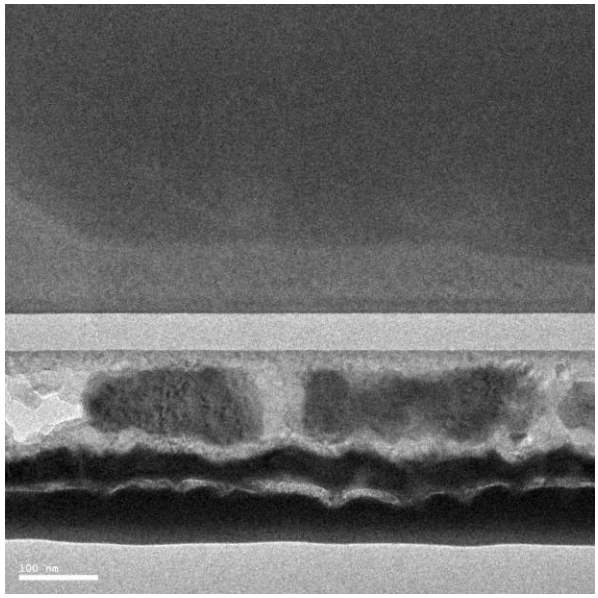


Figure B.9: Here is one of the TEM images used in this work, this is a cross-section of β-Ga_2O_3/Al_2O_3 sample. This was used to determine the thickness of the Al_2O_3 layer. This was using the scale and ImageJ and the tabulated data is seen in table B.7. In this table it is TEM image 1

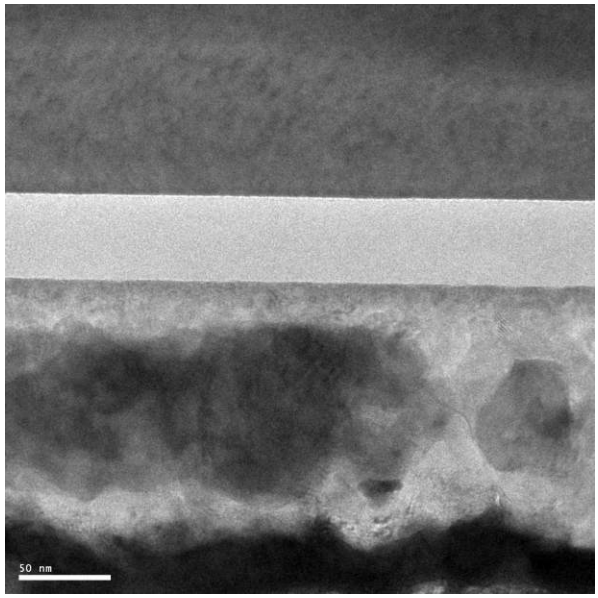


Figure B.10: Here is one of the TEM images used in this work, this is a cross-section of β-Ga_2O_3/Al_2O_3 sample. This was used to determine the thickness of the Al_2O_3 layer. This was using the scale and ImageJ and the tabulated data is seen in table B.7. In this table it is TEM image 2

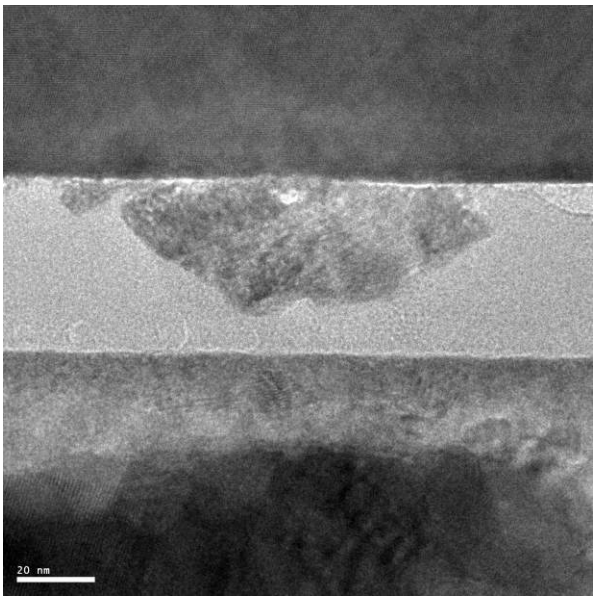


Figure B.11: Here is one of the TEM images used in this work, this is a cross-section of β-Ga_2O_3/Al_2O_3 sample. This was used to determine the thickness of the Al_2O_3 layer. This was using the scale and ImageJ and the tabulated data is seen in table B.7. In this table it is TEM image 3

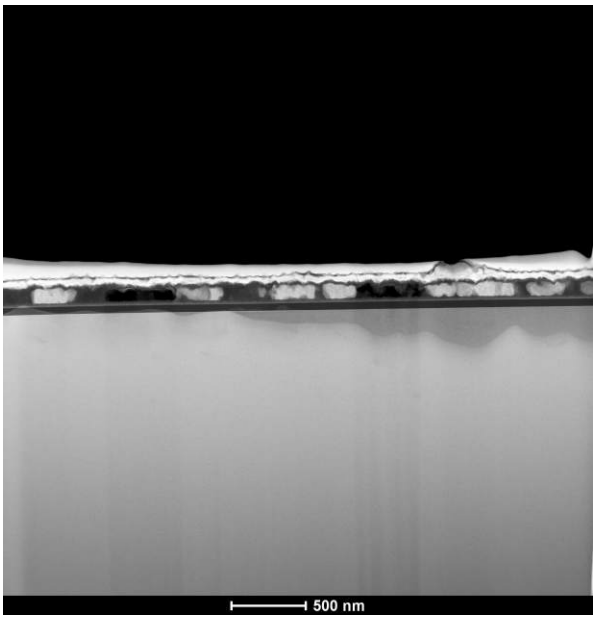


Figure B.12: Here is one of the TEM images used in this work, this is a cross-section of β-Ga_2O_3/Al_2O_3 sample. This was used to determine the thickness of the Al_2O_3 layer. This was using the scale and ImageJ and the tabulated data is seen in table B.7. In this table it is TEM image 4

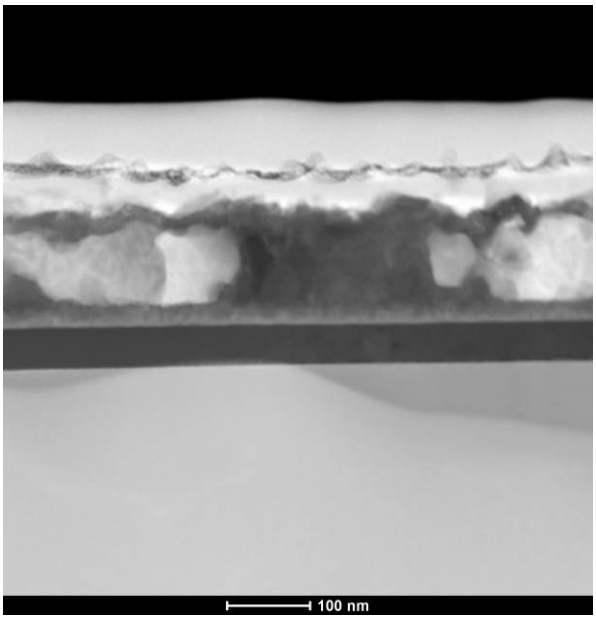


Figure B.13: Here is one of the TEM images used in this work, this is a cross-section of β-Ga_2O_3/Al_2O_3 sample. This was used to determine the thickness of the Al_2O_3 layer. This was using the scale and ImageJ and the tabulated data is seen in table B.7. In this table it is TEM image 5

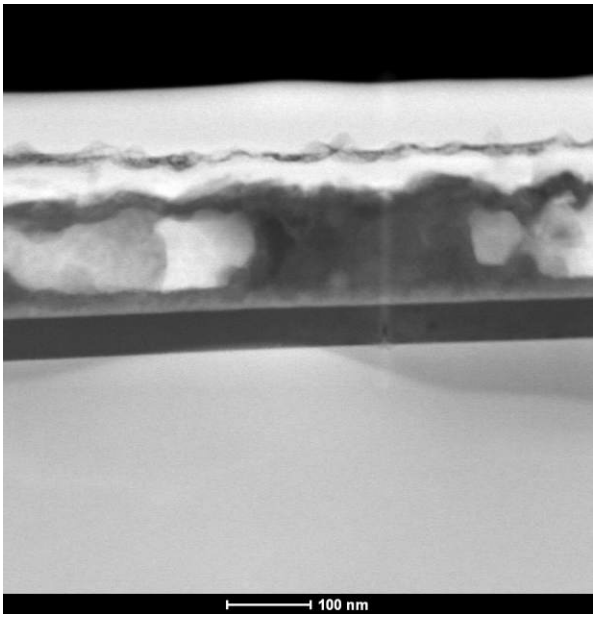


Figure B.14: Here is one of the TEM images used in this work, this is a cross-section of β-Ga_2O_3/Al_2O_3 sample. This was used to determine the thickness of the Al_2O_3 layer. This was using the scale and ImageJ and the tabulated data is seen in table B.7. In this table it is TEM image 6

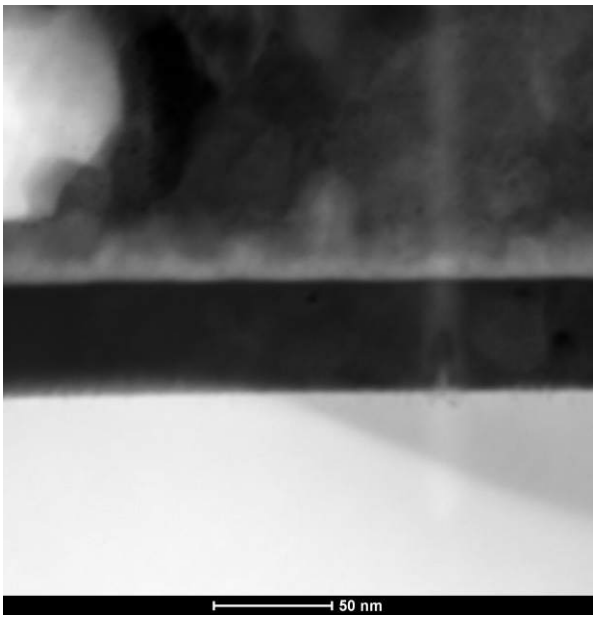


Figure B.15: Here is one of the TEM images used in this work, this is a cross-section of β-Ga_2O_3/Al_2O_3 sample. This was used to determine the thickness of the Al_2O_3 layer. This was using the scale and ImageJ and the tabulated data is seen in table B.7. In this table it is TEM image 7

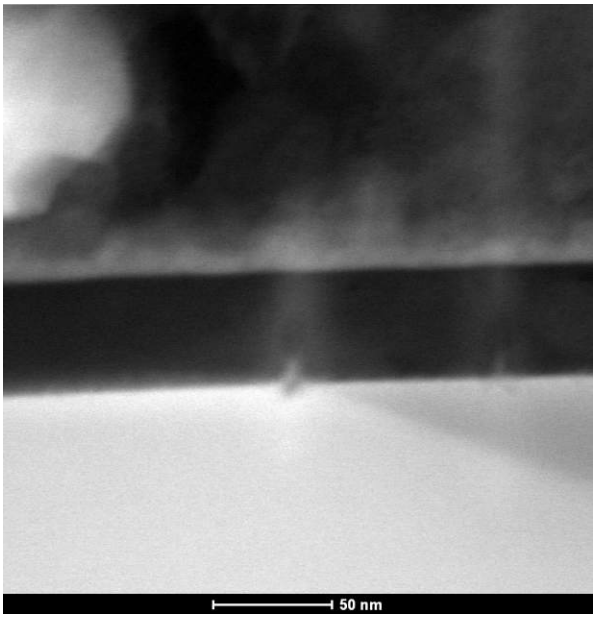


Figure B.16: Here is one of the TEM images used in this work, this is a cross-section of β-Ga_2O_3/Al_2O_3 sample. This was used to determine the thickness of the Al_2O_3 layer. This was using the scale and ImageJ and the tabulated data is seen in table B.7. In this table it is TEM image 8

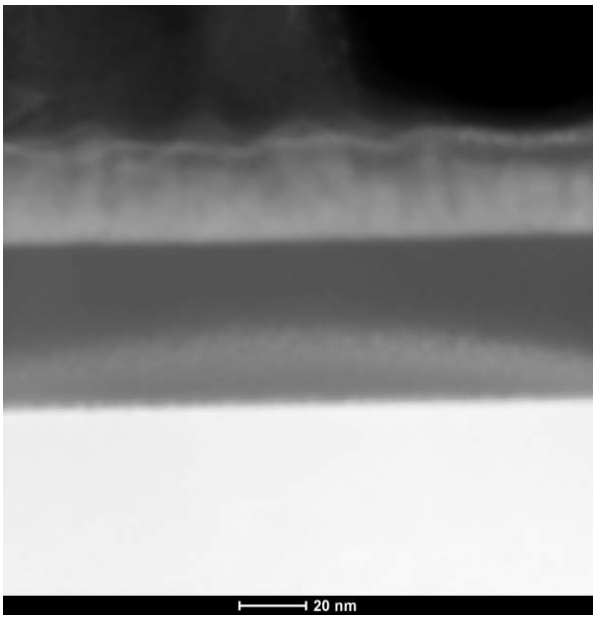


Figure B.17: Here is one of the TEM images used in this work, this is a cross-section of β-Ga_2O_3/Al_2O_3 sample. This was used to determine the thickness of the Al_2O_3 layer. This was using the scale and ImageJ and the tabulated data is seen in table B.7. In this table it is TEM image 9

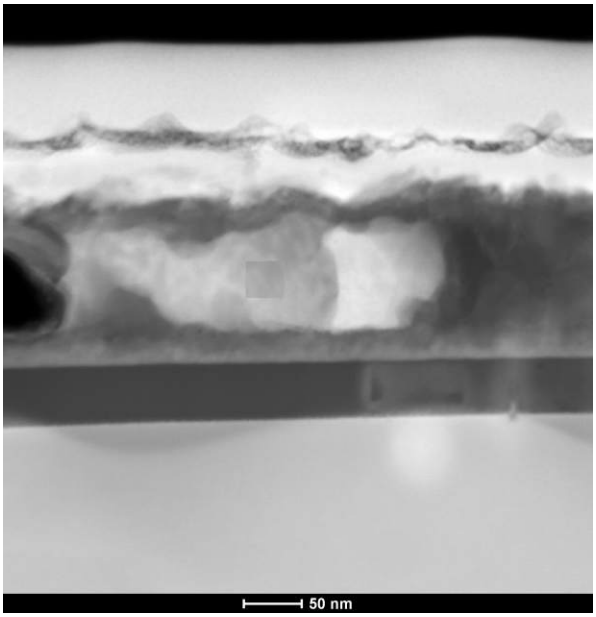


Figure B.18: Here is one of the TEM images used in this work, this is a cross-section of β-Ga_2O_3/Al_2O_3 sample. This was used to determine the thickness of the Al_2O_3 layer. This was using the scale and ImageJ and the tabulated data is seen in table B.7. In this table it is TEM image 10

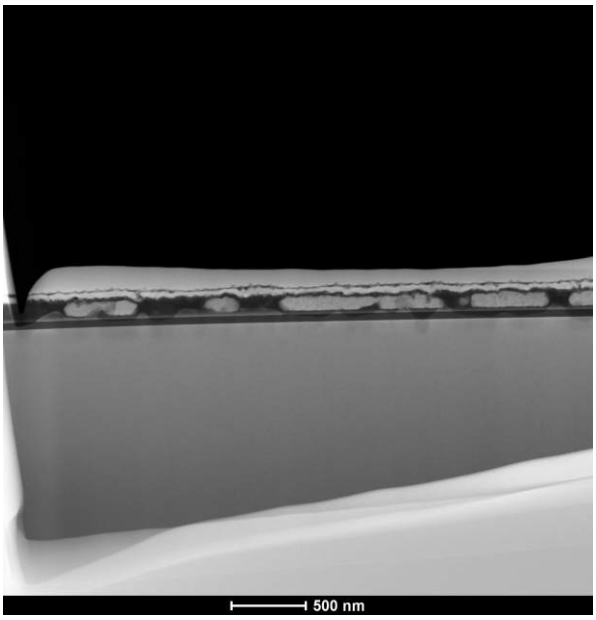


Figure B.19: Here is one of the TEM images used in this work, this is a cross-section of β-Ga_2O_3/Al_2O_3 sample. This was used to determine the thickness of the Al_2O_3 layer. This was using the scale and ImageJ and the tabulated data is seen in table B.7. In this table it is TEM image 11

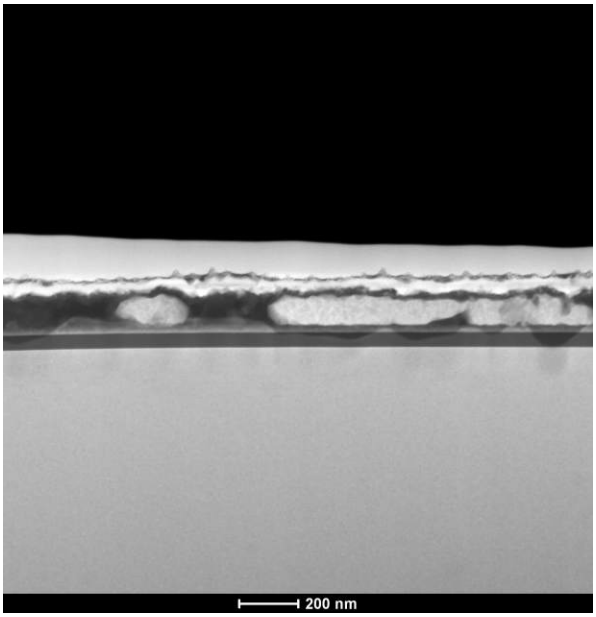


Figure B.20: Here is one of the TEM images used in this work, this is a cross-section of β-Ga_2O_3/Al_2O_3 sample. This was used to determine the thickness of the Al_2O_3 layer. This was using the scale and ImageJ and the tabulated data is seen in table B.7. In this table it is TEM image 12

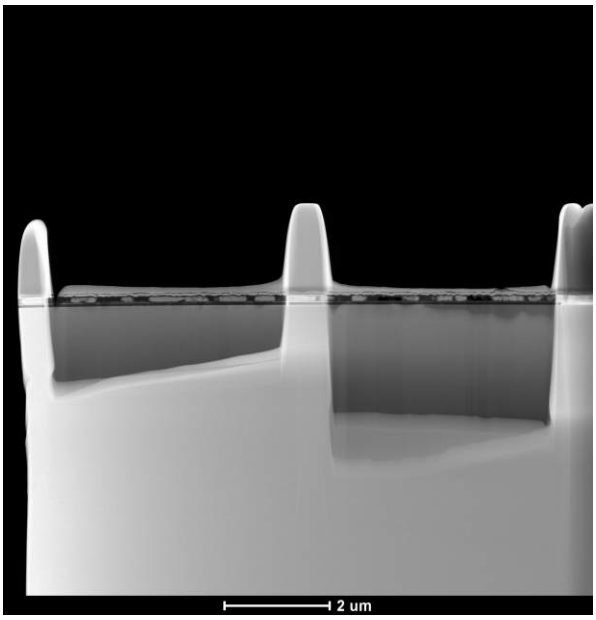


Figure B.21: Here is one of the TEM images used in this work, this is a cross-section of β-Ga_2O_3/Al_2O_3 sample. This was used to determine the thickness of the Al_2O_3 layer. This was using the scale and ImageJ and the tabulated data is seen in table B.7. In this table it is TEM image 13

B.5 Metal-Al_2O_3-β-Ga_2O_3 C_A

Contact	Accumulation Capacitance (nF)			
	As Deposited	100°C	200°C	300°C
1	$1.2238 \pm 3.51 \times 10^{-3}$	$1.23347 \pm 1.83 \times 10^{-3}$	-	$1.2509 \pm 2.22 \times 10^{-3}$
2	-	$1.24001 \pm 1.56 \times 10^{-3}$	$1.24562 \pm 1.68 \times 10^{-3}$	$1.25041 \pm 2.35 \times 10^{-3}$
3	-	$1.23421 \pm 1.80 \times 10^{-3}$	$1.2506 \pm 1.88 \times 10^{-3}$	$1.26228 \pm 1.44 \times 10^{-3}$
4	$1.24678 \pm 3.18 \times 10^{-3}$	$1.23766 \pm 1.82 \times 10^{-3}$	$1.24691 \pm 1.93 \times 10^{-3}$	$1.25368 \pm 2.30 \times 10^{-3}$
5	-	-	-	$1.25332 \pm 2.14 \times 10^{-3}$
6	$1.24268 \pm 3.71 \times 10^{-3}$	$1.23656 \pm 2.10 \times 10^{-3}$	-	$1.25214 \pm 1.82 \times 10^{-3}$
7	$1.2519 \pm 3.43 \times 10^{-3}$	-	-	-
8	-	-	$1.28141 \pm 1.77 \times 10^{-3}$	-
9	-	-	$1.3097 \pm 2.41 \times 10^{-3}$	-
10	$1.24366 \pm 3.78 \times 10^{-3}$	-	$1.33127 \pm 1.52 \times 10^{-3}$	-

Table B.8: The accumulation capacitance determined from the fitting to the plots in Figure 5.9, the errors are from the error of the fit.

Contact	Accumulation Capacitance (nF)			
	As Deposited	100°C	200°C	300°C
1	-	-	7.8922 ± 2.8910^{-3}	7.8533 ± 1.6010^{-3}
2	-	-	7.8779 ± 2.5510^{-3}	7.9089 ± 2.0510^{-3}
3	7.8460 ± 4.3210^{-3}	7.7875 ± 1.9110^{-3}	-	7.9163 ± 2.2410^{-3}
4	-	-	7.8292 ± 3.1910^{-3}	-
5	-	-	7.7963 ± 3.3310^{-3}	7.8879 ± 2.5710^{-3}
6	-	-	-	-
7	7.9239 ± 3.7310^{-3}	7.7558 ± 2.3410^{-3}	-	7.9487 ± 2.8810^{-3}
8	-	-	7.8779 ± 2.5510^{-3}	7.8210 ± 2.5110^{-3}
9	-	-	7.8760 ± 2.9110^{-3}	7.9031 ± 1.9910^{-3}
10	7.8631 ± 2.7210^{-3}	7.8103 ± 3.1610^{-3}	7.8867 ± 2.5510^{-3}	7.9088 ± 2.2710^{-3}

Table B.9: The accumulation capacitance determined from the fitting to the plots in Figure B.22, the errors are from the error of the fit.

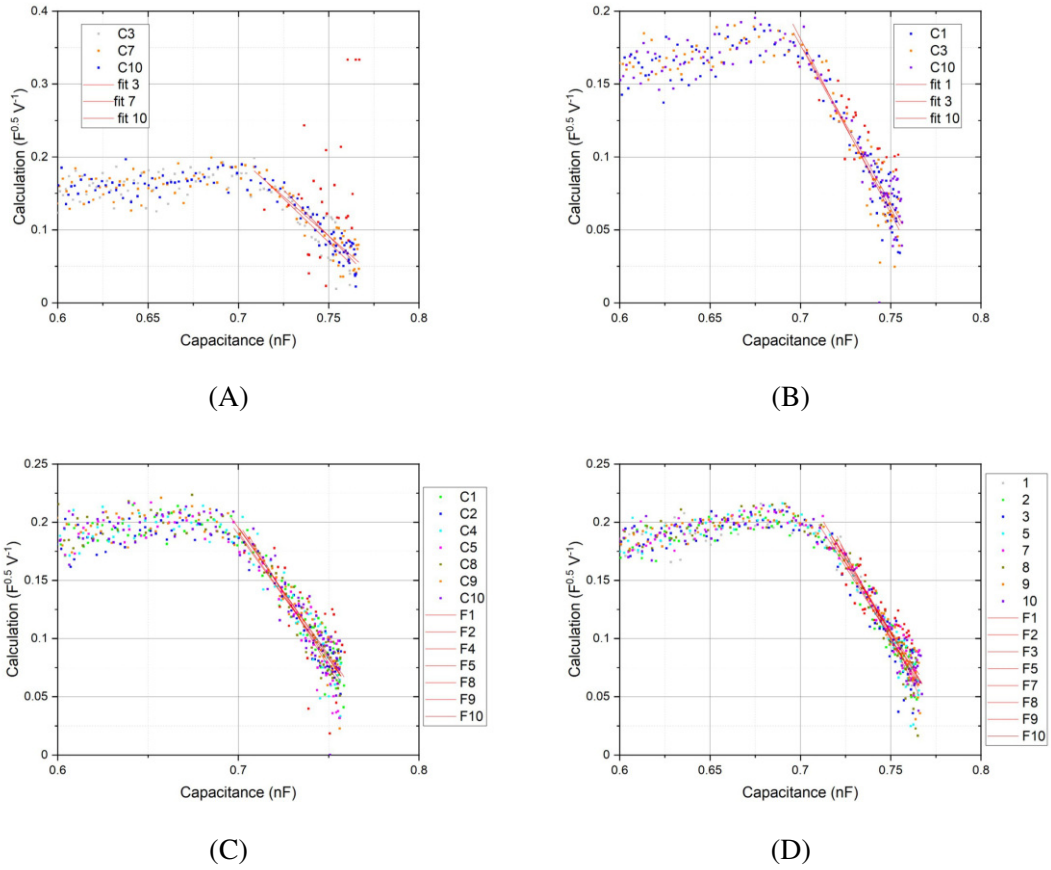


Figure B.22: The plots used to determine the accumulation capacitance for the Metal-Al_2O_3-β-Ga_2O_3, these are for the contacts with diameter of 800 μm. This is As deposited (A), and annealing at 100°C (B), 200°C (C) and 300°C (D) respectively. In each plot, the number in the legend refers to the contact position within that set of ten measurements. The intercepts for the individual fittings can be seen in Table B.9.

Contact	$\frac{d\frac{1}{C^2}}{dV_G}$ $F^{-2}V^{-1}$			
	As Deposited	100°C	200°C	300°C
1	-	6.02 ± 0.004	7.83 ± 0.007	7.70 ± 0.004
2	5.64 ± 0.005	5.84 ± 0.003	8.03 ± 0.006	7.85 ± 0.002
3	-	5.87 ± 0.004	8.17 ± 6.56687E13	7.72 ± 0.002
4	5.65 ± 0.004	6.01 ± 0.004	7.97 ± 0.005	7.82 ± 0.002
5	-	-	-	7.95 ± 0.002
6	5.76 ± 0.006	5.90 ± 0.004	8.26 ± 0.006	8.18 ± 0.002
7	5.93 ± 0.005	-	-	-
8	-	-	8.21 ± 0.00	-
9	-	-	8.31 ± 0.007	-
10	5.90 ± 0.005	-	8.51 ± 0.006	-

Table B.10: The calculated gradients of the plots shown in Figure 5.12 these were used to calculated the doping concentrations. It can be seen that the variance of the fitting is higher then errors of the fitting. The means was determined to be 5.78 ± 0.122, 4.94 ± 0.991, 8.21 ± 0.141 and 7.85 ± 0.171for as deposited, and annealed at 100°C, 200°C and 300°C respectively. The differences between these gradients is problematic, it is believed that the differences are due to a high density of trapped states interfering with the measurement.

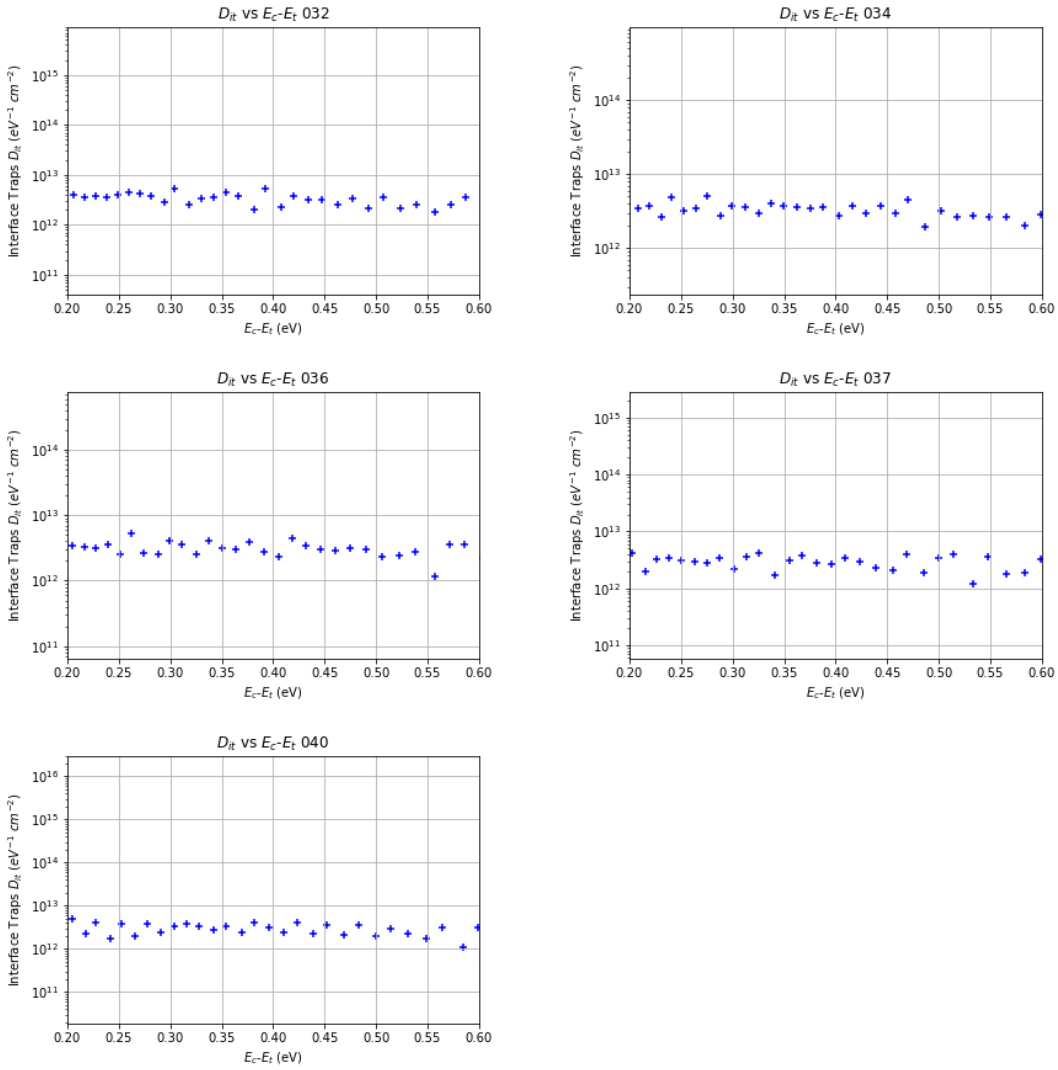


Figure B.23: The D_{it} as deposited for Al_2O_3/Ga_2O_3.

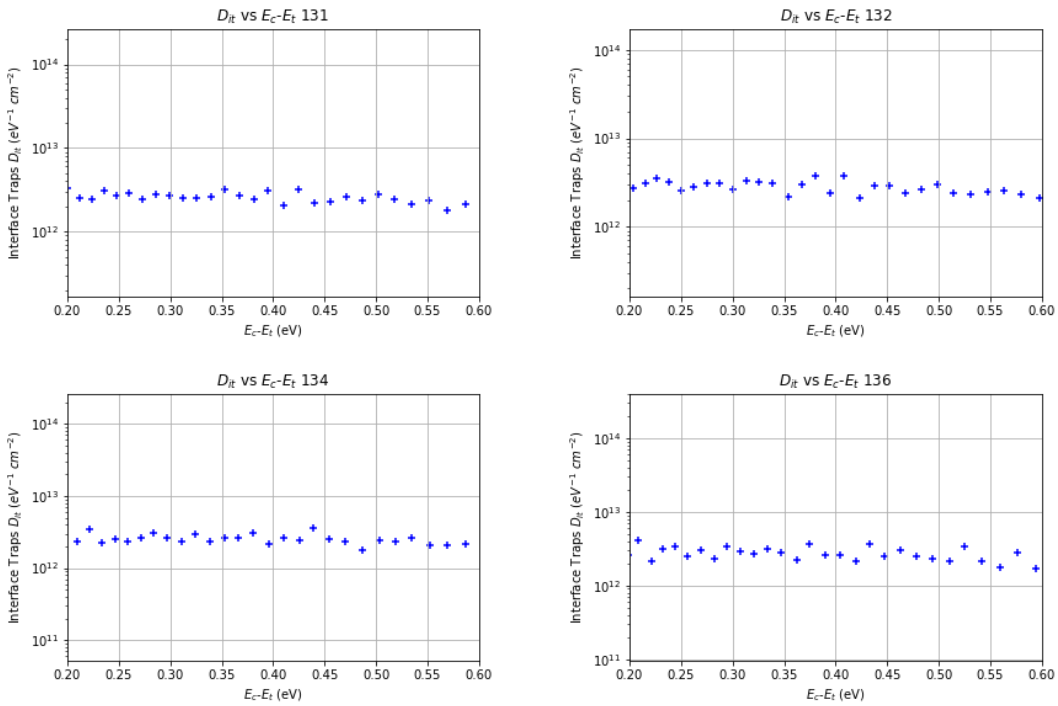


Figure B.24: The D_{it} after annealing at 100°C for Al_2O_3/Ga_2O_3.

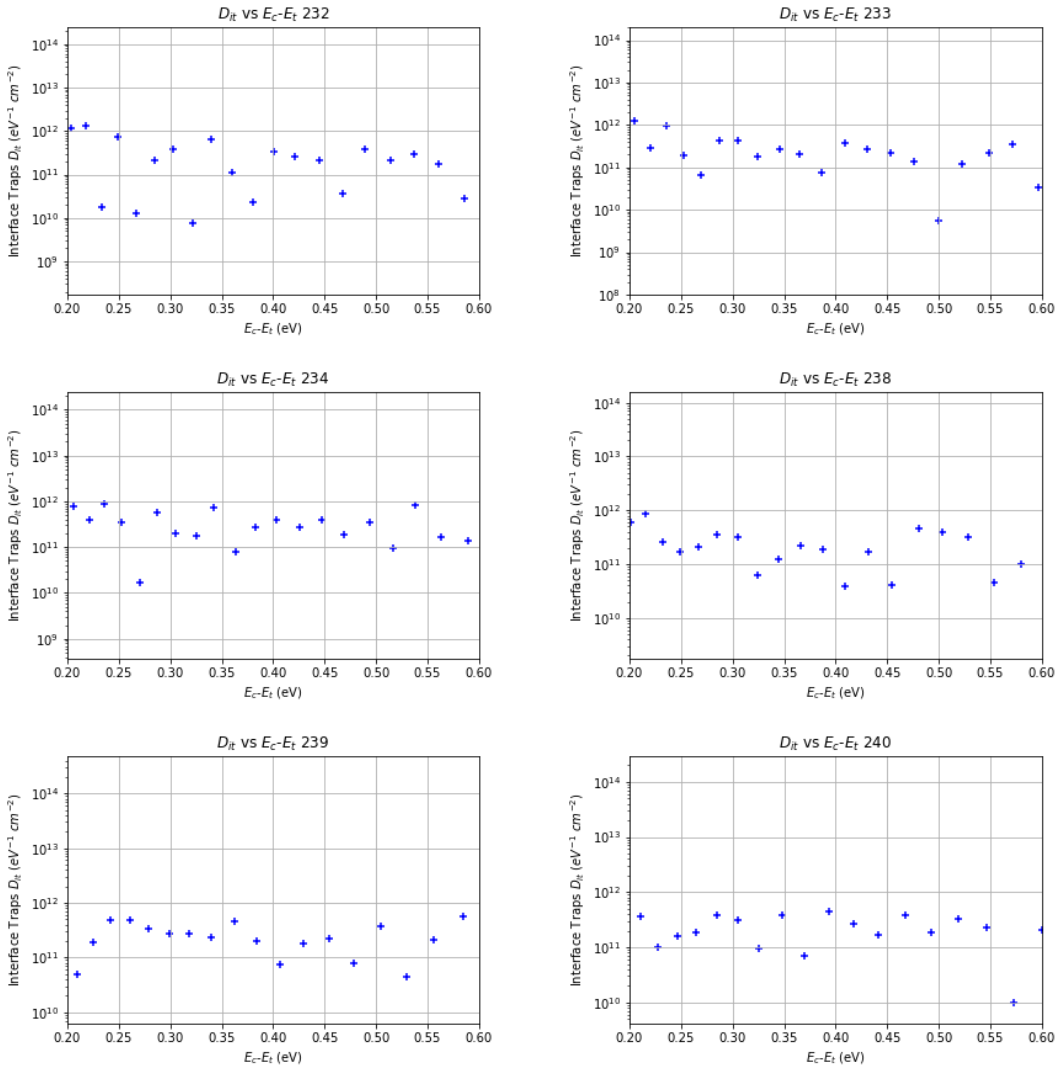


Figure B.25: The D_{it} after annealing at 200°C for Al_2O_3/Ga_2O_3.

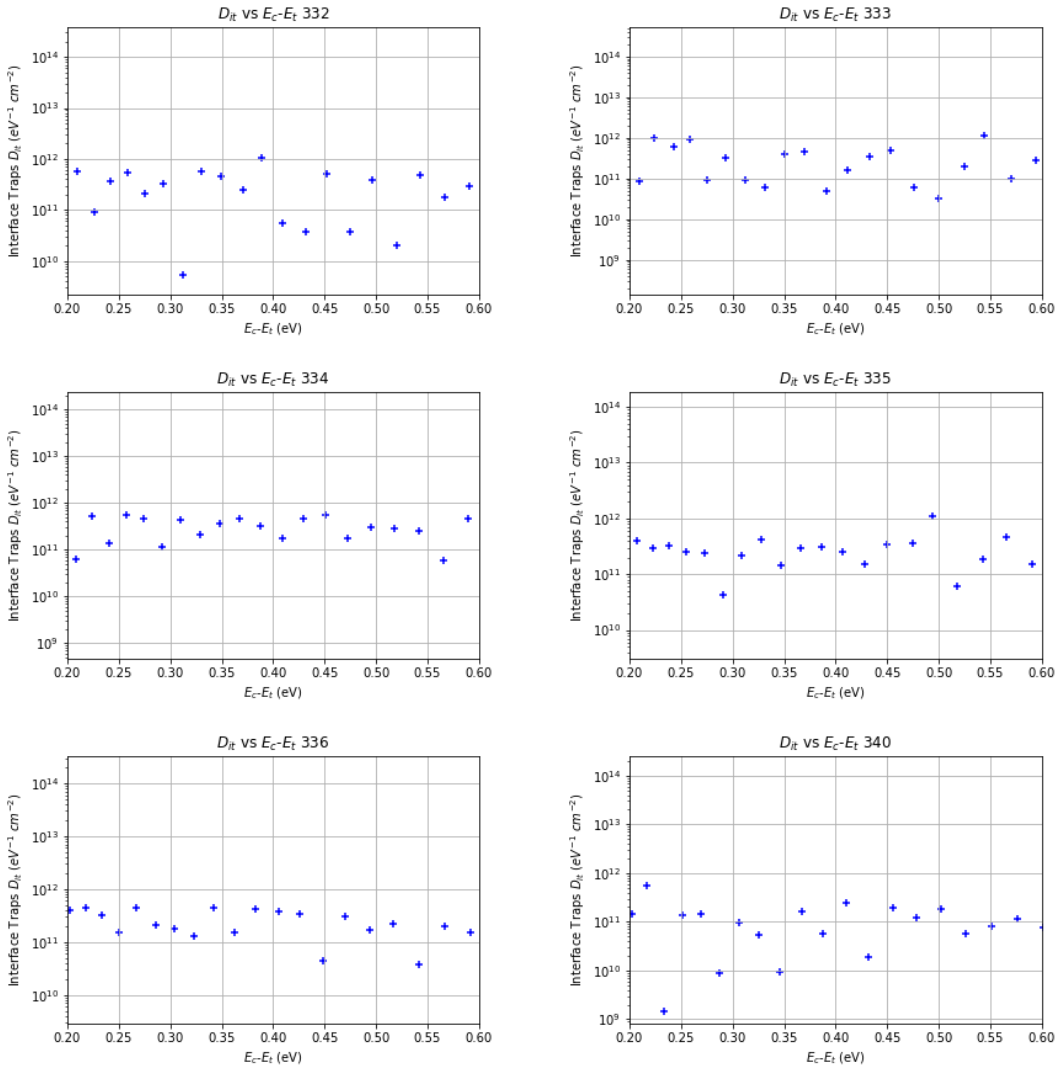


Figure B.26: The D_{it} after annealing at 300°C for Al_2O_3/Ga_2O_3.

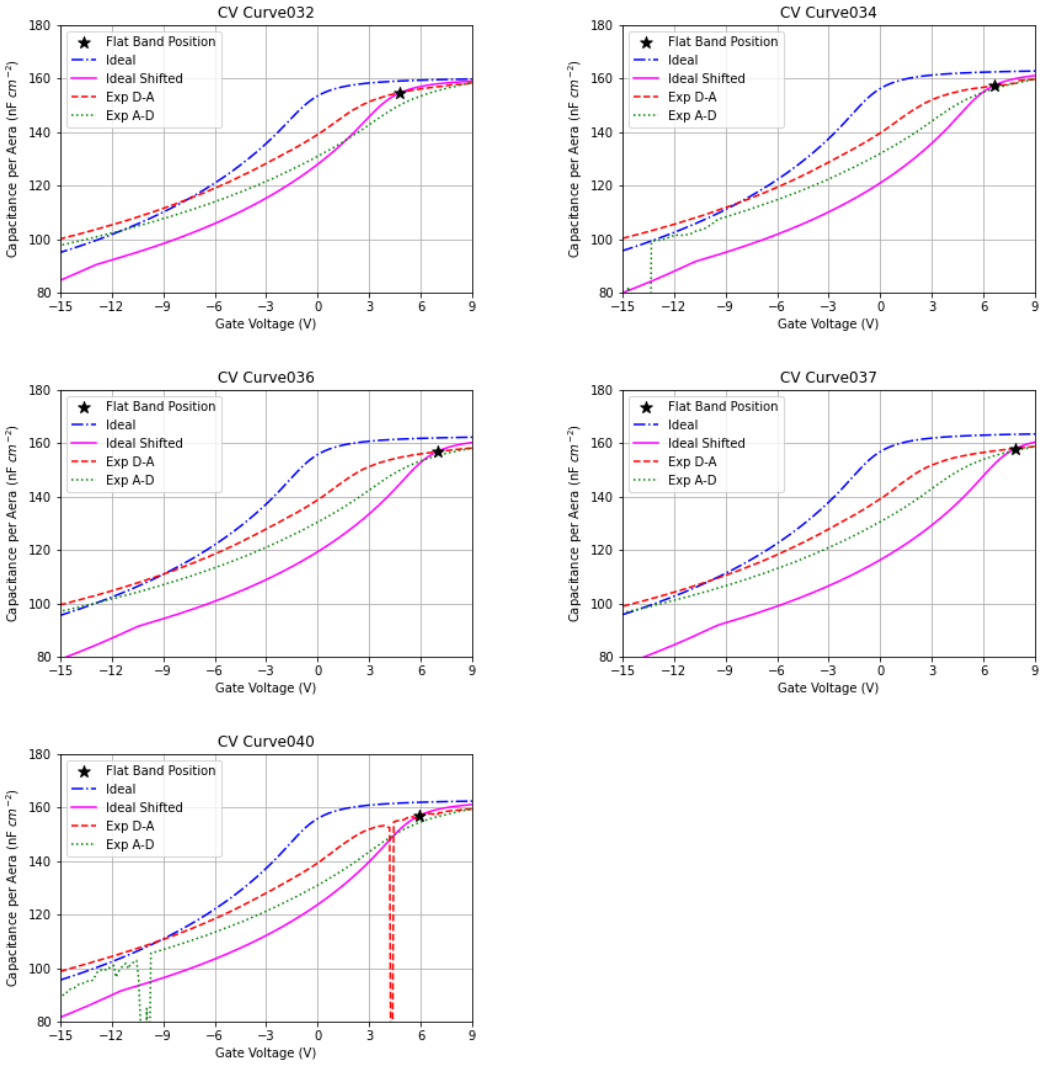


Figure B.27: The CV as deposited for Al_2O_3/Ga_2O_3.

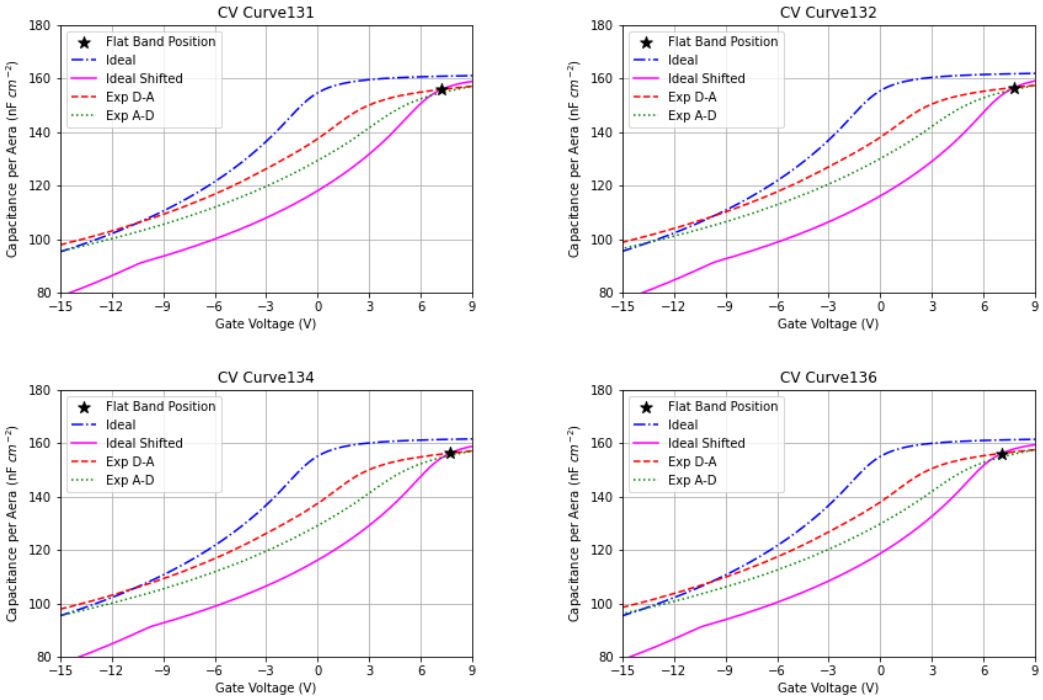


Figure B.28: The CV after annealing at 100°C for Al_2O_3/Ga_2O_3.

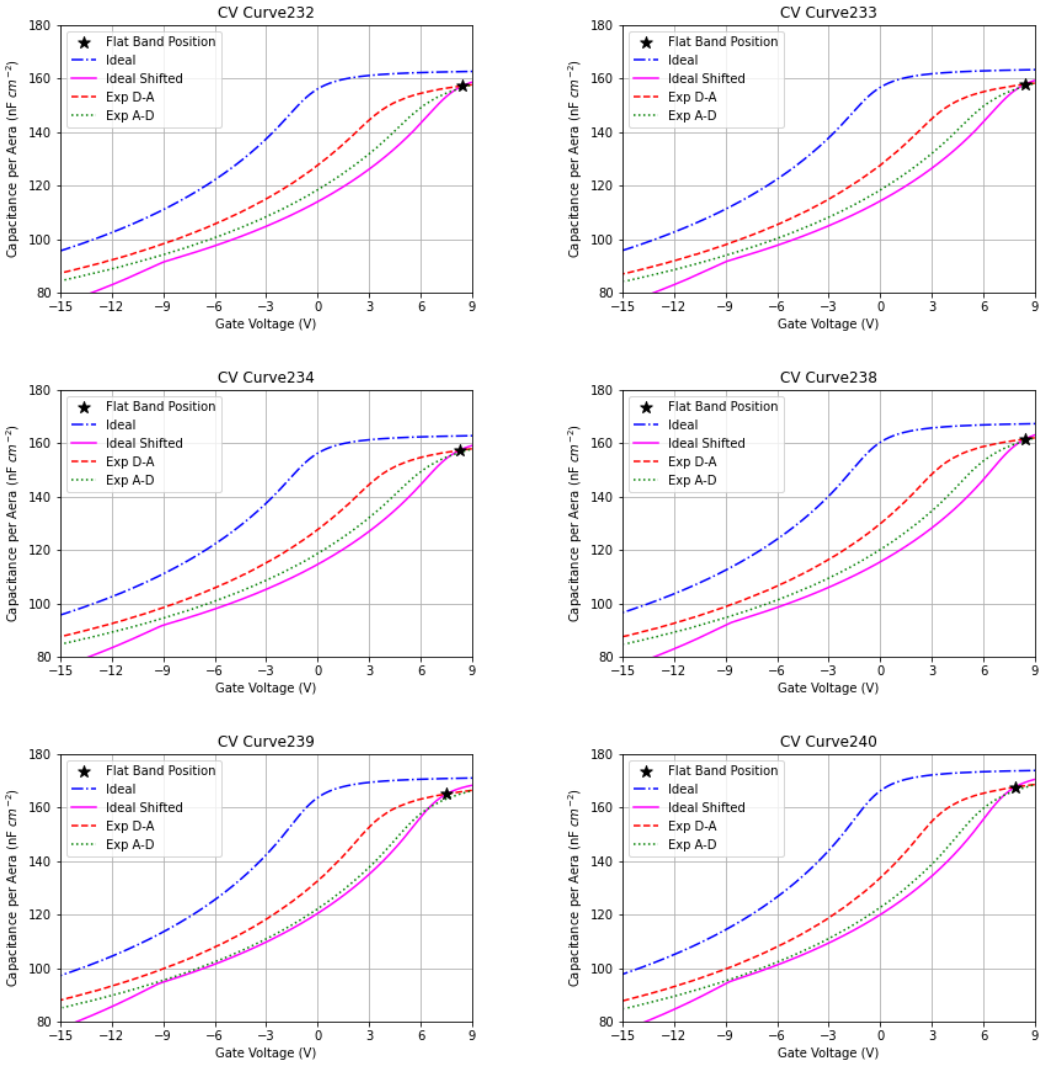


Figure B.29: The CV after annealing at 200°C for Al_2O_3/Ga_2O_3.

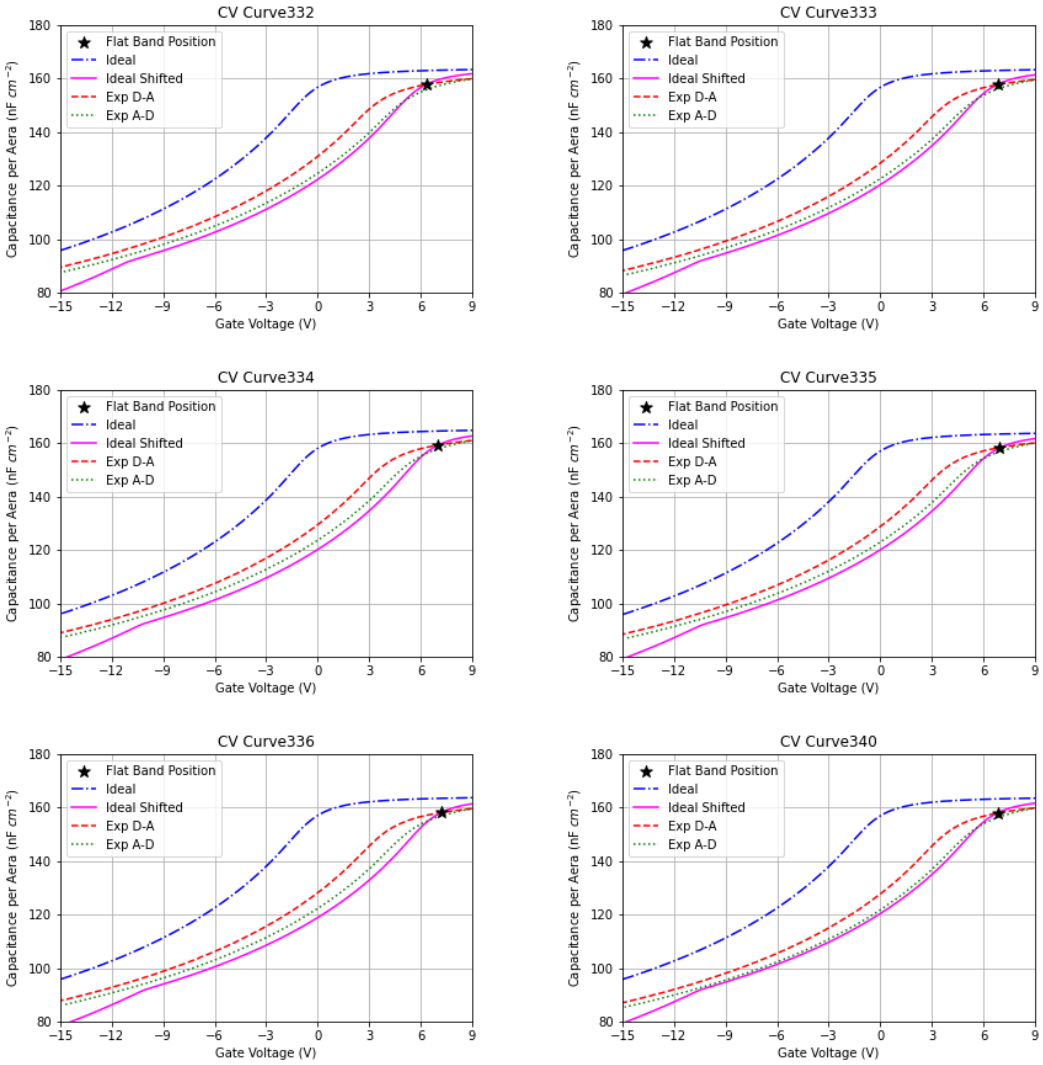


Figure B.30: The CV after annealing at 300°C for Al_2O_3/Ga_2O_3.

B.6 Terman Method

Relating the calculated D_{it} to the surface potential and position in the bandgap. This is derived from [260] and [522]. This is for an n-type semiconductor. The carrier concentrations in the semiconductor can be using Boltzmann statistics whey are,

$$n = n_0 e^{-\frac{q}{k_b T}\phi} = n_0 e^{\theta\phi_s} \tag{B.1}$$

and,

$$p = \frac{{n_i}^2}{n_0} e^{-\frac{q}{k_b T}\phi_s} = \frac{{n_i}^2}{n_0} e^{-\theta\phi_s} \tag{B.2}$$

where

$$\theta = \frac{q}{k_b T} \tag{B.3}$$

The Passions equation is,

$$\frac{d^2\phi_s}{dx^2} = -\frac{\rho(x)}{\epsilon_s} \tag{B.4}$$

with the total space charge density is given by,

$$\rho(x) = q(n - p - N_d). \tag{B.5}$$

The resultant Passions equation is then given by,

$$\frac{d^2\phi_s}{dx^2} = -\frac{\rho(x)}{\epsilon_s} = -\frac{q}{\epsilon_s}\left(n_0\left(e^{\theta\phi_s} - 1\right) - p_0\left(e^{-\theta\phi_s} - 1\right)\right) \tag{B.6}$$

Integrating this to the bulk to find the electric field at the surface is,

$$E_s = \frac{d\phi_s}{dx} = \int_0^{\frac{d\phi}{dx}} = -\frac{q}{\epsilon_s}\left(n_0\left(e^{\theta\phi_s} - 1\right) - p_0\left(e^{-\theta\phi_s} - 1\right)\right)d\phi_s \tag{B.7}$$

which is

$${E_s}^2 = \left(\frac{2}{\theta}\right)^2 \frac{qn_0\theta}{2\epsilon_s}\left(\left(e^{\theta\phi} + \theta\phi_s - 1\right) - \frac{n_0}{p_0}\left(e^{\theta\phi_s} + \theta\phi_s - 1\right)\right) \tag{B.8}$$

Defining,

$${L_D}^2 = \frac{\epsilon_s}{\theta q n_0} \tag{B.9}$$

and

$$F(\theta,\phi)^2 = \left(e^{\theta\phi_s} + \theta\phi_s - 1\right) - \frac{n_0}{p_0}\left(e^{\theta\phi} + \theta\phi_s - 1\right) \tag{B.10}$$

Then the electric field is,

$$E_s(x) = \pm\frac{\sqrt[2]{2}}{\theta L_D} F(\beta\phi_s, \frac{p_0}{n_0}). \tag{B.11}$$

At the interface between the semiconductor and dielectric the electric field must be continuos so,

$$\epsilon_s E_s = \epsilon_{die} E_{die} \tag{B.12}$$

Rearranged into,

$$E_{die} = \frac{\epsilon_s}{\epsilon_{die}} E_s. \tag{B.13}$$

Then the electric field in the dielectric layer can be given as,

$$E_{die} = \frac{\epsilon_s}{\epsilon_{die}} \frac{\sqrt[2]{2}}{\theta L_D} F(\beta\phi_s, \frac{p_0}{n_0}) \tag{B.14}$$

The voltage across the dielectric layer is,

$$V_{die} = E_{die} t \tag{B.15}$$

where t is the thickness of the dielectric layer.

$$V_{die} = V_g - V_F - V_s \tag{B.16}$$

Rearranged into,

$$V_s = V_g - V_F - V_{die} \tag{B.17}$$

Then the position in the bandgap can be found with,

$$E_c - E_t = qV_s + k_b T \log\left(\frac{n_0}{n_i}\right). \tag{B.18}$$

This is how the position of the D_{it} in the band gap is found in the Terman method.

APPENDIX C

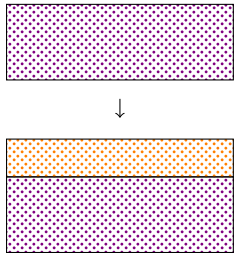
APPENDIX FOR CHAPTER 6

This is the Appendix is dealing with Chapter 6, this is split into a couple of different sections. This starts with theory regarding metal-semiconductor interface, then briefly about the current transport mechanism. Followed by a discussion about test structures which were to be used in this work. However, the reason why they were not used as intended is described there, then the process flow for the metal lift off procedure is shown. There is then a description of the band diagram for hetero-junctions, while not directly used in this work, it was a consideration in the initial ohmic works . After this, the IV results from the initial work are shown, then the images which informed the LNR-003 photoresist development are shown.

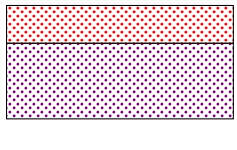
C.1 Lift-Off Process Flow

The basic process flow used for the metal lift off process used in the Chapter 6, this was used in Sections 6.2.2 and 6.2. Whereas both processes were using a lift-off protocol, that one was after dielectric layer(s) were deposited on top of the sample. This is a simple process which only uses the lift-off protocol once rather then multiple times, the exact protocol will vary dependent on the photoresist protocol being used.

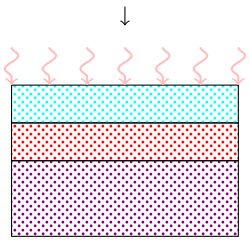
- The semiconductor substrate is solvent cleaned.



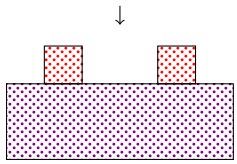
- Spin Ti-prime, an adhesive agent onto the sample and bake at 120°C for 120 s.



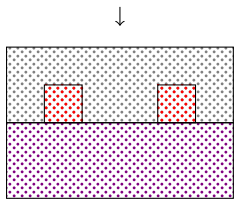
- Spin photoresist, onto the sample and baked.



- On a mask aligner, expose to 130 mJ $\cdot$ cm^{-2} of UV, then bake ar 110°C for 80 s.

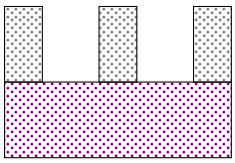


- The photoresist is developed in a solution, to leave behind a patterned sample.



- Deposit metal onto the sample.

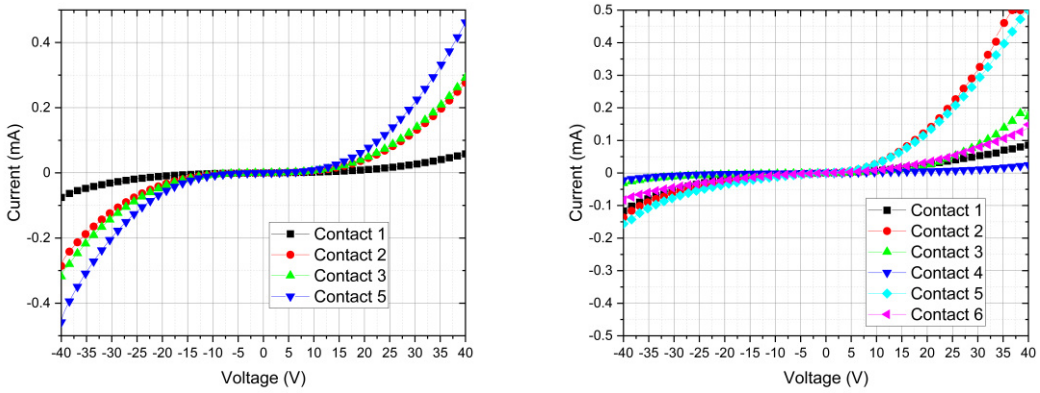
- The metal is lifted off with D350, leaving behind the patterned metal contact.



The end of the metal lift-off procedure, this dose not necessary mean the end of processing. In this work the samples at times required annealing which would be an additional step in the processing. It is also worth noting that the resit stripping in D350 sometimes required over night or even sonicating, this was different depending on the metal deposition, most commonly the manner in which it was deposited was the determining factor.

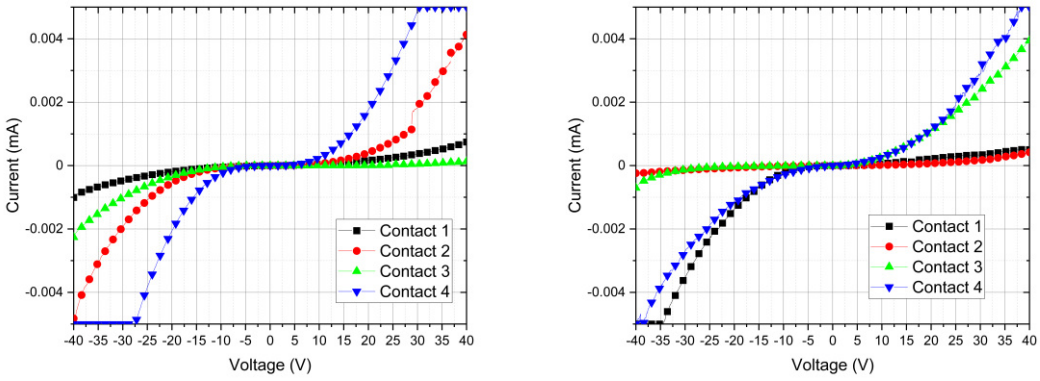
C.2 IV data from the Hetro

In this section the IV plots taken for the different sample from Section 6.2.1, while a sample will be shown there the entire data set will be shown here. This was part of the initial work performed on ohmic contacts, this material was in part discontinued to be used as details such as the doping concentration in the β-Ga_2O_3 was unknown (approximately 10^{18} cm^{-3}) and the doping in the substrate was only known to be p-type Si. The sample was purchased in 2017, so it is unknown how much the surface had changed. It was confirmed to be 201 β-Ga_2O_3. Due to this the data collected here was used as preliminary data which informed the main focus of the ohmic contact work.



(A) (B)

Figure C.1: IV measurements taken with Ti/Ag contacts on Sn doped β-Ga_2O_3/Si sample as described in Section 3.2.9 and fabricated in Section 6.2. (A) after annealed at 400°C and (B) after annealed at 500°C. After annealing it appears that the contact became more rectifying.



(A) (B)

Figure C.2: IV measurements taken with Ti/Ag contacts on unintentionally doped β-Ga_2O_3/Si sample as described in Section 3.2.9 and fabricated in Section 6.2. (A) after annealed at 400°C and (B) after annealed at 500°C. After annealing it appears that the contact became less rectifying, however still rectifying.

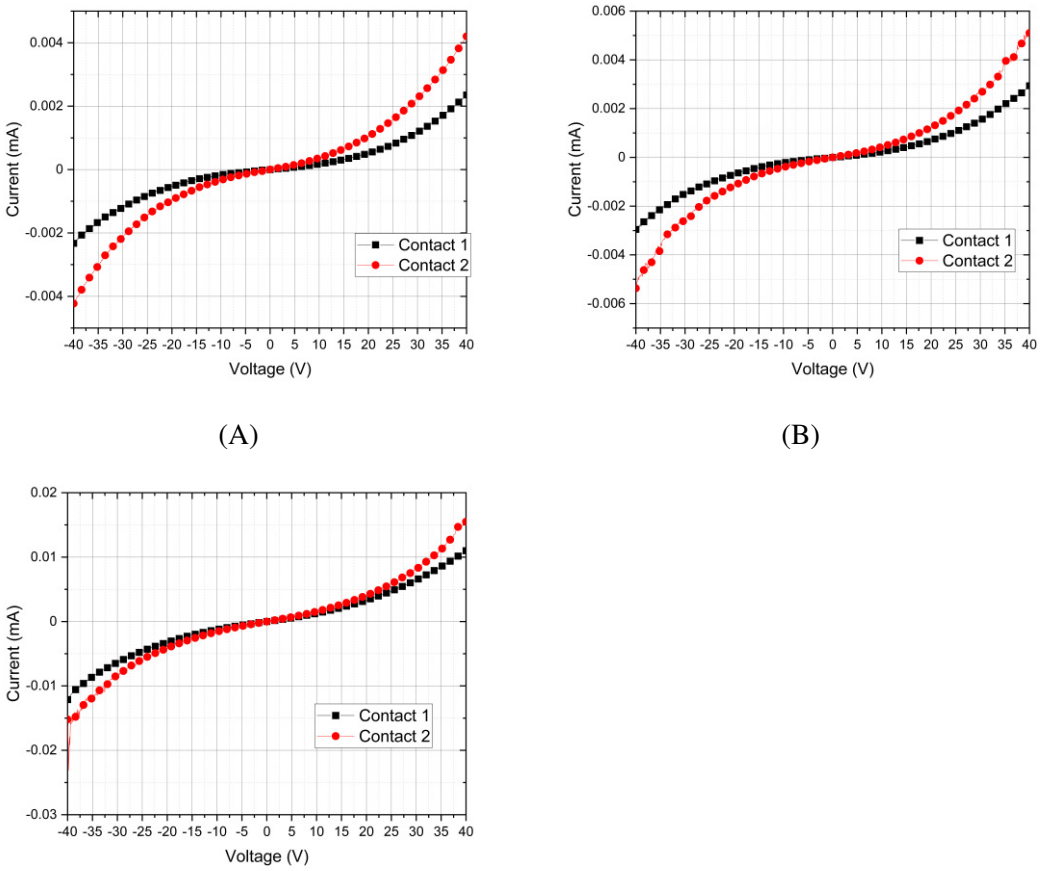
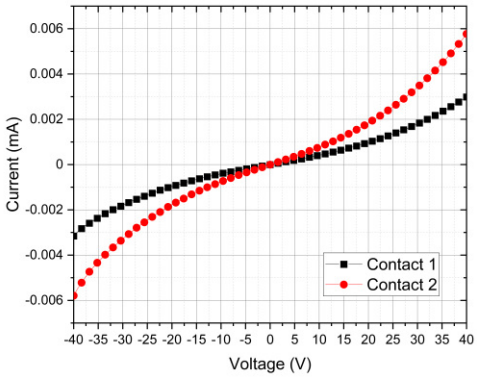
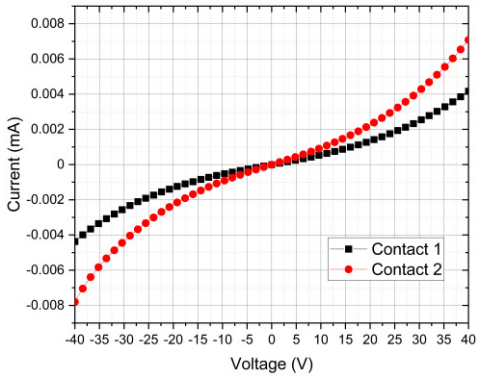


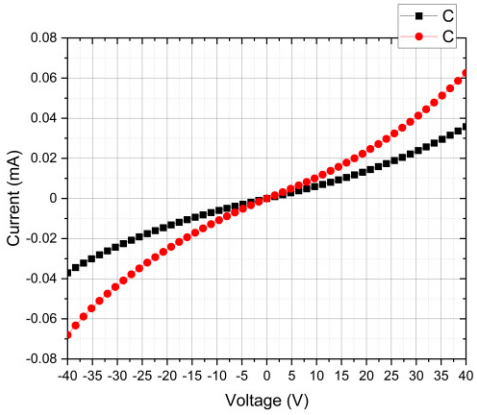
Figure C.3: IV measurements taken with Ag/Al contacts on Sn doped β-Ga_2O_3/Si sample as described in Section 3.2.9 and fabricated in Section 6.2. (A) after annealed at 300°C, (B) after annealed at 400°C and (C) after annealed at 500°C. This seemed to tend towards becoming ohmic is each annealing stage, however it was resistive compared to other metallisations.



(A)



(B)



(C)

Figure C.4: IV measurements taken with Ti/Al contacts on unintentionally doped β-Ga_2O_3/Si sample as described in Section 3.2.9 and fabricated in Section 6.2. (A) after annealed at 300°C, (B) after annealed at 400°C and (C) after annealed at 500°C. This seemed to tend towards becoming ohmic is each annealing stage, however it was resistive compared to other metallisations.

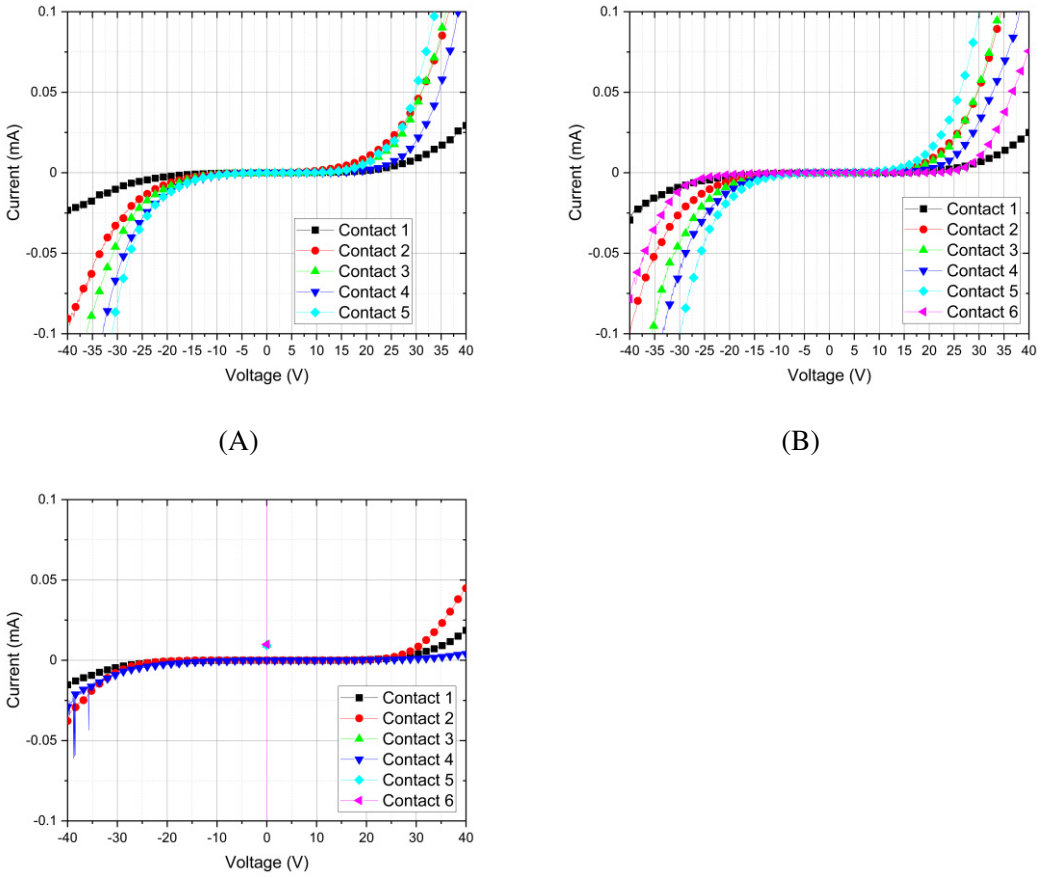
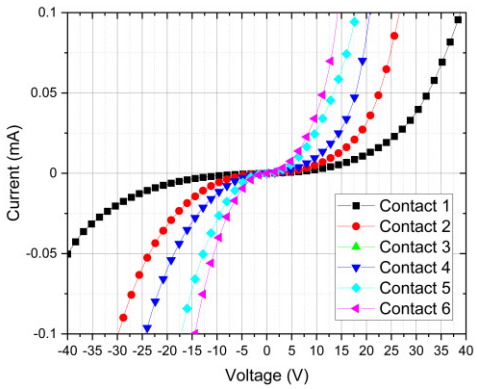
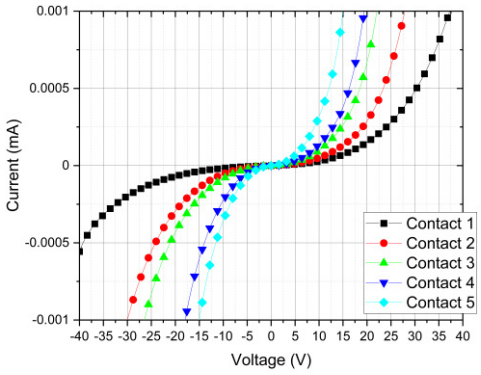


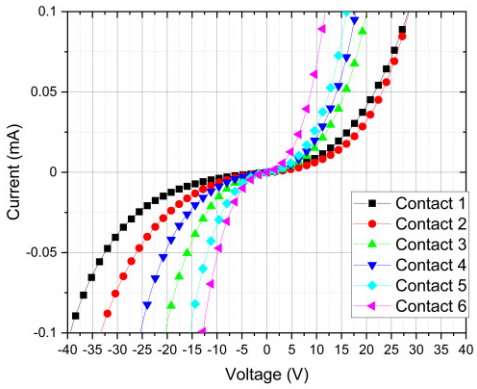
Figure C.5: IV measurements taken with Ti/Au contacts on Sn doped β-Ga_2O_3/Si sample as described in Section 3.2.9 and fabricated in Section 6.2. (A) after annealed at 300°C, (B) after annealed at 400°C and (C) after annealed at 500°C. The contacts seem to be rectifying however not very resistive.



(A)



(B)



(C)

Figure C.6: IV measurements taken with Ti/Au contacts on unintentionally doped β-Ga_2O_3/Si sample as described in Section 3.2.9 and fabricated in Section 6.2. (A) after annealed at 300°C, (B) after annealed at 400°C and (C) after annealed at 500°C. The contacts seem to be rectifying however not very resistive. After annealing it appeared to becoming less rectifying

C.3 Appendix AZ LNR-003 Development - Ellipsometry

In Section 6.2.2 ellipsometry measurements were taken, this was on Si wafers where the photoresist was spun at 3000 rpm. This had a measured thickness of 3 µm, which is in agreement with the manufacturer specifications MicroChemicals. This was measured using the ellipsometer described in Section 3.1.10, this tool is used to fit a Cauchy model to the thin film to approximate the thickness. In this section the fitting parameters and results are shown, this is to be used in conjunction with Section 6.2.2 so the reader can understand where the values were taken from. These fitting parameters and results are shown in this section in Table 6.1 and Figure C.7.

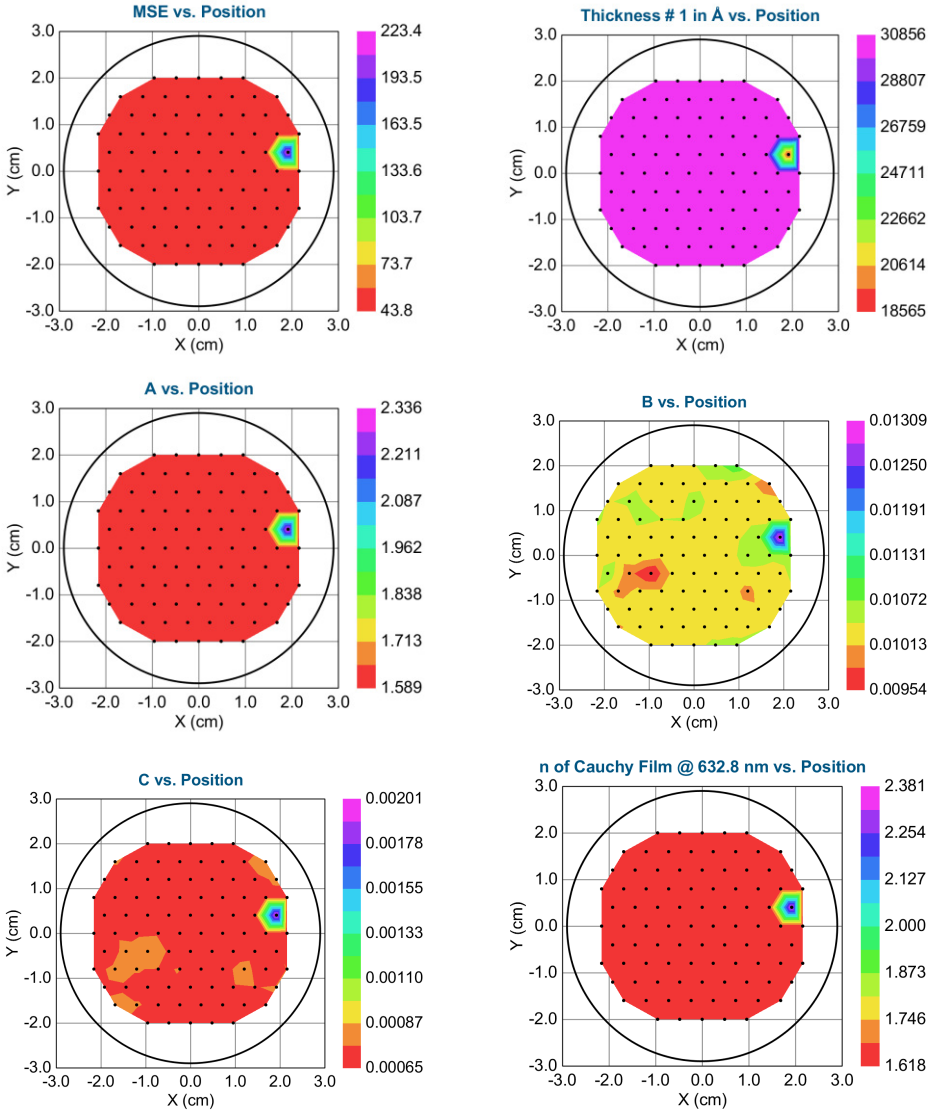


Figure C.7: The wafer map of the ellipsometer measurements from the Cauchy model to a sample, this sample was a Si wafer with AZ LNR 003 spun onto a Si wafer at 3000 rpm. This confirmed the manufacture protocol and hence this spin speed was used in the development of this protocol.

C.4 Appendix AZ LNR 003 Development - Exposure

In 6.2.2 2 inch wafers were coated with AZ LNR 003, to achieve 3 µm thick films. Then to optimise the protocol to develop an AZ LNR 003 lift-off protocol it was needed to determine the correct UV dose and developer process. This was done by exposing UV between 100 mJ $\cdot$ cm^{-2} to 275 mJ $\cdot$ cm^{-2} in steps of 25 mJ $\cdot$ cm^{-2}, these were then submerged on developer solution (AZ Developer) for 50 s to 80 s. This section is designed to show the results of this, with these different UV dose, development times and at different points in the process. The samples were measured under Keyenskt microscope the following Figures are the results of this.

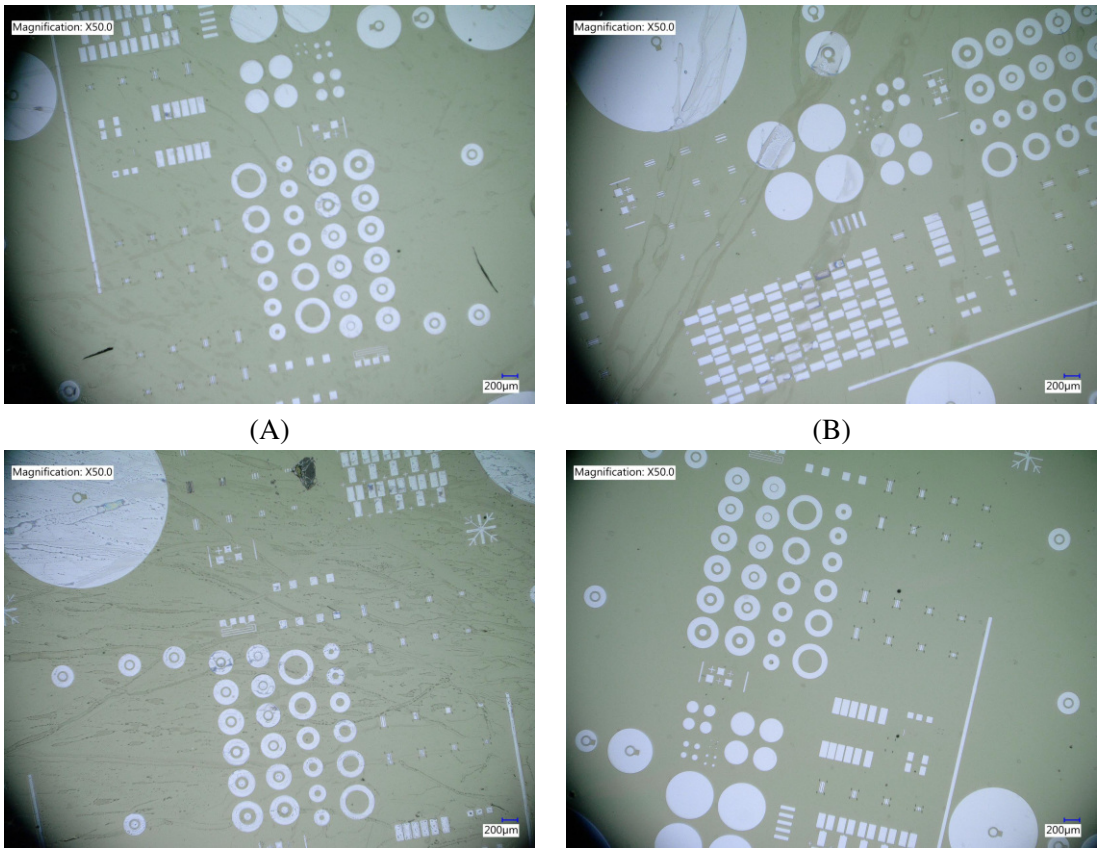


Figure C.8: AZ LNR-003 spun on 2 inch Si wafer, UV dose 100 mJ $\cdot$ cm^{-2}. This is pre-metal deposition. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

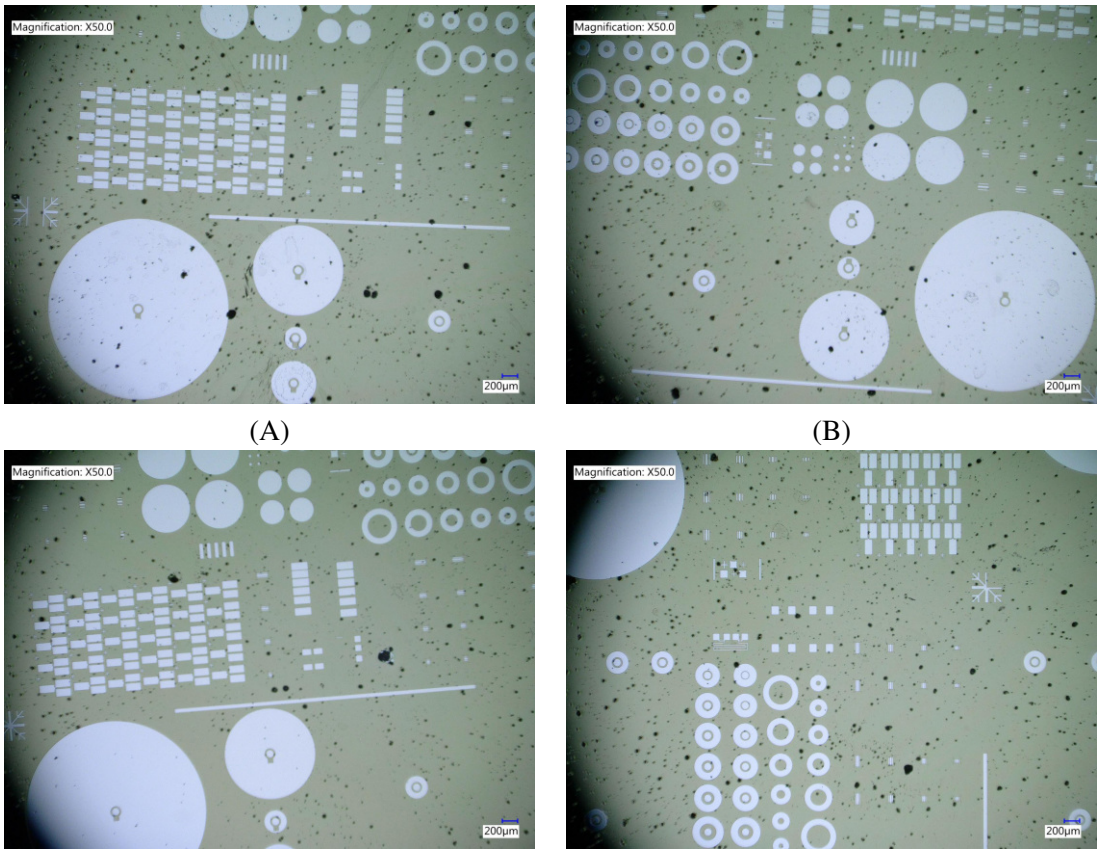


Figure C.9: AZ LNR-003 spun on 2 inch Si wafer, UV dose 125 mJ $\cdot$ cm^{-2}. This is pre-metal deposition. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

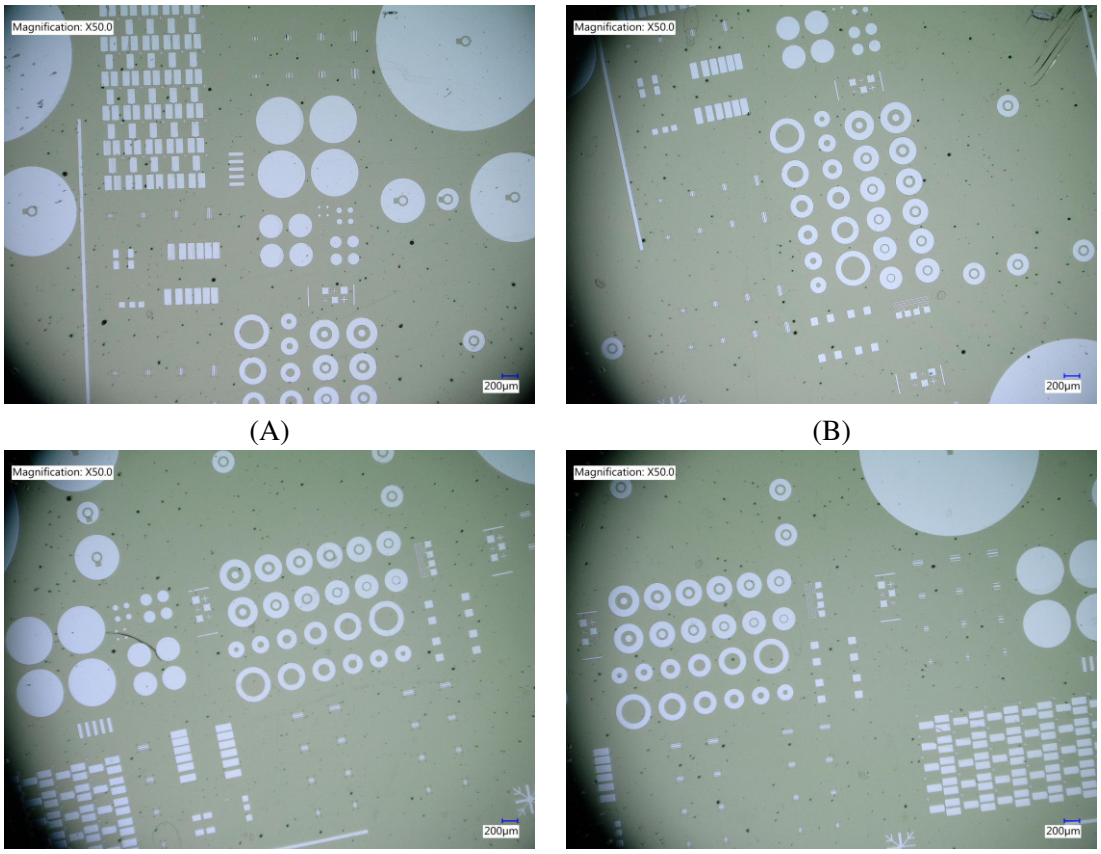


Figure C.10: AZ LNR-003 spun on 2 inch Si wafer, UV dose 150 mJ $\cdot$ cm^{-2}. This is pre-metal deposition. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

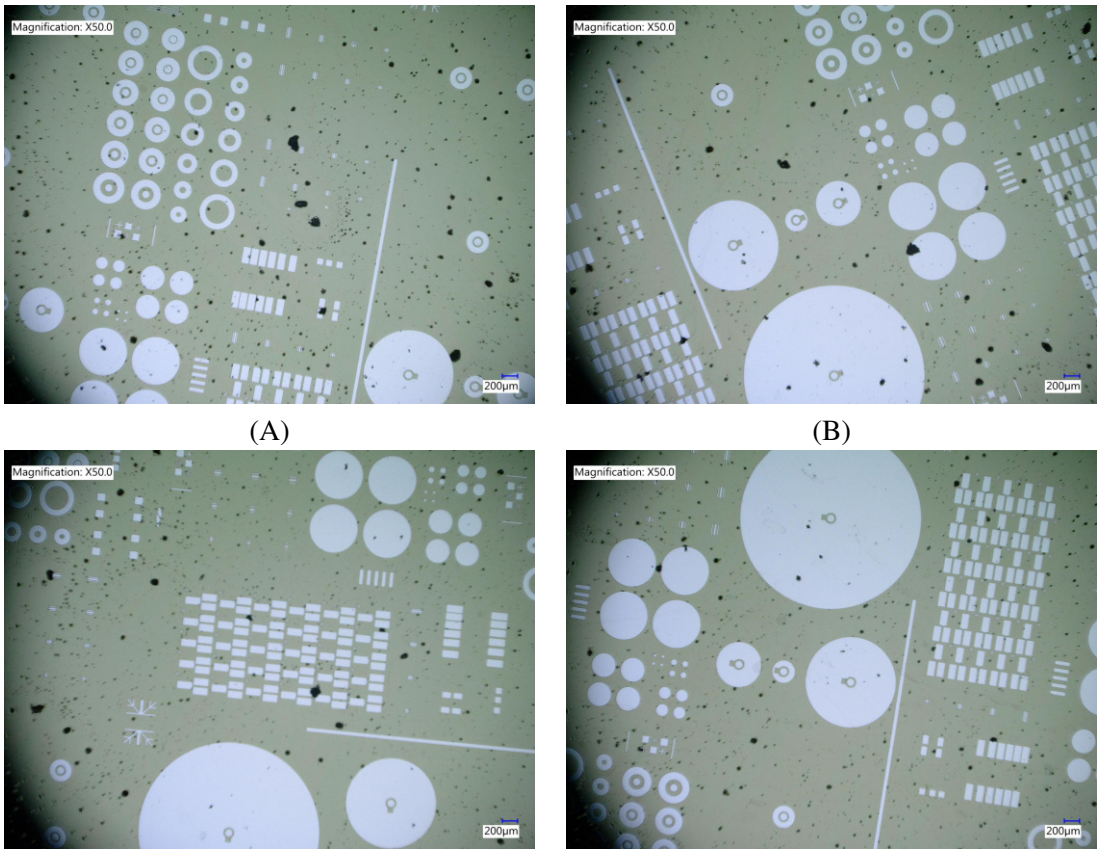


Figure C.11: AZ LNR-003 spun on 2 inch Si wafer, UV dose 175 mJ $\cdot$ cm^{-2}. This is pre-metal deposition. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

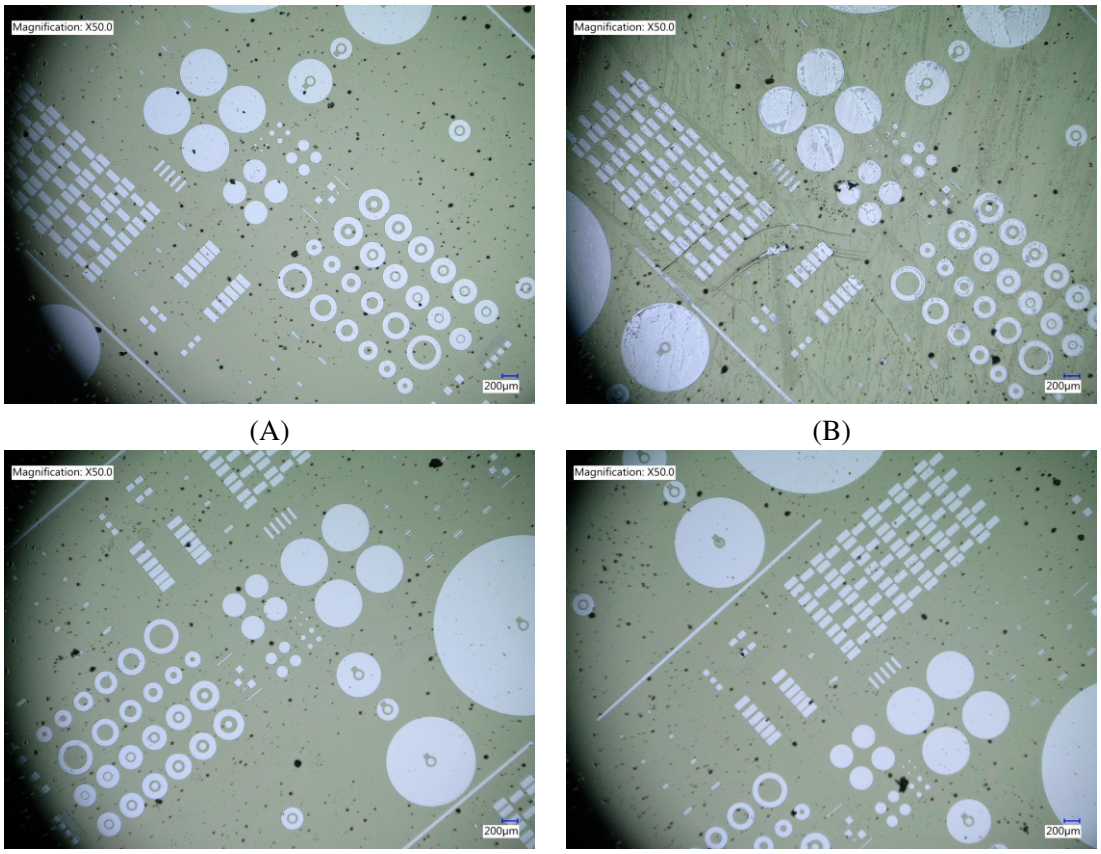


Figure C.12: AZ LNR-003 spun on 2 inch Si wafer, UV dose 200 mJ $\cdot$ cm^{-2}. This is pre-metal deposition. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

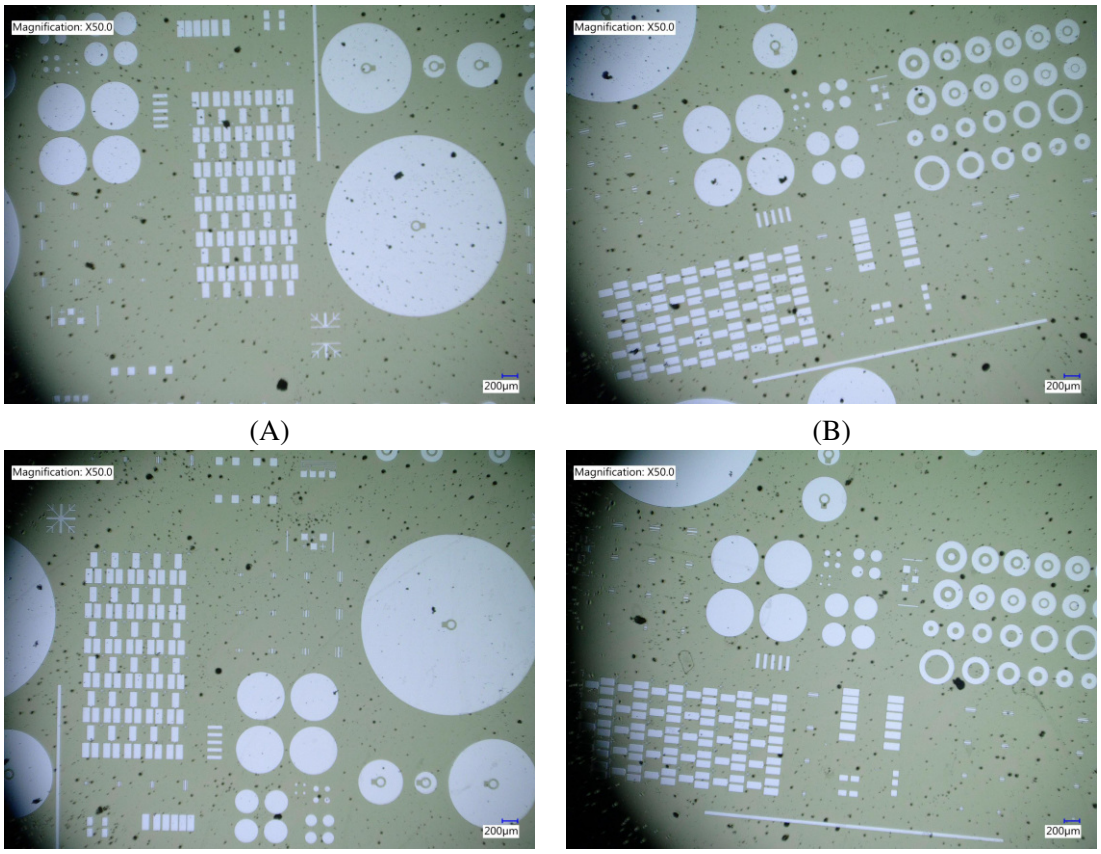


Figure C.13: AZ LNR-003 spun on 2 inch Si wafer, UV dose 225 mJ $\cdot$ cm^{-2}. This is pre-metal deposition. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

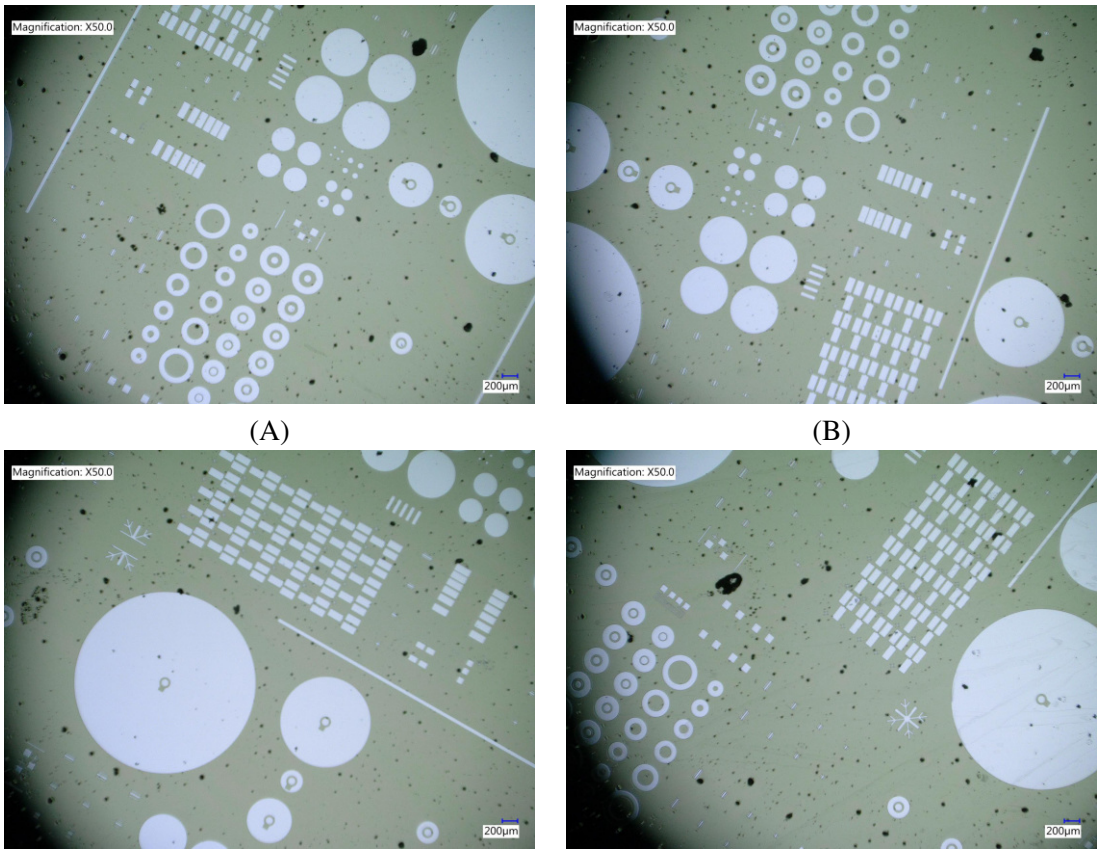


Figure C.14: AZ LNR-003 spun on 2 inch Si wafer, UV dose 250 mJ $\cdot$ cm^{-2}. This is pre-metal deposition. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

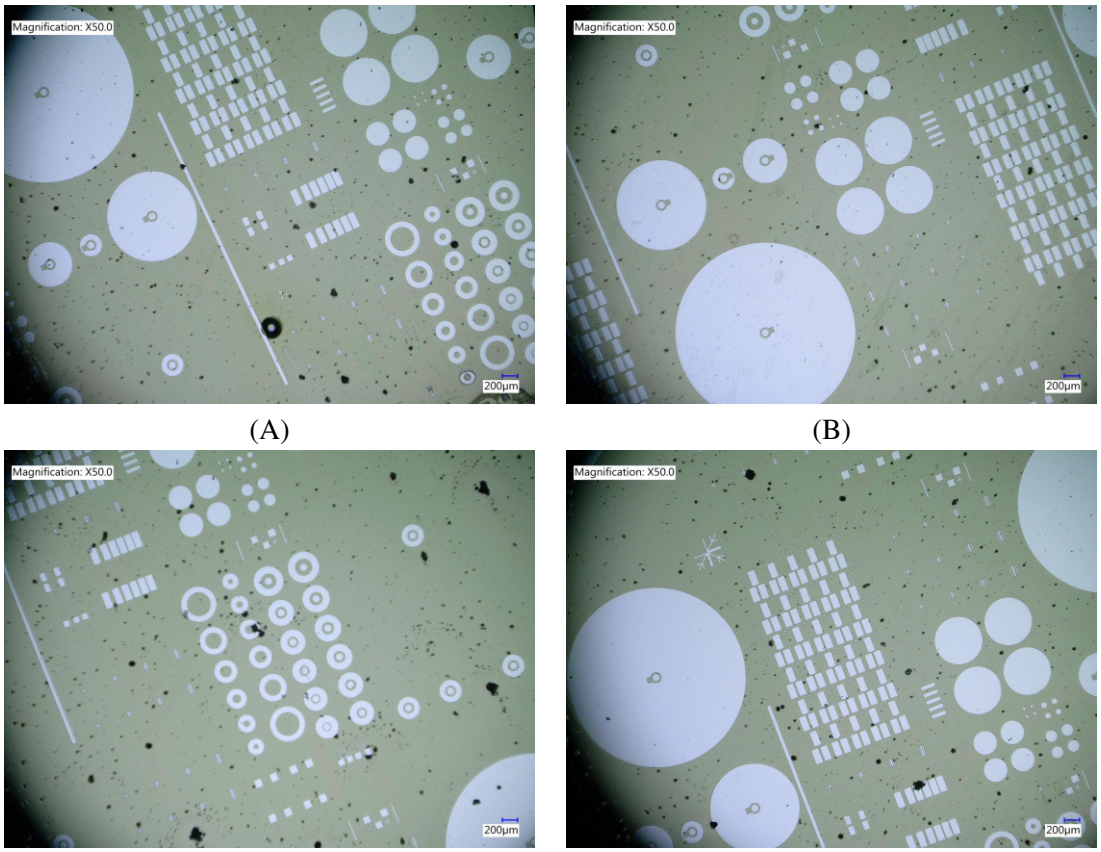


Figure C.15: AZ LNR-003 spun on 2 inch Si wafer, UV dose 275 mJ $\cdot$ cm^{-2}. This is pre-metal deposition. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

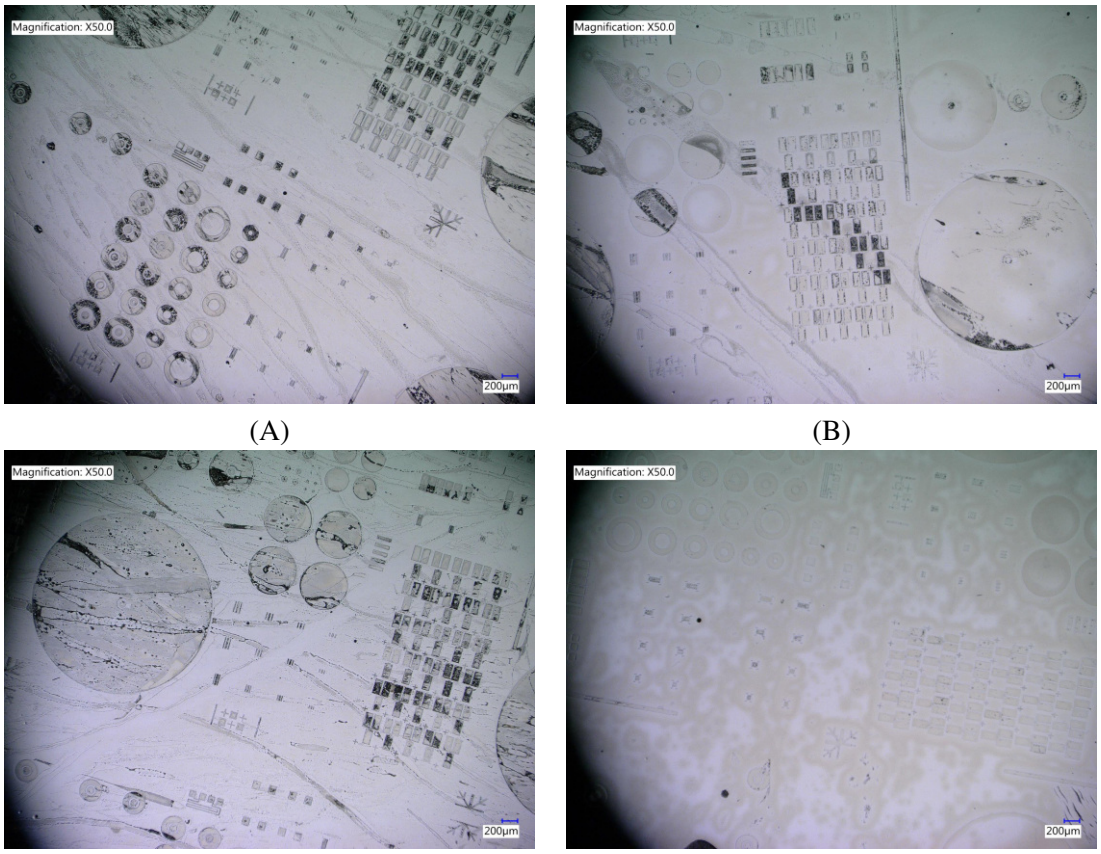


Figure C.16: AZ LNR-003 spun on 2 inch Si wafer, UV dose 100 mJ $\cdot$ cm^{-2}. This is post-metal deposition, 20/80 Ti/Al. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

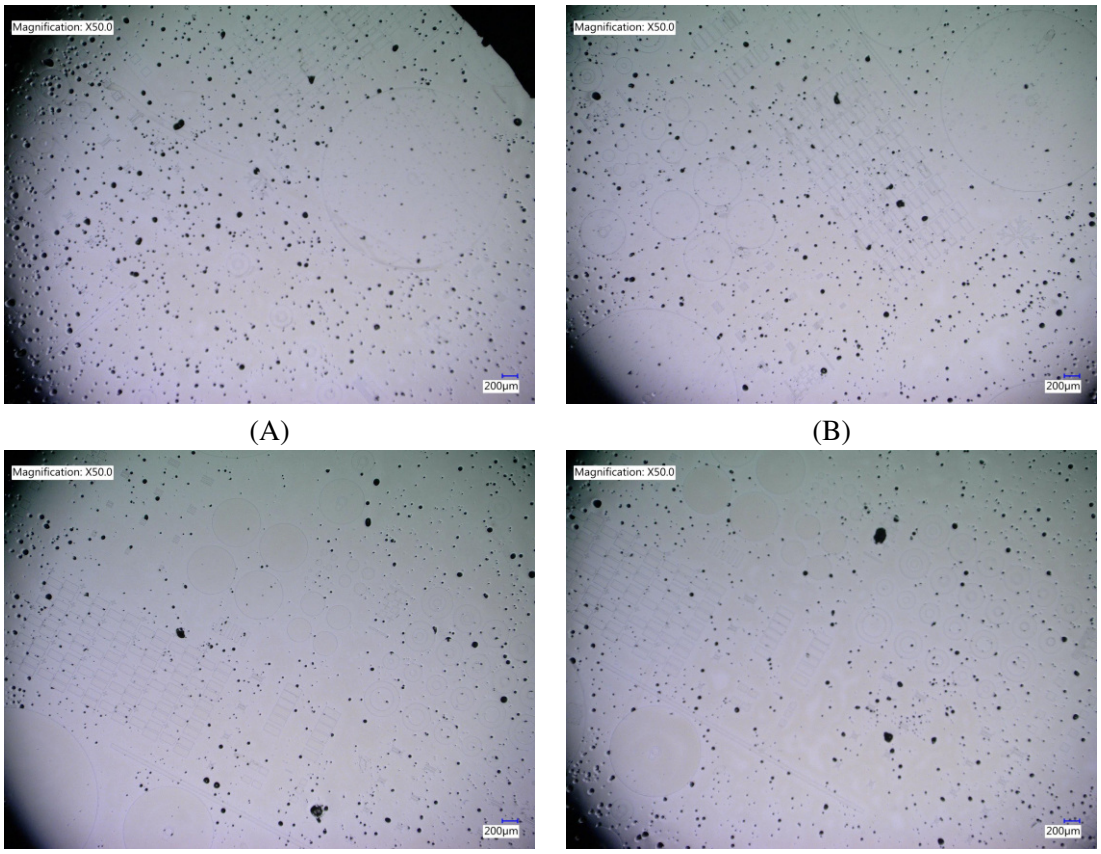


Figure C.17: AZ LNR-003 spun on 2 inch Si wafer, UV dose 125 mJ $\cdot$ cm^{-2}. This is post-metal deposition, 20/80 Ti/Al. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

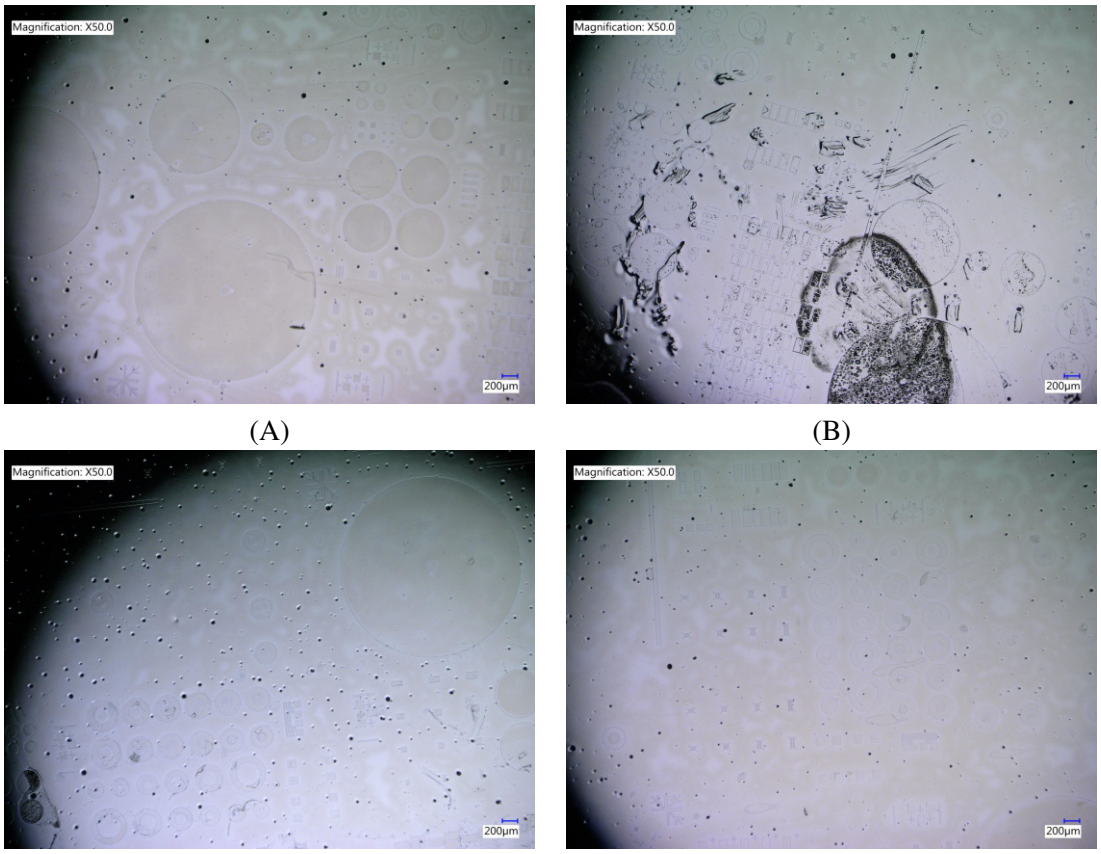


Figure C.18: AZ LNR-003 spun on 2 inch Si wafer, UV dose 150 mJ $\cdot$ cm^{-2}. This is post-metal deposition, 20/80 Ti/Al. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

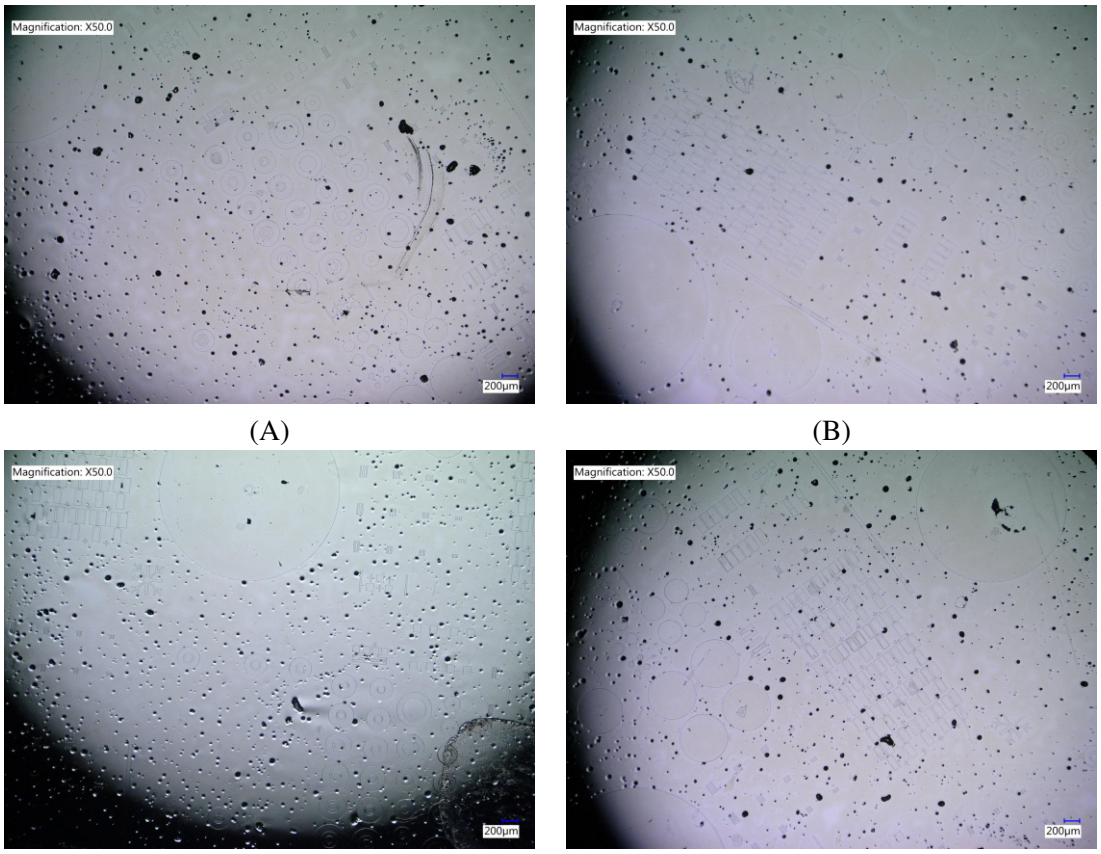


Figure C.19: AZ LNR-003 spun on 2 inch Si wafer, UV dose 175 mJ $\cdot$ cm^{-2}. This is post-metal deposition, 20/80 Ti/Al. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

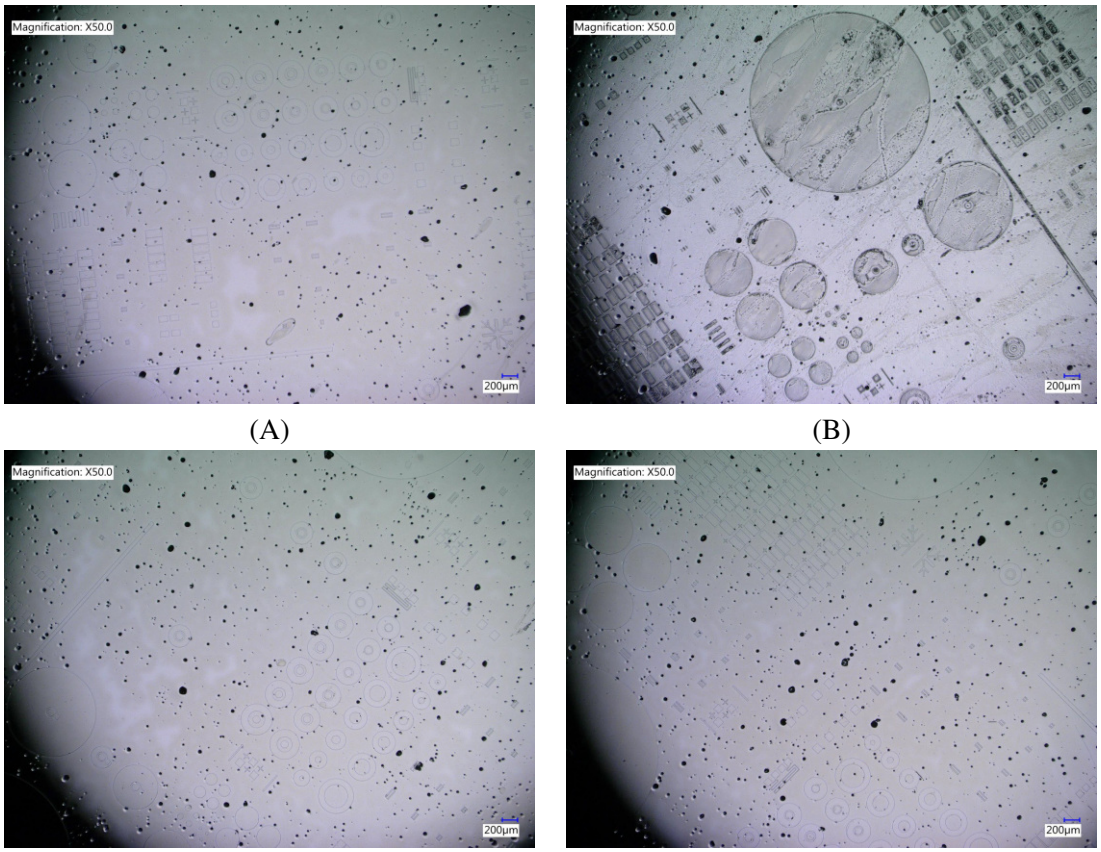


Figure C.20: AZ LNR-003 spun on 2 inch Si wafer, UV dose 200 mJ $\cdot$ cm^{-2}. This is post-metal deposition, 20/80 Ti/Al. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

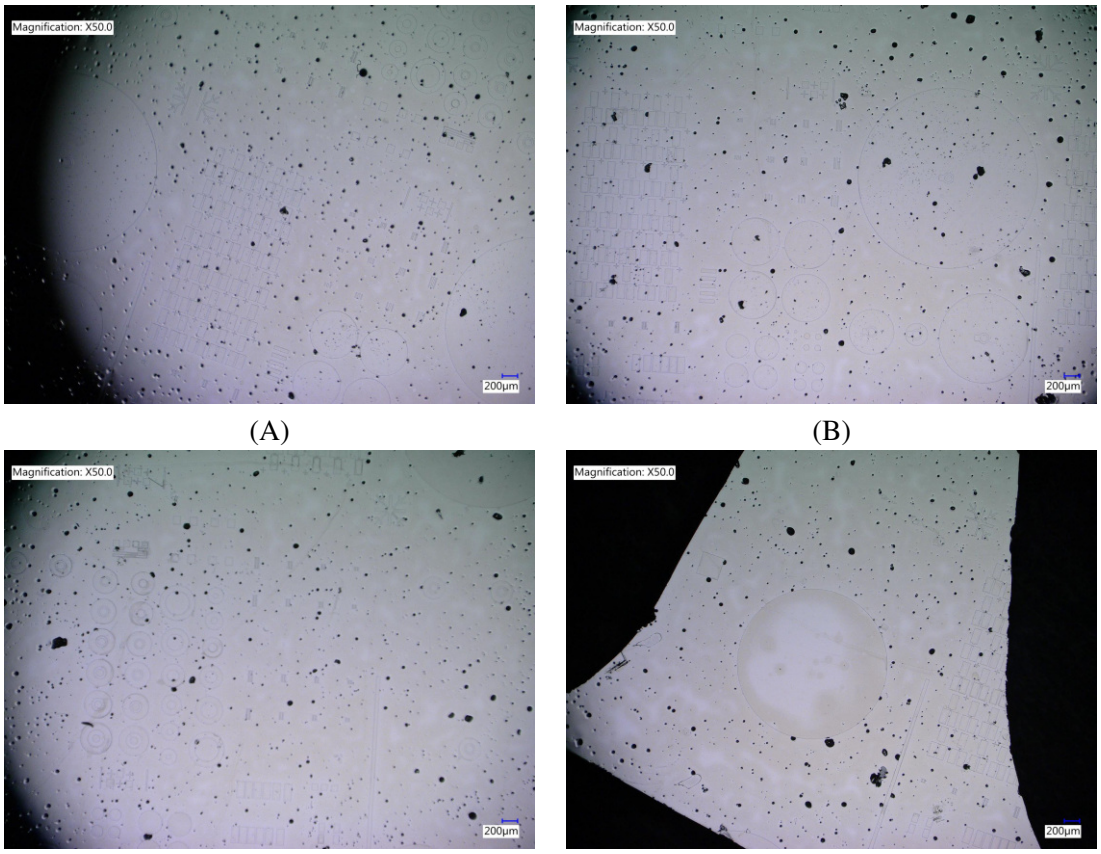


Figure C.21: AZ LNR-003 spun on 2 inch Si wafer, UV dose 225 mJ $\cdot$ cm^{-2}. This is post-metal deposition, 20/80 Ti/Al. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

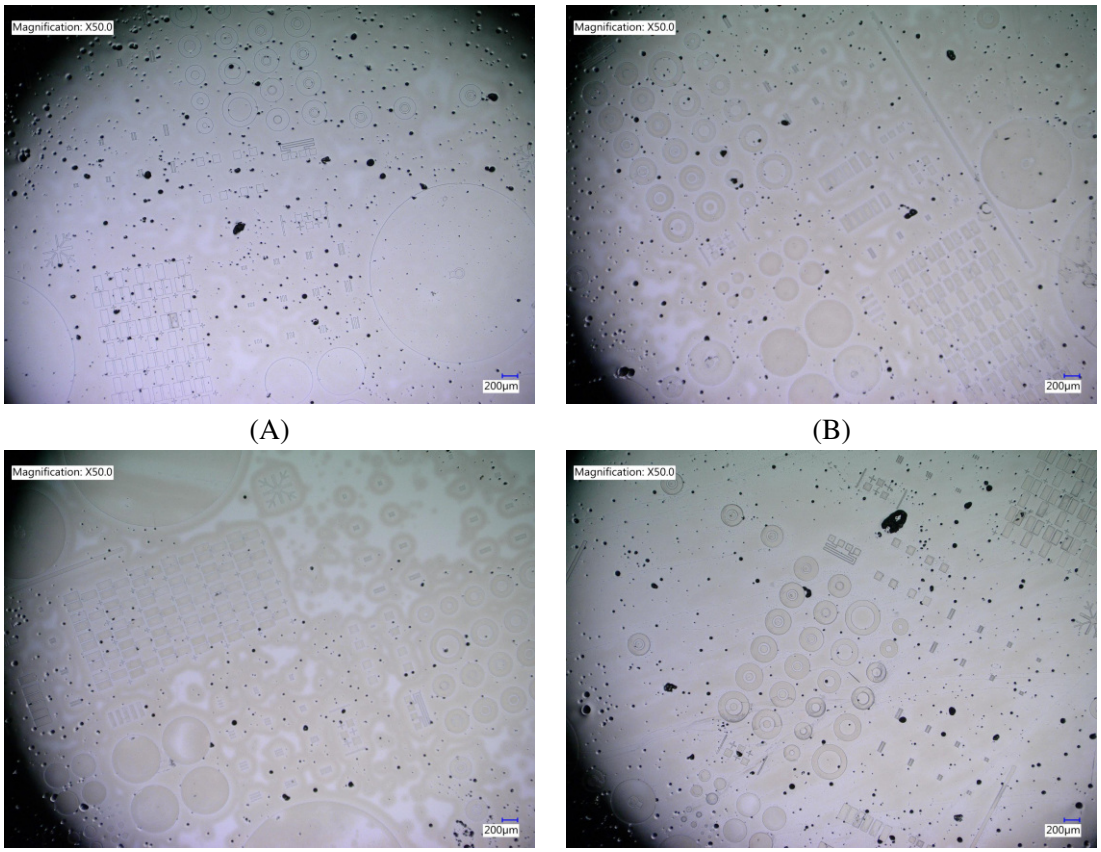


Figure C.22: AZ LNR-003 spun on 2 inch Si wafer, UV dose 250 mJ $\cdot$ cm^{-2}. This is post-metal deposition, 20/80 Ti/Al. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

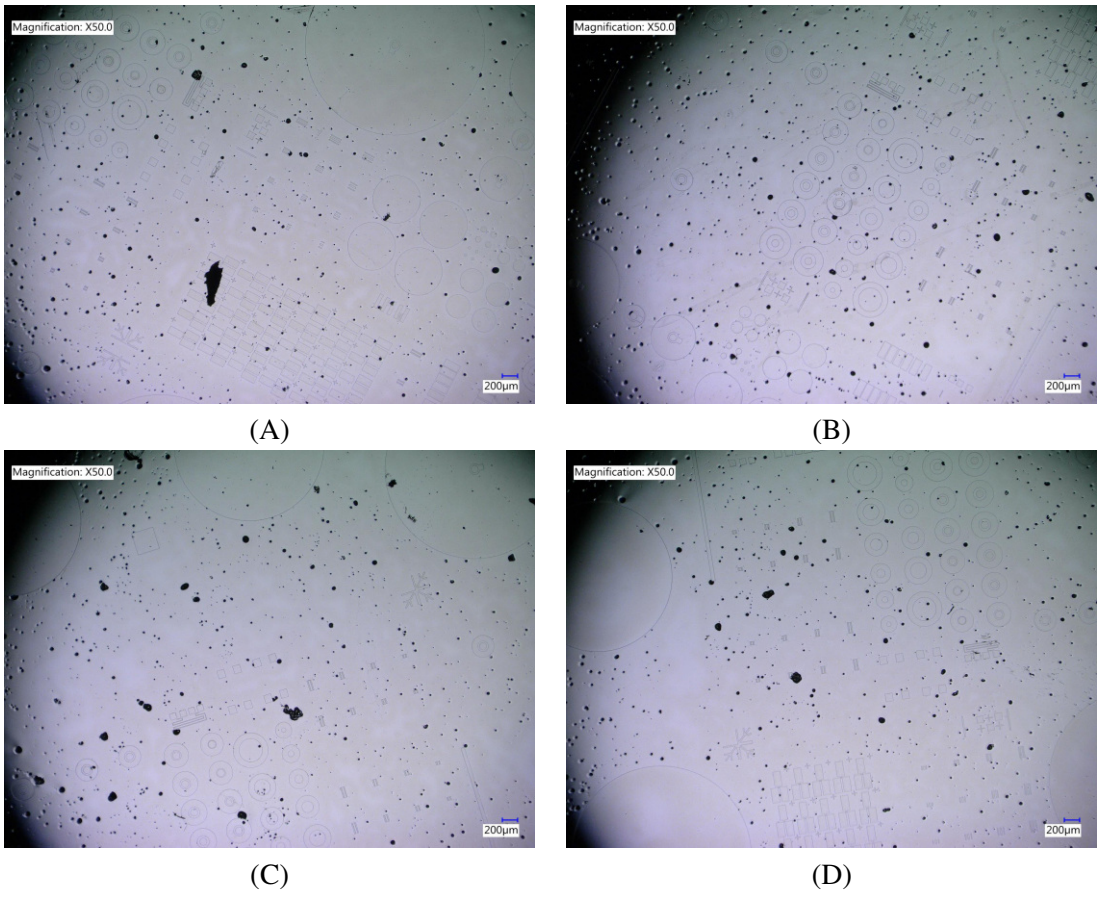


Figure C.23: AZ LNR-003 spun on 2 inch Si wafer, UV dose 275 mJ $\cdot$ cm^{-2}. This is post-metal deposition, 20/80 Ti/Al. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

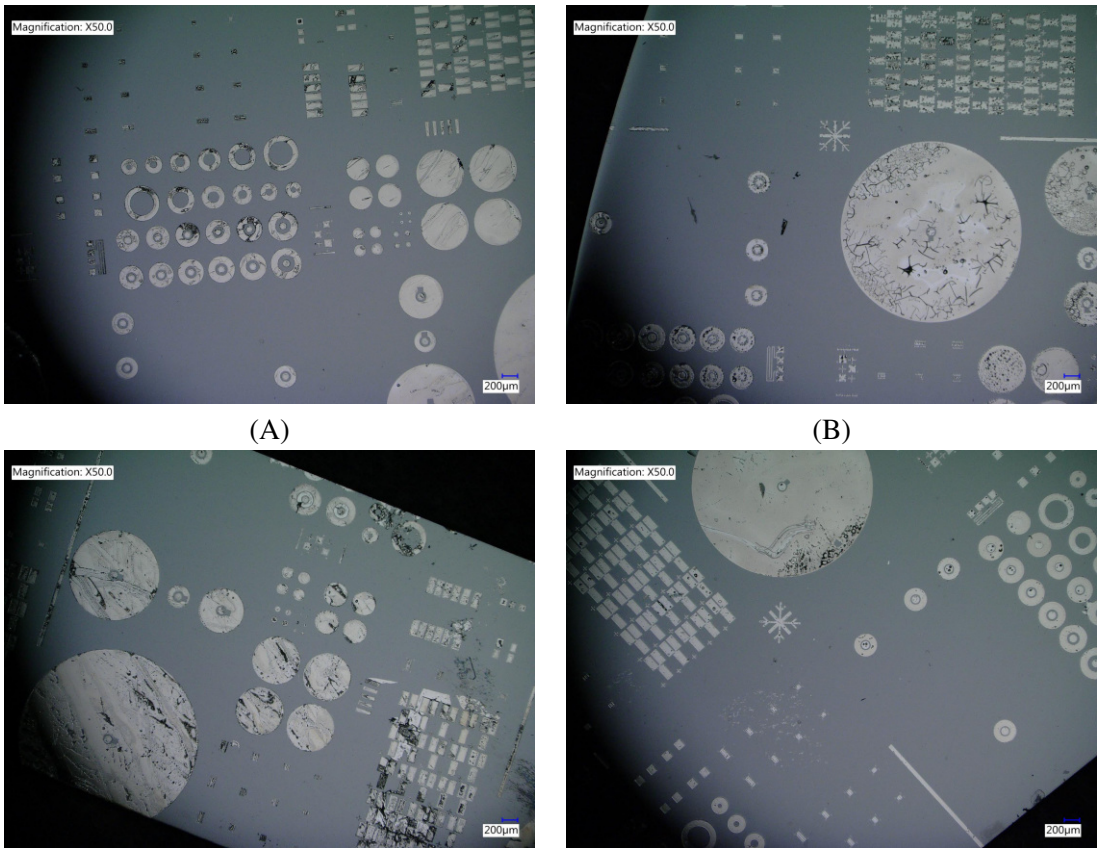


Figure C.24: AZ LNR-003 spun on 2 inch Si wafer, UV dose 100 mJ·cm^{-2}. This is post-metal lift-off, 20/80 Ti/Al. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

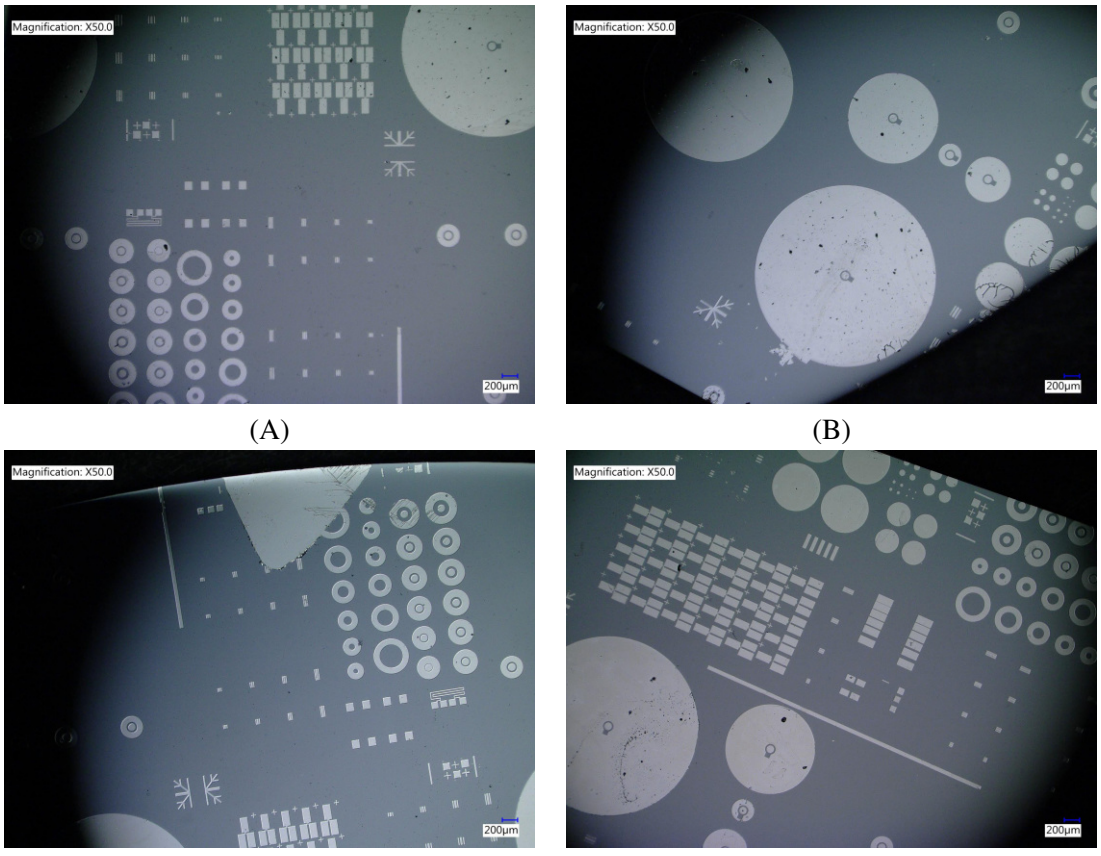


Figure C.25: AZ LNR-003 spun on 2 inch Si wafer, UV dose 125 mJ·cm^{-2}. This is post-metal lift-off, 20/80 Ti/Al. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

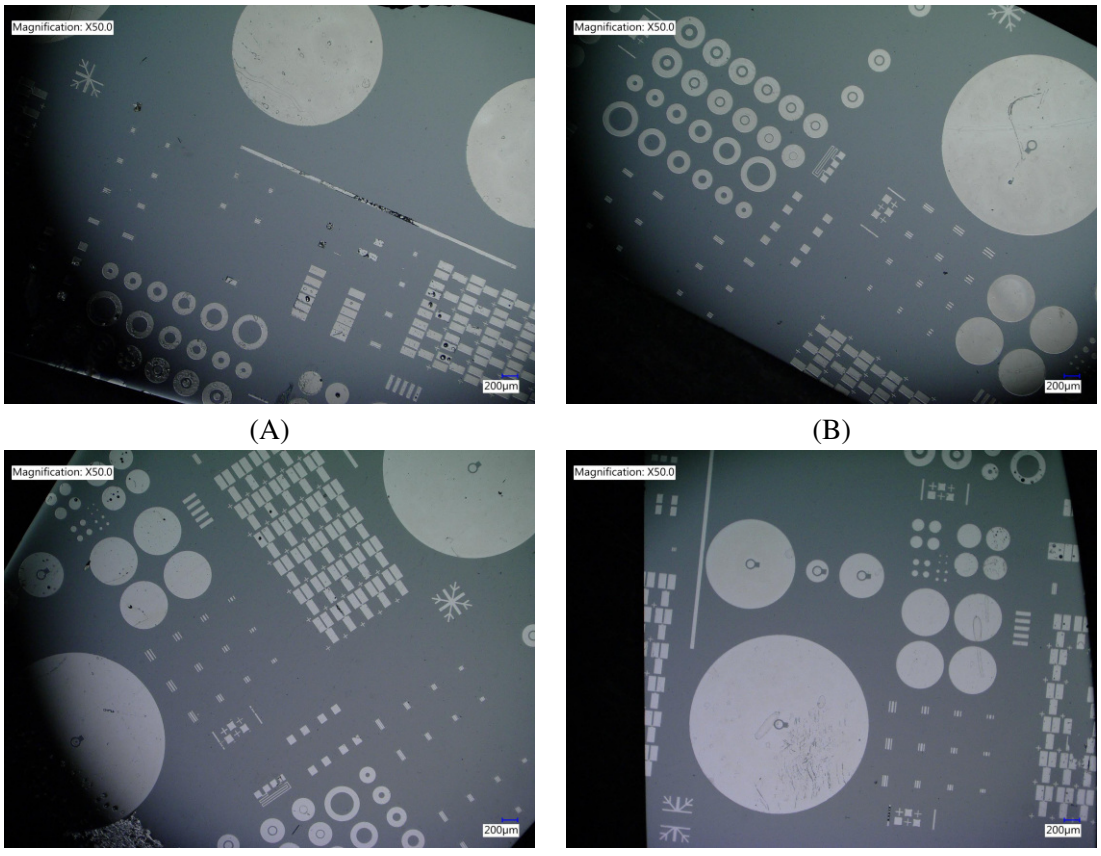


Figure C.26: AZ LNR-003 spun on 2 inch Si wafer, UV dose 150 mJ·cm^{-2}. This is post-metal lift-off, 20/80 Ti/Al. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

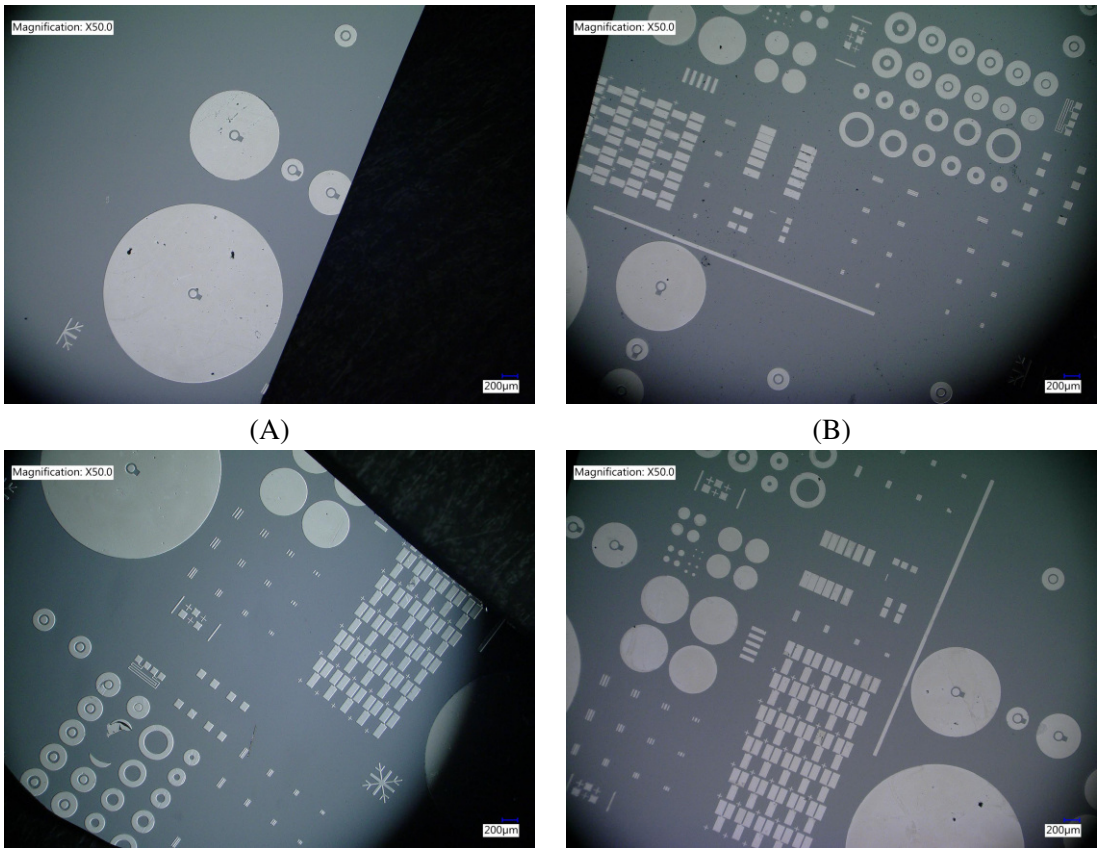


Figure C.27: AZ LNR-003 spun on 2 inch Si wafer, UV dose 175 mJ$\cdot$cm^{-2}. This is post-metal lift-off, 20/80 Ti/Al. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

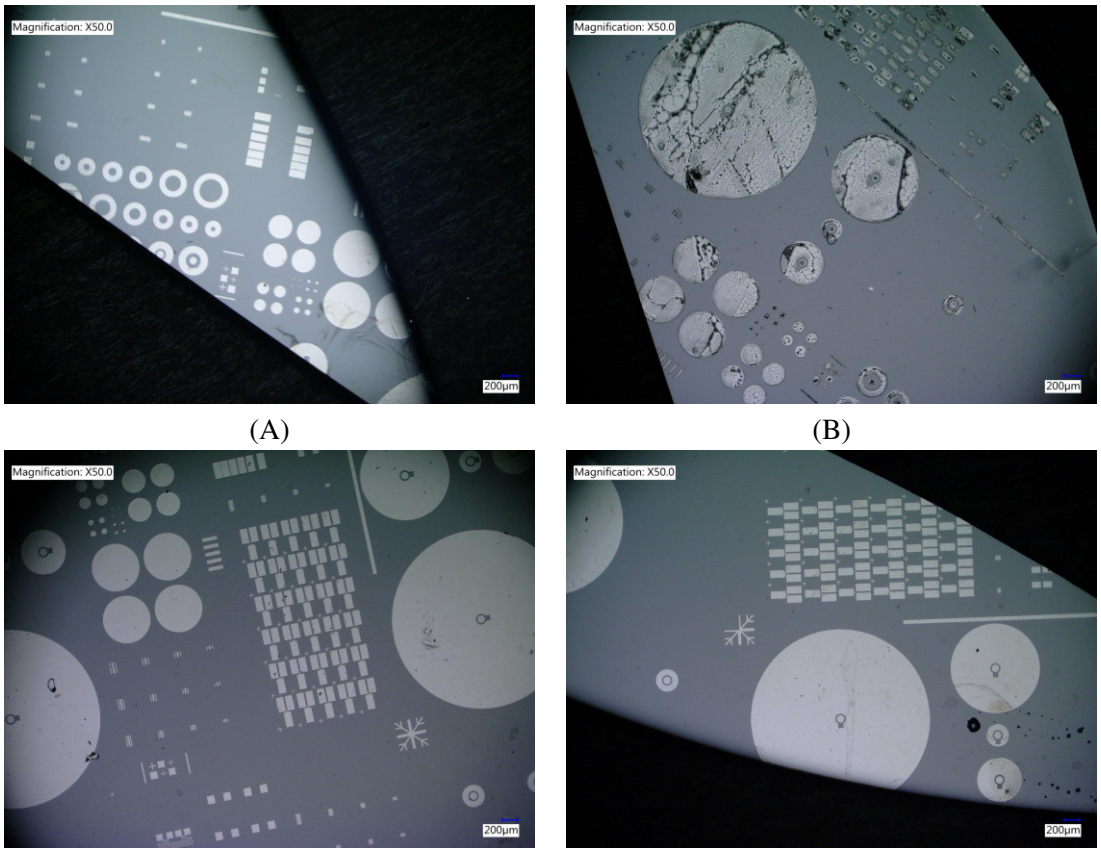


Figure C.28: AZ LNR-003 spun on 2 inch Si wafer, UV dose 200 mJ$\cdot$cm^{-2}. This is post-metal lift-off, 20/80 Ti/Al. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

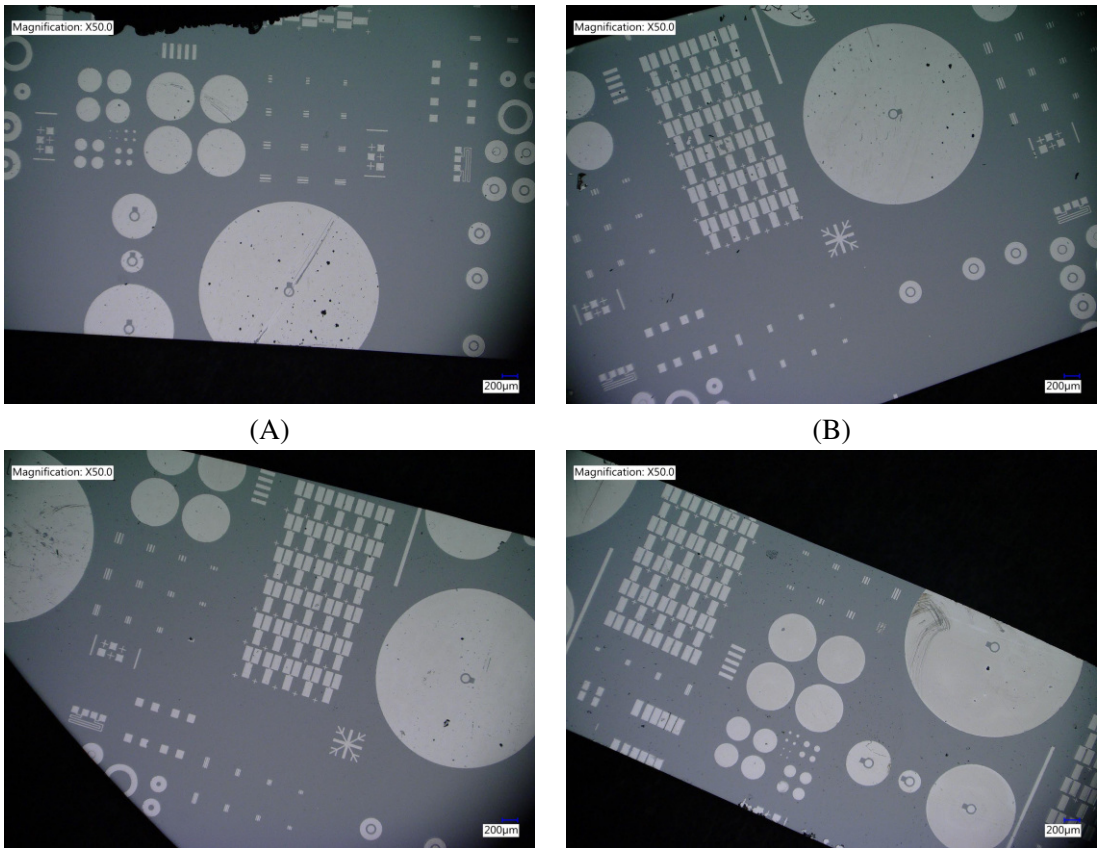


Figure C.29: AZ LNR-003 spun on 2 inch Si wafer, UV dose 225 mJ$\cdot$cm^{-2}. This is post-metal lift-off, 20/80 Ti/Al. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

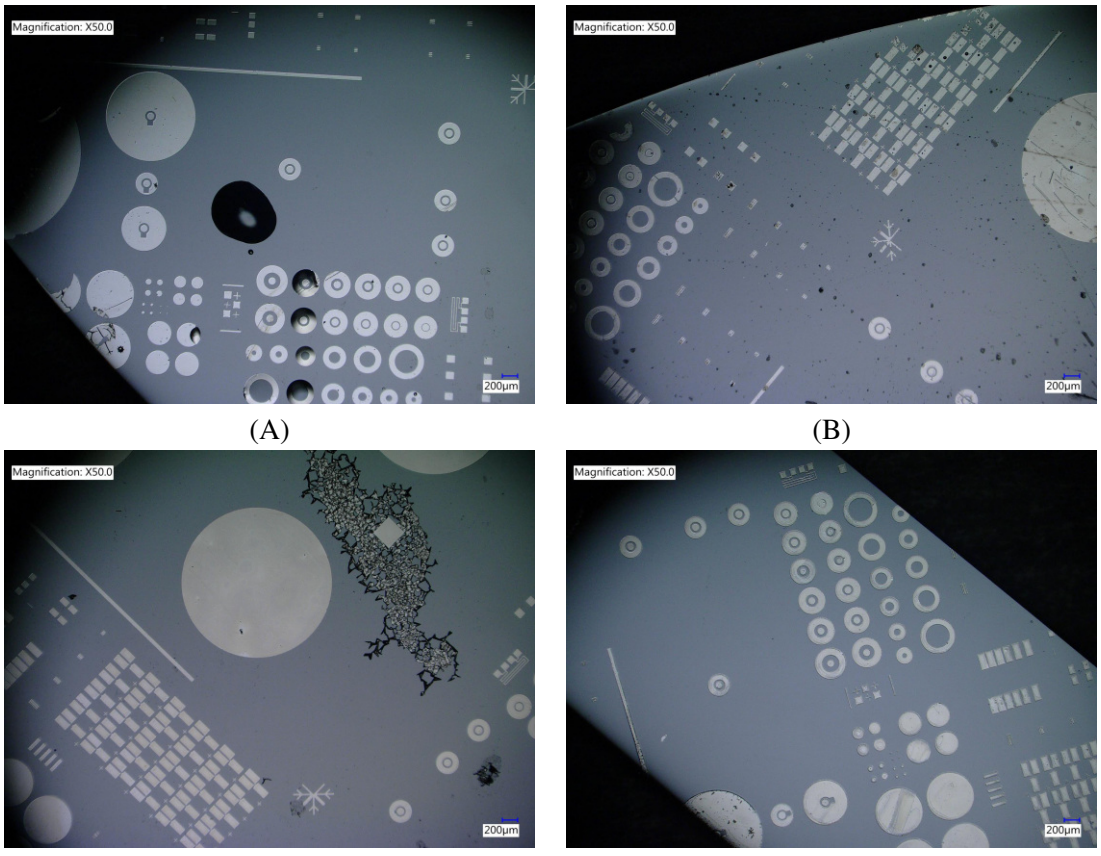


Figure C.30: AZ LNR-003 spun on 2 inch Si wafer, UV dose 250 mJ·cm^{-2}. This is post-metal lift-off, 20/80 Ti/Al. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

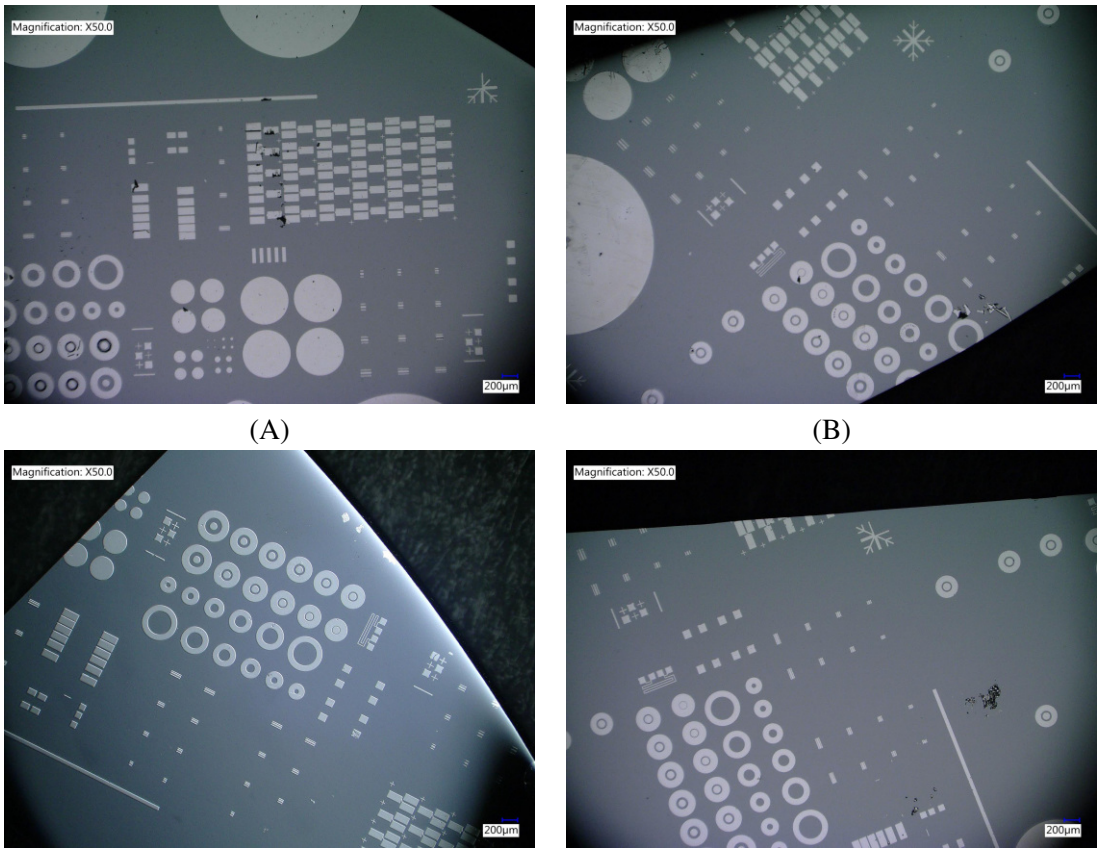
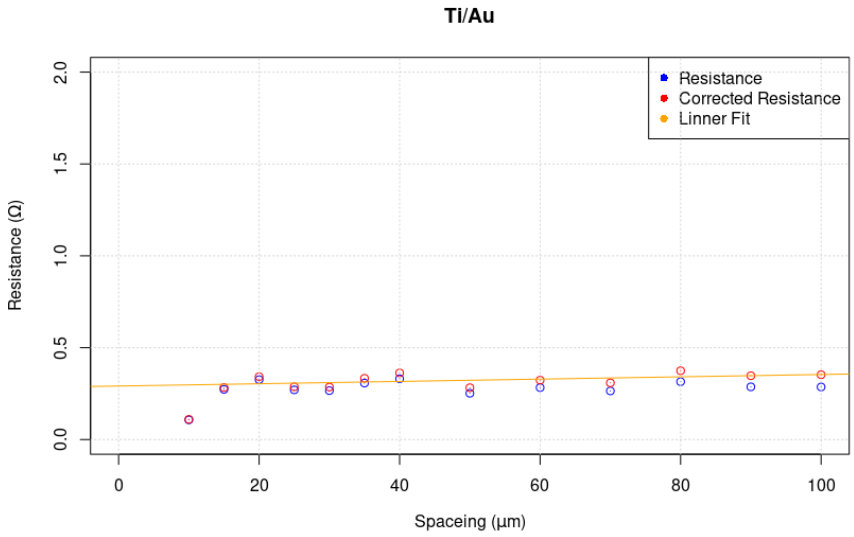
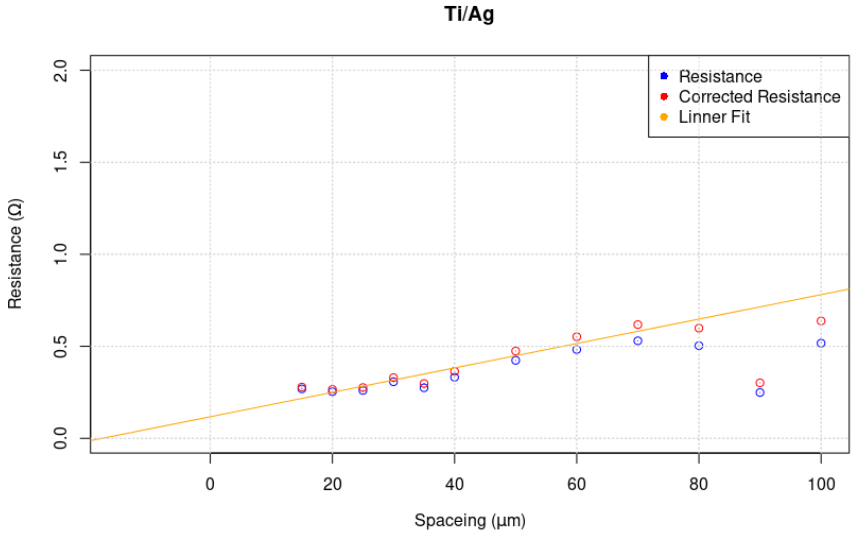


Figure C.31: AZ LNR-003 spun on 2 inch Si wafer, UV dose 275 mJ$\cdot$cm^{-2}. This is post-metal lift-off, 20/80 Ti/Al. A, B, C and D refer to development times of 50, 60, 70 and 80 s.

C.5 CTLM from cycle two

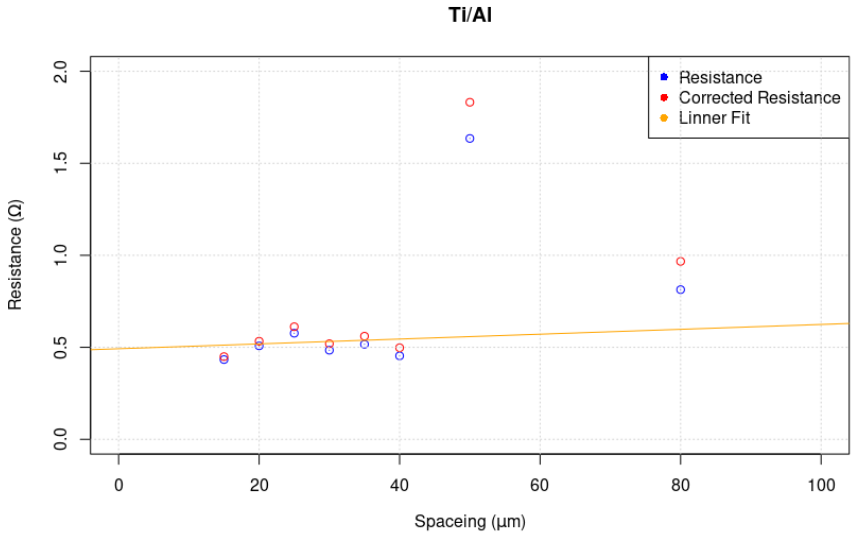


(A)

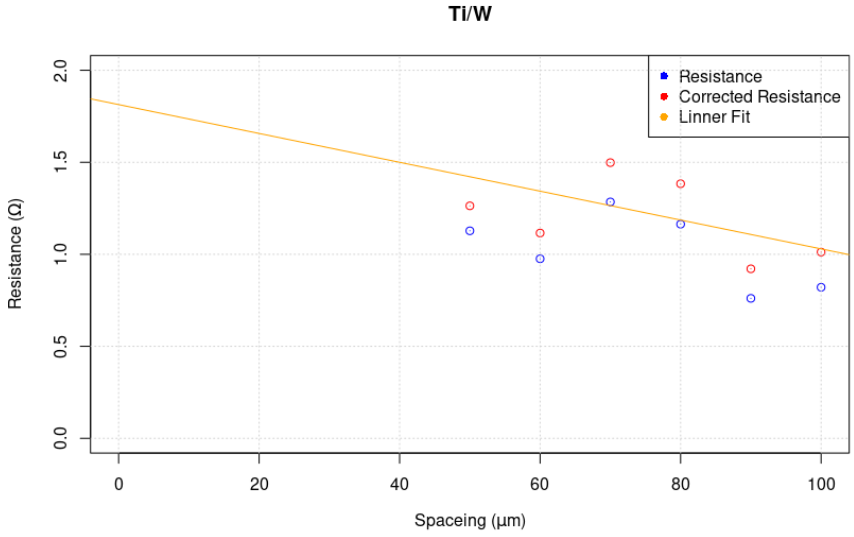


(B)

Figure C.32: The resistance from the CTLM contacts for Ti/Au, Ti/Ag, Ti/Al and Ti/W as (A), (B), (C), (D) and (E) combined onto a single plot, respectively. The blue markers are the original collected resistance, and the red markers are corrected for CTLM. The orange lines are linear fit to portions of the data, which are supposed to mimic TLM data. The combined data set shows Ti/Au, Ti/Ag, Ti/Al and Ti/W as blue, red, orange and green, respectively. It can be seen that of these, only Ti/Ag appears to be following a TLM pattern.

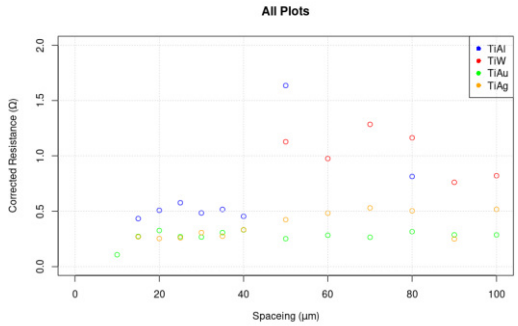


(C)



(D)

Figure C.32: The resistance from the CTLM contacts for Ti/Au, Ti/Ag, Ti/Al and Ti/W as (A), (B), (C), (D) and (E) combined onto a single plot, respectively. The blue markers are the original collected resistance, and the red markers are corrected for CTLM. The orange lines are linear fit to portions of the data, which are supposed to mimic TLM data. The combined data set shows Ti/Au, Ti/Ag, Ti/Al and Ti/W as blue, red, orange and green, respectively. It can be seen that of these, only Ti/Ag appears to be following a TLM pattern.



(E)

Figure C.32: The resistance from the CTLM contacts for Ti/Au, Ti/Ag, Ti/Al and Ti/W as (A), (B), (C), (D) and (E) combined onto a single plot, respectively. The blue markers are the original collected resistance, and the red markers are corrected for CTLM. The orange lines are linear fit to portions of the data, which are supposed to mimic TLM data. The combined data set shows Ti/Au, Ti/Ag, Ti/Al and Ti/W as blue, red, orange and green, respectively. It can be seen that of these, only Ti/Ag appears to be following a TLM pattern.

Contact		Ti/Au	Ti/Al	Ti/W	Ti/Ag
$2R_C$	Ω	0.291	0.492	1.813	0.117
$2\Delta R_C$	Ω	0.018	0.083	0.630	0.0306
Gradient	$\Omega \cdot \mu m$	0.0006283	0.001321	-0.007842	0.0066342
ΔGradient	$\Omega \cdot \mu m$	0.0003137	0.002880	0.007752	0.0006161
ρ_C	$\Omega \cdot cm^2$	7.375×10^{-5}	0.000309	0.00113944748	7.37×10^{-5}
$\Delta\rho_C$	$\Omega \cdot cm^2$	0.00022987	0.000400	0.0016294	0.00039502
L_T	μm	231	186	Na	8
ΔL_T	μm	16	75	Na	23
R_{Sh}	$\Omega \cdot \square$	0.126	0.264	-1.565	1.327
ΔR_{Sh}	$\Omega \cdot \square$	0.063	0.58	1.550	0.123

Table C.1: The liner fitting parameters and calculated, this is where the number can be calculated or calculated. This is fitting to $y = m \cdot x + c$, where the y intercept is $2R_C$, $-2L_T$ is the x intercept, m is the gradient $\frac{R_{Sh}}{L}$ and ρ_C is the specific contact resistance. The errors are calculated from the standard error (shown with Δ) of the fitting parameters with propagation of errors. Due to the negative gradient for Ti/W, the transfer length was not calculated as it would have been positive, in the wrong direction.

C.6 Appendix for cycle three

Table C.2: The tabulated data from the plots in Figures 6.3, showing the fitted gradients and intercepts of the plots between ±0.5 V. At the different metalisations and CTLM spacing.

Sample	**Anneal**	**Spacing** μ**m**	**m** Ω^{-1}	Δ**m** Ω^{-1}	$\mathbf{I_0}$ **A**	$\Delta\mathbf{I_0}$ $\Delta\mathbf{I_0}$	$\mathbf{V_0}$ **V**	$\Delta\mathbf{V_0}$ **V**
Ag	As deposited	5	4.68×10^{-6}	3.78×10^{-8}	1.87×10^{-8}	1.15×10^{-8}	0.004	0.00245
Ag	As deposited	10	3.26×10^{-6}	1.33×10^{-8}	3.63×10^{-9}	4.02×10^{-9}	-0.00111	0.00123
Ag	As deposited	15	2.62×10^{-6}	6.50×10^{-9}	4.99×10^{-10}	1.97×10^{-9}	-1.90×10^{-4}	7.51×10^{-4}
Ag	As deposited	20	2.28×10^{-6}	3.71×10^{-9}	-6.55×10^{-10}	1.12×10^{-9}	2.87×10^{-4}	4.91×10^{-4}
Ag	As deposited	25	1.66×10^{-6}	3.37×10^{-9}	6.62×10^{-10}	1.02×10^{-9}	-3.99×10^{-4}	6.15×10^{-4}
Ag	As deposited	30	1.52×10^{-6}	1.49×10^{-9}	-1.18×10^{-9}	4.50×10^{-10}	7.74×10^{-4}	2.96×10^{-4}
Ag	As deposited	35	1.46×10^{-6}	1.20×10^{-9}	-1.07×10^{-9}	3.62×10^{-10}	7.32×10^{-4}	2.49×10^{-4}
Ag	As deposited	40	1.37×10^{-6}	1.02×10^{-9}	-1.10×10^{-9}	3.10×10^{-10}	8.01×10^{-4}	2.26×10^{-4}
Ag	As deposited	50	1.06×10^{-6}	7.38×10^{-10}	-8.80×10^{-10}	2.24×10^{-10}	8.28×10^{-4}	2.10×10^{-4}
Ag	As deposited	60	9.49×10^{-7}	5.85×10^{-10}	-7.47×10^{-10}	1.77×10^{-10}	7.87×10^{-4}	1.87×10^{-4}
Ag	As deposited	70	8.72×10^{-7}	5.00×10^{-10}	-6.72×10^{-10}	1.51×10^{-10}	7.71×10^{-4}	1.73×10^{-4}
Ag	As deposited	80	8.22×10^{-7}	4.52×10^{-10}	-6.12×10^{-10}	1.37×10^{-10}	7.45×10^{-4}	1.67×10^{-4}
Ag	As deposited	90	5.49×10^{-7}	2.06×10^{-10}	-8.53×10^{-11}	6.24×10^{-11}	1.55×10^{-4}	1.14×10^{-4}
Ag	As deposited	100	5.52×10^{-7}	1.94×10^{-10}	-5.57×10^{-11}	5.87×10^{-11}	1.01×10^{-4}	1.06×10^{-4}
Ag	Annealed 100°C	5	5.32×10^{-6}	7.91×10^{-8}	1.03×10^{-9}	2.29×10^{-8}	-1.93×10^{-4}	0.0043
Ag	Annealed 100°C	10	2.52×10^{-6}	1.60×10^{-8}	1.48×10^{-9}	4.64×10^{-9}	-5.88×10^{-4}	0.00184
Ag	Annealed 100°C	15	1.96×10^{-6}	6.82×10^{-9}	-3.03×10^{-10}	1.97×10^{-9}	1.55×10^{-4}	0.00101
Ag	Annealed 100°C	20	1.65×10^{-6}	3.69×10^{-9}	-8.05×10^{-10}	1.07×10^{-9}	4.87×10^{-4}	6.47×10^{-4}
Ag	Annealed 100°C	25	1.28×10^{-6}	1.98×10^{-9}	-8.01×10^{-10}	5.73×10^{-10}	6.26×10^{-4}	4.48×10^{-4}
Ag	Annealed 100°C	30	1.18×10^{-6}	1.50×10^{-9}	-1.07×10^{-9}	4.34×10^{-10}	9.06×10^{-4}	3.67×10^{-4}
Ag	Annealed 100°C	35	1.06×10^{-6}	1.06×10^{-9}	-8.34×10^{-10}	3.08×10^{-10}	7.86×10^{-4}	2.91×10^{-4}
Ag	Annealed 100°C	40	1.01×10^{-6}	8.63×10^{-10}	-7.87×10^{-10}	2.50×10^{-10}	7.78×10^{-4}	2.47×10^{-4}
Ag	Annealed 100°C	50	7.97×10^{-7}	5.53×10^{-10}	-6.41×10^{-10}	1.60×10^{-10}	8.04×10^{-4}	2.01×10^{-4}
Ag	Annealed 100°C	60	7.16×10^{-7}	4.95×10^{-10}	-6.46×10^{-10}	1.43×10^{-10}	9.02×10^{-4}	2.00×10^{-4}
Ag	Annealed 100°C	70	6.69×10^{-7}	4.45×10^{-10}	-6.11×10^{-10}	1.29×10^{-10}	9.12×10^{-4}	1.92×10^{-4}
Ag	Annealed 100°C	80	6.22×10^{-7}	3.97×10^{-10}	-5.39×10^{-10}	1.15×10^{-10}	8.66×10^{-4}	1.85×10^{-4}

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Table C.2 – Continued From Previous Page

Sample	**Anneal**	**Spacing** μm	**m** Ω^{-1}	**Δm** Ω^{-1}	$\mathbf{I_0}$ **A**	$\mathbf{\Delta I_0}$ $\mathbf{\Delta I_0}$	$\mathbf{V_0}$ **V**	$\mathbf{\Delta V_0}$ **V**
Ag	Annealed 100°C	90	3.59×10^{-7}	2.61×10^{-10}	-3.16×10^{-10}	7.56×10^{-11}	8.80×10^{-4}	2.11×10^{-4}
Ag	Annealed 100°C	100	3.58×10^{-7}	2.64×10^{-10}	-3.18×10^{-10}	7.64×10^{-11}	8.88×10^{-4}	2.13×10^{-4}
Ag	Annealed 400°C	5	1.96×10^{-4}	5.05×10^{-6}	5.54×10^{-7}	1.53×10^{-6}	-0.00283	0.00781
Ag	Annealed 400°C	10	6.94×10^{-5}	1.15×10^{-6}	4.31×10^{-8}	3.49×10^{-7}	-6.22×10^{-4}	0.00503
Ag	Annealed 400°C	15	2.02×10^{-5}	2.14×10^{-7}	1.35×10^{-9}	6.49×10^{-8}	-6.68×10^{-5}	0.0032
Ag	Annealed 400°C	20	2.94×10^{-5}	2.65×10^{-7}	5.29×10^{-9}	8.02×10^{-8}	-1.80×10^{-4}	0.00273
Ag	Annealed 400°C	25	1.98×10^{-5}	1.05×10^{-7}	-9.51×10^{-10}	3.17×10^{-8}	4.80×10^{-5}	0.0016
Ag	Annealed 400°C	30	1.60×10^{-5}	6.05×10^{-8}	-1.12×10^{-9}	1.83×10^{-8}	7.00×10^{-5}	0.00114
Ag	Annealed 400°C	35	1.41×10^{-5}	4.29×10^{-8}	-2.13×10^{-9}	1.30×10^{-8}	1.51×10^{-4}	9.22×10^{-4}
Ag	Annealed 400°C	40	41.16×10^{-5}	2.56×10^{-8}	-2.58×10^{-9}	7.75×10^{-9}	2.22×10^{-4}	6.66×10^{-4}
Ag	Annealed 400°C	50	9.27×10^{-6}	1.27×10^{-8}	-3.22×10^{-9}	3.85×10^{-9}	3.47×10^{-4}	4.15×10^{-4}
Ag	Annealed 400°C	60	7.73×10^{-6}	7.77×10^{-9}	-3.70×10^{-9}	2.35×10^{-9}	4.79×10^{-4}	3.05×10^{-4}
Ag	Annealed 400°C	70	5.76×10^{-6}	3.85×10^{-9}	-3.62×10^{-9}	1.16×10^{-9}	6.30×10^{-4}	2.02×10^{-4}
Ag	Annealed 400°C	80	6.88×10^{-6}	4.30×10^{-9}	-3.87×10^{-9}	1.30×10^{-9}	5.62×10^{-4}	1.89×10^{-4}
Ag	Annealed 400°C	90	6.64×10^{-6}	4.13×10^{-9}	-3.58×10^{-9}	1.25×10^{-9}	5.40×10^{-4}	1.88×10^{-4}
Ag	Annealed 400°C	100	5.69×10^{-6}	2.97×10^{-9}	-3.32×10^{-9}	8.98×10^{-10}	5.84×10^{-4}	1.58×10^{-4}
Ag	Annealed 500°C	5	5.18×10^{-4}	9.50×10^{-6}	2.18×10^{-7}	2.88×10^{-6}	-4.22×10^{-4}	0.00556
Ag	Annealed 500°C	10	1.41×10^{-4}	1.87×10^{-6}	-5.80×10^{-8}	5.65×10^{-7}	4.12×10^{-4}	0.00401
Ag	Annealed 500°C	15	1.03×10^{-4}	1.30×10^{-6}	3.18×10^{-8}	3.93×10^{-7}	-3.09×10^{-4}	0.00382
Ag	Annealed 500°C	20	6.43×10^{-5}	6.15×10^{-7}	2.40×10^{-8}	1.86×10^{-7}	-3.73×10^{-4}	0.0029
Ag	Annealed 500°C	25	3.78×10^{-5}	2.53×10^{-7}	3.97×10^{-9}	7.65×10^{-8}	-1.05×10^{-4}	0.00202
Ag	Annealed 500°C	30	3.14×10^{-5}	1.43×10^{-7}	-6.18×10^{-9}	4.34×10^{-8}	1.97×10^{-4}	0.00138
Ag	Annealed 500°C	35	2.69×10^{-5}	9.37×10^{-8}	-6.89×10^{-9}	2.84×10^{-8}	2.56×10^{-4}	0.00106
Ag	Annealed 500°C	40	2.58×10^{-5}	7.56×10^{-8}	-7.62×10^{-9}	2.29×10^{-8}	2.95×10^{-4}	8.86×10^{-4}
Ag	Annealed 500°C	50	1.62×10^{-5}	2.71×10^{-8}	-6.18×10^{-9}	8.20×10^{-9}	3.83×10^{-4}	5.07×10^{-4}
Ag	Annealed 500°C	60	1.44×10^{-5}	1.78×10^{-8}	-5.60×10^{-9}	5.40×10^{-9}	3.88×10^{-4}	3.75×10^{-4}
Ag	Annealed 500°C	70	1.29×10^{-5}	1.21×10^{-8}	-5.52×10^{-9}	3.65×10^{-9}	4.28×10^{-4}	2.83×10^{-4}

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Table C.2 – Continued From Previous Page

Sample	**Anneal**	**Spacing** μm	**m** Ω^{-1}	**Δm** Ω^{-1}	$\mathbf{I_0}$ **A**	$\mathbf{\Delta I_0}$ $\mathbf{\Delta I_0}$	$\mathbf{V_0}$ **V**	$\mathbf{\Delta V_0}$ **V**
Ag	Annealed 500°C	80	1.19×10^{-5}	9.07×10^{-9}	-4.03×10^{-9}	2.75×10^{-9}	3.39×10^{-4}	2.31×10^{-4}
Ag	Annealed 500°C	90	1.28×10^{-5}	9.18×10^{-9}	-6.46×10^{-9}	2.78×10^{-9}	5.04×10^{-4}	2.17×10^{-4}
Ag	Annealed 500°C	100	8.16×10^{-6}	3.61×10^{-9}	-4.23×10^{-9}	1.09×10^{-9}	5.19×10^{-4}	1.34×10^{-4}
Au	As deposited	5	Na	Na	Na	Na	Na	Na
Au	As deposited	10	6.83×10^{-6}	5.92×10^{-8}	-1.04×10^{-9}	1.79×10^{-8}	1.53×10^{-4}	0.00263
Au	As deposited	15	Na	Na	Na	Na	Na	Na
Au	As deposited	20	3.40×10^{-6}	1.01×10^{-8}	3.90×10^{-9}	3.07×10^{-9}	-0.00115	9.03×10^{-4}
Au	As deposited	25	2.84×10^{-6}	5.00×10^{-9}	-1.08×10^{-9}	1.52×10^{-9}	3.83×10^{-4}	5.34×10^{-4}
Au	As deposited	30	2.43×10^{-6}	3.84×10^{-9}	-4.75×10^{-10}	1.16×10^{-9}	1.95×10^{-4}	4.78×10^{-4}
Au	As deposited	35	2.19×10^{-6}	3.07×10^{-9}	-2.45×10^{-9}	9.31×10^{-10}	0.00112	4.26×10^{-4}
Au	As deposited	40	1.99×10^{-6}	3.18×10^{-9}	6.30×10^{-9}	9.63×10^{-10}	-0.00317	4.83×10^{-4}
Au	As deposited	50	1.96×10^{-6}	1.69×10^{-9}	-1.15×10^{-9}	5.12×10^{-10}	5.85×10^{-4}	2.61×10^{-4}
Au	As deposited	60	1.56×10^{-6}	9.76×10^{-10}	1.02×10^{-9}	2.96×10^{-10}	-6.54×10^{-4}	1.90×10^{-4}
Au	As deposited	70	1.50×10^{-6}	5.35×10^{-10}	1.75×10^{-10}	1.62×10^{-10}	-1.17×10^{-4}	1.08×10^{-4}
Au	As deposited	80	1.42×10^{-6}	4.91×10^{-10}	-2.25×10^{-10}	1.49×10^{-10}	1.59×10^{-4}	1.05×10^{-4}
Au	As deposited	90	7.91×10^{-7}	3.12×10^{-10}	-2.65×10^{-10}	9.46×10^{-11}	3.35×10^{-4}	1.20×10^{-4}
Au	As deposited	100	8.27×10^{-7}	4.27×10^{-10}	-4.82×10^{-10}	1.29×10^{-10}	5.83×10^{-4}	1.57×10^{-4}
Au	Annealed 100°C	5	1.54×10^{-5}	1.41×10^{-7}	2.50×10^{-9}	4.28×10^{-8}	-1.63×10^{-4}	0.00279
Au	Annealed 100°C	10	9.39×10^{-6}	5.16×10^{-8}	3.39×10^{-10}	1.56×10^{-8}	-3.61×10^{-5}	1.67×10^{-3}
Au	Annealed 100°C	15	6.34×10^{-6}	2.50×10^{-8}	-1.24×10^{-9}	7.58×10^{-9}	1.95×10^{-4}	0.0012
Au	Annealed 100°C	20	5.84×10^{-6}	1.25×10^{-8}	-1.92×10^{-9}	3.78×10^{-9}	3.29×10^{-4}	6.48×10^{-4}
Au	Annealed 100°C	25	4.61×10^{-6}	8.27×10^{-9}	-2.26×10^{-9}	2.50×10^{-9}	4.89×10^{-4}	5.43×10^{-4}
Au	Annealed 100°C	30	Na	Na	Na	Na	Na	Na
Au	Annealed 100°C	35	3.95×10^{-6}	7.28×10^{-9}	-2.05×10^{-9}	2.21×10^{-9}	5.18×10^{-4}	5.58×10^{-4}
Au	Annealed 100°C	40	2.35×10^{-6}	9.06×10^{-9}	2.03×10^{-9}	2.74×10^{-9}	-8.65×10^{-4}	0.00117
Au	Annealed 100°C	50	3.06×10^{-6}	2.39×10^{-9}	-1.69×10^{-9}	7.23×10^{-10}	5.52×10^{-4}	2.36×10^{-4}
Au	Annealed 100°C	60	2.26×10^{-6}	1.60×10^{-9}	-1.57×10^{-9}	4.84×10^{-10}	6.96×10^{-4}	2.14×10^{-4}

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Table C.2 – Continued From Previous Page

Sample	Anneal	Spacing μm	m Ω^{-1}	Δm Ω^{-1}	I_0 A	ΔI_0 ΔI_0	V_0 V	ΔV_0 V
Au	Annealed 100°C	70	1.98×10^{-6}	1.66×10^{-9}	-1.61×10^{-9}	5.03×10^{-10}	8.14×10^{-4}	2.54×10^{-4}
Au	Annealed 100°C	80	2.80×10^{-6}	3.00×10^{-9}	-3.76×10^{-9}	9.09×10^{-10}	0.00134	3.25×10^{-4}
Au	Annealed 100°C	90	2.36×10^{-6}	1.03×10^{-9}	-1.20×10^{-9}	3.12×10^{-10}	5.10×10^{-4}	1.32×10^{-4}
Au	Annealed 100°C	100	1.88×10^{-6}	7.86×10^{-10}	-1.17×10^{-9}	2.38×10^{-10}	6.20×10^{-4}	1.27×10^{-4}
Au	Annealed 400°C	5	7.12×10^{-6}	9.95×10^{-8}	1.16×10^{-8}	3.01×10^{-8}	-0.00162	0.00423
Au	Annealed 400°C	10	3.18×10^{-6}	1.77×10^{-8}	-5.36×10^{-10}	5.36×10^{-9}	1.69×10^{-4}	0.00169
Au	Annealed 400°C	15	2.43×10^{-6}	7.50×10^{-9}	-1.14×10^{-9}	2.27×10^{-9}	4.67×10^{-4}	9.34×10^{-4}
Au	Annealed 400°C	20	2.82×10^{-6}	5.20×10^{-8}	-2.67×10^{-8}	1.57×10^{-8}	0.00946	0.00559
Au	Annealed 400°C	25	1.79×10^{-6}	2.40×10^{-9}	-1.24×10^{-9}	7.26×10^{-10}	6.93×10^{-4}	4.07×10^{-4}
Au	Annealed 400°C	30	1.53×10^{-6}	2.10×10^{-9}	-1.27×10^{-9}	6.35×10^{-10}	8.32×10^{-4}	4.15×10^{-4}
Au	Annealed 400°C	35	1.32×10^{-6}	1.72×10^{-9}	-1.20×10^{-9}	5.20×10^{-10}	9.14×10^{-4}	3.95×10^{-4}
Au	Annealed 400°C	40	8.93×10^{-7}	6.63×10^{-10}	-4.91×10^{-10}	2.01×10^{-10}	5.50×10^{-4}	2.25×10^{-4}
Au	Annealed 400°C	50	1.15×10^{-6}	1.83×10^{-8}	-1.07×10^{-8}	5.55×10^{-9}	0.00927	0.00481
Au	Annealed 400°C	60	9.01×10^{-7}	6.98×10^{-10}	-8.85×10^{-10}	2.11×10^{-10}	9.82×10^{-4}	2.35×10^{-4}
Au	Annealed 400°C	70	Na	0	Na	Na	Na	Na
Au	Annealed 400°C	80	6.51×10^{-7}	4.34×10^{-10}	-6.32×10^{-10}	1.31×10^{-10}	9.71×10^{-4}	2.02×10^{-4}
Au	Annealed 400°C	90	7.53×10^{-7}	4.22×10^{-10}	-6.22×10^{-10}	1.28×10^{-10}	8.26×10^{-4}	1.70×10^{-4}
Au	Annealed 400°C	100	6.66×10^{-7}	3.91×10^{-10}	-5.89×10^{-10}	1.18×10^{-10}	8.84×10^{-4}	1.78×10^{-4}
Au	Annealed 500°C	5	1.24×10^{-5}	2.61×10^{-8}	-1.04×10^{-9}	7.92×10^{-9}	8.41×10^{-5}	6.41×10^{-4}
Au	Annealed 500°C	10	1.09×10^{-5}	1.36×10^{-8}	-3.05×10^{-9}	4.11×10^{-9}	2.79×10^{-4}	3.76×10^{-4}
Au	Annealed 500°C	15	9.95×10^{-6}	9.09×10^{-9}	8.99×10^{-9}	2.75×10^{-9}	-9.04×10^{-4}	2.77×10^{-4}
Au	Annealed 500°C	20	Na	0	Na	Na	Na	Na
Au	Annealed 500°C	25	6.60×10^{-6}	3.47×10^{-9}	-3.17×10^{-9}	1.05×10^{-9}	4.80×10^{-4}	1.59×10^{-4}
Au	Annealed 500°C	30	5.98×10^{-6}	2.90×10^{-9}	-3.15×10^{-9}	8.79×10^{-10}	5.26×10^{-4}	1.47×10^{-4}
Au	Annealed 500°C	35	5.81×10^{-6}	2.50×10^{-9}	-2.99×10^{-9}	7.57×10^{-10}	5.14×10^{-4}	1.30×10^{-4}
Au	Annealed 500°C	40	As deposited	0	As deposited	0	As deposited	0
Au	Annealed 500°C	50	3.64×10^{-6}	1.51×10^{-9}	-2.38×10^{-9}	4.59×10^{-10}	6.55×10^{-4}	1.26×10^{-4}

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Table C.2 – Continued From Previous Page

Sample	**Anneal**	**Spacing** μ**m**	**m** Ω^{-1}	Δ**m** Ω^{-1}	$\mathbf{I_0}$ **A**	$\Delta\mathbf{I_0}$ $\Delta\mathbf{I_0}$	$\mathbf{V_0}$ **V**	$\Delta\mathbf{V_0}$ **V**
Au	Annealed 500°C	60	3.41×10^{-6}	1.43×10^{-9}	-2.30×10^{-9}	4.32×10^{-10}	6.76×10^{-4}	1.27×10^{-4}
Au	Annealed 500°C	70	3.14×10^{-6}	1.30×10^{-9}	-2.18×10^{-9}	3.93×10^{-10}	6.93×10^{-4}	1.25×10^{-4}
Au	Annealed 500°C	80	3.20×10^{-6}	1.27×10^{-9}	-2.22×10^{-9}	3.84×10^{-10}	6.95×10^{-4}	1.20×10^{-4}
Au	Annealed 500°C	90	2.23×10^{-6}	9.42×10^{-10}	-1.59×10^{-9}	2.85×10^{-10}	7.15×10^{-4}	1.28×10^{-4}
Au	Annealed 500°C	100	1.81×10^{-6}	8.41×10^{-10}	-1.40×10^{-9}	2.55×10^{-10}	7.72×10^{-4}	1.41×10^{-4}

APPENDIX D

APPENDIX FOR CHAPTER 7

This is the appendix section for Chapter 7, for other CV techniques which can be used to measure the D_{it}.

D.1 Quasi static

There are Quasi static method, this is where CV measurements are taken at a sufficiently low AC frequency so that the interface traps and minority charge carriers (holes in this case) have sufficient time to react to the AC signal. Then this is compared to a ideal CV or experimental CV taken at a high AC frequency so that these interface traps and minority charge carriers do not have enough time to react. This means that the low frequency can be approximated as,

$$\frac{1}{C_{LF}} = \frac{1}{C_{Acc}} + \frac{1}{C_S + C_{it}}, \tag{D.1}$$

and so the interface traps can be expressed as,

$$D_{it} = \frac{1}{denq^2}\left(\frac{C_{Acc}C_{LF}}{C_{Acc}C_{LF}} - C_S\right). \tag{D.2}$$

In 1966 Berglund proposed [523],

$$\phi_s = \int_{VG1}^{VG2}\left(1 - \frac{C_{LF}}{C_{Acc}}\right)dV + \Delta. \tag{D.3}$$

Where Δ is an integration constant at VG1, by choosing of VG1 to be V_{FB} means that Δ is zero. An approach was put forward by R. Castagné, A. Vapaille in 1971 [524] suggest a way to avoid the integral in Equation D.3. This is by assuming that,

$$C_S = \frac{C_{Acc}C_{HF}}{C_{Acc} - C_{HF}}, \tag{D.4}$$

which then applied to Equation D.2 becomes,

$$D_{it} = \frac{C_{Acc}}{q^2}\left(\frac{\frac{C_{LF}}{C_{Acc}}}{1-\frac{C_{LF}}{C_{Acc}}} - \frac{\frac{C_{HF}}{C_{Acc}}}{1-\frac{C_{HF}}{C_{Acc}}}\right). \tag{D.5}$$

D.2 Conductance Method

This section is to show how the D_{it} is calculated using the conductance methods, for determining D_{it}. This was not used in this work but is stated here as it is of interest when discussing further work.

$$C_P = C_S + \frac{C_{it}}{1+(\omega\tau_{it})^2} \tag{D.6}$$

and

$$\frac{G_P}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2} \tag{D.7}$$

Traps are predominately active within a few $\frac{kT}{q}$ of the of the Fermi level. A normalised conductance as,

$$\frac{G_P}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}}\log\left(1+(\omega\tau_{it})^2\right) \tag{D.8}$$

This avoids the need to generate a value for capacitance (C_S) only the conductance (G_P) and this is easier to deal with.

$$\frac{G_P}{\omega} = \frac{q}{2}\int_{-\infty}^{\infty}\frac{D_{it}}{\omega\tau_{it}}1+(\omega\tau_{it})^2P(U_s)dU_s. \tag{D.9}$$

Where $P(U_s)$ is the probability distribution defined by a Gaussian of the form,

$$P(U_s) = \frac{1}{\sqrt[2]{2\pi\sigma^2}}\exp^{-\frac{(U_s-\bar{U_s})^2}{2\sigma^2}}. \tag{D.10}$$

Where σ_2 is the standard deviation and $\bar{U_s}$ is the mean of the normalised surface potential. The D_{it} can be approximated from the peak of Equation D.9 by,

$$D_{it} \approx \frac{2.5}{q}\left(\frac{G_P}{\omega}\right)_{max}. \tag{D.11}$$

In practice it is a measured capacitance C_M not C_P so the equation for $\frac{G_P}{\omega}$ is given by,

$$\frac{G_P}{\omega} = \frac{\omega G_M {C_{Acc}}^2}{G_M+\omega^2(C_{Acc}-C_M)^2} \tag{D.12}$$

ACKNOWLEDGEMENTS

I acknowledge using two AI generative tools to check spelling and improve grammar, presenting the work more suitably and enhancing readability. Helping with the generation of structure, this also inadvertently raised questions about possible interpretations of how the initial versions could be interpreted by the reader, identifying possible misinterpretations and where certain subjects required more explicit explanation. This action was predominantly performed in the experimental sections to limit the chance of incorporating other people's work in the literature review. In the experimental sections, there was little risk as it is my work, and like the ship of Theseus, even if every plank was replaced, it is still the ship of Theseus. On a personal note, as someone with dyslexia, this has been invaluable as anyone who has read my work can likely attest to.The two AIs used were:

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