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RESEARCH ARTICLE

# A Resonant Switched-Capacitor Voltage Equalizer Circuit for Series-Connected Battery Cells

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**ABSTRACT** Conventional switched-capacitor voltage-equalizer circuits have several limitations, including low balancing speed as the number of battery-pack cells increases, capacitor inrush currents, and EMI noise. A voltage-equalizer circuit that uses a resonant structure to improve performance is proposed to address these issues. It includes a small optimal capacitor network, which transfers energy from any-cell-to-any-cell (AC2AC) in a battery pack, ensuring constant balancing speed, regardless of the number of cells or their initial voltage distribution. Additionally, soft-switching conditions are provided to reduce switching losses and EMI noise, which ultimately increase converter efficiency and make it possible to increase the switching frequency. Consequently, the passive-component volumes are effectively reduced and high power density is practically available. The proposed circuit has been mathematically analyzed and simulated using PSpice for six series-connected battery cells. Its prototype circuit has also been implemented to confirm the analyses and simulation results, which provides an efficiency of 94.6%. Finally, it has been compared with previously introduced structures, which clearly shows a significant improvement in balancing speed, for instance, 70% and 56% improvement as compared to the mesh and delta structures, respectively.

**INDEX TERMS** Electric vehicles (EVs), lithium-ion batteries, resonant conversion, switched-capacitor circuit, voltage equalizer.

## I. INTRODUCTION

The world is currently facing unprecedented crises, such as fossil fuel depletion and global warming. As a result, energy conservation has become an essential concern worldwide. To address these crises, electric vehicles (EVs) and renewable energy sources, such as wind and solar power, have been implemented and developed [1].

Lithium-ion batteries offer numerous advantages, including high power density, low discharge rate, lightweight construction, high safety, and no memory effect. However, because each cell has low power and a low open-circuit voltage, lithium-ion batteries must be connected in series or parallel for high-power applications [2]. In series connections, differences in the chemical and electrical properties of the batteries, along with repeated charging and discharging over time, can cause uneven aging and temperature distribution. This results in variability in cell capacity and state of charge (SoC). To address these issues, battery management systems (BMS) protect lithium-ion battery cells from over-voltage and under-voltage. In charging mode, if the voltage of one cell reaches its maximum, the entire charging process stops. Similarly, in discharging mode, if the voltage of one cell reaches its minimum, the discharging process stops. Equalizer circuits can mitigate this mismatch, significantly increasing the overall capacity, efficiency, and lifespan of the batteries [3].

Battery equalizers can be classified into two types: passive or active. Passive circuits use a parallel resistor for each cell to balance the voltage levels. When some cells have higher voltage levels than others, their excess energy is drained through their parallel resistances. The advantages of this circuit include small size, low cost, and ease of construction. However, there are also disadvantages, such as energy loss and slow balancing speed [4]. Additionally, the battery discharge capacity is limited because much

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energy is drawn from high-voltage cells during the balancing process.

Active balancing circuits use non-absorbing energy transfer elements to transfer energy from high-voltage cells to low-voltage cells [5]. There are four types of active voltage equalizers: capacitor-based [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], inductor-based [35], [36], [37], transformer-based [38], [39], [40], and converter-based [41], [43]. However, circuits based on inductors and transformers require bulky magnetic components to transfer energy between cells, making them large, expensive, and heavy. Moreover, these circuits cause high voltage stress on the switches due to the presence of magnetic energy, which can reduce system reliability. In addition, production errors and mismatches in the inductors or transformers used in these equalizers can cause voltage imbalances and poor balancing [6].

Capacitor-based equalizers are a type of active cell balancing circuit known for their small size and ease of control and implementation [7]. However, conventional capacitor-based voltage equalizers can only transfer energy from adjacent cell-to-cell (AC2C). As the number of battery cells in these equalizers increases, the balancing speed decreases. To improve the balancing speed, various structures have been proposed, such as those with an additional layer [3], double-tiered structures [9], and chain structures [10]. Unfortunately, these structures also experience a decrease in balancing speed as the number of battery cells increases. The series-parallel structure has been introduced in [11], [12], and [13] to increase the balancing speed while remaining independent of the number of battery cells. However, this circuit requires a high number of switches, which increases the volume and cost and reduces system efficiency. The star structure [4], [6], [7] has been proposed to solve this problem, reducing the number of switches by half. Additionally, increasing the number of cells in this structure does not affect the balancing speed. However, the presence of two capacitors in the energy transmission path causes high impedance, which reduces the balancing current and efficiency. The equalizers with delta [14] and mesh [15] structures have solved the high path impedance problem. In [22], a balancing circuit with a series-parallel structure uses supercapacitors (SCs) instead of conventional capacitors. This equalizer also uses SCs to provide high instantaneous energy, eliminating the need for additional capacitors. Single-capacitor structures [33] facilitate direct energy transfer between the cells, but their speed is limited because the energy transfer is confined to just two cells.

Another problem with capacitor-based equalizers is the inrush currents drawn by the capacitors when they are connected to the battery. To address this issue, a resonant inductor can be placed in the energy transfer path to limit this current and provide soft-switching conditions as well [1], [5], [7], [16], [17], [18], [19], [20], [21], [34].

Typically, existing equalizers address only one or two challenges, such as high switch count, low speed, or inrush current of capacitors. In this paper, a capacitor-based resonant voltage equalizer is presented that offers several advantages over previous circuits. First, the balancing speed is increased by increasing the energy transfer paths and decreasing the path impedance. Second, by incorporating an inductor and establishing a resonance tank, soft-switching conditions are provided for switches connected in parallel with cells having higher-than-average voltage, substantially reducing switching losses. Third, by reducing switching losses and EMI issues, it is possible to increase the switching frequency, which can effectively reduce the volumes of passive elements in the circuit, including inductors and capacitors, thereby improving power density. Fourth, the modularization of the circuit is straightforward, increasing circuit reliability. In addition, the simultaneous operation of modules increases the balancing speed. Fifth, this circuit allows simultaneous charging and voltage balancing, as well as discharging and voltage balancing. Finally, by reducing switching losses and increasing the balancing speed, the efficiency of the circuit is significantly improved.

The details of the proposed equalizer are introduced in Section II. Then, the simulation and experimental results are presented in Sections III and IV. Finally, a comprehensive comparison of existing equalizer circuits and the conclusions are provided in Sections V and VI, respectively.

## II. PROPOSED VOLTAGE EQUALIZER CIRCUIT

### A. CONFIGURATION OF THE PROPOSED CIRCUIT

Fig. 1 shows the proposed equalizer structure for six battery cells. The capacitive structure of the proposed circuit is similar to the mesh structure found in recent articles. However, with the same number and capacitance of each capacitor, the overall capacitive network capacity is increased. To better illustrate this, converting the two inner delta configurations of the proposed network to star configurations makes the network resemble the mesh structure (with the difference that the centers of the two stars are not connected, which does not significantly affect system performance due to the system's symmetry). As a result, the capacitance of the central capacitors is effectively tripled.

For two and three cells, a single capacitor and a triangular structure with one capacitor per cell are required, respectively. For four, five, and six cells, it is necessary to employ capacitors to facilitate energy transfer between adjacent cells and the cells in-between, as shown in Fig. 2. Therefore, different numbers of cells can be used in each module, and the circuit can be easily modified if necessary. However, using a higher number of cells per module increases the number of capacitors and the impedances of the energy transfer paths, which reduces the current and balancing speed and leads to higher voltage stresses on the capacitors. Therefore, a proper tradeoff must be made to choose the optimum number of cells per module, depending on the available components and the

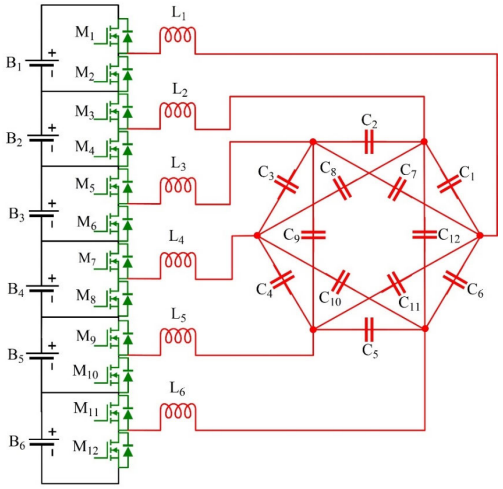


**FIGURE 1.** Proposed resonant SCC voltage equalizer circuit general structure.

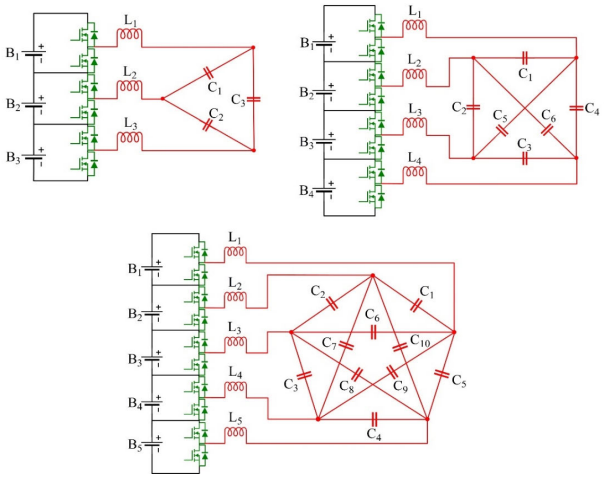


**FIGURE 2.** Proposed voltage equalizer circuit for different cells number per each module.

desired cell balancing speed in practice. In addition, using the modular concept is preferred for a large number of cells.

Similar to the conventional structure [8], each cell is connected to a pair of switches in parallel as a half-bridge. The switching network is connected to the capacitor network through the resonant inductors. In this new structure, the energy transmission path between two adjacent cells consists of a capacitor, which resolves the high path impedance problem found in the star structure [7]. By providing more energy transfer paths with lower impedances, the proposed structure can balance the battery cells much more effectively. Moreover, it minimizes switching losses and EMI noise by utilizing soft switching.

### B. OPERATION PRINCIPLES

The control method of the proposed voltage equalizer circuit closely resembles the conventional equalizer, utilizing two complementary square waveforms for even and odd switches. In Fig. 3, the switching signal waveforms, along with the corresponding voltage and current of the switches, as well as the equivalent inductor current and capacitor voltage, are illustrated. The circuit operational modes, as shown in Fig. 4(a)–(d), and their corresponding equations are outlined here in sequence. It is important to note that since all paths are simultaneously involved in both charging and discharging processes, and due to the symmetrical structure of the resonant network, they can be collectively represented as a single path with equivalent impedance.

*Mode I* ($t_0 \sim t_1$): In this mode, the odd switches are turned on, causing the current to flow from the cell with higher voltage ($B_1$) to the resonant network. During this process, the resonant network gets charged, and the current and voltage values are determined as follow:

$$\begin{cases} \dfrac{dV_{C_{eq}}}{dt} = \dfrac{i_r}{C_{eq}} \\ \dfrac{di_r}{dt} = \dfrac{V_{B_1} - V_{C_{eq}}}{L_{eq}} \end{cases} \tag{1}$$

$$\begin{cases} i_r\,(t) = V_{B_1}\sqrt{\dfrac{C_{eq}}{L_{eq}}}\,sin(\omega_r\,(t-t_0)) \\ V_{C_{eq}}\,(t) = V_{B_1}\,(1 - cos\,(\omega_r\,(t-t_0))) \end{cases} \tag{2}$$

$$\omega_r = \frac{1}{\sqrt{L_{eq}C_{eq}}} \tag{3}$$

Here, $L_{eq}$ and $C_{eq}$ refer to the equivalent inductor and capacitor values within each energy transmission path, respectively.

*Mode II* ($t_1 \sim t_2$): In this mode, the odd switches are turned off, and the current of the resonant network remains positive. This current flows through the body diodes of the middle switches, reducing the voltage across these switches to zero. As a result, soft switching conditions are created for the switch $M_2$.

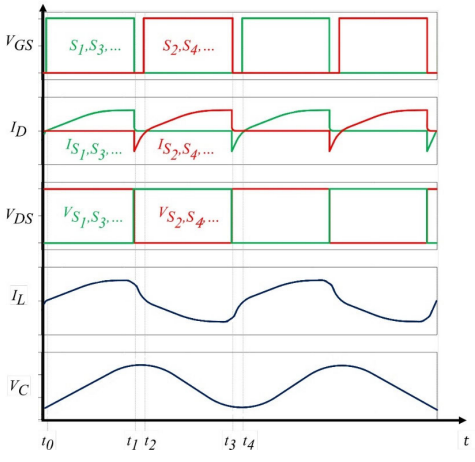


**FIGURE 3.** Ideal PWM currents and voltages typical key waveforms.

*Mode III* ($t_2 \sim t_3$): During this mode, the even switches are activated, allowing the current to flow from the resonance network to the cell with a lower voltage ($B_2$). As a result,

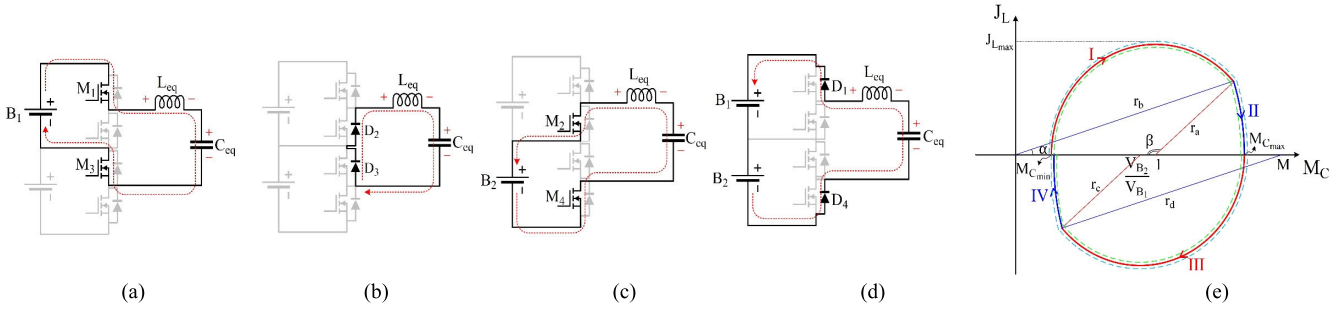


**FIGURE 4.** Different operation modes, (a) mode I, (b) mode II, (c) mode III, (d) mode IV, and (e) normalized state-plane trajectory of the circuit.

the resonant network gets discharged and the corresponding current and voltage values are computed in the following manner:

$$\begin{cases} \dfrac{dV_{C_{eq}}}{dt} = -\dfrac{i_r}{C_{eq}} \\ \dfrac{di_r}{dt} = \dfrac{V_{C_{eq}} - V_{B_2}}{L_{eq}} \end{cases} \tag{4}$$

$$\begin{cases} i_r\,(t) = -V_{B_1}\sqrt{\dfrac{C_{eq}}{L_{eq}}}\,sin(\omega_r\,(t-t_2)) \\ V_{C_{eq}}\,(t) = V_{B_1}\,(1 - cos\,(\omega_r\,(t-t_2))) \end{cases} \tag{5}$$

*Mode IV* ($t_3 \sim t_4$): In this mode, all switches are turned off, and the current within the resonant network remains negative. This negative current flows through the body diodes of both the upper and lower switches, consequently reducing their voltage to zero. Consequently, this results in the creation of soft switching conditions for the switch $M_1$ at zero voltage. The circuit normalized state-plane trajectory is shown in Fig. 4(e).

Figs. 5 and 6 illustrate the energy transfer paths between cells in two main switching states, where $V_{B1}{>}V_{B2}{>}\ldots{>}V_{B6}$. Notably, energy flows from cells with higher voltage to those with lower voltage. The proposed circuit is capable of directly balancing all cells, eliminating the need for additional monitoring circuits or closed-loop controllers. Additionally, voltage balancing occurs simultaneously across all cells, resulting in enhanced balancing speed and efficiency, independent of the number of cells or their initial voltage distribution.

In practice, burst-mode operation can be used to ensure that the maximum voltage difference between cells remains sufficiently small. Thus, by defining minimum and maximum allowable voltage thresholds, unnecessary operation is avoided when the voltage difference falls within acceptable limits. As shown in the algorithm in Fig. 7, the constant switching operation of the circuit can be started or stopped accordingly. Consequently, only a simple voltage monitoring circuit is required rather than a complex closed-loop control system, in practice.

### C. PARAMETER DESIGN

For the analysis of the converter, the following parameters are defined:

$$\begin{cases} Z_{eq} = \sqrt{\dfrac{L_{eq}}{C_{eq}}}, \quad \gamma = \alpha + \beta = \omega_r \dfrac{T_s}{2} \\ M = 1 + \dfrac{V_{B2}}{V_{B_1}}, \quad F = \dfrac{f_s}{f_r} > 1 \end{cases} \tag{6}$$

Based on [44] and Fig. 4 (e), the normalized current is given:

$$\begin{aligned} J &= \frac{1}{2\gamma}\left(M_{C_{max}} - M_{C_{min}}\right) \\ &= \frac{1}{2\gamma}\left(\sqrt{1-(M-1)^2\,sin^2\left(\frac{\gamma}{2}\right)}sec\left(\frac{\gamma}{2}\right) - 1\right) \end{aligned} \tag{7}$$

The maximum values of equivalent capacitor voltage and equivalent inductor current are determined using equation (7), as specified in [44].

$$\begin{cases} M_{C_{max}} = \dfrac{V_{C_{max}}}{V_{B_1}} = \dfrac{1}{2}M + \gamma J \\ J_{L_{max}} = \dfrac{I_{L_{max}}}{\frac{V_{B_{max}}}{Z_{eq}}} = \gamma J + 1 - \dfrac{1}{2}M \end{cases} \tag{8}$$

By obtaining the value of P (power transmitted by the resonant network at any given moment), it becomes possible to determine the resonance impedance, which in turn allows for the calculation of the element values.

$$Z_r = V_{B_2} V_{B_1} \frac{J}{P} \tag{9}$$

$$\begin{cases} C_{eq} = \dfrac{1}{2\pi f_r Z_r} = 56\ nF \\ L_{eq} = \dfrac{Z_r}{2\pi f_r} = 20\ \mu H \end{cases} \tag{10}$$

(9) and (10) clearly show that using higher resonant frequencies reduces the resonant tank component values.

Since the network is symmetrical and all component capacitances are identical, their variations are also considered identical. By selecting a switching frequency slightly higher than the resonance frequency, it is ensured that soft switching

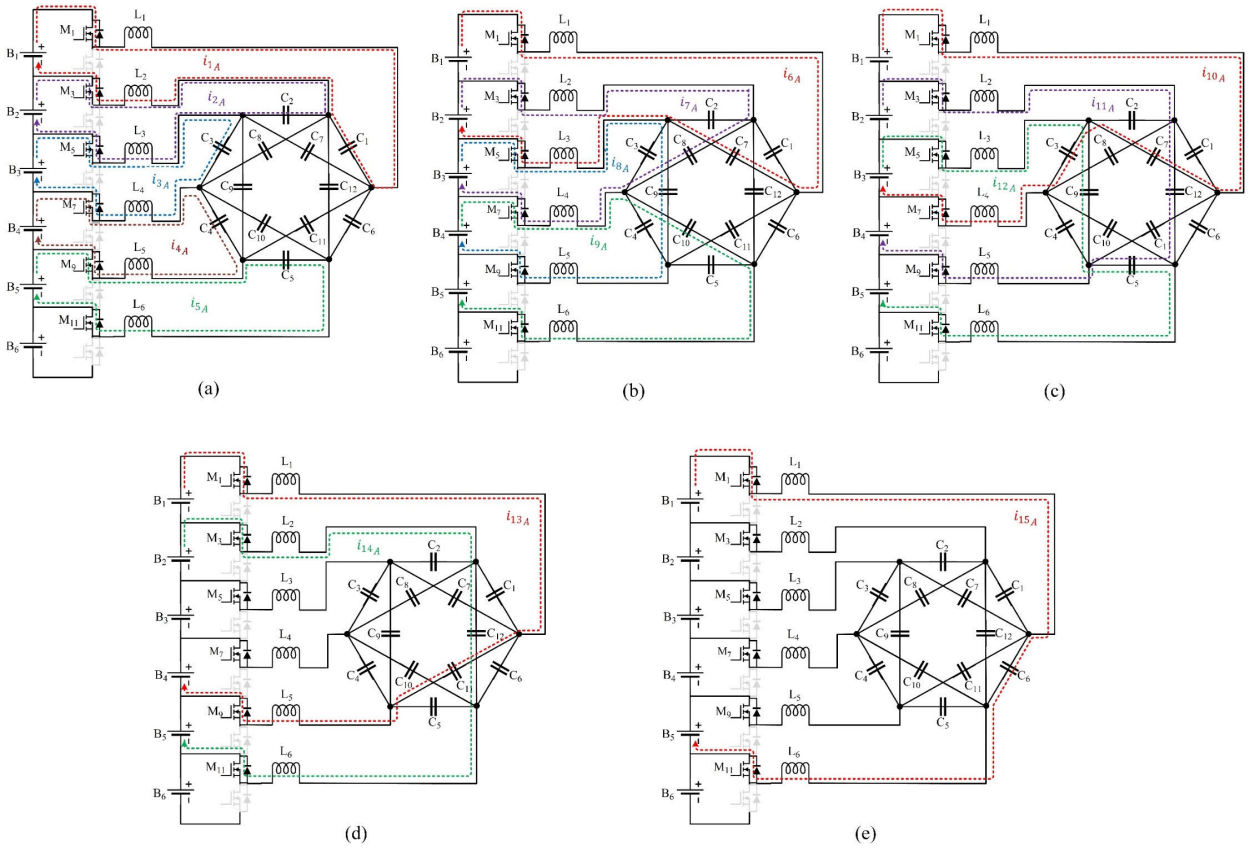


**FIGURE 5.** Energy transfer paths between cells in discharging mode, where $V_{B1} > V_{B2} > \ldots > V_{B6}$.

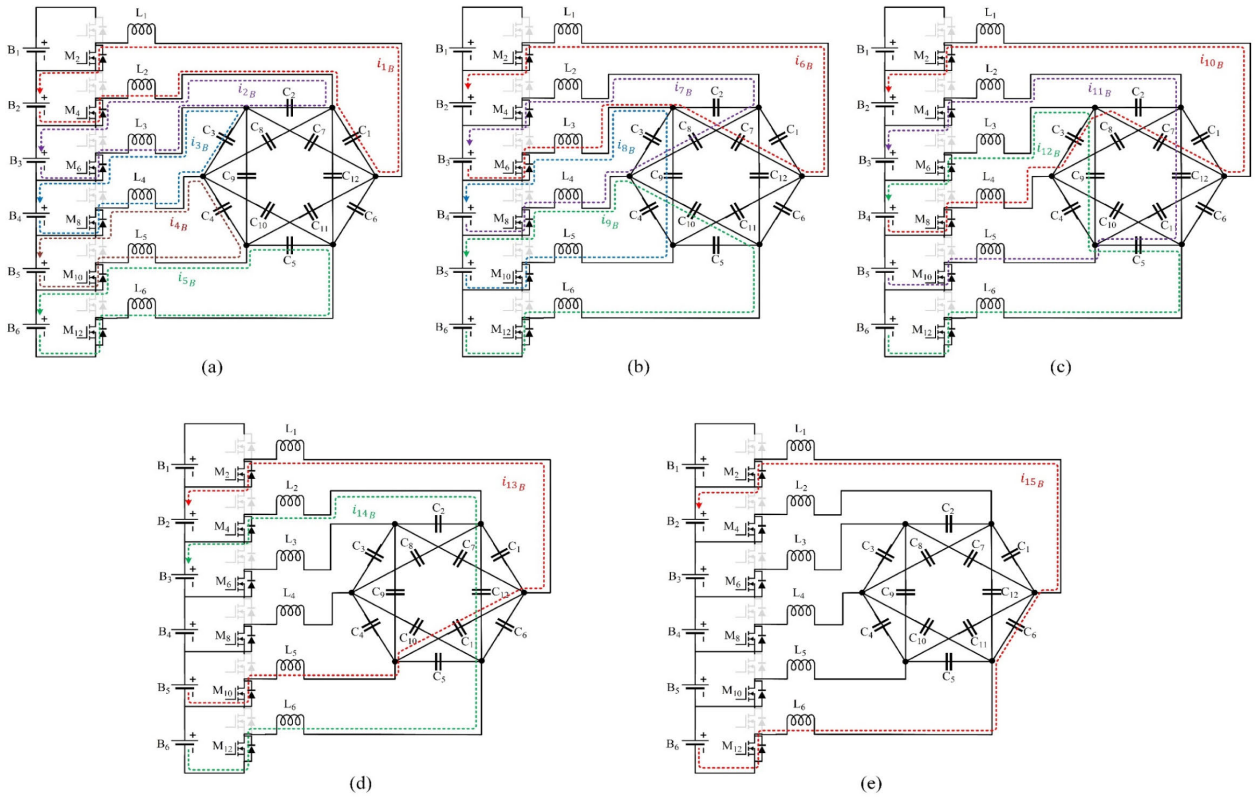


**FIGURE 6.** Energy transfer paths between cells in charging mode, where $V_{B1} > V_{B2} > \ldots > V_{B6}$.

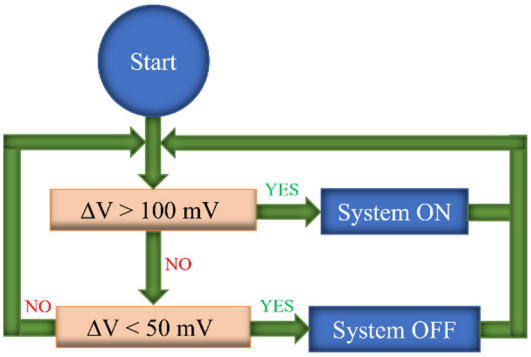


**FIGURE 7.** The burst mode control algorithm of the proposed system.

is maintained over time, even if the component capacitances decrease or vary. This ensures ZVS operation, helps reduce EMI issues, and improves the converter efficiency.

Using the method of superposition and star-to-delta and delta-to-star transformations, the following relationships have been derived with reasonable approximation. These relationships can be used to calculate the value of each inductor and capacitor from their equivalent values:

$$\begin{cases} C = \dfrac{C_{eq}}{1.42} \\ L = \dfrac{L_{eq}}{2} \end{cases} \tag{11}$$

### D. SWITCHING IMPEDANCE ANALYSIS

Given that one of the paper's main claims is to enhance balancing speed and optimize the arrangement of the capacitor network, this section specifically focuses on evaluating the performance of the capacitor network and highlighting the improvements achieved in this regard.

The slow and fast switching impedances [45] of the given circuit are presented and analyzed here. All components are assumed ideal for simplicity, and considering their non-ideal characteristics does not noticeably affect the results. Moreover, the same component values are used for all circuits under comparison. Because the network is symmetrical and shifting the batteries does not affect the circuit analysis, the voltage difference between the adjacent cells is assumed here to be equal, i.e., $V_{B1} = V_{B2} + \Delta V = V_{B3} + 2\Delta V = V_{B4} + 3\Delta V = V_{B5} + 4\Delta V = V_{B6} + 5\Delta V$.

The current required to balance the charge between the cells is directly proportional to the impedance of the capacitor and the voltage difference between the cells. In Figs. 5 and 6, the currents can be expressed by the following equation set.

$$\begin{cases} i_{1_A} = i_{2_A} = i_{3_A} = i_{4_A} = i_{5_A} = 2I_r \\ i_{6_A} = i_{7_A} = i_{8_A} = i_{9_A} = 4I_r \\ i_{10_A} = i_{11_A} = i_{12_A} = 3I_r \\ i_{13_A} = i_{14_A} = 8I_r \\ i_{15_A} = 10I_r \end{cases} \tag{12}$$

where, $I_r$ denotes the reference current flowing through the voltage of a battery cell and the impedance path created by two capacitors. By using (12) and applying Kirchhoff's current law, we can calculate the average currents flowing through the capacitors and cells during the state A.

$$\begin{cases} i_{C_{1_A}} = i_{C_{2_A}} = i_{1_A} = 2I_r, & i_{B_{1_A}} = -i_{1_A} - i_{6_A} - i_{10_A} - i_{13_A} - i_{15_A} = -27I_r \\ i_{C_{3_A}} = i_{3_A} + i_{10_A} = 5I_r, & i_{B_{2_A}} = -i_{2_A} - i_{6_A} - i_{7_A} - i_{10_A} - i_{11_A} - i_{13_A} \\ i_{C_{4_A}} = i_{4_A} = 2I_r, & -i_{14_A} - i_{15_A} = -42I_r \\ i_{C_{5_A}} = i_{5_A} + i_{12_A} = 5I_r, & i_{B_{3_A}} = -i_{3_A} - i_{7_A} - i_{8_A} - i_{10_A} - i_{11_A} - i_{12_A} \\ i_{C_{6_A}} = i_{15_A} = 10I_r, & -i_{13_A} - i_{14_A} - i_{15_A} = -45I_r \\ i_{C_{7_A}} = i_{6_A} + i_{10_A} = 7I_r, & i_{B_{4_A}} = -i_{4_A} - i_{8_A} - i_{9_A} - i_{11_A} - i_{12_A} - i_{13_A} \\ i_{C_{8_A}} = i_{7_A} = 4I_r, & -i_{14_A} - i_{15_A} = -42I_r \\ i_{C_{9_A}} = i_{8_A} = i_{12_A} = 7I_r, & i_{B_{5_A}} = -i_{5_A} - i_{9_A} - i_{12_A} - i_{14_A} - i_{15_A} = -27I_r \\ i_{C_{10_A}} = i_{9_A} = 4I_r, & \\ i_{C_{11_A}} = i_{13_A} = 8I_r, & \\ i_{C_{12_A}} = i_{11_A} + i_{14_A} = 11I_r, & \end{cases} \tag{13}$$

In the same manner, different currents in state B are given as follows:

$$\begin{cases} i_{C_{1_B}} = i_{C_{2_B}} = -2I_r & i_{C_{8_B}} = -4I_r & i_{B_{2_B}} = 27I_r \\ i_{C_{3_B}} = -5I_r & i_{C_{9_B}} = -7I_r & i_{B_{3_B}} = 42I_r \\ i_{C_{4_B}} = -2I_r & i_{C_{10_B}} = -4I_r & qi_{B_{4_B}} = 45I_r \\ i_{C_{5_B}} = -5I_r & i_{C_{11_B}} = -8I_r & i_{B_{5_B}} = 42I_r \\ i_{C_{6_B}} = -10I_r & i_{C_{12_B}} = -11I_r & i_{B_{6_B}} = 27I_r \\ i_{C_{7_B}} = -7I_r & & \end{cases} \tag{14}$$

Here, $i_{C_i}$ represents the average current passing through the capacitors, while $i_{B_i}$ represents the average current passing through the battery cells.

(13) and (14) demonstrate that batteries $B_2 - B_5$ undergo discharge during the state A, followed by charging in the state B. However, $B_2$ and $B_3$ serve as input during a switching period, while $B_4$ and $B_5$ operate as output. Fig. 8 illustrates the use of four virtual capacitors ($C_{13}-C_{16}$), which are connected in parallel with $B_2 - B_5$, respectively. The virtual capacitors charge and discharge during a switching period, allowing for $B_2$ and $B_3$ to be discharged only in the state A, while $B_4$ and $B_5$ are charged solely in the state B. The virtual capacitors, similar to the conventional capacitors $C_1 - C_{12}$, function as energy transfer media with a constant charge during the balancing process.

In summary, $B_1 - B_3$ are discharging during the state A, while $B_4-B_6$ are only charging during the state B, as shown in Fig. 8. As a result, we can utilize the limited impedance analysis method [45] to examine the slow switching limit (SSL) and fast switching limit (FSL) impedances of the proposed equalizer. (13) and (14) can be used to express the total input

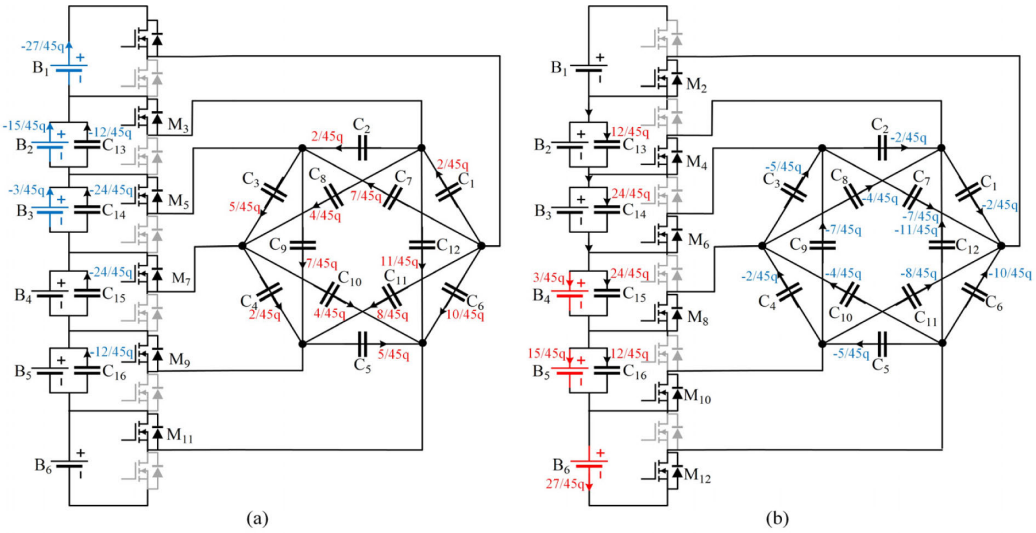


**FIGURE 8.** Charge flows of the proposed voltage equalizer circuit during the different states, (a) state A and (b) state B.

charge ($q_{in}$) during the state A and the total output charge ($q_{out}$) during the state B, respectively.

$$q_{in} = q_{out} = q = 45 I_r T \tag{15}$$

where, $T$ is the switching period, according to the charge conservation law, the total input charge $q_{in}$ during a switching period is equal to the total output charge $q_{out}$.

Based on (13) and (15), the charges through the capacitors during the states A and B, shown in Fig. 8, are deduced as follows:

$$a^A = [a^A_{out}\ a^A_{C_1}\ a^A_{C_2}\ \dots\ a^A_{C_{15}}\ a^A_{C_{16}}\ a^A_{in}\ ]^T = \frac{1}{45}$$
$$[0\ 2\ 2\ 5\ 2\ 5\ 10\ 7\ 4\ 7\ 4\ 8\ 11\ -27\ -42\ -42\ -27\ -45]^T \tag{16}$$

$$a^B = [a^B_{out}\ a^B_{C1}\ a^B_{C2}\ \dots a^B_{C15}\ a^B_{C16}\ a^B_{in}]^T = \frac{1}{45}$$
$$[45\ -2\ -2\ -5\ -2\ -5\ -10\ -7\ -4\ -7\ -4\ -8$$
$$-11\ 27\ 42\ 42\ 27\ 0]^T \tag{17}$$

The variables $a^A_{C_i}$ and $a^B_{C_i}$ represent ratios of the charges transferred in each capacitor during the states A and B, respectively, to the total output charge over a switching period. Similarly, $a^A_{in}$ and $a^B_{in}$ represent the ratios of input charges in these two modes to the total input charge during a period, respectively. Additionally, $a^A_{out}$ and $a^B_{out}$ indicate the ratios of the output loads in these two states to the total output charge in a switching period. It should be noted that when the charge flows into an element, the ratio is positive, while it is negative when charge flows out of the element. Using (16) and (17), the following relation is obtained:

$$V_{out}\left(a^A_{out} + a^B_{out}\right) + \sum_{capacitors}\left(a^A_{c_i} v^A_{c_i} + a^B_{c_i} v^B_{c_i}\right) = 0 \tag{18}$$

The equation consists of the first term, which is associated with the constant output voltage source, and the subsequent terms, which are associated with the capacitor branches. It must be mentioned that in each capacitor branch, $a^A_{out} + a^B_{out} = 1$ and $a^A_{c_i} = -a^B_{c_i}$ (as a result of the charge remaining in periodic steady state).

By defining $a_{c_i} = a^A_{c_i} = -a^B_{c_i}$ and $q_i = q_{c_i} q_{out}$ and multiplying (18) by $q_{out}$, the net charge delivered to the output in one period is obtained.

$$q_{out} v_{out} + \sum_{capacitors} q_i \Delta v_i = 0 \tag{19}$$

where, $\Delta v_i = v^A_{c_i} - v^B_{c_i}$. The first term is determined by multiplying the constant output voltage by the total load current of the independent voltage source. Each subsequent term in the sum corresponds to the energy loss, associated with a specific capacitor. It must be mentioned that in this analysis, it is not necessary to explicitly calculate the voltage of each capacitor. Alternatively, $\Delta v_i$ can be derived as follows:

$$\Delta v_i = \frac{q_i}{C_i} \tag{20}$$

where, $C_i$ represents the capacity of the $i^{th}$ capacitor. After integrating the equations (19) and (20) and dividing the result by $q^2_{out}$, we can write:

$$\frac{v_{out}}{q_{out}} + \sum_{capacitors}\left(\frac{q_i}{q_{out}}\right)^2 \frac{1}{C_i} = 0 \tag{21}$$

At low switching frequencies, the small resistances associated with the switching and connections can be disregarded. The capacitive part of the impedance, seen by the switching network, is then primarily determined by the charging and discharging of the capacitor. As a result, it is possible to deduce the SSL capacitive part as given in [45]:

$$X_{SSL} = \sum_i \frac{a^2_{c_i}}{C_i \times f_{sw}} = \frac{5.4}{C_{eq} \times f_{sw}} \tag{22}$$

where, $C_{eq}$ is the equivalent capacitor and $f_{sw}$ is the switching frequency.

According to (22), in order to decrease SSL impedance, it is needed to either increase capacitor or switching frequency. In contrast, the FSL impedance is mainly affected by some parameters such as the on-resistances of the MOSFETs, parasitic inductances, and switching losses. At higher switching frequencies, the decrease in capacitor impedance becomes significant, causing other components to play a more prominent role in determining FSL impedance.

At high switching frequencies, the voltages across the capacitors are commonly considered constant in models. In this scenario, the FSL impedance is determined by the constant current flowing between the capacitors, which is typically influencing by the equivalent resistance of the switch and the interconnections, and remains relatively stable.

As shown in Fig. 8, the load current in the switches can be expressed as follows:

$$a_r = \left[a_{ri}^A\right] = \frac{1}{45} [27\ 27\ 15\ 15\ 3\ 3\ -3\ -3\ -12\ -12\ -30\ -30]^{\mathrm{T}} \tag{23}$$

where, $a_{ri}$ represents the charging current through the switch during a single phase when the switch is on, the total loss of the proposed equalizer in FSL is the sum of the switch losses [45], as given by (24).

$$R_{FSL} = \sum_i \frac{R_i \left(a_{r_i}\right)^2}{D_i} \tag{24}$$

Here, $R_i$ and $D_i$ are the resistance and duty cycle values of the $i^{th}$ switch, respectively.

Assuming a duty cycle of 50% in the proposed voltage equalizer circuit, FSL impedance is obtained as follows:

$$R_{FSL} = 2\sum_i R_i \left(a_{r_i}\right)^2 = 3.98R_{eq} \tag{25}$$

where, $R_{eq}$ is the equivalent resistance of each switch. The FSL impedance mainly represents the resistive conduction loss independent of the switching frequency.

In conclusion, based on the calculated impedance values, it is evident that these values have decreased, leading to an increase in the balancing current compared to previous articles. This heightened balancing current is expected to enhance the equalizer's balancing speed.

### E. THE CIRCUIT TOTAL STORED ENERGY AND ITS EFFICIENCY

The total energy stored in the elements of the proposed equalizer is calculated using the following equations and compared with those of previous structures, as illustrated in Fig. 9.

$$\begin{cases} V_{C_1,\ldots,C_5} = V_B V_{C_7,\ldots,C_{10}} = 2V_B \\ V_{C_6} = 5V_B V_{C_{11},C_{12}} = 4V_B \end{cases} \tag{26}$$

$$W_C = \frac{1}{2}CV^2 \overset{for\ all\ capacitors}{\Longrightarrow}$$

$$W_C = \frac{1}{2}C\sum V_k^2 = \frac{1}{2}C\left[5V_B^2 + 25V_B^2 + 16V_B^2 + 32V_B^2\right] = 39CV_B^2 \tag{27}$$

$$W_L = \frac{1}{2}LI^2 \overset{for\ all\ inductors}{\Longrightarrow} W_L = \frac{1}{2}L\sum I_k^2 = \frac{1}{2}L\left[6I^2\right] = 3LI^2 \tag{28}$$

Additionally, the efficiency of this voltage equalizer circuit is determined using (29) and is calculated at various frequencies, as shown in Fig. 10 for two types of diodes. To compute efficiency at different frequencies through simulation, a load is connected to the battery pack, and the battery is charged concurrently using a voltage source. It is essential to carefully choose both the voltage source and load to maintain the average cell voltage. Efficiency is then calculated by dividing the power transferred to the load by the power received from the source during the balancing time. It is noteworthy that the efficiency of the converter remains unaffected by alterations in the initial voltage distribution of the batteries, owing to the symmetrical structure of the resonant network. Therefore, changing the order of the initial voltage distribution does not significantly affect the converter efficiency in practice. In battery equalizer circuits, balancing time is considered one of the key factors. Lower efficiency at lower switching frequencies results from the reduction in energy transfer speed, which leads to a slower balancing process.

$$Efficiency = \frac{P_{out}}{P_{out} + P_{loss}} \times 100 \tag{29}$$

### F. MODULARIZATION

Fig. 11 illustrates the implementation of the proposed equalizer as a module. Each module consists of six cells connected in series and linked by a capacitor, forming a star structure [7]. To improve the balancing speed further, the proposed capacitor structure can be employed to balance the modules. For a given number of cells, they should be arranged into groups of six and balanced by connecting them to the proposed equalizer module. If the total number of battery cells is not a multiple of six, the extra cells should be integrated into the system as described in Section A. This design enables simultaneous balancing between the cells and modules, which enhances the balancing speed. Additionally, modularizing the circuit improves reliability and reduces the overall system cost in practice.

## III. SIMULATION RESULTS

The proposed voltage equalizer circuit has been simulated using PSpice software for six series-connected cells, using 47 nF capacitors and 10 $\mu$H inductors in the resonant network. The values of the equivalent inductor and capacitor were determined using the impedance measurement block in MATLAB software. The resonance frequency of the resonant tank is established at 150 kHz. The switching frequency is set slightly above the resonance frequency, specifically at 160 kHz.

For fixed switching frequency operation, reducing the values of the inductor and capacitor decreases the energy density and slows down the balancing speed. Conversely, increasing

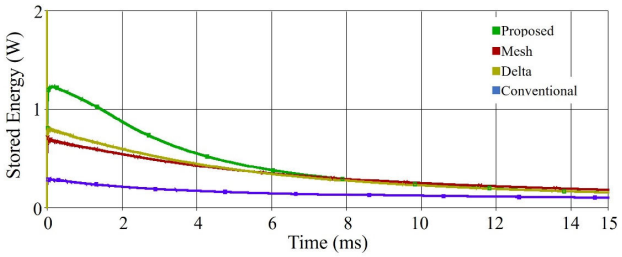


**FIGURE 9.** Comparing the stored energy in the energy transfer networks of the proposed voltage equalizer circuit and some other well-known structures.

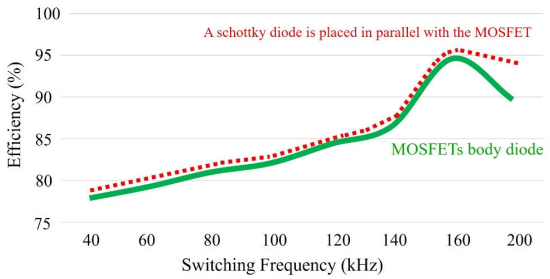


**FIGURE 10.** Efficiency of the proposed voltage equalizer circuit versus switching frequency.

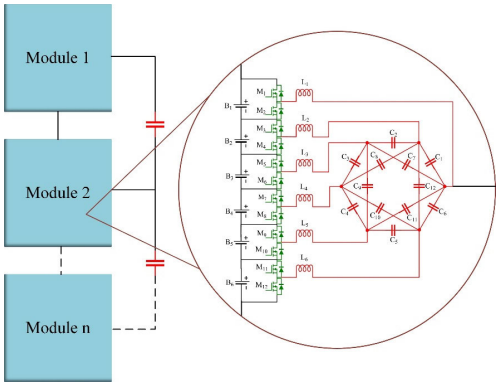


**FIGURE 11.** Modularized structure of the proposed voltage equalizer circuit.

these values speeds up the balancing process. It is important to note that the resistances of the switches only affect their losses and efficiency. Furthermore, altering the values of inductors and capacitors can lead to a shift in resonant frequency, which may impact the performance of soft switching. However, this issue can be effectively mitigated by setting the switching frequency sufficiently higher than the resonant frequency. Moreover, given the symmetrical nature of the resonant network and the negligible variation in battery voltages, setting the switching frequency more than 10 kHz above the resonant frequency ensures that component tolerances do not affect zero-voltage switching (ZVS). Consequently, the existing tolerances of the passive components do not significantly affect the voltage equalizer circuit performance in practice. Selecting a switching frequency higher than the resonance frequency guarantees soft-switching conditions, specifically zero-voltage switching (ZVS). Fig. 12 depicts the current, drain-source voltage, and gate-source voltage waveforms of the switch "M1," which is connected in parallel with battery "B1" (with the highest voltage). Before applying the gate-source voltage to the switch, its body diode conducts the current due to the resonant inductor and the gradual current flow, causing the drain-source voltage to drop to zero. This results in a notable reduction in switching losses during the turn-on sequence, as shown in Fig. 13(a), which depicts the product of the drain-source voltage and the switch current for a given switch.

While a subset of switches may undergo hard switching in this circuit, at elevated frequencies, the soft-switching operation of the remaining switches substantially mitigates losses. As shown in Fig. 13(b), comparing the total losses of the switches in the proposed circuit with those of previous circuits reveals that the proposed circuit exhibits lower losses and higher efficiency.

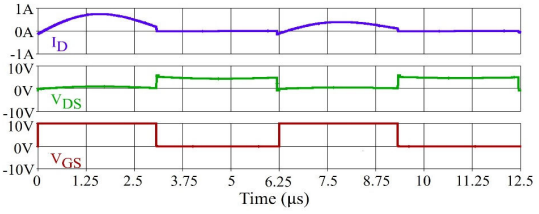


**FIGURE 12.** Simulation waveforms of $I_D$, $V_{DS}$, and $V_{GS}$ of switch $M_1$.

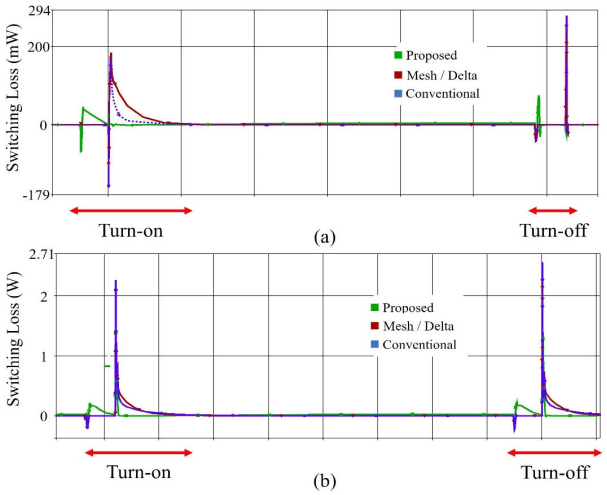


**FIGURE 13.** Simulation waveforms of the losses of the switches for different voltage equalizer circuits, (a) instantaneous losses of switch $M_1$, and (b) total losses of all switches.

According to the categories given in [14] and [15], the AC2AC, or any-cell-to-any-cell method, is easily controllable. The proposed structure can simultaneously transfer energy from any cell to any other cell. This means that the balancing speed remains consistent regardless of battery placement or initial voltage distribution. Fig. 14 shows the performance of the proposed circuit in balancing cells with

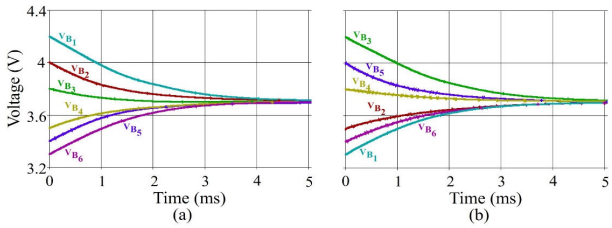


**FIGURE 14.** Voltage balancing of the six series-connected different cells, (a) and (b) different distributions of the initial voltages of the cells.

**TABLE 1.** Different cells voltages values.

| Distribution | $B_1$ | $B_2$ | $B_3$ | $B_4$ | $B_5$ | $B_6$ |
|---|---|---|---|---|---|---|
| (a) | 4.2 V | 4.0 V | 3.8 V | 3.5 V | 3.4 V | 3.3 V |
| (b) | 3.3 V | 3.5 V | 4.2 V | 3.8 V | 4.0 V | 3.4 V |

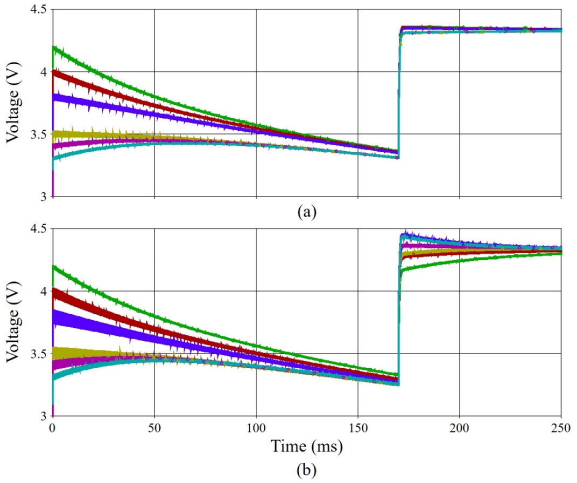


**FIGURE 15.** Operation of the voltage equalizer circuit in charging, discharging and no-load operation modes, (a) when all cells are healthy, and (b) when some cells are defective.

different voltage distributions given in Table 1, which confirms its effectiveness.

Furthermore, Fig. 15 demonstrates the proposed voltage equalizer circuit's ability to balance battery cells during charging and discharging processes in two scenarios: a) when all cells are healthy, and b) when some cells are defective (a cell with reduced capacity and increased internal resistance [46]). Fig. 16 illustrates the performance of the circuit in simultaneous charge and discharge operation modes with step changes in these modes.

Fig. 17 illustrates the voltage balancing of six series-connected cells using the proposed circuit, as well as the mesh and delta structures, under the same switching frequency, element values, and initial battery voltages for all three simulated systems. As shown in Fig. 17, the proposed voltage equalizer circuit outperforms the other two structures in terms of balancing speed. To accelerate the simulation process, 100 $\mu$F capacitors were used instead of real battery cells. In the battery model, the capacitors were included instead of

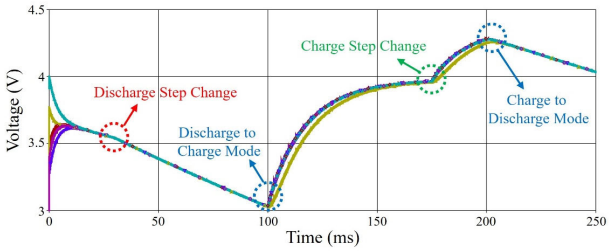


**FIGURE 16.** Simultaneous operation of the voltage equalizer circuit in charging and discharging operation modes including step changes in these modes.

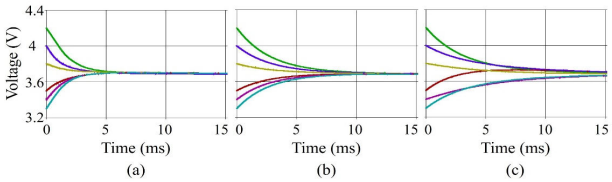


**FIGURE 17.** Voltage balancing of the six series-connected different cells by using the different circuits, (a) proposed, (b) delta, and (c) mesh.

an ideal voltage source, and the series and parallel resistances of the cells were also incorporated to closely resemble real battery behavior. As observed, the balancing speed of the proposed structure is higher than that of the previous structures. Under completely identical conditions, and based on the simulation times at which the cell voltage differences reach an acceptable level, the proposed converter achieves approximately 70% faster balancing compared to the mesh structure and about 56% faster balancing compared to the delta structure.

## IV. EXPERIMENTAL RESULTS

Fig. 18 shows a photograph of the prototype of the proposed voltage equalizer circuit, designed for six 2200 mAh lithium-ion battery cells. The equalizer circuit operates as follows: it turns on when the maximum voltage difference among the cells reaches 100 millivolts and remains active until the voltage difference decreases to 50 millivolts, at which point it turns off. In a no-load mode, where no current is drawn from the batteries, the voltage difference is maintained at approximately 50 millivolts for an extended period. However, if a defective cell is present within the battery pack, this voltage difference may increase over time. In response to the rising voltage difference caused by defective cells, the equalizer circuit is automatically activated to reduce the voltage difference, ensuring the overall health and performance of the battery pack.

The switching network is implemented using DMG2302UK MOSFETs. The STM32F103C8T6 micro-controller generates complementary square waveforms, which are amplified by a dual-channel gate driver and applied to the switches through two single-to-six pulse transformers with a 1:1 turns ratio (Figs. 18–19). One waveform drives the odd switches, and the other drives the even switches. Because the circuit has many switches with no common ground and no shared control

signals, the pulse transformers provide effective isolation. The magnetizing inductance of each transformer is designed based on the switching frequency and the gate driver's current rating.

There are various methods to control the switches. One approach involves driving the switches using a source with positive and negative outputs to power the gate driver. With this method, it is feasible to utilize only one pulse transformer, particularly an isolated single-input-twelve-output transformer, by generating symmetrical positive and negative signals. Another method for driving switches from different sources is to employ isolated ICs and optical couplers, similar to a bootstrap circuit. Overall, this highlights an open research area concerning the design of integrated drive circuits for this converter, particularly in the context of industrialization. Therefore, developing an optimal drive circuit for future applications represents a promising avenue for further investigation.

A dead time is incorporated between these two square waveforms to prevent simultaneous activation of the switches, ensuring soft-switching conditions. The main specifications of all components used in this setup are detailed in Table 2.

**TABLE 2. Specifications of experimental prototype.**

| Parameter | Type | Value | Unit |
|---|---|---|---|
| MOSFET (on-resistance) | DMG2302UK | 90 | $m\Omega$ |
| Capacitor | SMD 0805 package | 47 | $nF$ |
| Inductor | SMD 7×7 package | 10 | $\mu H$ |
| Battery Cell | 2200 mAh Li-ion | 3.7 | $V$ |
| Gate Driver | TC4427 | - | - |
| Switching Frequency | - | 160 | $kHz$ |

Fig. 20 depicts the current, voltage, and instantaneous loss waveforms corresponding to the switch "M1" during both low and high voltage differences of the battery cells (refer to Table 3 ). As shown, when the body diode is on, the switch is turned on, and soft switching is successfully realized at zero voltage in both operation modes. Note that, according to Ohm's Law, in the presence of a large voltage difference, the switch current, representing the balancing current, is higher.

Furthermore, Fig. 21 illustrates the capacitor "C1" voltage and inductor "L1" current and voltage waveforms. The capacitor current is proportional to the inductor current, and the figure shows that the inrush current of the capacitor has been effectively eliminated, resulting in reduced noise and switching losses.

The voltage values of the battery cells were measured during the balancing process using the proposed circuit. With the aging of some cells, the circuit performance remains largely unaffected, with only a slight reduction in balancing speed, since aged battery cells have higher internal resistance, which limits the balancing current. These measurements were conducted under three different conditions: no-load, charging, and discharging operation modes. Additionally, step changes were applied in these modes, as illustrated in Fig. 22.

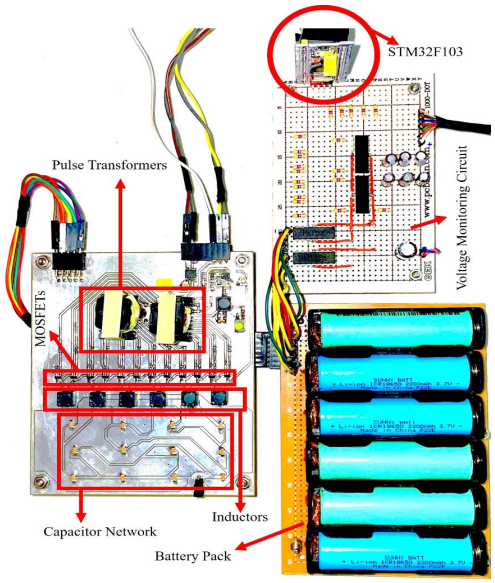


**FIGURE 18. Proposed voltage equalizer circuit prototype photograph.**


**FIGURE 19. Gate drives control signals of the switches.**

In the experimental results, the modular behavior of the system has not been examined; however, based on the star connection of the modules—which is a well-established structure—and the simulation results, this behavior is verifiable and can be implemented. Furthermore, the system's EMI has been significantly reduced due to the limitation of inrush currents.

**TABLE 3. Different cells voltages values under large and small unbalancing conditions.**

| | $B_1$ | $B_2$ | $B_3$ | $B_4$ | $B_5$ | $B_6$ |
|---|---|---|---|---|---|---|
| Large Unbalancing Condition | 3.68 V | 3.38 V | 3.55 V | 3.48 V | 3.46 V | 3.57 V |
| Small Unbalancing Condition | 3.46 V | 3.45 V | 3.5 V | 3.44 V | 3.45 V | 3.48 V |

## V. COMPARISON OF THE DIFFERENT VOLTAGE EQUALIZER CIRCUITS

Table 4 compares the proposed equalizer circuit with some previous ones in terms of element count, energy transfer method, balancing speed, voltage stress, size, control level, efficiency (based on simulations) and EMI. Additionally, the circuits are compared based on the balancing time required

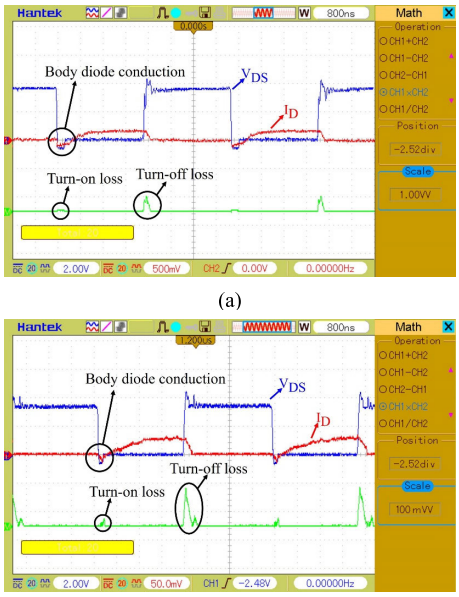


**FIGURE 20.** Experimental waveforms of the voltage, current and instantaneous power losses of a switch under the different (a) large unbalancing and (b) small unbalancing conditions.

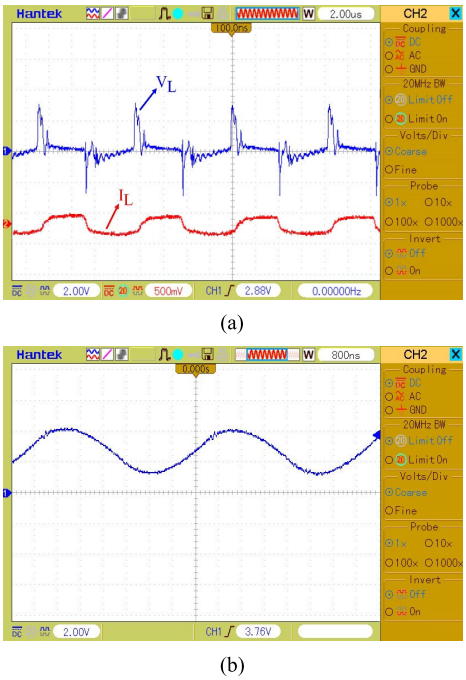


**FIGURE 21.** Experimental different waveforms, (a) inductor ($L_1$) voltage and current, and (b) capacitor ($C_1$) voltage.

to achieve a voltage difference of 60 mV, efficiency, peak switching loss, and peak power received by the capacitors, as shown in Fig. 23.

The yellow and blue columns in Fig. 23 represent the power capacity of the capacitor network and the peak losses of the switches, respectively. Consequently, in the proposed structure, both the energy storage capacity of the capacitors is increased and the peak losses of the switches are reduced,

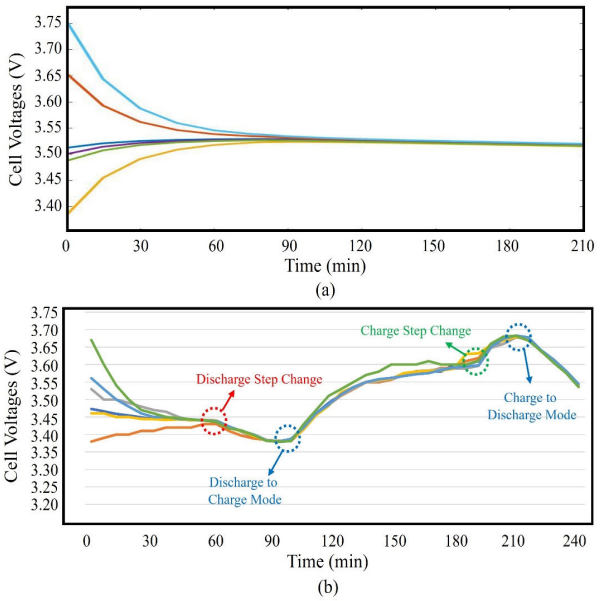


**FIGURE 22.** Experimental different voltages waveforms of the different battery cells during the balancing process by using the proposed circuit under the different conditions, (a) no load, and (b) charging and discharging operation modes including step changes during these operation modes.

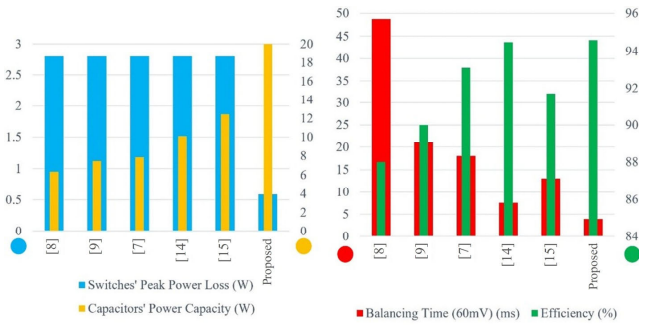


**FIGURE 23.** Comparison of switched-capacitor voltage equalizer circuits.

which are both beneficial. These comparisons clearly demonstrate that the proposed voltage equalizer circuit outperforms previously established circuits, offering lower switching losses, higher power density, higher balancing speed, and improved efficiency.

Considering Table 4, although the proposed structure is similar to the delta structure [14] for a small number of cells, these two structures diverge as the number of cells increases (six or more), and the proposed scheme requires fewer capacitors. This reduces both the volume and cost of the system in practice.

In addition, inductors are included in the proposed structure to provide soft-switching conditions for some power switches in the circuit, which reduces switching losses and EMI noise, while increasing system efficiency and performance. Consequently, the proposed circuit is suitable for high switching frequency operation, which can reduce the volume of passive components in the converter and achieve high power density in practice.

**TABLE 4. Comparison of some SC voltage equalizer circuits.**

| Structure | Switch No | Capacitor No | Inductor No | Balancing Method | Speed | CVS | SVS | Size | Control Level | Efficiency (%) | EMI |
|---|---|---|---|---|---|---|---|---|---|---|---|
| [6] | 2N | N | N | AC2AC | Normal | $(N-1)V_b/2$ | $V_b$ | Normal | Easy | 93.6 | Low |
| [7] | 2N | N | 0 | AC2AC | Normal | $(N-1)V_b/2$ | $V_b$ | Low | Easy | 93.1 | High |
| [8] | 2N | N-1 | 0 | AC2C | Very Low | $V_b$ | $V_b$ | Low | Easy | - | High |
| [9] | 2N | N | 0 | AC2C | Low | $(N-1)V_b$ | $V_b$ | Low | Easy | - | High |
| [10] | 2N+4 | N | 0 | AC2C | Low | $V_b$ | $(N-1)V_b$ | Normal | Easy | - | High |
| [11] | 4N | N | 0 | AC2AC | Very Fast | $V_b$ | $(N-1)V_b/2$ | High | Easy | - | High |
| [14] | 2N | N(N-1)/2 | 0 | AC2AC | Fast | $(N-1)V_b$ | $V_b$ | Normal | Easy | 94.5 | High |
| [15] | 2N | 2N | 0 | AC2AC | Fast | $(N-1)V_b$ | $V_b$ | Normal | Easy | 91.7 | High |
| [33] | 2N | 1 | 0 | DC2C | Low | $V_b$ | $(N-1)V_b/2$ | Very Low | Hard | - | High |
| [34] | 4N | N | N | AC2AC | Very Fast | $V_b$ | $(N-1)V_b/2$ | Very High | Easy | 95.2 | Low |
| Proposed | 2N | 2N | N | AC2AC | Very Fast | $(N-1)V_b$ | $V_b$ | Normal | Easy | 94.6 | Low |

It should be noted that, unlike conventional SC equalizer circuits, there are no high spikes or inrush currents in the resonant structures during the transient turn-on moments of their power switches in each switching period. This feature allows higher power transfer to improve balancing speed, reduces switching losses and EMI noise, and improves efficiency compared to conventional SC circuits.

In addition, the improved balancing speed—mainly due to the lower impedance of the paths and higher power transfer capability of the resonant structure—directly affects system efficiency.

Finally, the main advantages of the proposed voltage equalizer circuit are the reduced number of capacitors, improved system efficiency and balancing speed, and enhanced power density.

## VI. CONCLUSION

Switched-capacitor voltage equalizer circuits have some important issues such as low balancing speed, switching loss, and inrush current. Here, an optimized voltage equalizer circuit is introduced and analyzed, which increases the balancing speed, provides soft-switching conditions, and prevents inrush currents in the capacitors and switches to reduce switching losses and EMI.

Its general configuration, operating principles, parameter design, total energy and efficiency, impedance analysis, modular design, as well as simulation and experimental results under different operation modes are presented in detail, demonstrating the following advantages:

- Soft-switching conditions are provided, which ultimately reduce switching losses and EMI issues and improve efficiency, making high switching frequency operation possible to enhance the circuit power density.
- The modularity feature increases the balancing speed through the simultaneous operation of different modules and enhances system reliability.
- Its optimized structure and reduced energy transfer path impedances result in higher balancing current and faster balancing speed.
- The voltage balancing process is effectively performed during charging, discharging, no-load, and transient conditions.
- The simulation results show that the voltage balancing time is reduced by 70% and 56% compared to the mesh and delta structures, respectively.
- Although the proposed structure can be used with any number of cells by inserting capacitors into the energy transfer paths between both adjacent and one-in-between cells, the 6-cell module demonstrates better performance. Using the module concept is preferred for a larger number of cells. If the total number of cells is not a multiple of six, the extra cells can be connected using the method mentioned earlier.

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