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Development of ZnO Buffer Layers for As-Doped CdSeTe/CdTe Solar Cells with Efficiency Exceeding 20%

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The front buffer layer plays an important role in CdSeTe/CdTe solar cells and helps achieve high conversion efficiencies. Incorporating ZnO buffer layers in the CdSeTe/CdTe device structure has led to highly efficient and stable solar cells. In this study, the optimization of ZnO buffer layers for CdSeTe/CdTe solar cells is reported. The ZnO films are radio frequency sputter-deposited on SnO_2:F coated soda-lime glass substrates. The substrate temperature for the ZnO deposition is varied from 22 to 500 °C. An efficiency of 20.74% is achieved using ZnO deposited at 100 °C. The ZnO thickness is varied between 40 nm and 75 nm. Following the ZnO depositions, devices were fabricated using First Solar's CdSeTe/CdTe absorber, $CdCl_2$ treatment, and back contact. The optimal ZnO deposition temperature and thickness is 100 °C and 65 nm, respectively. The STEM-EDX analysis shows that within the detection limits, chlorine is not detected at the front interface of the devices using ZnO deposited at 22 °C and 100 °C. However, depositing ZnO at 500 °C results in chlorine segregation appearing at the ZnO/CdSeTe boundary. This suggests that chlorine is not needed to passivate the ZnO/CdSeTe interface during the lower temperature depositions. The nanocrystalline ZnO deposited at lower temperatures results in a high-quality interface.

1. Introduction

Thin film CdTe based solar cells are the most successful second-generation photovoltaic technology, with the worldwide installed capacity currently exceeding 30 GW peak.[1] Among the various photovoltaic technologies, CdTe-based modules exhibit a lower embedded carbon footprint than thin film $Cu(In,Ga)Se_2$ (CIGSe), monocrystalline and polycrystalline silicon modules.[2,3,4,5] Cadmium telluride is a direct bandgap material which only requires a few microns to fully absorb light due to the absorption coefficient being greater than 10^4 cm^{-1}.[6] The fabrication of thin film CdTe modules is a highly efficient process taking less than 3 h to complete. The fabrication of CdTe solar cells can be achieved through various cost-effective methods, including electro-deposition, close space sublimation and vapor transport deposition.[7] Improving the efficiency of CdTe solar cells will further reduce the cost of electricity and help meet the global net zero carbon emission target by 2050.[8]

1.1. CdS Buffer Layers in CdTe Devices

The efficiency of CdTe solar cells has steadily improved over the years. The front buffer layer plays a critical role in enhancing

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the performance of CdTe solar cells. Cadmium sulfide was commonly used as the n-type buffer layer in CdTe solar cells. Chemical bath deposition (CBD) was used to deposit CdS buffer layers, leading to an efficiency of 16.5%.[9] However, CdS has a narrow bandgap of 2.4 eV and forms a slight cliff-like band alignment to CdTe.[1] The small bandgap causes parasitic absorption losses, leading to a reduction in short-circuit current density (J_{sc}). To reduce these losses, researchers replaced CdS with radio frequency (RF) sputtered oxygenated CdS (CdS:O), resulting in 16.7% efficiency.[1,10] This is because the sputtered CdS:O has a wider bandgap of 2.5–3.1 eV and the higher oxygen content can suppress the interdiffusion of Te which forms CdS_xTe_{1-x} (lower bandgap) during device fabrication.[11] Although the oxygenated CdS led to an increase in photocurrent, it still caused some parasitic absorption losses. Furthermore, CdS:O does not maintain its nanocrystalline structure throughout the CdTe device fabrication.[12] This resulted in difficulties with experimental repeatability and stability, which has significantly limited the widespread use of CdS:O.

1.2. Graded CdSeTe/CdTe Absorber

Incorporating a p-type CdSeTe layer at the front interface followed by a CdTe layer has led to further increases in photocurrent. Selenium incorporation is achieved by depositing either CdSe or CdSeTe and then performing a $CdCl_2$ heat treatment to diffuse Se into the CdTe, creating a graded absorber. The Se lowers the bandgap at the front interface to ~1.4 eV, leading to the wavelength range of the CdSeTe/CdTe solar cell increasing from 850 to 900 nm. Furthermore, Se has been observed to passivate defects in CdTe grain interiors and grain boundaries.[13,14]

1.3. Replacing the CdS Buffer Layer

Replacing CdS and CdS:O with wide bandgap materials such as MgZnO (MZO) and SnO_2 has led to efficiency improvements due to the reduced optical losses.[1,15,16] Alloying with Mg increases the bandgap of ZnO by tuning the conduction band minimum,[17] allowing the adjustment of the conduction band offset (CBO) between MZO and CdTe.[18] The use of MZO buffer layers in Cu-doped CdTe solar cells has led to efficiencies exceeding 18%.[15] Alloying CdTe with Se has led to a J_{sc} increase from 26 to over 28 mA cm^{-2} for an MZO-based device.[19] Furthermore, an efficiency of 20.14% was achieved for an anti-reflection coated Cu-doped MZO/CdSeTe/CdTe device.[20] However, incorporating MZO as a buffer layer in devices often leads to "S" shape behavior in the current–voltage curves.[21] The S-kink can be removed after light soaking, with the recovery typically lasting for ~3 days.[22] Because of this, it is important to study alternative buffer layer materials to further improve device performance while ensuring long-term stability.

1.4. Device Performance Limitations

First Solar Inc currently holds the CdTe research-cell efficiency record of 23.1%.[10] However, open-circuit voltage (V_{oc}) losses remain a limiting factor.[1] The absolute V_{oc} loss (E_g/q - V_{oc}) of the previous record cell with 22.6% efficiency is around 491 mV (assuming an absorber bandgap of 1.39 eV). This voltage deficit is considerably higher than that of silicon, CIGSe, and perovskite solar cells.[23] Because of this, present research on CdTe solar cells largely focuses on decreasing V_{oc} losses. Researchers have increased the carrier concentration in the CdSeTe/CdTe absorber to increase V_{oc}. Copper has commonly been used as the dopant in CdTe and CdSeTe/CdTe absorbers. However, Cu doping limits the hole density to 10^{14}–10^{15} cm^{-3} and is known to cause lifetime reduction and device instability.[1] Arsenic has been used to dope the CdTe and CdSeTe/CdTe absorbers to increase hole densities beyond 10^{16} cm^{-3},[24,25] resulting in a conversion efficiency of 22.3%[26] while also improving long-term stability.[27] Due to the increase in hole density obtained with As doping, it is important to find a suitable front n-type buffer layer material.

1.5. ZnO Buffer Layers in As-doped CdSeTe/CdTe Devices

The incorporation of ZnO buffer layers in the CdSeTe/CdTe device structure has led to highly efficient and stable solar cells.[28] This was due to the high quality of the ZnO/CdSeTe interface, resulting in the reduction of Cl segregation at the front interface, where Cl usually accumulates to passivate defects.

In this study, we report on the optimization of ZnO buffer layers for CdSeTe/CdTe solar cells. The ZnO deposition temperature and thickness is varied to optimize device performance. Following the ZnO buffer layer deposition, devices are fabricated using

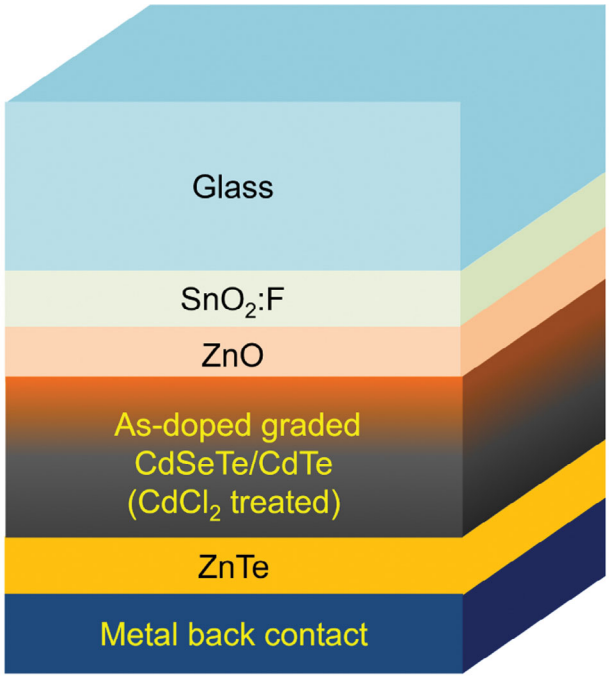


Figure 1. The device structure incorporating a ZnO buffer layer (not to scale).

First Solar's CdSeTe/CdTe absorber, $CdCl_2$ heat treatment, and back contact. The device structure is presented in **Figure 1**.

After device fabrication, the devices are characterized using current density–voltage (*J–V*), capacitance–voltage (*C–V*), external quantum efficiency (EQE) measurements, and cross-sectional scanning transmission electron microscopy (STEM) and energy dispersive X-ray spectroscopy (EDX) for elemental mapping. The optimization of ZnO buffer layers for CdSeTe/CdTe solar cells will help to achieve higher conversion efficiencies.

2. Results

2.1. Electrical Measurements

2.1.1. Effect of Temperature During the ZnO Deposition

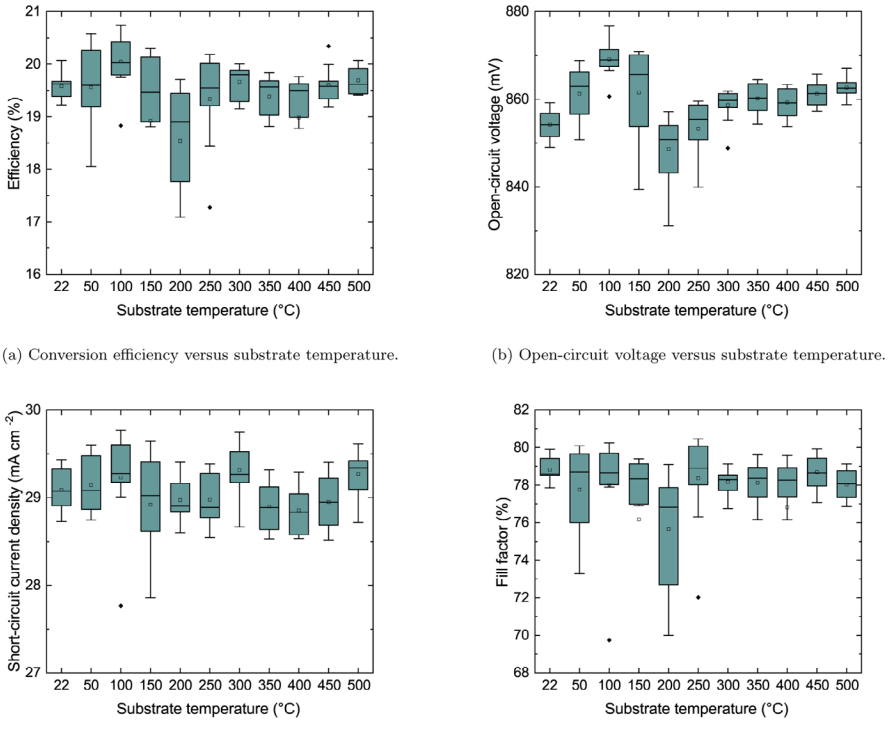
The device performance parameters are presented in **Figure 2** as a function of the substrate temperatures used during the ZnO deposition. As shown in Figure 2, the device performance increases with substrate temperatures up to 100 °C. Temperatures exceeding 100 °C resulted in a lower device performance. The highest conversion efficiency of 20.74%, V_{oc} of 876.7 mV and J_{sc} of 29.77 mA cm^{-2} was achieved using the ZnO layer deposited at 100 °C. While the maximum fill factor (FF) does not vary significantly, the highest FF of 80.47% is achieved using the ZnO deposited at 250 °C, the second highest FF of 80.25% is achieved using the ZnO deposited at 100 °C. The corresponding series resistance (R_s), shunt resistance (R_{sh}), saturation current density (J_0) and ideality factor (n) values are shown in **Figure 3**.

As shown in Figure 3, the J_0 and n increase as the substrate temperature increases from 22 °C to 200 °C, suggesting that a substrate temperature of 200 °C degrades the quality of the p-n junction. The R_s is observed to decrease between 22 °C and 100 °C while the R_{sh} does not show a trend. However, the buffer layer deposited at 200 °C leads to the lowest R_{sh}.

2.1.2. Best Performing Solar Cells

Figure 4a presents the *J–V* curves of the best performing cells and the EQE of the best performing cell overall. The corresponding hole concentration as a function of profile depth is obtained from *C–V* measurements and is shown in Figure 4b. From the *J–V* curves in Figure 4a, it is clear that the solar cell incorporating the ZnO deposited at 100 °C results in the highest V_{oc}. The performance parameters of the cells presented in Figure 4a are summarized in **Table 1**.

The best performing cell achieved a conversion efficiency of 20.74%, V_{oc} of 876.7 mV, J_{sc} of 29.60 mA cm^{-2} and FF of 79.90%. The corresponding EQE curve shows high EQE in the short wavelengths due to the wide bandgap of the ZnO buffer layer. The bandgap of ZnO was extrapolated to be 3.23–3.25 eV using Tauc plots. The transmittance spectra and corresponding Tauc plots are presented in Figure S1 (Supporting Information). Furthermore, the effect of the CdSeTe bandgap grading is clearly shown by the EQE wavelength range reaching 900 nm. The first



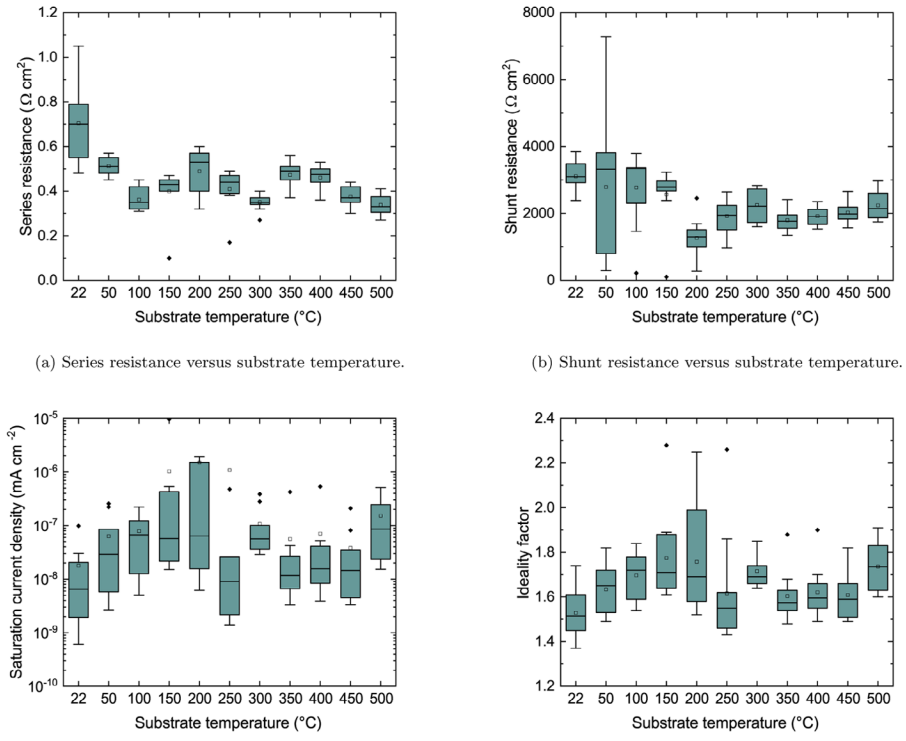
(a) Conversion efficiency versus substrate temperature.

(b) Open-circuit voltage versus substrate temperature.

(c) Short-circuit current density versus substrate temperature.

(d) Fill factor versus substrate temperature.

Figure 2. Device performance for varying substrate temperatures during the ZnO deposition. Each plot consists of 11 devices which have 12 cells each. The 11 devices were fabricated in the same batch.



(a) Series resistance versus substrate temperature.

(b) Shunt resistance versus substrate temperature.

(c) Saturation current density versus substrate temperature.

(d) Ideality factor versus substrate temperature.

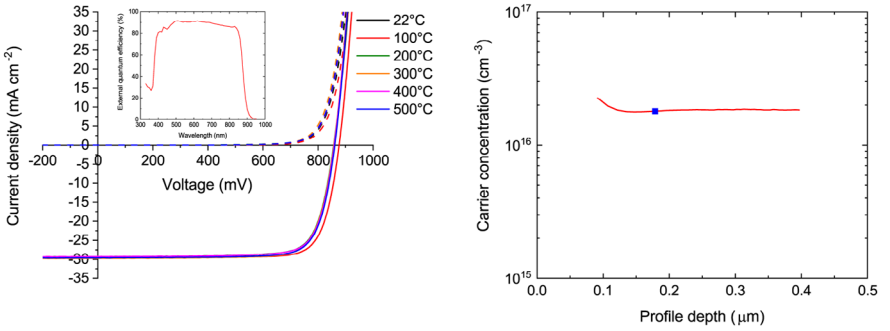
Figure 3. The extracted R_s, R_{sh}, J_0 and n values for varying substrate temperatures during the ZnO deposition. Each plot consists of 11 devices which have 12 cells each.

derivative of the EQE as a function of wavelength is used to calculate the absorber bandgap,[29] resulting in a bandgap of 1.41 eV.

As shown in Figure 4b, the hole density is ~1.8×10^{16} cm^{-3} (extracted at the zero-voltage bias point).

The *C–V* profiles can be affected by the presence of deep defects or interface defects, whereas drive-level capacitance profiling (DLCP) is insensitive to the response from the interface defects due to an improved signal-to-noise ratio. The interface defect density can be estimated by calculating the difference between the carrier concentrations obtained from C–V and DLCP measurements.[30] **Figure 5** presents the interface defect density as a function of substrate temperature during the ZnO deposition.

As shown in Figure 5, the interface defect density slightly decreases from 1.92×10^{14} to 8.57×10^{13} cm^{-3} when changing the substrate temperature from 22 to 100 °C. This reduction in interface defect density correlates to the performance improvement between 22 and 100 °C, as observed in Figure 2. Furthermore, increasing the substrate temperature from 100 to 200/500 °C leads to a significant increase in interface defect density.



(a) Illuminated (solid) and dark (dashed) J-V curves of the best performing cells incorporating ZnO deposited at different temperatures, the EQE of the best performing cell is included.

(b) Hole concentration as a function of profile depth (extracted from C-V measurements), the blue square represents the zero-voltage bias point.

Figure 4. Characteristics of the best performing cells, the lines in red correspond to the cell incorporating a ZnO layer deposited at 100 °C, achieving the highest efficiency of 20.74%.

Table 1. The *J–V* characteristics and extracted parameters of the best performing cells.

Substrate temp. (°C)	Eff. (%)	V_{oc} (mV)	J_{sc} (mA cm^{-2})	FF (%)	R_s (Ω cm^2)	R_{sh} (Ω cm^2)	J_0 (mA cm^{-2})	n
22	20.1	859	29.4	79.4	0.54	3482	9.14×10^{-9}	1.55
100	20.7	877	29.6	79.9	0.42	3346	6.90×10^{-9}	1.56
200	19.7	857	29.3	78.5	0.58	1443	6.19×10^{-9}	1.61
300	20.0	858	29.7	78.4	0.35	2729	1.00×10^{-7}	1.74
400	19.8	859	29.3	78.6	0.44	2120	1.56×10^{-8}	1.59
500	20.1	861	29.6	78.7	0.36	2545	3.54×10^{-8}	1.66

However, increasing the substrate temperature from 200 to 500 °C does not affect the interface defect density ($1.98 \times 10^{15} - 2.07 \times 10^{15}$ cm^{-3}).

The ZnO-based solar cells are expected to be stable, ZnO deposited at room temperature on glass (unencapsulated) did not show signs of degradation after being exposed to ultraviolet radiation and damp heat for 1000 h.[31]

2.1.3. Effect of ZnO Thickness

The device performance versus ZnO thickness is presented in **Figure 6**. When comparing the performance of the device incorporating a 65 nm thick ZnO layer to the previously reported optimal thickness of 50 nm,[28] the mean/median efficiency, V_{oc} and FF are higher when using a 15 nm thicker ZnO layer. While the highest efficiency of 20.14%, V_{oc} of 858.9 mV and FF of 81.06% are achieved using a ZnO thickness of 65 nm, it can be seen that device performance is reasonably insensitive to thickness variations between 40 and 70 nm. The mean and median J_{sc} are observed to slightly decrease as the ZnO thickness is increased from 40 to 70 nm, due to parasitic absorption in the short wavelength region. This is consistent with the results presented for a less granular set of ZnO thickness variations from 50 to 200 nm.[28]

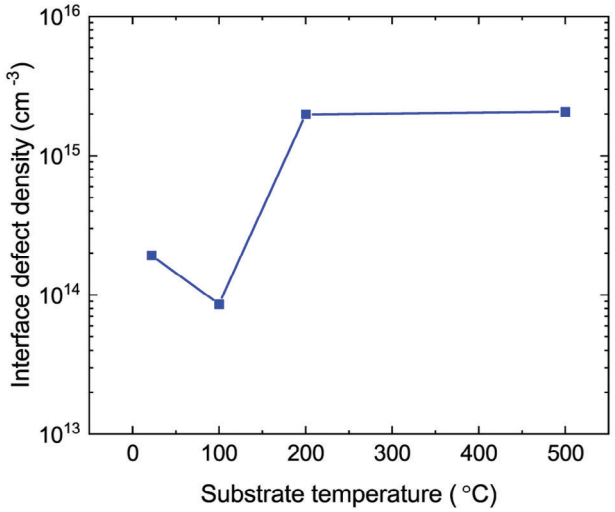


Figure 5. Interface defect density for varying substrate temperatures during the ZnO sputtering process. The temperatures include 22, 100, 200, and 500 °C.

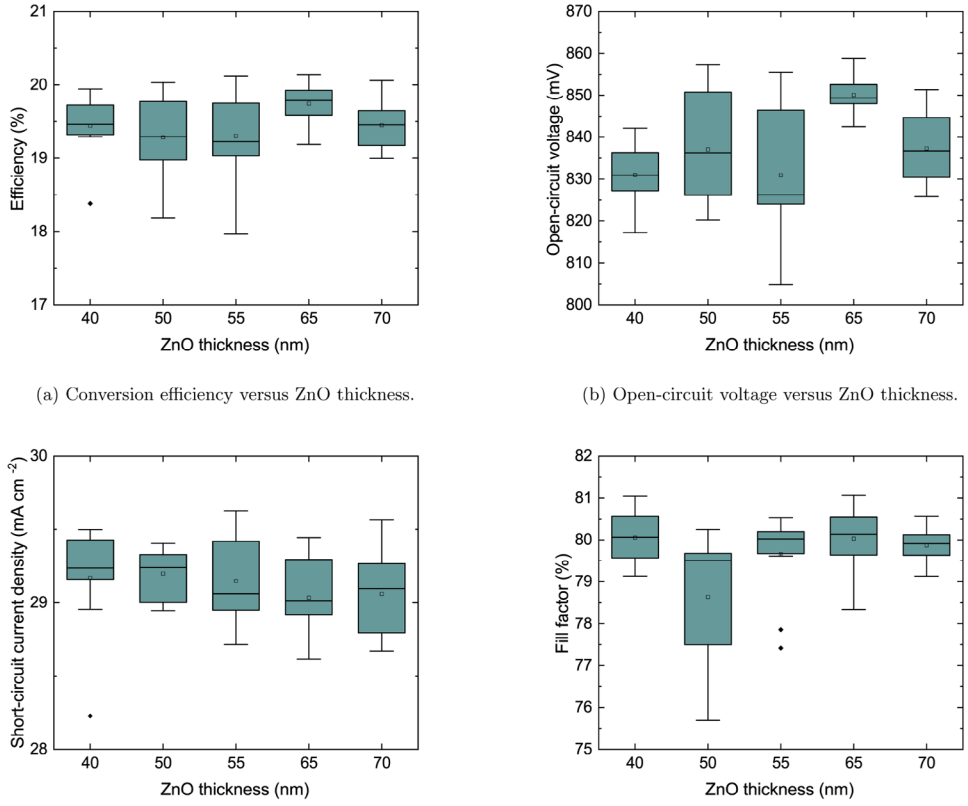
2.2. Materials Characterization

The STEM-EDX images of the front interface of the devices corresponding to the ZnO (~75 nm thick) deposited at substrate temperatures of 100 °C and 500 °C are presented in **Figure 7**.

The electron images and Zn maps show a uniform and conformal layer of ZnO on the relatively rough SnO_2:F (FTO) surface. Chlorine diffuses along grain boundaries and accumulates at the front interface, where it passivates defects.[32] The unusual absence of Cl at the front interface was first observed in a CdSeTe/CdTe device incorporating a ZnO buffer layer deposited at room temperature.[28] As shown in Figure 7, the Cl map of the buffer layer deposited at 100 °C does not show Cl segregation at the junction, unlike in the case of an MZO-based device.[33] However, Cl does decorate the front interface of the 500 °C sample. This suggests that the substrate temperature used during the ZnO deposition can greatly impact the quality of the ZnO/CdSeTe interface. The ZnO layer in the best performing devices is nanocrystalline. Additionally, high-resolution TEM imaging has shown that ZnO deposited at room temperature maintained its nanocrystalline phase throughout the device fabrication,[28] unlike in the case of CdS:O buffer layers.[12] Depositing ZnO at lower temperatures (22–100 °C) leads to the highest-quality front interface. Furthermore, atomic force microscopy (AFM) measurements show that depositing 75 nm thick ZnO at 100 °C results in the lowest average roughness and root mean square (RMS) roughness, as shown in Figure S2 (Supporting Information). This suggests that the ZnO deposited at 100 °C has the smallest crystallite size. Grazing incidence X-ray diffraction (GIXRD) measurement results are presented in Figure S3 (Supporting Information), the ZnO films possess a hexagonal polycrystalline structure. The three main peaks are (002), (102), and (103), with (002) being the most intense. Figure S3 (Supporting Information) shows the calculated crystallite size (using the Scherrer equation) as a function of substrate temperature, the film deposited at 100 °C has the smallest crystallite size, this corroborates the findings of Hajara et al.[34] The ZnO deposited at 500 °C has the largest crystallite size, creating an interface which may be more susceptible to chlorine segregation.

3. Conclusion

The ZnO deposition temperature and thickness was varied to improve the CdSeTe/CdTe device performance. Depositing the



(a) Conversion efficiency versus ZnO thickness.

(b) Open-circuit voltage versus ZnO thickness.

(c) Short-circuit current density versus ZnO thickness.

(d) Fill factor versus ZnO thickness.

Figure 6. Device performance for varying ZnO thickness deposited at 100 °C, each plot consists of 5 devices which have 12 cells each. The 5 devices were fabricated in the same batch.

ZnO at 100 °C resulted in the best performing cell with a conversion efficiency of 20.74%, without an anti-reflection coating. While varying the ZnO thickness from 40 to 70 nm did not have a significant effect on device performance, the 65 nm thick ZnO led to the best performing cell. The extracted J_0 and n values suggest that the quality of the front p-n junction deteriorates as the substrate temperature is increased from 22 to 200 °C. Furthermore, the interface defect density has been observed to increase when depositing ZnO at temperatures exceeding 100 °C. Chlorine is usually observed at the buffer layer/absorber interface of high efficiency devices, where the presence of Cl passivates defects. The STEM-EDX analysis shows that Cl is only detected by EDX at the front interface of the 500 °C sample, suggesting that the quality of the front interface is dependent on the buffer layer deposition temperature. The analysis shows that the density of defects is an important factor influencing the concentration of Cl segregation at the front interface, where a more defective interface leads to a higher concentration of Cl. Increasing the substrate temperature results in a more distinct grain structure in the ZnO. The nanocrystalline microstructure of the ZnO buffer obtained at lower temperatures results in a higher quality interface. Future work will investigate the effect of varying the oxygen content during the ZnO deposition on the film properties and device performance.

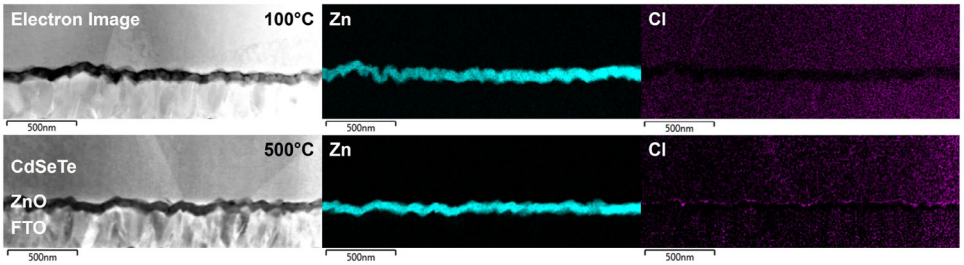


Figure 7. STEM-EDX elemental maps showing the front interface of the devices incorporating a ZnO buffer layer deposited at 100 °C (top) and 500 °C (bottom). The ZnO buffer layer is uniform and continuous. Note that Cl is detected above the buffer layer in the EDX map obtained from the device containing ZnO deposited at 500 °C. Background/peak overlap subtraction was not applied to the Cl maps.

4. Experimental Section

Preparation of the ZnO Films: The 40–75 nm thick ZnO films were deposited using RF sputtering from a compound target. The substrates used were commercial (NSG-Pilkington) FTO coated soda-lime glass (SLG) for device fabrication and uncoated SLG for film characterization. An anti-reflection coating was not deposited on the sun-facing side of the glass. The substrate size is 5 × 5 cm, with an FTO coated SLG thickness of 2.65 mm. Prior to depositions, compressed air was used to remove any particles from the glass/FTO surface. This was followed by wiping the surfaces with Kimtech wipes and 99.5+% pure isopropanol (IPA). Compressed air was used again to dry the substrates and remove particles. The substrates were then cleaned using an ultrasonic cleaner in three 15-min cycles, at a temperature of 45 °C. The first cycle included deionized water and multipurpose detergent. The second and third cycles included >95% pure acetone and 99.5+% pure IPA, respectively. The substrates were rinsed using deionized water after the first and second cycle. Following the third cycle, the samples were stored in IPA.

A magnetron sputtering system from AJA International, Inc. was used to deposit the ZnO films. The sample holder allows simultaneous sputter-deposition on 4 substrates. The diameter of the ZnO target (with purity 99.99%) is 4 inches and was supplied by Plasmaterials, Inc. A 5-min plasma clean was used to remove atmospheric contamination and activate the glass/FTO surface which rotated at a speed of 10 rpm. The plasma cleaning gas pressure was set to 5 mTorr with 20% oxygen and 80% argon, a power of 100 W was used to generate plasma at 22 °C. Following the plasma clean, ZnO was sputtered on the glass/FTO using a power density of 1.85 W cm^{-2}. The substrates were set to rotate at 10 rpm and were 18.4 cm above the ZnO target. The working gas pressure was set to 1 mTorr with 1% oxygen and 99% argon. Prior to each deposition, the chamber base pressure was between 2.0×10^{-4} and 4.0×10^{-4} mTorr. The ZnO layers fabricated under these conditions are highly resistive. No signal could be extracted using a high-sensitivity parallel dipole line Hall effect system,[35] indicating that the carrier concentration of the as-deposited material is $<10^{12}$ cm^{-3}.

To study the optimal substrate temperature during the ZnO deposition, 75 nm thick ZnO layers were deposited at 22, 50, 100, 150, 200, 250, 300, 350, 400, 450, and 500 °C. The deposition time was adjusted for each temperature to ensure the film thickness was consistent. Using the optimal temperature, the thickness of the ZnO layer was varied around the previously reported best performing thickness of 50 nm.[28] The ZnO thicknesses were 40, 50, 55, 65, and 70 nm.

Device Fabrication: Vapor transport deposition was used at First Solar to deposit the 3–4 µm thick CdSeTe/CdTe absorber on the ZnO layer. Arsenic was used to dope the CdSeTe/CdTe absorber. The samples were activated with an anneal in a $CdCl_2$-vapor environment between 400 and 500 °C.[26] Following the $CdCl_2$ heat treatment, ZnTe and a metal back-contact were deposited.[36] The cell area of 0.445 cm^2 was defined using laser scribing.

Characterization: The *J–V* measurements were obtained at room temperature under one Sun (AM 1.5G) with a class AAA Oriel Sol1A solar simulator. The R_s, R_{sh}, J_0 and n values were extracted by fitting *J–V* curves to the single diode model using the Lambert W function in MATLAB.[37] External quantum efficiency measurements were calibrated using a silicon reference diode with a known (NIST-traceable) spectrum.[36] Capacitance-voltage data was measured at a frequency of 40 kHz using the Agilent E4980A LCR meter to obtain the data presented in Figure 4b. Additional capacitance spectroscopy measurements (both *C–V* and DLCP) were performed in the dark at room temperature using a Keysight E4990 impedance analyzer. The net carrier concentration of the absorber layer was extracted from both *C–V* and DLCP depth profiles. The interface defect density was estimated by calculating the difference between the carrier concentrations obtained from *C–V* and DLCP measurements.

The sample foil for STEM analysis was prepared with an FEI FIB dual-beam system, using a standard in situ lift out method.[38] The STEM images were obtained using an FEI Tecnai F20 S/TEM, equipped with Gatan bright and dark-field STEM detectors, a Fischione high-angle annular dark-field (HAADF) STEM detector and an Oxford Instruments X-Max 80 mm^2 windowless EDX spectrometer. The detection limit of EDX is 0.1 wt%. Images were taken at 200 kV, with a camera length of 100 mm and a condenser aperture size of 70 µm.[13]

Statistical Analysis: The 25th ($Q1$) and 75th ($Q3$) percentiles were used to create the box plots in Figures 2, 3, and 6, where the interquartile range (IQR) was given by the difference between $Q3$ and $Q1$. The minimum and maximum points were defined by $Q1 - 1.5IQR$ and $Q3 + 1.5IQR$, respectively. Outliers were set by the data points which were less than the minimum or greater than the maximum. The box plots include the calculated mean and median values. A sample size of 12 solar cells was used for each box. Statistical analysis and plotting were performed using Origin 2020 (OriginLab).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

W.Z., C.L., T.N., D.L. and G.X. work at First Solar Inc., a publicly traded company which manufactures thin film CdTe solar panels and develops photovoltaic power plants. Apart from this and the funding mentioned in the acknowledgments section, the authors have no other conflict of interest to declare.

Data Availability Statement

The data that support the findings of this study are available from the Wiley Online Library or the corresponding author upon reasonable request.

Keywords

buffer layer, CdSeTe/CdTe, solar cells, ZnO

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