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Cascadable Enhanced Quasi-Z-Source Inverter with Reduced Current Stress

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ABSTRACT

In magnetically coupled impedance source (MCIS) inverters, the turn ratio of the coupled inductor offers design flexibility. The leakage inductance, however, poses additional challenges, mainly voltage spikes. This paper proposes a novel quasi-Z-source inverter (qZSI) with the coupled inductor's voltages effectively clamped in each operating state without any additional snubber, reducing the stresses on the semiconductors and providing a smooth DC-link voltage. It also features significantly lower peak shoot-through (ST) current compared to other high-gain impedance source networks, resulting in enhanced efficiency and lower rating of semiconductors. Furthermore, the input current is continuous and there is a common ground between the input source and the H-bridge, which brings practical advantages. Theoretical analysis and comparison of performance with similar topologies are presented and confirmed through extensive experiments on a 500 W prototype.

1 | Introduction

Traditional voltage-source inverters (VSIs) operate only in buck mode and are prone to unintentional short circuits in the legs. Dead-time insertion is a solution to the shoot-through problem that results in low-quality output waveforms.

The Z-source inverter (ZSI) was introduced to overcome the aforementioned issues of traditional inverters. Additionally, the inversion gain can theoretically extend to infinity, eliminating the need for a separate boost stage. As a further development, the quasi-Z-source (qZSI) was then introduced to tackle some of the limitations of the ZSI, mainly high stresses on its capacitors, discontinuous input current, and no direct connection between the input and the DC link [1, 2]. Additionally, the various possible applications that have already been well explored are adjustable speed drives [3, 4], uninterruptible power supplies [5], galvanically isolated DC-DC converters [6], inverters [7–11], and electric vehicles [12].

Ultra-high voltage gain applications require a long shoot-through (ST), which leads to a low modulation index for the inverter. As a consequence, the output voltage deteriorates and semiconductors are exposed to higher voltage stresses due to the high DC-link voltage requirement.

By adding passive elements and diodes to the aforementioned networks, the boost ratio can be improved considerably and ultra-high-voltage gain application can be achievable. In [13], the enhanced-boost Z-source inverter with the switched network (EBS-ZSI) was proposed to achieve a high voltage gain. EBS-ZSI still suffers from the drawbacks of the ZSI, such as the lack of common ground and input inrush current. By replacing the inductors of the qZSI with switched impedance cells, the enhanced boost qZSI with two-switched impedance networks (EB2S-qZSI) was proposed [14]. This network not only benefits the advantages of qZSI but also can be used for high-gain applications. Another converter proposed in [15] slightly improved the voltage gain, although it still suffers from a high number of elements. These

converters often face challenges such as increased volume, complexity and a high number of components. To reduce the volume and number of elements, Gu et al. [16] proposed an enhanced-boost qZSI with an active switched Z-network (EBASZN-qZSI) which is a combination of SBI (switched boost inverter) [17] and qZSI. The volume of this converter is significantly decreased compared to other mentioned converters, which are appropriate for high-gain applications. Also, the number of elements is lower.

It is possible to enhance the boost ratio further for ultra-high gain applications with magnetically coupled impedance source (MCIS) networks. The turn ratio of the coupled inductors provides design flexibility and allows for achieving higher gains with smaller STs. Y-source [18], Δ-Source [19] and their quasi-versions [20] can be truly regarded as the origins of MCIS as most other topologies based on coupled inductors can be derived from these general structures. A typical issue found in MCIS networks is the occurrence of voltage and current spikes and ringing on the H-bridge switches. To mitigate these issues, cascade techniques and snubber circuits have been proposed [21–23]. By recovering stored energy, these circuits can smooth currents and voltages and ultimately lead to lower component ratings and reduced magnetic circuit volume and cost. However, two primary considerations should be taken into account: minimizing the number of additional components and performance dependence on the leakage inductance. Recently, an integrated energy recovery scheme is proposed in [24], which suppresses the spikes and clamps the DC-link voltage by introducing an auxiliary circuit to the impedance-source networks. However, constructing the coupled inductor can be complex due to its three-winding setup and the DC-link voltage fluctuates between two different levels.

This paper proposes a cascadable coupled-inductor quasi-Z-source inverter with a clamped DC-link voltage. During different operation states, the voltage across the windings is naturally clamped due to the specific arrangement of reactive components, which allows the stored energy in leakage inductors to be recovered without requiring additional snubber or auxiliary circuits. The voltage spikes are mitigated through this clamping mechanism, while the shoot-through currents are inherently reduced by the converter's structure. As a key feature of the proposed converter, the winding turn ratio is adjusted to achieve high voltage gains, even when the turn ratio is unity. Furthermore, the DC-link voltage is constant, and the harmonic content is lower than its counterparts. The operating principle and analysis are presented in Section 2, while Section 3 explains parameter design considerations. Section 4 presents comparisons, and experimental results in Section 6 validate the theoretical analysis.

2 | Fundamental Operating Principles

The proposed converter is presented in Figure 1a. The circuit consists of the qZSI, an active switch and unique magnetic element boost cells (MEBC). It worth mentioning that the first winding of the all cells is similar. Also, Figure 1b shows the equivalent circuit of the proposed converter with one cell, simplifying the introduction. It utilizes a two-winding coupled inductor to increase the conversion ratio, which will be modeled as an ideal transformer with the magnetizing inductance, L_m, transferred to the primary side. The leakage inductors are very small and have almost no significant impact on operational waveforms and are ignored in calculations. It is also assumed that the capacitors and inductors are large enough to be treated as voltage and current sources, respectively.

2.1 | Operation at Steady State in CCM Mode

To simplify the operating states of the proposed converter, analysis is applied to a network with one cell. The operating modes of the proposed topology can be divided into two main modes: shoot-through (ST), which itself consists of two states, and non-shoot-through (NST), which includes three distinct states. The key waveforms and equivalent circuits for different states are illustrated in Figures 2 and 3, respectively.

2.1.1 | ST-I State $[t_0 - t_1]$

As shown in Figure 3a, at the beginning of this interval, all switches are turned on, and the diode D_2 conducts until the stored energy in the leakage inductor (L_k) reaches zero. The remaining diodes are reverse-biased. Compared to reactive elements of the proposed converter, L_k is very small. Therefore, this time interval can be considered negligible compared to the ST. As a result, the energies of other reactive elements do not change during this mode.

2.1.2 | ST-II State $[t_1 - t_2]$

During this state, as shown in Figure 3b, all diodes are reverse-biased, while both switches conduct and capacitors C_3 and C_4 charge the coupled inductor through winding N1. As diode D_2 is blocking, no current flows through capacitor C_2, resulting in a fixed voltage across C_2 during this state. The voltage source and C_1 charge the input inductor Lin. It can be noted that the L_m core is energized only through winding N_1.

2.1.3 | NST-I State $[t_2 - t_3]$

Figure 3c illustrates the NST states. During these states, switch S_2 is off, and the impedance network supplies power to the load. As shown, all diodes conduct and C_2 is charged, while other capacitors discharge. The capacitors C_3 and C_4 charge through winding N_2 and the input inductor, respectively. As depicted in Figure 2, the currents of C_1 and C_2 change linearly. The current of C_2 reaches zero at the end of this time interval.

2.1.4 | NST-II State $[t_3 - t_4]$

This time interval is similar to the previous state, with the only difference being that the current of C_2 starts to increase through winding N_2, which discharges C_1. At the end of this time interval, the current of C_1 reaches zero.

2.1.5 | NST-III State $[t_4 - T_S]$

During this time interval, the current of C_2 continues to increase, while the current of C_1 rises in the opposite direction linearly.

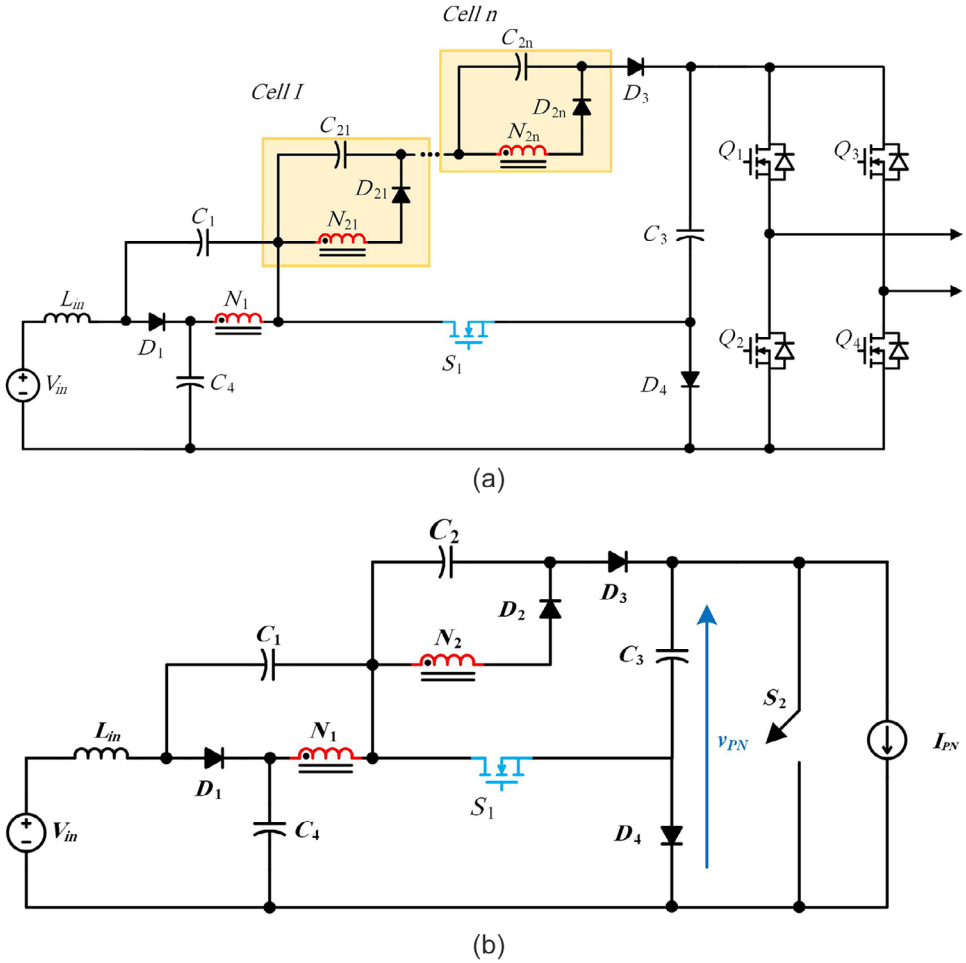

FIGURE 1 | Proposed cascadable enhanced qZSI. (a) Multi-cell scheme, and (b) one cell equivalent circuit.

2.2 | Current Analysis

As mentioned before, the time interval of the ST-I state is very short and its effect can be disregarded. Hence, the analysis starts from Figure 3b, where all diodes block and the switches are turned on that gives:

$$i_{C1}^{ST,II} = -I_{in} \tag{1}$$

$$i_{C2}^{ST,II} = 0 \tag{2}$$

$$i_{C3}^{ST,II} = -\left(I_{in} + I_{N1}^{ST,II}\right) \tag{3}$$

$$i_{C4}^{ST,II} = -I_{N1}^{ST,II} \tag{4}$$

The ampere-turn law for the two-winding coupled inductor is:

$$N_1 i_{N1} + N_2 i_{N2} = N_1 I_m \tag{5}$$

Thus, the magnetizing current can be derived by solving Equations (1)–(5) as:

$$I_m = \frac{1 + (1-D)N}{1 + ND} \times I_{in} \tag{6}$$

where $N = N1/N2$. Equation (6) shows that in the higher duty cycles, the magnetizing current would be lower. In the NST states, the currents of capacitors C_1 and C_2 change linearly. The current slope can be determined by comparing two currents at two different instants. The coupled-inductor windings are clamped by capacitors in parallel, resulting in a continuous current flow through both windings. Therefore, at the beginning of the NST state $i_{Nx}(t_2^+)$ is equal to the current at the end of the ST state $i_{Nx}(t_2^-)$, where $x = 1, 2$. The current of capacitors at t_2^+ can be expressed as (7).

$$\begin{aligned} i_{C1}\left(t_2^+\right) - i_{C2}\left(t_2^+\right) &= I_m \\ i_{C2}\left(t_2^+\right) + i_{C3}\left(t_2^+\right) &= -I_{PN} \\ i_{C3}\left(t_2^+\right) + i_{C4}\left(t_2^+\right) &= I_{in} - I_{PN} \end{aligned} \tag{7}$$

The same equations are obtained at T_s^- as:

$$\begin{aligned} i_{C1}(T_s^-) - i_{C2}(T_s^-) &= \frac{-1}{N} I_m \\ i_{C2}(T_s^-) + i_{C3}(T_s^-) &= -I_{PN} \\ i_{C3}(T_s^-) + i_{C4}(T_s^-) &= I_{in} - I_{PN} \end{aligned} \tag{8}$$

Assuming that $i_{C2}(t)$ changes linearly, the ampere-second balance means the absolute values of $i_C2(T_s^-)$ and $i_C2(t_2^+)$ are equal and the duration of D2 is half of the duration of the NST state. $i_{C1}(t)$ also changes linearly. According to the ampere-second balance on C_1

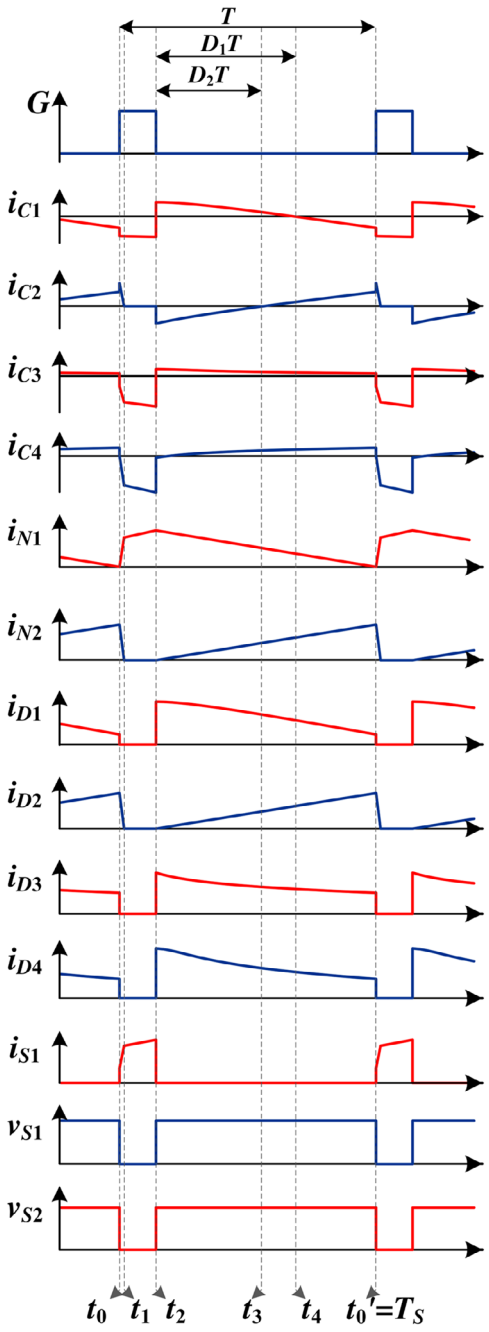

FIGURE 2 | Steady-state waveforms.

and C_2, the average current over one switching period is zero:

$$\int_0^T i_{Cx}(t)dt = 0 \tag{9}$$

where $x = 1,2$ is the number of argued capacitor. According to Figure 2, Equation (7), and Equation (8), one can conclude:

$$\begin{aligned} D_1 &= \frac{3N-1}{2(N+1)}(1-D) \\ D_2 &= \frac{1-D}{2} \end{aligned} \tag{10}$$

$$I_{PN} = \frac{1-(N+4)D}{(1+ND)(1-D)} I_{in} \tag{11}$$

By applying KCLs, the currents flowing through all elements can be obtained.

2.3 | Voltage Analysis

The inductors' voltages can be calculated during each state. As ST-I is negligible compared to the shoot-through interval, the voltage across inductors is considered only during states ST-II and NST. In ST interval, the voltages are:

$$V_{Lin}^{STII} = V_{in} + V_{C1} + V_{C3} \tag{12}$$

$$V_{Lm}^{STII} = V_{C3} + V_{C4} \tag{13}$$

and in NST state:

$$V_{Lin}^{NST} = V_{in} - V_{C4} \tag{14}$$

$$V_{Lm}^{NST} = -\frac{1}{N} V_{C2} \tag{15}$$

Then, the volt-second balance for the magnetizing and the input inductors gives the boost factor and the voltage across the capacitors. The following equations are for the capacitor voltages and the boost factor (B), where V_{PN} is the maximum output voltage in NST state. The boost factor is defined as the ratio of the amplitude of output voltage in NST states to the input voltage.

$$\begin{cases} V_{C1} = \dfrac{2D}{1+ND} \times \hat{V}_{PN} \\ V_{C2} = \dfrac{2ND}{1+ND} \times \hat{V}_{PN} \\ V_{C3} = \hat{V}_{PN} \\ V_{C4} = \dfrac{1-(N+2)D}{1+ND} \times \hat{V}_{PN} \end{cases} \tag{16}$$

$$B = \frac{\hat{V}_{PN}}{V_{in}} = \frac{1+ND}{1-(N+4)D} \tag{17}$$

The boost factor is plotted in Figure 4. Clearly, a higher turn ratio (N) leads to a higher boost ability. It is worth noting that by choosing a unity turn ratio, an ultra-high boost factor can be readily achieved.

Considering the parasitic inductance of the coupled inductor for one cell network would lead to the following boost factor.

$$B = \frac{1+ND(1-\gamma)}{1-(N(1-\gamma)+4)D} \tag{18}$$

where γ is $L_k/(L_k + L_m)$. It confirms that the parasitic inductance do not affect the boost factor considerably.

To determine the blocking voltage of the semiconductors, KVLs can be used, resulting in the values given in Table 1.

The general boost factor for the proposed converter is:

$$B = \frac{\hat{V}_{PN}}{V_{in}} = \frac{1+\sum_{i=1}^{n} N_{2i} D}{1-\left(\sum_{i=1}^{n} N_{2i} + 4\right) D} \tag{19}$$

where i is the turn ratio of the cell number i.

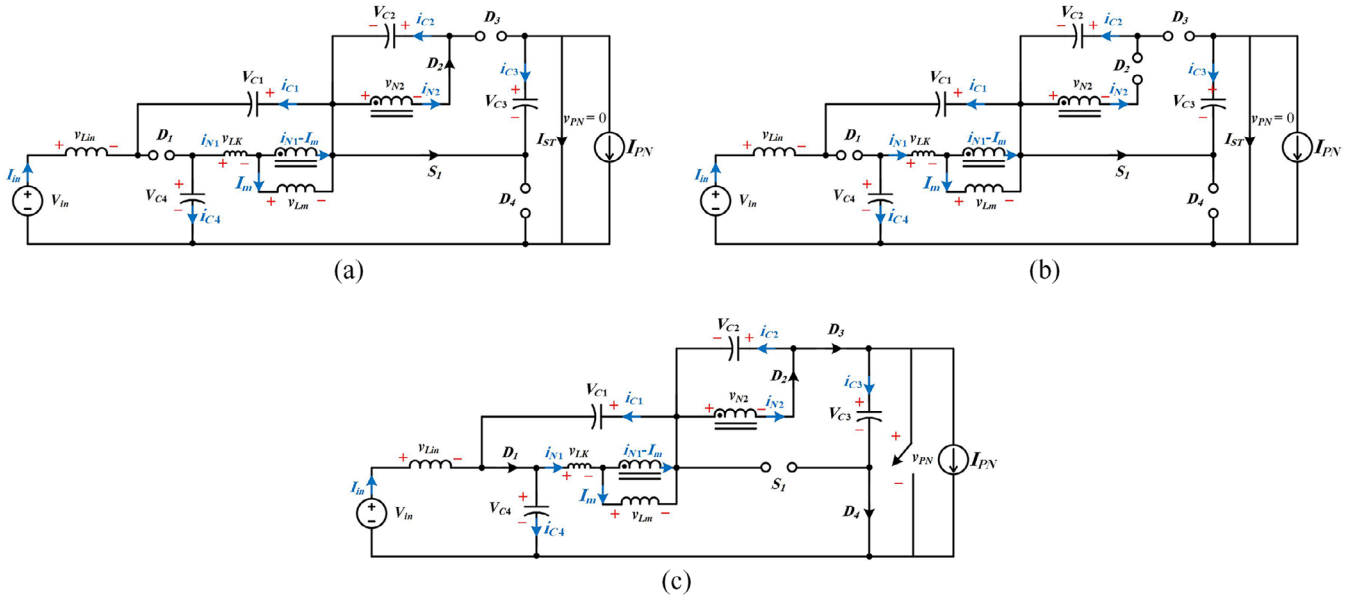

FIGURE 3 | Operation during (a) ST-I state, (b) ST-II state, and (c) NST states.

TABLE 1 | Voltage and current stresses.

Converter	HS-YSI [21]	LCD-qYSI [22]	SDL-YSI [24]	Proposed
K	$(N_1+N_3)/(N_3-N_2)$	$(N_1+N_3)/(N_2-N_3)$	$(N_1+N_3)/(N_2-N_3)$	$N_2/N_1=N=K$
B	$1/(1-(2+K)D$	$1/(1-(1+K)D)$	$1/(1-2(1+K)D)$	$1+KD/(1-(4+K)D$
V_{C1}/Vin	$(1-2D)B$	$(1-D)B$	$(1-2D)B$	$2DB/(1+ND)$
V_{C2}/Vin	KDB	KDB	$2KDB$	$2NDB/(1+ND)$
V_{C3}/Vin	$(1-D)B$	$V_{C3}^{LCD(1)}$	B	B
V_{C4}/Vin	DB	NA	NA	$B(1-(N+2)D)/(1+ND)$
I_m/I_{in}	$1+N_3/N_1$	0	0	$(1+(1-D)N)/(1+ND)$
I_{Lo}/I_{in}	1	V_{C3}^{LCD}/L_o	NA	NA
I_{D1}/I_{in}	$(K+1)/(1-D)K$	$1/(1-D)$	$(K+(K+1)D)/(K(1-D))$	$(3N^2+6N-1+ND+ND^2)/(4N(1+ND))$
I_{D2}/I_{in}	$(K+1)/(1-D)$	$K/(1-D)+I_{Lo}/I_{in}$	$(K+1)(1-D)-1/(1-D)$	$(N+1-ND)/(N(1+ND))$
I_{D3}/I_{in}	NA	I_{Lo}/I_{in}	$K+1$	$((N+1)^2-ND(1+N))/(4N(1+ND)$
I_{D4}/I_{in}	NA	NA	NA	$((N-1)^2+12ND+2N^2D)/(4N(1+ND)(1-D))$
I_{S1}/I_{in}	NA	NA	$K+1$	$(N+2)/(1+ND)$
I_{S2}/I_{in}	$K+2$	$K+1$	$K+1$	$(N+2)D/(1+ND)$
V_{D1}^{BR}/V_{in}	KB	KB	$2KB$	$2B/(1+ND)$
V_{D2}^{BR}/V_{in}	B	$(1-D)B+V_{C3}^{LCD}$	B	$2NB/(1+ND)$
V_{D3}^{BR}/V_{in}	NA	$V_{PN}-V_{C3}^{LCD}$	B	$(1-ND)B/(1+ND)$
V_{D4}^{BR}/V_{in}	NA	NA	NA	B
V_{S1}^{BR}/V_{in}	NA	NA	B	$(1-ND)B/(1+ND)$

(1) $V_{C3}^{LCD}=0.5DB+0.5\sqrt{(DB)^2+4L_kL_oI_N1^2/(DTV_{in})^2}$.

By applying simple boost modulation as described in [17], the maximum modulation index is $1-D$. So, the maximum voltage gain of the proposed converter with one cell is:

$$G=M.B=\frac{V_{DC}^{\max}}{V_{in}}=\frac{\hat{V}_{PN}}{V_{in}}\frac{(1-D)(1+ND)}{1-(N+4)D} \tag{20}$$

3 | Component Parameter Design

The design of passive components has been considered in this section, including the values of capacitors, L_{in} and L_m.

3.1 | Inductive Components

The inductances of the circuit can be determined using the voltage across the windings during states and their dwell times. As mentioned in Section 2, both L_m and L_{in} are charged during the ST mode. Thus, from (12), and (13), one can obtain:

$$\begin{cases} L_{in} = L_{Base} \times \dfrac{2D(1-D)}{1-(N+4)D} \\ L_m = L_{Base} \times \dfrac{2D(1-D)(1+ND)}{(1+N(1-D))(1-(N+4)D)} \\ L_{Base} = \dfrac{V_{in}^2 T}{\alpha\% P} \end{cases} \tag{21}$$

where $\alpha\%$ is the maximum tolerable ripple of the inductors which can be different for each inductor, T is the time interval of the switching and P is the output power.

3.2 | Capacitive Components

The voltage ripple across a capacitor can be written as:

$$\Delta V_C = \frac{I_C^{ST} DT}{C} \rightarrow C = \frac{I_C^{ST} DT}{\Delta V_C} \tag{22}$$

Assuming the maximum allowable voltage ripple for each capacitor is $\beta\%$ then the mathematical relations for the required capacitances can be defined as:

$$\begin{aligned} C_1 &= C_B \times \frac{1-(4+N)D}{2} \\ C_2 &= C_B \times \frac{N+1}{8N} \times \frac{D(1-D)(1+N-ND)(1-(4+N)D)}{(1+ND)^2} \\ C_3 &= C_B \times \frac{D.(2+N).(1-(4+N)D)}{(1+ND)^2} \\ C_4 &= C_B \times \frac{D.(1+N(1-D)).(1-(4+N)D)}{(1+ND)(1-2D-ND)} \\ C_B &= \frac{P_o T}{\beta\%\ V_{in}^2} \end{aligned} \tag{23}$$

4 | Comparison

The proposed converter offers several advantages over other Z-source inverters. The discussion of comparison goes beyond the number of elements. To do so, this subsection provides a detailed analysis to highlight the significant features of the proposed converter. For the sake of a fair comparison and as already mentioned in [24], all converters have the same δ (equal to $N = 1$, in the proposed converter).

4.1 | Active Components

The shoot-through (ST) current is one of the major issues with impedance networks. Figure 5a compares the normalized ST currents. The ST current in both the proposed converter and SDL-qYSI is considerably lower than that of other counterparts, leading to cost-effective switches of H-bridge and a more efficient converter.

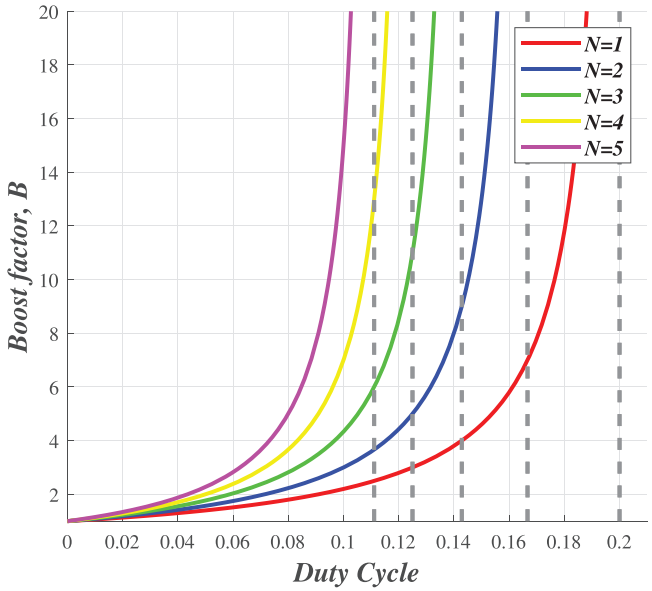

FIGURE 4 | Voltage boost factor for different turn ratios.

From Table 1, one can calculate the peak currents and the blocking voltages for each semiconductor. Another challenge in MCIS is the maximum voltage stress on diodes. For the proposed converter, it happens across D_2. In Figure 5b, this maximum blocking requirement is compared to those of others. To gain a better understanding, Figure 6c is plotted at $\delta = 5$. The blocking voltage of D_2 is the lowest for the proposed converter which make its rating considerably lower than others.

Since current rating of semiconductors is high in ZSIs, the proposed converter provides lower current rating. Figure 6a confirms this and shows the normalized current flowing through each semiconductor. Another important parameter of semiconductors is maximum blocking voltage across them. The normalized blocking voltage is also plotted in Figure 6b. It shows that the proposed network is not advantageous compared to others. However, to select a semiconductor, both voltage and current should be considered simultaneously. The switching device power (SDP) parameter is commonly used to evaluate the ratings of switching devices, as already described in [7]. The peak SDP can be calculated as:

$$SDP_{peak} = \sum_{i=1}^{n} V_i^{peak} I_i^{peak} \tag{24}$$

where n is the number of semiconductors and V_i^{peak} and I_i^{peak} are the peak voltage and current of the i-th semiconductor, respectively.

Normalized peak SDP is presented in Figure 6c, which evidences that the overall rating of semiconductors in the proposed converter is significantly lower than its counterparts. Moreover, unlike other networks, higher values of δ do not lead to significant increase of SDP. Figure 6d illustrates SDP at $\delta = 5$, making it clear that the proposed converter has much lower SDP at high boost factors. It confirms that the proposed converter is more suitable for high-gain applications. Also, it offers reduced power handling requirements and consequently reduced costs and losses on the switching devices.

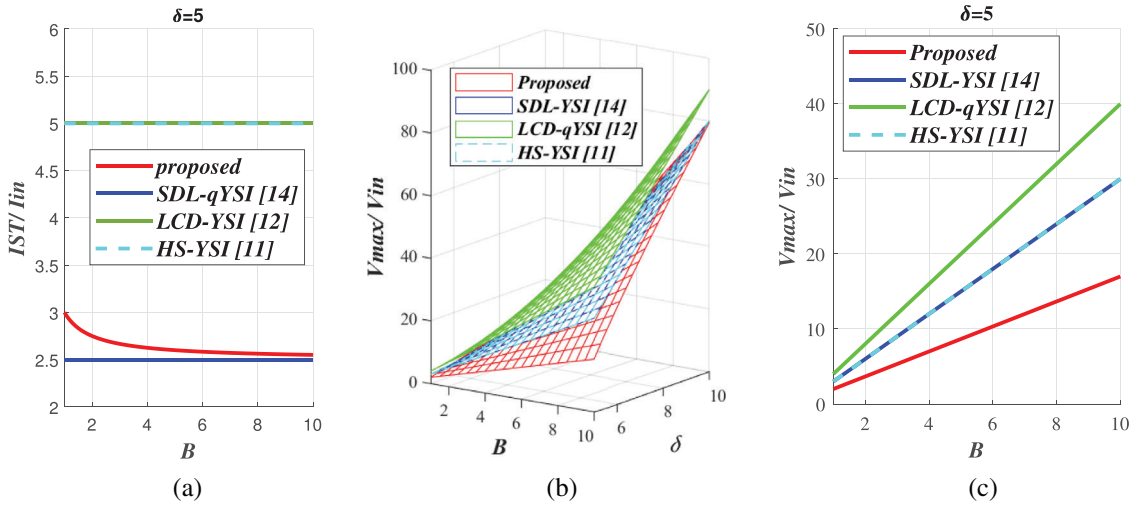

FIGURE 5 | (a) ST current at $\delta = 5$, (b) maximum voltage stress on semiconductors, and (c) maximum voltage stress on semiconductors at $\delta = 5$.

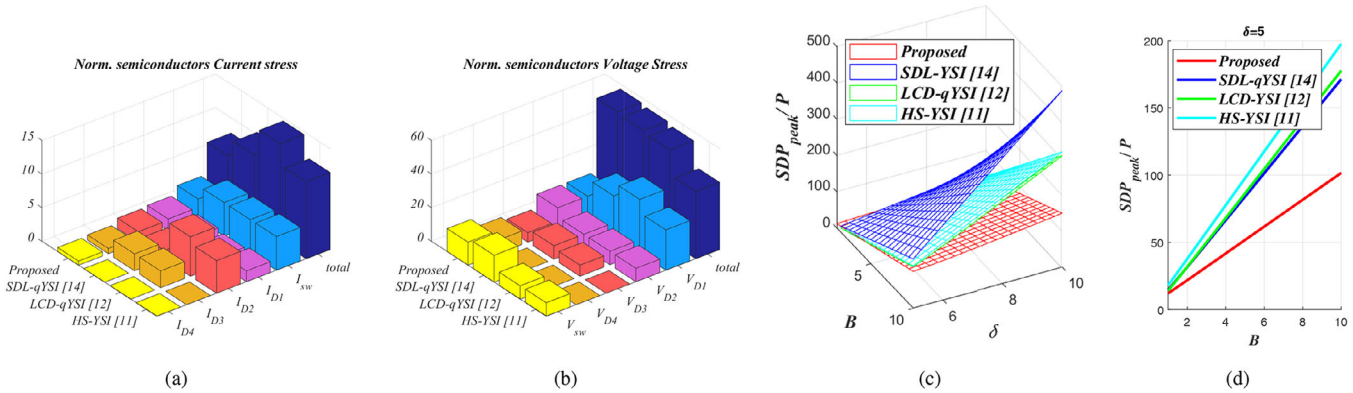

FIGURE 6 | Normalized semiconductors' (a) current stress, (b) voltage stress, (c) SDP, and (d) SDP at $\delta = 5$.

4.2 | Reactive Components

The stored energy in reactive elements is one of the main factor for comparing size and volume of power electronic converters. The normalized total stored energy of capacitors is compared in Figure 6a. The energy is calculated based on Equations (16) and (23). It shows that the proposed converter requires higher stored energy in the capacitors than SDL-qYSI. However, the main components that determine the size of passive elements in a converter are magnetic elements. One of the feature of the proposed converter is the two-winding coupled inductor. This is important because the practical procedure of building three-winding coupled inductors requires lots of precision and calculations. Unlike other MCISs based on YSI, the proposed network doesn't require complex calculations and considerations for precise turn-ratios. Moreover, the unity turn-ratio, a desirable feature for transformer design, simplifies the construction process. This, coupled with the fact that the proposed network can achieve a high voltage gain at unity turn-ratio, further highlights its advantages in high-gain applications. To compare the size of the magnetic elements, based on the method in [25] Table 2 is provided. To make a fair comparison, the Magnetics core are selected because they have wider range of sizes. Parameters of the table is calculated in the conditions mentioned in the simulation section. Also, the current ripple is assumed to be the same for all of the converters. The most important parameter is the maximum stored energy of inductors ($L(I_{L,max})^2$) which is the indicator of volume and size of magnetic components. This parameter is calculated in the first column. It shows that the least amount of energy is stored in the magnetic elements of the proposed network. Also, the Volume of core and winding is much lower than counterparts as its weight is. So, the proposed network is much superior in case of volume and size of magnetic elements.

4.3 | Effect of Parasitic Elements on Gain Characteristics

Renewable energy and EV industries demand high-voltage gains, making gain comparisons important. Also, it is the most important feature which distinguish the proposed converter. The boost factor and gain introduced in Section 2 is obtained under lossless condition. According to (20), the ideal gain can expand from zero to infinity. However, various parasitic elements restrict the voltage gain, including equivalent series resistance of the capacitors and inductors, diodes' forward voltage, and resistance in the conducting mode of semiconductors. To compare the effect of parasitic elements on voltage gain, Figure 7b is plotted based on the method in [26]. The proposed converter parasitic gain is marginally higher than others. This means that the voltage

TABLE 2 | Calculated parameters of magnetic elements.

Conv.		$L(I_{L,max})^2$ ($mH.A^2$)	Current of windings (RMS A)	Prat num. of core	Volume(mm^3)		Weight(gr)		Turns	Ku (%)	MLT (mm)
					Core	Win.	Core	Win.			
HS-YSI [21]	*Lm*	241.73	11.92:20.42:17.16	77735	91400	113481.47	482.41	871.81	70:70:140	54	135.5
	Lo	61.87	10	77212	20700	20316.17	508.91	156.08	147	33	67.25
	Lin	442.73	10	77336	220000	83032.3	450.6	637.89	314	14	124
	Tot.	746.33			332100	216829.94	1441.92	1665.78			
LCD-qYSI [22]	*Lm*	2.246	5.57:22.8:28.03	77336	220000	415278.84	1084.6	3190.35	81:324:243	54	167.5
	Lo	1.06	1.17	77210	1120	680.5	1314.28	5.23	52	30	27.8
	Lin	305.55	10	77735	91400	53735.18	1161.16	412.82	169	29	119
	Tot.	308.856			312520	469694.52	3560.04	3608.4			
SDL-YSI [24]	*Lm*	2.246	6.64:10.49:17.12	77776	43400	87726.94	229.06	673.95	44:176:88	60	126
	Lin	495	10	77336	220000	83827.35	1161.16	644	362	15	125
	Tot.	497.246			263400	171554.29	1390.22	1317.95			
Proposed	*Lm*	130.44	1005.6	77735	91400	24542.42	482.41	188.54	72:72	15	110.4
	Lin	103.67	10	77615	51800	23257.65	273.4	178.67	121	31	94.9
	Tot.	234.11			143200	47800.07	755.81	367.21			

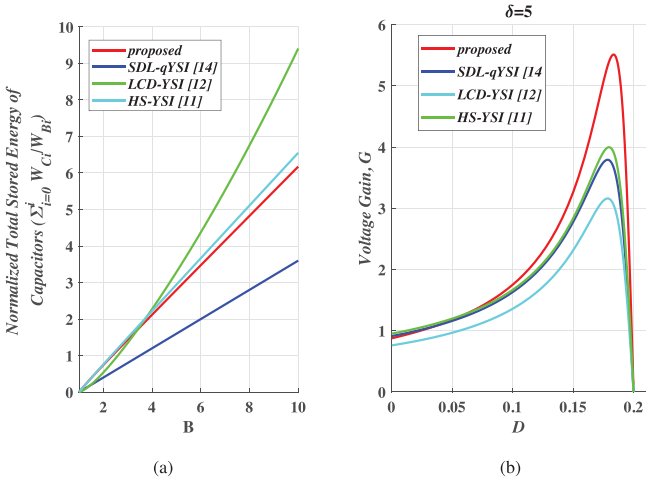

FIGURE 7 | (a) Normalized stored energy of capacitors. (b) Practical gain considering the effect of parasitic elements.

drop is compensated better in the proposed network compared to counterparts.

4.4 | Efficiency

Finally, efficiencies and power distribution are compared in Figure 8. For the sake of fairness, all the converters have the same parameters, the current ripple of the inductors is kept equal and the semiconductors used in all converters are the same. To achieve an output voltage of 220 Vrms with power ranging from 200 W to 500 W, the shoot-through duty cycle is adjusted. The power losses and efficiencies are calculated using the method described in [27] and [28]. As shown in Figure 8a, the proposed converter exhibits the highest efficiency. This is mainly due to the low current requirements of the semiconductors. At a 200 W load, the efficiency of the proposed converter is about 93.4%. With the increasing output power, the slope of the efficiency variation in the proposed converter is much lower compared to other, indicating that the proposed converter can be effectively utilized at higher power levels. Figure 8b depicts the distribution of power losses among different elements of the proposed converter and competitors.

5 | Small Signal Model

The dynamic behaviour of the proposed converter is presented by the small-signal model of the circuit. To do so, the model is approximated by the method presented in [29]. This technique models the diodes and switches as dependent voltage or current sources, as shown in Figure 9a. These sources are obtained based on the parameters of Table 1, applying KVLs and KCLs to the circuit results in the transfer function of the duty cycle to C_3 voltage, $G_{Vc3-d}(s)$, while the input voltage deviations are neglected. This transfer function is given in (25) and plotted in Figure 9b. Simulations with MATLAB/Simulink confirm the accuracy of the transfer function. This transfer function can be used for dynamic analysis and control design.

$$G_{v_{C3}-d}(s) = \frac{\tilde{V}_{C3}}{\tilde{d}} = \frac{-255.7s^7 - 3.43e07s^6 - 1.67e12s^5 - 3.8e16s^4 - 4.11e20s^3 - 3.76e23s^2 - 5.18e26s + 2.92e28}{s^7 + 8.81e04s^6 + 2.79e09s^5 + 4.46e13s^4 + 2.24e17s^3 + 2.48e20s^2 + 3.48e23s + 3.81e25} \quad (25)$$

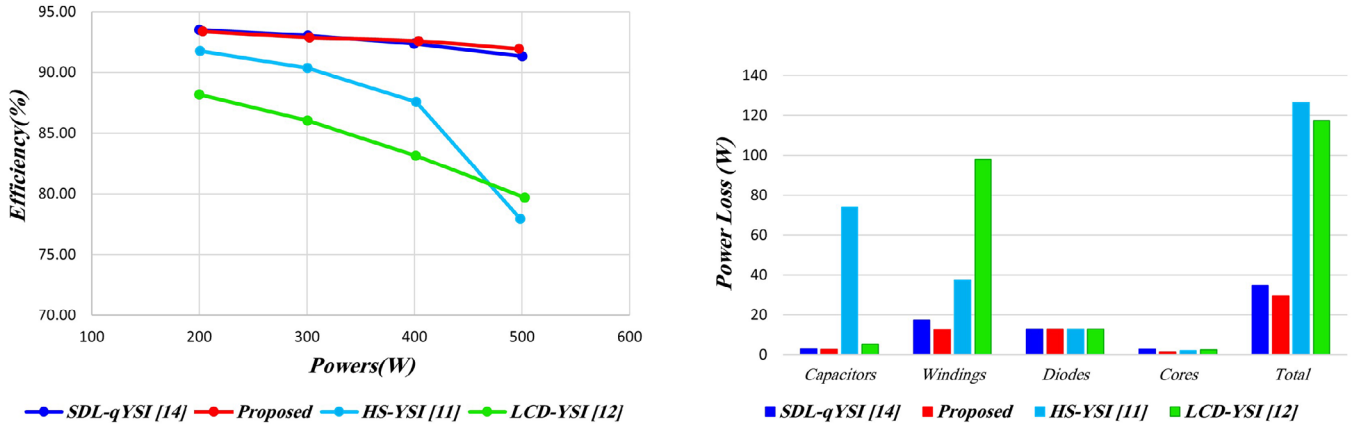

FIGURE 8 | Power analysis: (a) efficiency and (b) power distribution at 500 W.

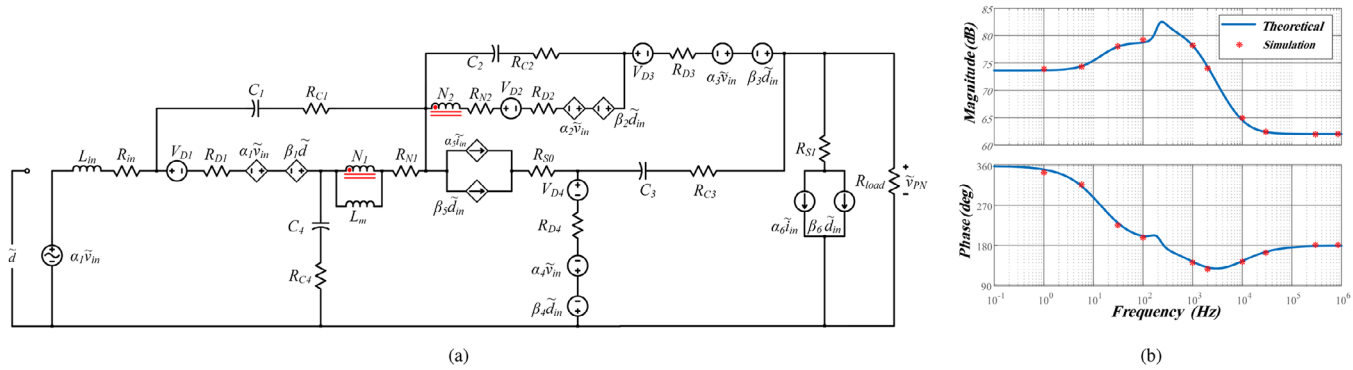

FIGURE 9 | (a) AC small signal model, and (b) Bode diagram of the proposed converter.

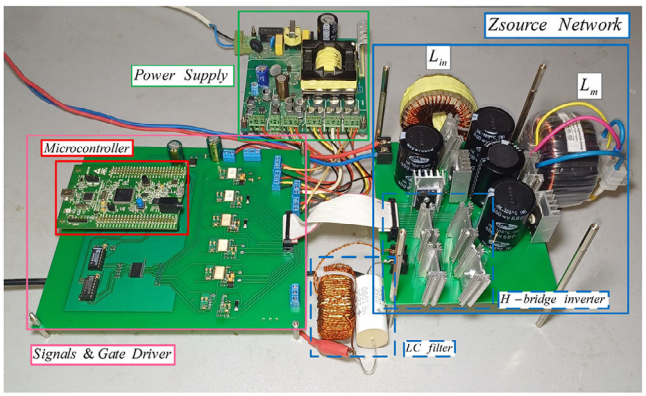

FIGURE 10 | Laboratory experimental setup.

where the values with a ~ are perturbations around the operation point.

6 | Experimental Verification

To validate the operation of the proposed converter, a 500 W prototype was implemented using the parameters in Table 3. The experimental setup is depicted in Figure 10. The required gating signals are generated by an STM32F407-VG microcontroller. An LC filter smooths the H-bridge output voltage [30]. To mitigate the 2ω ripple of the inverter, sufficiently large capacitors were used. Considering parasitic components, a practical duty cycle slightly

TABLE 3 | Experimental parameters.

Power		500 W
Load voltage		220 Vrms & 50 Hz
Source voltage		50 VDC
Carrier frequency		20 kHz
L_{in}		900 μH & 128 mΩ
L_m		400 μH
Magnetic cores of L_{in}, L_m		0077615, 0077735
Turn ratio N_1 : N_2		72:72
R_{N1}:R_{N2}		84:140 $m\Omega$
Capacitors		680 μF / 400V & 36 $m\Omega$
Switches		IGW75N60H3
Diodes	D_1, D_2	DSEP30-06A
	D_3, D_4	STTH6003CW
Filter inductor		1 mH & 50 mΩ
Filter capacitor		25 μF & 30 mΩ

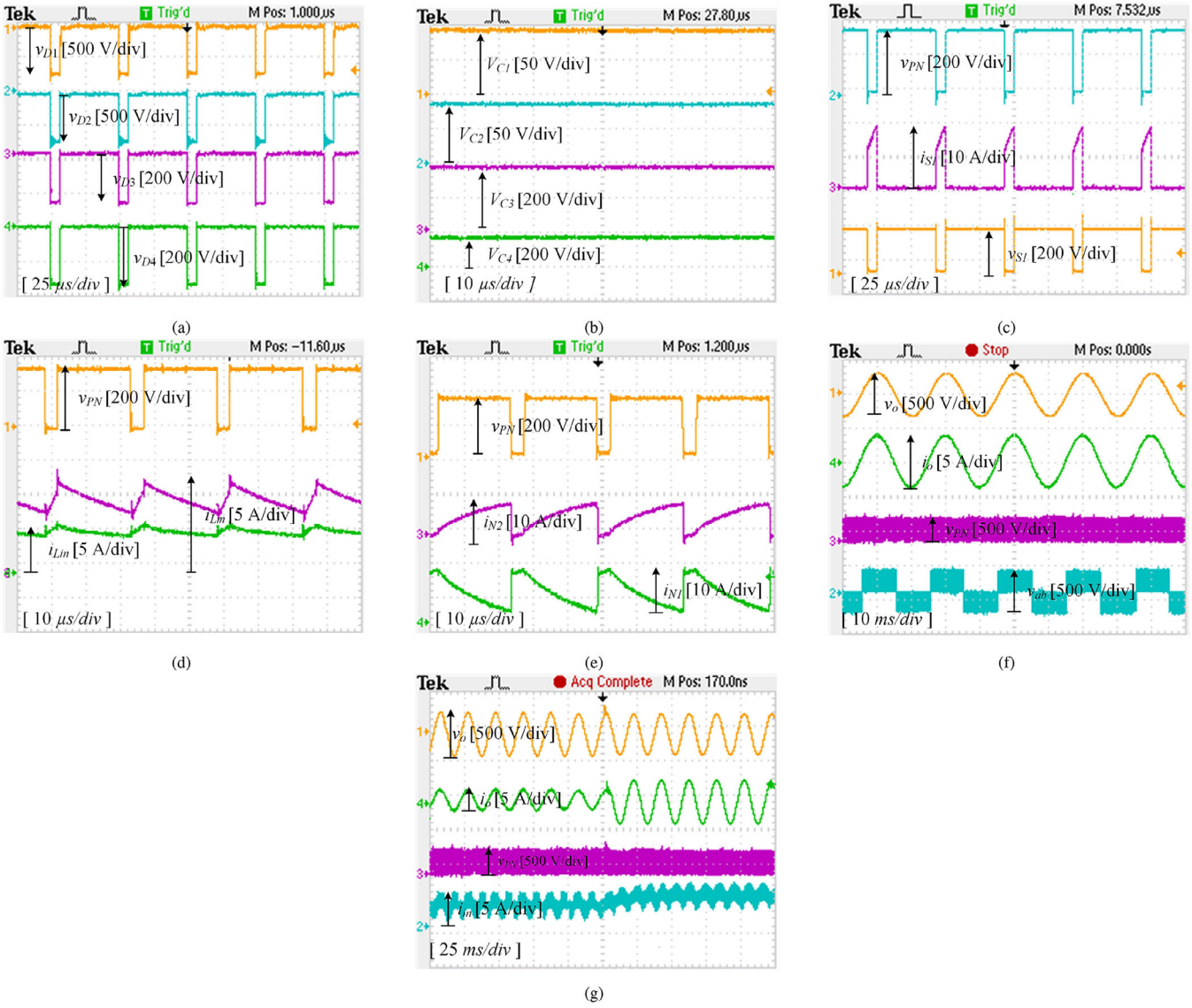

FIGURE 11 | Experimental waveforms of the proposed converter: (a) diodes voltages, (b) capacitors voltages, (c) voltage and current of the switch and DC-link voltage, (d) magnetizing and input currents, (e) windings currents, (f) output voltage and current, and (g) power step change.

larger than the calculated value was chosen. By setting the duty cycle to 0.146, the desired output voltage is achieved at nominal power, corresponding to a modulation index of 0.854. As a result, the output voltage is 220 Vrms.

Key experimental waveforms are presented in Figure 11. Figure 11a shows the diode voltages, where all diodes block during the ST state. Figure 11b confirms that capacitors effectively clamp other semiconductors, mitigating spikes and resonances. Figure 11c illustrates the voltage across the switches and DC-link, along with the current through S_1. During the NST state, S_1 turns off, forward-biasing the diodes, which then conduct. Notably, the only observed resonance involves the coupled inductor's leakage inductance and the capacitance of D_2, causing ringing exclusively on this voltage. To highlight this behavior, no snubber circuit was used in the setup; however, a small RC snubber can effectively suppress this ringing. These results align with the theoretical values in Table 1. The DC-link voltage is approximately 370 V, yielding 220 Vrms at the output.

Figure 11d presents the input and magnetizing currents, which charge during ST states and transfer energy to the load during NST states, as discussed in Section 2. The winding currents are shown in Figure 11e. During ST states, the first winding current increases linearly, energizing the magnetizing core, while the second winding current remains zero. A slight variation occurs at the start of the ST states, verifying theoretical analysis and having negligible impact on the waveforms. In NST states, i_{N1} decreases linearly while i_{N2} increases, with the first winding clamped by C_1 and the second by C_2. Thus, winding currents change almost linearly, with no significant spikes.

The inverter and load output waveforms are shown in Figure 11f. The simple boost technique achieves the desired DC-link voltage, approximately equal to the voltage across C_3. The DC-link remains smooth, eliminating the need for a snubber circuit. The AC voltage total harmonic distortion (THD) is about 3.69%, indicating a high-quality sinusoidal waveform. These steady-state waveforms closely match the theoretical waveforms in Figure 2.

To evaluate the effect of changing load, Figure 11g is presented. A step change in load power from 300 W to 500 W is applied, demonstrating that the converter provides a fast and smooth transient response.

7 | Conclusion

A new MCIS inverter is proposed, featuring a coupled inductor with clamped windings that reduces the effect of leakage inductance, which minimizes voltage spikes. Compared to competitors, the inverter lowers ST requirements and semiconductor currents while enhancing power density and efficiency. Efficiency diagram reveals that the inverter maintains an efficiency of 93.4% at a 500 W load with only a minimal efficiency drop of around 2% under peak operating conditions, in contrast to larger declines observed in competing designs. It achieves high-voltage gain even with a unity turn ratio, ideal for high-gain applications. Additionally, the two-winding coupled inductor results in lower copper losses and simpler fabrication, all within a compact structure that is half the size of the nearest competitor. Testing on a 500 W setup confirms the theoretical analysis and practicality of the clamped quasi-Z-source inverter.

Author Contributions

Ahmad Mahdave: conceptualization, formal analysis, methodology, validation, visualization, writing – original draft, writing – review & editing. **Mohammad Monfared**: conceptualization, methodology, project administration, resources, supervision, validation, writing – original draft, writing – review & editing. **Ali Nikbahar**: methodology, validation, writing – original draft. **Wahid Eskandary**: methodology, validation, visualization, writing – original draft.

Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

Data are available on request from the authors.

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