ADVANCED PHYSICS RESEARCH
Open Access
www.advphysicsres.com

GaAs Growth on Ge-Buffered Discontinuous (111)-Faceted V-Groove Silicon Substrates

Makhayeni Mtunzi, Hui Jia,* Mateus G. Masteghin,* Yaonan Hou, Haotian Zeng, Huiwen Deng, Jae-Seong Park, Chong Chen, Jun Li, Xingzhao Yan, Ilias Skandalos, Frederic Gardes, Mingchu Tang, Alwyn Seeds, and Huiyun Liu*

The propagation of antiphase boundaries (APBs) and threading dislocations (TDs) poses a significant impediment to the realisation of high-quality group III–V semiconductors grown on group IV platforms. The complete annihilation of APBs and a substantial reduction in threading dislocation density (TDD) are essential for achieving high-efficiency III–V devices compatible with complementary metal-oxide semiconductor (CMOS) technology. In this study, a novel growth technique is proposed and developed to fabricate a faceted germanium (Ge) buffer on a discontinuous (111)-faceted V-groove silicon (Si) substrate with a 500 nm flat ridge width. Subsequently, a GaAs buffer is grown on the Ge/V-groove Si virtual substrate using a ramped temperature growth process to minimise the prevalence of line and planar defects in the buffer structure. An APB-free GaAs buffer is successfully achieved, as confirmed by cross-sectional and plan-view transmission electron microscopy (TEM) and atomic force microscopy (AFM) analyses. The faceted Ge buffer layer obtained through this innovative approach alleviates the stringent fabrication requirements and intricate processing typically associated with conventional continuous V-groove Si substrates. This advancement facilitates the development of photonic integrated circuits by providing a simplified and efficient alternative substrate solution.

1. Introduction

Currently, the need for high-performance light sources that can be efficiently coupled to Si-based photonic integrated circuits is of great interest and demand.[1–3] The monolithic integration of direct-bandgap III–V lasers onto Si substrates has emerged as a promising and cost-effective long-term solution, combining the superior optoelectronic properties of III–V materials along with the well-established, low-cost fabrication processes inherent to Si technology. GaAs-based laser devices utilising quantum dot (QD) structures have for many years been developed for O-band emission in telecom applications.[4–6] However, the inevitable emergence of defects resulting from the lattice mismatch between GaAs and Si of 4% can result in threading dislocation densities (TDDs) on the order of 10^9 cm^{-2} when left untreated. As noted extensively in the literature, Ge can serve as a mediator between the

M. Mtunzi, H. Jia, H. Zeng, H. Deng, J.-S. Park, C. Chen, J. Li, M. Tang, A. Seeds, H. Liu
Department of Electronic and Electrical Engineering
University College London
Torrington Place
London WC1E 7JE, UK
E-mail: makhayeni.mtunzi.20@ucl.ac.uk; hui.jia@ucl.ac.uk

M. G. Masteghin
Advanced Technology Institute
University of Surrey
Guildford, Surrey GU2 7XH, UK
E-mail: matmas@dtu.dk

M. G. Masteghin
DTU Nanolab
Technical University of Denmark
Fysikvej
Kongens Lyngby 2800, Denmark

Y. Hou, X. Yan, I. Skandalos, F. Gardes
Optoelectronics Research Centre
University of Southampton
Southampton SO17 1BJ, UK

Y. Hou
Department of Electronic and Electrical Engineering
Bay Campus
Swansea University
Swansea SA1 8EN, UK

Y. Hou
Centre for Integrative Semiconductor Materials (CISM)
Swansea University
Bay Campus
Swansea SA1 8EN, UK

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/apxr.202500026

DOI: 10.1002/apxr.202500026

strain-induced heteroepitaxy of GaAs and Si, where there is a lattice mismatch of less than 0.1% between GaAs and Ge.[7,8] While this significantly reduces threading dislocations (TDs), it does not address antiphase boundaries (APBs), which often necessitate the use of offcut Si substrates to eliminate APBs at the interface.[9] Due to them being 2D planar defects, it is a necessity that they are eliminated entirely before propagating into the active region where they would seriously affect carrier flow and overall quantum efficiency of the eventual device.[10,11] To solve such an issue, methods include using substrates with offcuts of more than 4°[12,13] which possess double atomic steps but such substrates are not compatible in complementary metal-oxide semiconductor (CMOS) foundries which require (100) on-axis substrates with maximum offcut errors of ±0.5°.[14] For untreated Si substrates, monatomic steps exist in the form of alternating (1 × 2) and (2 × 1) dimerizations. It has however, been detailed that for large offcut substrates, an individual (2 × 1) single domain Si surface can be achieved through thermally induced surface reconstruction.[15] For such a case, each terrace consists of parallel Si–Si dimers, which also exhibit the necessary double atomic steps required to prevent APB formation. Monatomic Si steps typically form with alternating dimers. However, on substrates with an offcut toward the [110] crystallographic direction, double atomic steps become energetically favourable. A more promising and recently demonstrated technique is to form an alternating array of monoatomic S_a and S_b steps where the subsequent GaAs buffer recipe can be tailored in order to ensure the self-annihilation of periodically formed APBs at each step edge, thereby ensuring an APB-free surface on an on-axis Si substrate.[16] In addition, a ramped GaAs growth process is crucial to "kinking" APBs from their preferred (110) propagation planes to higher planes such as (111), (112), and (113) planes where, similarly with TDs, the mutual interaction can halt their motion.[17] However, a more concrete understanding of the formation of periodic monatomic Si steps is necessary for both replication and optimisation.

Conversely, the V-groove technology leverages the offcut substrate's capability to prevent APBs while being fabricated onto on-axis substrates. Numerous examples in the literature demonstrate the utilisation of V-groove substrates to fabricate APB-free III-V materials through metal–organic chemical vapor deposition (MOCVD).[18–21] Notably, recent work has demonstrated a similar outcome using all-MBE (molecular beam epitaxy),[22] by using U-shaped Si substrates that evolved into V-groove structures during growth. When considering III–V on group IV heteroepitaxy, the crystallographic orientation of the (111) plane ensures that in theory, the APB does not form.[23] Even with the existence of monatomic steps, which on the (111) plane have heights of ≈0.31 nm, the alternating array of group III and group V atoms can be maintained. Whilst the V-shape forms as a result of the slow etching rate of the (111) plane, achieving sharp, continuous facets remains a challenge.[24,25] Besides, other facet planes can also provide the required offcut to hinder APB formation. Lu et al.[26] demonstrated APB-free GaAs on a thin sandwiched (113)-Ge buffer. First, a GaAs buffer is grown on a (113)B GaAs substrate. The facet offcut is maintained through the initial GaAs buffer, after which a Ge layer is then grown. The thin Ge was shown to maintain the (113) facet, which then enabled an APB-free GaAs layer on top. Zhang et al.[27] also used (113)-faceted Ge grown above a U-shaped Si substrate to achieve APB-free GaAs. In recent work, Mtunzi et al.[28] observed how the facet shape of a Ge buffer is related to the substrate geometry and the growth temperature. It discussed the possibility of using the V-groove substrate to achieve low TDD and flat group IV structures, as well as its potential use for APB-free III-V/IV heteroepitaxy. To maintain the V-groove facet necessary for APB-free III–V growth, the growing Ge buffer must maintain the inclined facet shape. Additionally, the mismatch between Si and Ge will predictably result in a large number of defects, but with the known advantages of V-groove substrates, particularly in regard to their aspect-ratio-trapping (ART) capabilities, the TDD can be mitigated to some extent.[18,28,29] By exploiting these advantages, V-groove technology enables the fabrication of both low defect density and APB-free thin films on the same substrate, offering a cost-effective solution for industrial applications.

In this study, we report on the systematic development of single-domain GaAs on Ge-buffered V-groove Si. The prevalence of defects in the buffer structure was investigated with particular attention to the suppression of APBs using a faceted Ge buffer. A 300 nm two-step Ge buffer was deposited on the discontinuous V-groove Si substrate prior to the growth of a thick GaAs buffer. The effect of temperature and V-groove size on the growth of the Ge buffer was explored in detail. Substrate chips are patterned with five different V-groove sizes to evaluate growth quality across varying geometries on the same wafer. With the substrate itself being on-axis, this approach offers an exciting future prospect for the development of CMOS-compatible Si-based devices. The subsequent GaAs buffer growth highlights the influence of the underlying Ge facet shape and the V-groove substrate geometry on TD and APB behaviour. High-quality cross-sectional transmission electron microscopy (TEM) scans reveal the behaviour of line- and planar-defects near and at each relevant heterointerface. Ultimately, an APB-free GaAs buffer was grown on an on-axis Ge/Si virtual substrate. Further characterisations include atomic force microscopy (AFM), cross-sectional scanning electron microscopy (SEM) and plan-view election channelling contrast imaging (ECCI). Lastly, energy dispersive X-ray spectroscopy (EDS) mapping was conducted to observe the quality of the interfaces as well as the degree of intermixing with respect to atomic concentration across a defined area of the buffer.

2. Experimental Section

A standard 8-inch on-axis Si (100) wafer was used to fabricate the V-grooved Si wafer. To begin with, a 100 nm SiO_2 hard mask was deposited using plasma-enhanced chemical vapour deposition (PECVD). Five differently sized grating patterns with dimension intervals of 150 nm were etched onto the SiO_2-coated wafer via deep ultraviolet lithography (DUV). Each grating measures 12 mm in length with widths of 350, 500, 650, 800, and 950 nm. Fluorine-based inductively coupled plasma (ICP) dry etching was then used to etch the SiO_2 layer, with the photoresist subsequently eliminated using wet chemical cleaning and plasma ashing. The V-grooved Si was achieved through room temperature wet etching in a 25% tetramethylammonium hydroxide (TMAH) solution, with a preliminary 10-s hydrofluoric acid (HF) (20:1)

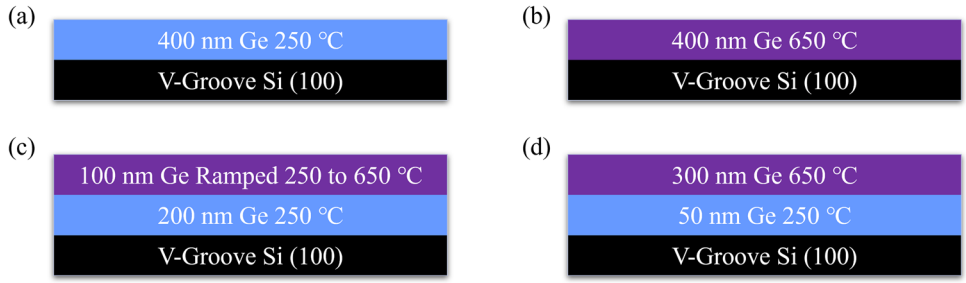

Figure 1. Ge buffer schematics for Samples A-D.

treatment to eliminate native oxide layers. Ref.[28] displays an SEM image of the V-grooves in a 45° tilted view, showing the substrate geometry for the 950 nm ridge width dimension for reference. The (111)-faceted V-groove shape is formed by selective etching on (100) and (111) planes. However, the ridges between them align with the (100) plane. The 8-inch wafer was then cleaved into 2.1 cm^2 dies prior to being loaded into the MBE system for further growth.

The growths were conducted inside a Veeco Gen 930 solid-source MBE system. Each sample was degassed for 1 h at 600 °C and deoxidised at 1000 °C for 20 min to remove surface contaminations and the native oxide. Samples A, B, C, and D represent the four different Ge buffer structures that are investigated, as depicted in **Figure 1**. Sample A employs 400 nm deposition of Ge using both a low-temperature (LT) and a low growth rate of 250 °C and 0.5 Å s^{-1}, respectively. Sample B uses the same thickness of 400 nm but was grown with both a high-temperature (HT) and a high growth rate of 650 °C and 1.5 Å s^{-1}, respectively. Sample C is a 300 nm thick structure which first uses a 200 nm LT nucleation layer grown using a growth rate of 0.5 Å s^{-1}, followed by a 100 nm thick layer which was ramped from LT to HT using 250 to 650 °C, respectively, with a growth rate of 1.5 Å s^{-1}. Lastly, Sample D employs a 50 nm thin nucleation layer grown at a LT of 250 °C with a growth rate of 0.5 Å s^{-1} with an additional 300 nm thick layer grown at 650 °C using a growth rate of 1.5 Å s^{-1}.

After the Ge buffer investigation, a thick GaAs buffer structure with a total thickness of 1.27 µm was grown on a Ge/Si virtual substrate based on Sample C due to having the clearest facets. As detailed later, the GaAs structure begins with migration-enhanced epitaxy (MEE) of alternating Ga and As, depositing the first initial 5 nm of GaAs onto the Ge buffer at a LT of 400 °C with a low growth rate of 0.1 ML s^{-1}. This technique enables LT growth while ensuring a uniform surface morphology across the Ge buffer, which is essential to minimizing interdiffusion and preventing defect generation.[30,31] The main buffer was grown using a ramped temperature growth process from 400 to 600 °C using a growth rate of 0.6 ML s^{-1} to prevent the thermodynamic equilibrium of APBs and reduce the surface roughness from the undulating Ge/Si virtual substrate.

AFM in tapping mode was performed to show the surface morphology of the GaAs buffer using a Veeco Dimension 3100. SEM and ECCI scans were performed using a Focused Ion Beam Zeiss XB1540 Crossbeam to visualise the cross-section of the Ge buffers and the surface of the GaAs, respectively, using a 30 µm aperture and an electron high tension (EHT) of 30 kV.

A scanning electron and a focused ion beam (FIB) dual-beam microscope, Tescan FERA3, were used to prepare the TEM lamellae with sub-100 nm thickness. A single-charged xenon (Xe^+) beam accelerated at 30 keV was used for the lift-off and course milling, followed by a progressive decrease of the acceleration voltage and beam current for finer polishing. TEM and scanning TEM (STEM) analyses were conducted in a Talos F200i accelerated at 200 keV and a double-aberration corrected Spectra Ultra accelerated at 300 keV, both from Thermo Fisher Scientific. Higher resolution probe-corrected STEM images were acquired in the Ultra with <150 pA screen current. EDS analysis was carried out in the Talos with increased screen current to improve signal collection in the Bruker X-Flash detector.

3. Results and Discussion

3.1. Ge Buffer Growth Morphology

The first investigation assesses the growth evolution of each Ge buffer to examine the surface morphology, for which results are shown in **Figure 2**. Each sample was evaluated on its ability to achieve inclined facets, which are required for preventing APBs. Sample A, employing 400 nm of Ge growth, shows, as expected, a buffer surface which appears to closely resemble the V-groove substrate underneath for all groove sizes owing to the reduced mobility of the Ge atoms during LT deposition. A well-defined facet shape is necessary to prevent the formation of APBs, which is the main limitation to Sample A due to the maintained (100) surface in between facet walls, which has widths identical to its respective V-groove substrate size. Sample B was grown exclusively at HT and shows more variation across the different widths. For smaller grooves, 350–650 nm, the surface appears to be flat with some slight undulation for the 650 nm size. It is thought that for these sizes, the grooves are well-covered and filled before 400 nm of deposition, therefore allowing the flattening process to occur prior to the termination of growth. The Ge facet shape is seen to be most distinct at larger dimensions (≥800 nm) using this growth process. At 800 and 950 nm, the peaks and troughs match those of the Si substrate beneath. The growing surfaces within the grooves likely meet each other and coalesce above the flat region of the V-groove substrate, thereby maintaining the periodic undulating surface. The width of the (100) regions between facets also increases for larger sizes. These gaps are then likely to serve as sites for APB formation. For large V-groove patterns, it is reasonable to believe the groove depth

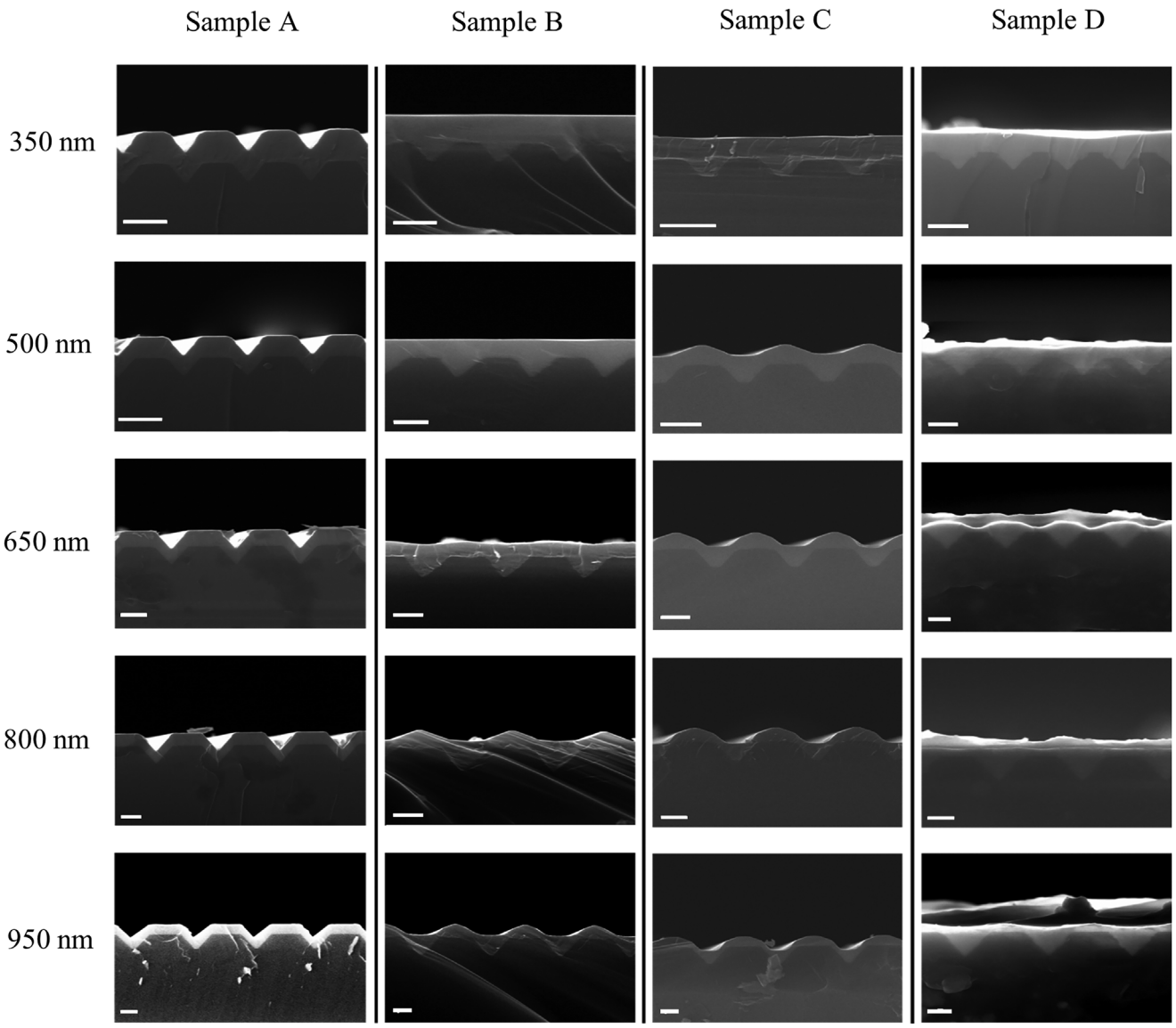

Figure 2. Variations in the Ge buffer surface are depicted for each Sample (A, B, C, and D) with respect to the flat ridge dimension size of the V-groove Si substrate. Based on the requirements for a well-faceted Ge/Si virtual substrate, the 500 nm ridge width for Sample C is ideal. Each scale bar represents 500 nm.

helps to maintain surface morphology in the form of a faceted buffer shape. Moreover, after coalescing above the ridges, the HT can encourage rounding of the peaks, providing the surface with varying facet shapes.

In Sample C, only the 350 nm size shows a flat surface, whilst the remainder have facets of varying degrees, likely due to the 350 nm size having a shallower groove depth. This sample employs a 200 nm LT layer followed by a 100 nm layer ramped from LT–HT. The ramped layer seeks to provide a more gradual shape change and rounding of the facet. Among all samples, the facet shape above the 500 nm width in Sample C demonstrates the most desirable geometry for subsequent GaAs growth. Its steady incline and minimal (100) regions are crucial parameters for preventing APBs. For larger sizes, > 500 nm, the gaps between each facet and unevenly rounded edges remain undesirable as they will likely facilitate defect formation. Lastly, Sample D primarily shows flat surfaces for all groove sizes due to prolonged HT growth, except for the 650 nm size. During the initial LT growth phase, a uniform coverage of Ge is deposited as in Sample A. As the temperature increases, Ge atoms move into the grooved areas to even out the buffer surface. This is indicated by the Ge facets for 650 nm size showing peaks above the grooves but troughs above the (100) flat surface, suggesting the flattening process is not yet complete. From these observations, the growth sequence for Sample C provides the best buffer shape for subsequent GaAs growth. Its combination of facet inclination and reduced (100) area makes it suitable for suppressing APBs. These results highlight the critical role played by groove dimensions and growth temperature in the morphology of the growing faceted Ge buffer.

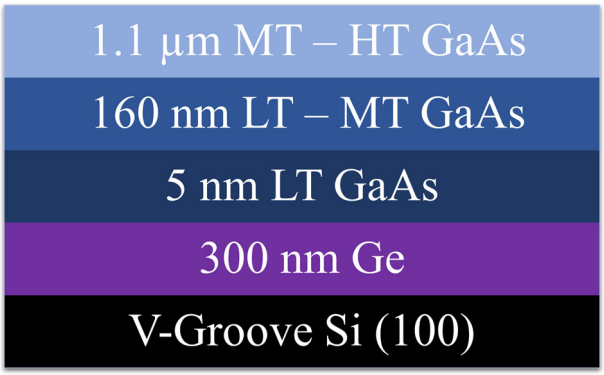

Figure 3. Schematic for the GaAs/Ge/V-groove Si buffer.

3.2. GaAs Buffer on (113)-Faceted Ge/Si Virtual Substrate

The Ge buffer with a 500 nm width in Sample C appears to closely resemble (113) facets, in contrast to the (111) facets of the underlying substrate. However, each facet is connected by a small (100) surface (≈20 nm) where APBs are most likely to form and propagate upward. This highlights the need for an appropriately designed GaAs buffer as depicted in **Figure 3**. The inclusion of mid-to-high temperature ramping has been shown to be a key factor, effectively changing the index plane of such defects and thereby causing their mutual self-annihilation.[17]

Following the growth of the GaAs buffer, the formation of defects can first be considered at each heterointerface. Notably, an array of misfit dislocations (MDs) is observed at the Ge/Si interface, as in **Figure** 4a. This is to be expected due to the large lattice mismatch of ≈4%. The misfit strain fields can also be seen by the rounded black and white areas of contrast. Furthermore, additional relaxation is provided via the formation of TDs, which travel in their typical (111) plane in the [110] direction. These defects can be seen penetrating through into the Si substrate, but the symmetric nature of their travel ensures their quick annihilation. The inclusion of thermal cyclic annealing (TCA), which is commonly employed in Ge buffer growth[32,33] would likely further reduce the TDD but would also simultaneously greatly impact the Ge buffer shape. Its absence likely increases the probability of defects propagating upward unless they are trapped by the grooved trench or encounter opposing defects with opposite Burgers vectors, leading to potential annihilation due to their high density. Few dislocations are observed within the V-groove area, although they appear to emerge predominantly from the corner and flat surface of the substrate. A contrast in quality is evident between the (100) and (111) planes at the Ge/Si interface. High-resolution (HR)-STEM images in Figure 4b,c provide further insight into this difference. Atomic disruption caused by minor intermixing and MDs is observed along the (100) plane, as shown in Figure 4b, while the inclined (111) facet, shown in Figure 4c, appears nearly defect-free.

Figure 5 highlights the benefit of employing various TEM imaging modes in revealing different types of defects, with certain modes enhancing the visibility of specific features more effectively than others. The zoomed-out STEM images in Figure 5a and b show the same area in bright and dark field mode, respectively. APBs are made visible by the high contrast provided by the STEM, where they appear as shaded patches. Typically, bright-field images are not ideal for highlighting APBs or TDs. However, the low convergence semi-angle on the uncorrected Talos enabled some diffraction-based contrast contribution, even at the inner part of the detector. These APBs originate at the GaAs/Ge interface where the Ge buffer has flattened, and the facets meet and round off–making a (100) surface where such defects are inevitably going to form. Smaller and infrequent regions at the troughs between the facets also show APB development but are quickly annihilated. As is expected along the Ge facet, APBs are not observable; however, inclined stacking faults (SFs) travel along guided (113) planes up to where the buffer flattens out, as labelled in Figure 5c. A close examination of two adjacent APBs above the Ge buffer shows their clear vertical component, consistent with descriptions in the literature regarding their (110) plane propagation.[34–36] They propagate upward for ≈200 nm before their directions undergo a distinct change, as depicted by the dashed red line. The change in orientation reflects their transition into higher-index planes, facilitating crucial interactions and eventual annihilation. This corresponds with the beginning of the mid-to-high temperature stage, where the volatile APB is able to overcome the energy barrier associated with additional index planes. The periodic nature of the APBs combined with the narrow widths of the antiphase domains (APDs) simplifies the process of achieving complete annihilation. Each APB has one adjacent counterpart as opposed to the randomly distributed APBs commonly seen from the on-axis system.[10,37] The APBs are subsequently eliminated through the interaction and merging of two slightly asymmetrical APBs. Self-annihilation is strongly influenced by the APB orientation, with Rubel et al.[38] previously demonstrating that the (111), (112), and (113) planes are all suitable orientations for APB annihilation. The APB formation energies of GaAs were determined to be 43 meV/Å^2 for the (111) plane and slightly lower energies of 39 meV Å^{-2} for both the (112) and (113) planes. Nevertheless, such data only alludes to the actual kinking of pre-existing APBs into higher planes as opposed to preventing their formation altogether from an inclined facet. It was their finding that kinking APBs into (112) and (113) planes is more energy efficient than into the (111) plane.

Besides the elimination of planar defects, TDs are observed to continue propagating upward, contributing to the surface defect density. The GaAs/Ge interface shows much fewer TDs emerging due to a smaller lattice mismatch of 0.08%, whilst pre-existing TDs from the Ge/Si interface are observed to continue travelling upward, although their direction of travel is occasionally altered due to the slight misfit force exerted on them at the Ge facet. Bai et al.[39] describes how "growth facets" can alter the direction of TDs and cause them to travel normal with respect to the facet. This effect is observed intermittently while other TDs continue along their original trajectory from the Ge/Si interface; on some instances forming closed loops. Some defects are seen to be trapped within the Si V-groove facet walls although it is evident that by increasing the aspect ratio, which can be defined by h/w where h is the trench depth and w is the width,[40] the substrate would exhibit more effective trapping capabilities. Figure 5d demonstrates how weak-beam dark-field (WBDF) imaging is particularly effective for visualising TDs. In WBDF, the sample is tilted to bring the 3 g diffraction spot

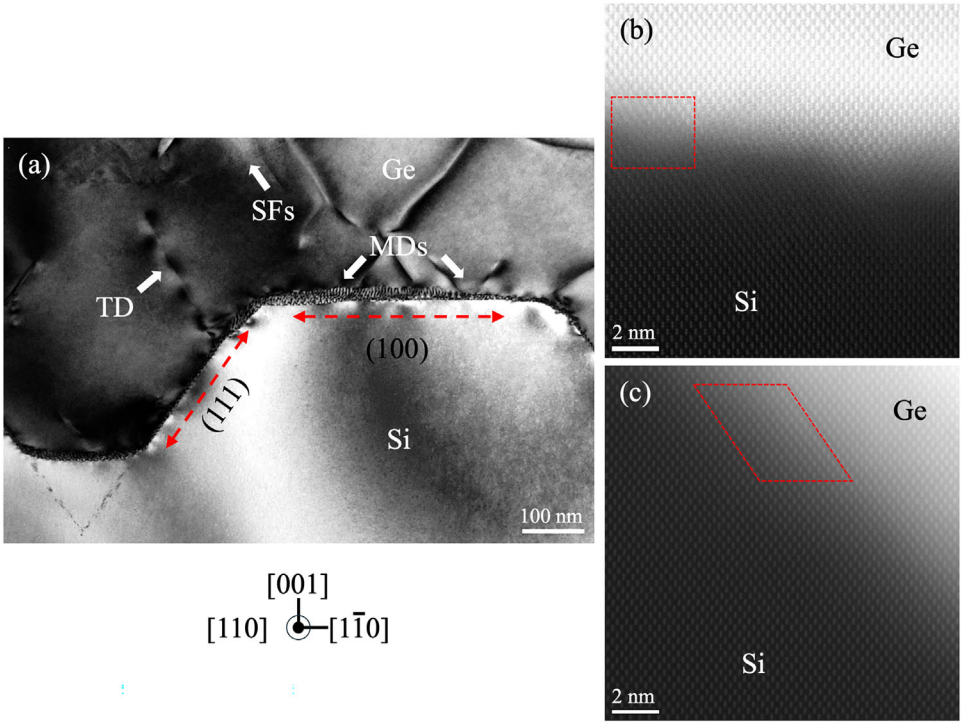

Figure 4. Cross-section high-angle annular dark-field (HAADF) STEM shows Ge/Si interface in (a) where the strain is relaxed mainly through MDs and TDs. MDs appear to exist predominantly above flat ridges on the (100) planes located between the (111) facets, as well as the flat region inside the groove. Stacking faults (SFs) are also observed along the Ge facet. b,c) present high-magnification HAADF images of the (100) and (111) interfaces, respectively, highlighting differences in crystal quality in the regions marked by the red dashed polygons.

to the Bragg condition. The first-order diffraction spot is then selected using an objective aperture, and therefore, the scattered electrons are mainly responsible for generating the image.[41,42] In contrast, for bright field scans, the direct beam is used, allowing for an overall brighter image, although weakly scattered electron beams from defects are detected less strongly, resulting in darker shading for defects. However, it can still collectively show each type of defect within the scanned area, although the resolution of smaller defects, such as MDs degrades as the scan area increases. A combination of the two modes helps provide a more holistic understanding of defect behaviour in the buffer layer.

To evaluate the effectiveness of the groove structures above the 500 nm ridge in reducing APBs, both plan-view ECCI and AFM scans were performed. A 54 μm^2 ECCI scan in **Figure 6**a reveals a TDD of 3×10^8 cm^{-2}, which is reasonable given the large surface area spanned by the GaAs/Ge/Si interfaces. The absence of any observable APBs further supports the structural quality of the layer. In this scan, TDs appear as small, highly-contrasted circular pits—two of which are circled for reference. The 10×10 μm AFM scan in Figure 6b similarly shows no visible APBs, with an RMS roughness of 6.59 nm. Bright and dark contrast variations are observed, which result from the coalescence of distinct growth domains and contribute to the overall surface roughness. While AFM can reveal TDs on smoother surfaces, the relatively high roughness here likely masks such features, preventing their clear identification. A wide-scale cross-sectional STEM in Figure S1 (Supporting Information) confirms the periodic nature of APB annihilation, showing that only TDs propagate toward the surface. A larger-scale plan-view SEM in Figure S2 (Supporting Information) presents a 46×69 μm scan highlighting the emergence of multiple hole defects, likely caused by surface perturbations from TDs, although alternative explanations have been proposed.[43–45]

Relaxation via interdiffusion is a common phenomenon in GaAs/Ge heterostructures and is highly dependent on growth temperature.[46] To assess the extent of intermixing at the III–V/IV interface, EDS mapping was performed. As depicted in **Figure 7**a,b, the smoother regions along the (113) planes suggest minimal interdiffusion and highlight the role of facet orientation in determining interface quality. Meanwhile, Figure 7c,d reinforce earlier observations from Figure 4, showing well-preserved interfaces along the (111) planes but slightly lower quality at the ridge edges and on the (100) surfaces. This can be attributed to the reduced surface energy of Si{111}, which arises from its densely packed atomic arrangement and fewer dangling bonds compared to the (100) plane.[47] The same principle applies to the (113) planes, where the lower density of dangling bonds contributes to smoother morphology. This characteristic promotes a more favourable layer-by-layer growth mode, in contrast to the dominant Stranski-Krastanov (SK) growth mode observed on the (100) plane.[48] A similar explanation can be provided for the smoother regions of the (113) planes as seen from Figure 7a,b. The atomic concentration profile across a ≈750 nm segment of the GaAs/Ge/Si buffer provides additional insight into the interface quality, as shown in the concentration graph

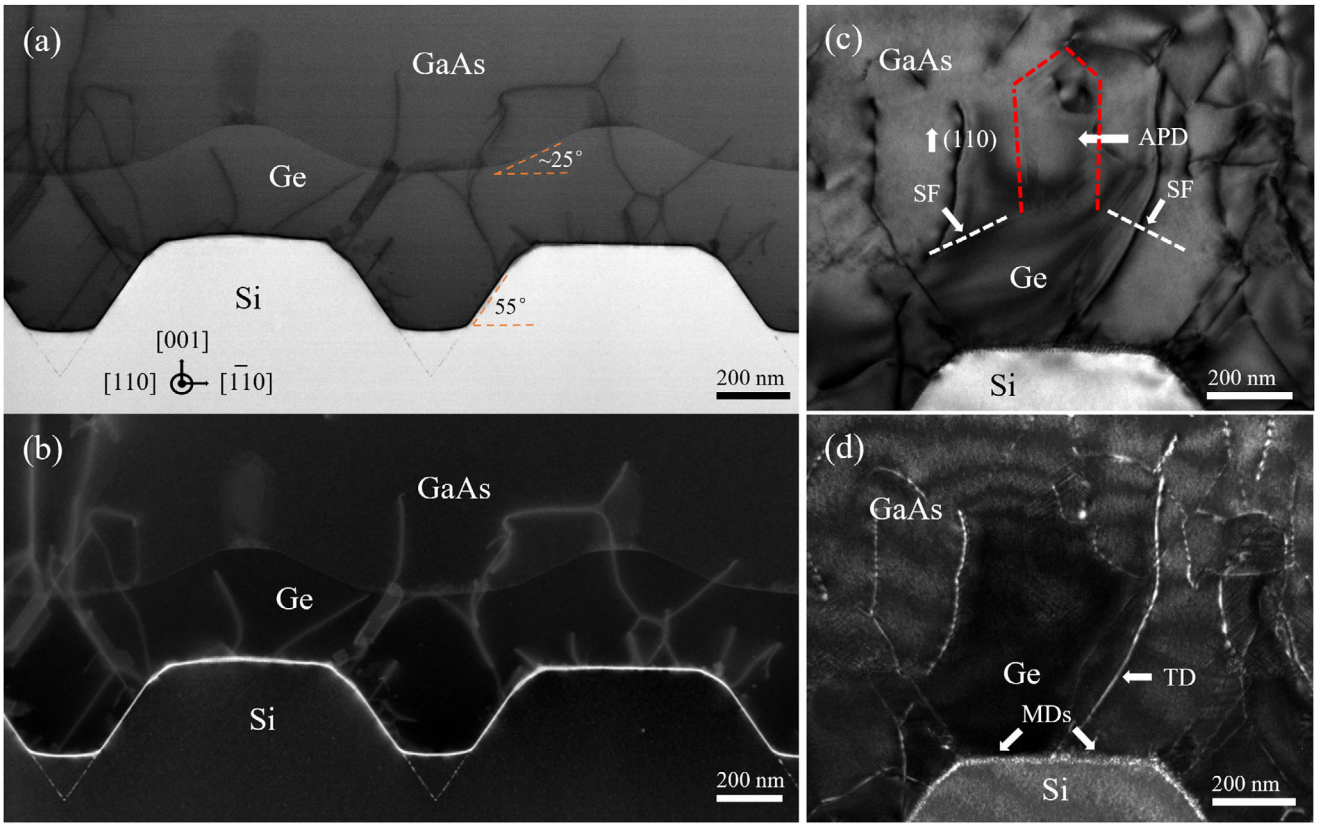

Figure 5. S/TEM images provide insight into crystal quality across each interface in various scanning modes. a,b) present bright- and dark-field STEM images of the buffer cross-section. The annotated angles of 25° and 55° reflect the (113) and (111) planes, respectively. c) encapsulates an APD above the GaAs/Ge interface as well as stacking faults following the (113) plane on both sides, viewed in TEM bright field. (d) highlights TDs and MDs under TEM weak-beam dark-field (WBDF) scanning.

in Figure 7e. The specific region scanned for this analysis is depicted in Figure S3 (Supporting Information). Abrupt changes in the percentage values indicate sharp interfaces with little intermixing. This suggests that moderately increasing the growth temperature could be a viable strategy to further reduce the TDD by enhancing the glide of glissile TDs and promoting defect annihilation, without significantly compromising the interface integrity.

4. Conclusion

In summary, we have explored the growth and development of a single-domain GaAs buffer on a Ge/V-groove Si virtual substrate with a focus on the formation of defects at each interface. The growth evolution of a Ge buffer on the discontinuous V-groove substrate was found to strongly depend on the V-groove ridge width and the growth temperature. A Ge buffer closely re-

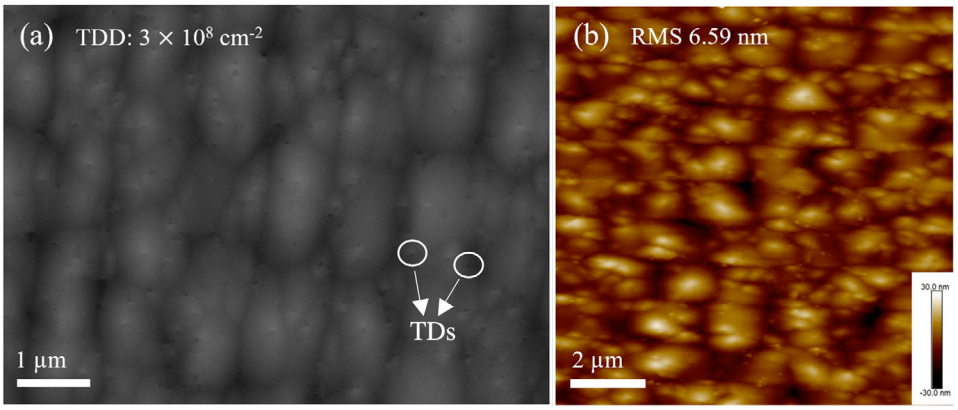

Figure 6. a,b) show the ECCI image and AFM scan for the surface of the GaAs/Ge/Si buffer, respectively. Example TDs are circled in (a).

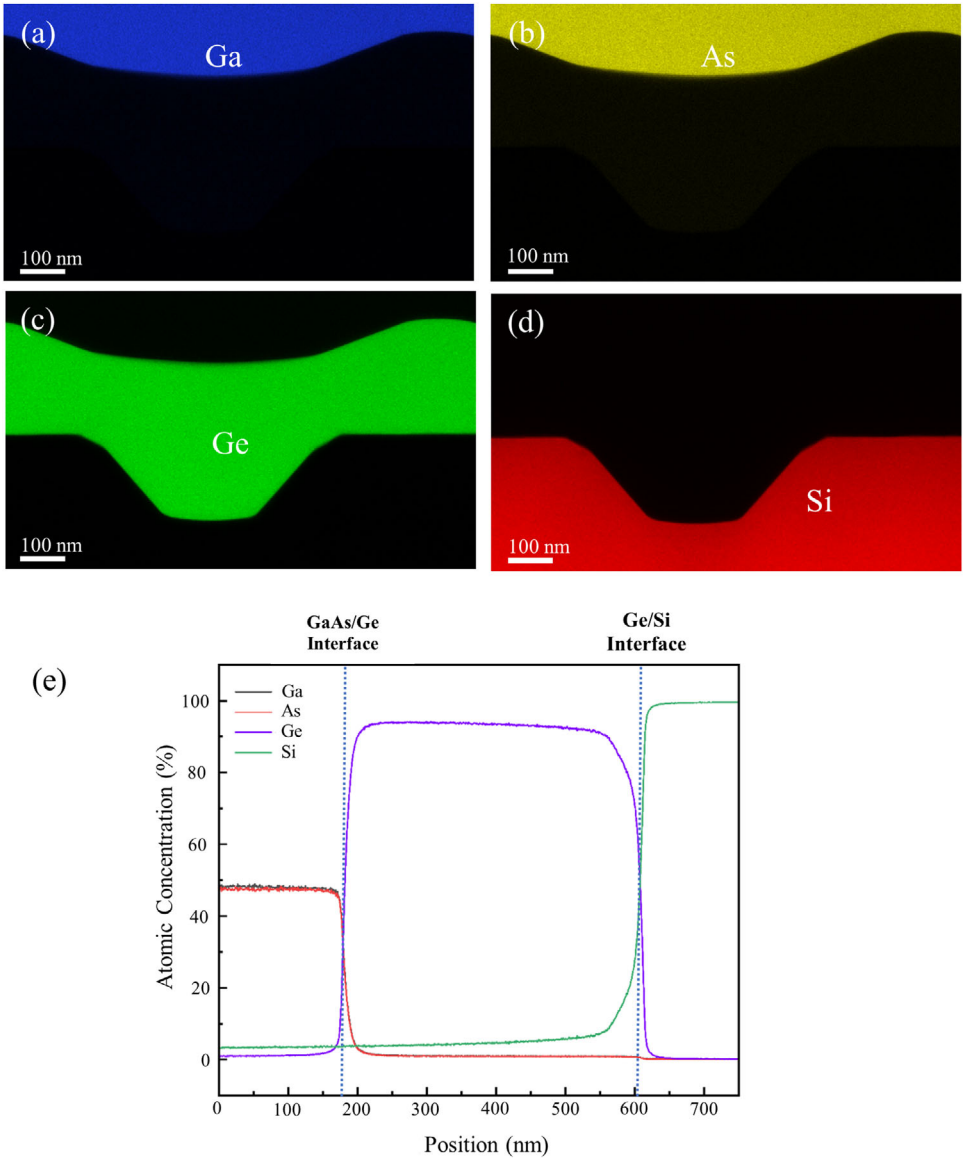

Figure 7. EDS mapping showing the material interfaces between Ga a), As b), Ge c), and Si d). The varying atomic concentration across a ≈750 nm region of the GaAs/Ge/Si is shown in (e).

sembling (113) facets that enabled the suppression of APBs was achieved. While numerous TDs originate at the Ge/Si interface due to the significant lattice mismatch, APBs are absent along the Ge facets, although they periodically appear at the flattened peaks of the Ge buffer. Cross-sectional TEM revealed the effectiveness of the growth approach in minimising defects at each heterointerface, offering valuable insights into defect engineering of III-V materials on Si substrates. The mid-to-high temperature growth regime redirects APBs traveling in the (110) plane to higher-index planes, promoting their complete annihilation. Ultimately, an APB-free GaAs buffer was demonstrated, proving the feasibility of this approach to achieve a high-quality platform for the integration of III-V photonic components onto on-axis Si substrates. These results highlight the potential for further optimising growth parameters to enhance material quality and device performance.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This work was supported by the UK Engineering and Physical Sciences Research Council (EP/Z532848/1, EP/X015300/1, EP/T028475/1, EP/S024441/1, and EP/P006973/1).

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

antiphase boundaries, aspect ratio trapping, threading dislocations, v-groove

Received: March 1, 2025
Revised: April 24, 2025
Published online:

[1] Z. Zhou, B. Yin, J. Michel, *Light: Sci. Appl.* **2015**, *4*, 358.
[2] M. Tang, J. S. Park, Z. Wang, S. Chen, P. Jurczak, A. Seeds, H. Liu, *Prog. in Quant. Elect.* **2019**, *66*, 1.
[3] Anon, *Nat. Photonics* **2010**, *4*, 491.
[4] H. Liu, T. Tang, Q. Jiang, R. Hogg, F. Tutu, F. Pozzi, A. Seeds, *Nat. Photonics* **2011**, *5*, 416.
[5] S. Chen, W. Li, J. Wu, Q. Jiang, M. Tang, S. Shutts, S. N. Elliot, A. Sobiesierski, A. Seeds, I. Ross, P. Smowton, H. Liu, *Nat. Photonics* **2016**, *10*, 307.
[6] J. Yang, Z. Liu, P. Jurczak, M. Tang, K. Li, S. Pan, A. Sanchez, R. Beanland, J.-C. Zhang, H. Wang, F. Liu, Z. Li, S. Shutts, P. Smowton, S. Chen, A. Seeds, H. Liu, *J. Phys. D. Appl. Phys.* **2021**, *54*, 035103.
[7] Y. Bogumilowicz, J. M. Hartmann, N. Rochat, A. Salaun, M. Martin, F. Bassani, T. Baron, S. David, X. Y. Bao, E. Sanchez, *J. Cryst. Growth* **2016**, *453*, 180.
[8] J. Yang, P. Jurczak, F. Cui, K. Li, M. Tang, L. Billiald, R. Beanland, A. Sanchez, H. Liu, *J. Cryst. Growth* **2019**, *514*, 109.
[9] T. Soga, H. Nishikawa, T. Jimbo, M. Umeno, *Japan J. Appl. Phys.* **1993**, *32*, 4912.
[10] R. Alcotte, M. Martin, J. Moeyaert, R. Cipro, S. David, F. Bassani, F. Ducriquet, Y. Bogumilowicz, E. Sanchez, Z. Ye, X. Y. Bao, J. B. Pin, T. Baron, *APL Mater.* **2016**, *4*, 046101.
[11] S. F. Fang, K. Adomi, S. Iyer, H. Morkoç, H. Zabel, C. Choi, N. Otsuka, *J. Appl. Phys.* **1990**, *68*, R31.
[12] M. Kawabe, T. Ueda, *Japan J. Appl. Phys.* **1986**, *25*, L285.
[13] C. Jiang, H. Liu, Z. Liu, J. Ye, H. Zhai, S. Liu, J. Lin, Q. Wang, X. Ren, *Appl. Phys. A* **2024** *130*, 5.
[14] J. Dabrowski, H.-J. Mussig, *Phys. Today* **2000** *54*, 76.
[15] J. Park, M. Tang, S. Chen, H. Liu, *Nanodevices* **2021** *20*, 353.
[16] K. Li, J. Yang, Y. Liu, M. Tang, P. Jurczak, Z. Liu, X. Yu, J.-S. Park, H. Deng, H. Jia, M. Dang, A. M. Sanchez, R. Beanland, W. Li, X. Han, J.-C. Zhang, H. Wang, F. Liu, S. Chen, A. Seeds, P. Smowton, H. Liu, *Adv. Opt. Mat.* **2020**, *8*, 2000970.
[17] J. Yang, K. Li, H. Jia, H. Deng, X. Yu, P. Jurczak, J.-S. Park, S. Pan, W. Li, S. Chen, A. Seeds, M. Tang, H. Liu, *Nanoscale* **2022**, *14*, 17247.
[18] B. Shi, L. Wang, A. A. Taylor, S. S. Brunelli, H. Zhao, B. Song, J. Klamkin, *Appl. Phys. Lett.* **2019**, *114*, 172102.
[19] T. E. Saenz, J. S. Mangum, O. D. Schneble, A. N. Neumann, R. M. France, W. E. McMahon, J. D. Zimmerman, E. L. Warren, *ACS Appl. Elec. Mat.* **2023**, *5*, 721.
[20] Y. Wan, Q. Li, A. Y. Liu, A. C. Gossard, J. E. Bowers, E. L. Hu, K. M. Lau, *Opt. Lett.* **2016**, *41*, 1664.
[21] Q. Li, Y. Wan, A. Y. Liu, A. C. Gossard, J. E. Bowers, E. L. Hu, K. M. Lau, *Opt. Exp.* **2016**, *24*, 21038.
[22] W. Q. Wei, J.-H. Wang, B. Zhang, J.-Y. Zhang, H.-L. Wang, Q. Feng, H.-X. Xu, T. Wang, J.-J. Zhang, *Appl. Phys. Lett.* **2018**, *113*, 053107.
[23] Q. Li, K. M. Lau, *Prog. Cryst. Growth Charact. Mat.* **2017**, *63*, 105.
[24] I. A. Shah, *Surface Morphology of Si (111) in Alkaline Etching Solutions*, Universiteit Nijmegen, Netherlands **2011**.
[25] T. E. Saenz, W. E. McMahon, A. G. Norman, C. Perkins, *Cryst. Growth Design.* **2020**, *20*, 6745.
[26] X. Lu, N. Kumagai, Y. Minami, T. Kitada, *Appl. Phys. Exp.* **2018**, *11*, 015501.
[27] J.-Y. Zhang, W. Q. Wei, J.-H. Wang, H. Cong, Q. Feng, Z.-H. Wang, T. Wang, J.-J. Zhang, *Opt. Mat. Exp.* **2020**, *10*, 1045.
[28] M. Mtunzi, H. Jia, Y. Hou, X. Yu, H. Zeng, J. Yang, X. Yan, I. Skandalos, H. Deng, J.-S. Park, W. Li, A. Li, K. El Hajraoui, Q. Ramasse, F. Gardes, M. Tang, S. Chen, A. Seeds, H. Liu, *J. Phys. D: Appl. Phys.* **2024**, *57*, 255101.
[29] M. F. Bin Amin, J. A. Piedra-Lorenzana, K. Yamane, T. Hizawa, T. Nakai, Y. Ishikawa, *Jpn. J. Appl. Phys.* **2024**, *63*, 02SP78.
[30] H. Tanoto, S. F. Yoon, W. K. Loke, K. P. Chen, E. A. Fitzgerald, C. Dohrman, B. Narayanan, *J. Appl. Phys.* **2008**, *103*, 104901.
[31] L. Liu, Z. Deng, G. Liu, C. Kong, H. Du, R. Chen, J. Yan, L. Qin, S. Song, X. Zhang, W. Wang, *Crystals* **2024**, *14*, 421.
[32] X. Yu, H. Jia, J. Yang, M. G. Masteghin, H. Beere, M. Mtunzi, H. Deng, S. Huo, C. Chen, S. Chen, M. Tang, S. J. Sweeney, D. Ritchie, A. Seeds, H. Liu, *Sci. Rep.* **2024**, *14*, 7969.
[33] Z. Liu, X. Hao, A. Ho-Baillie, C.-Y. Tsao, M. A. Green, *Thin Solid Films* **2015**, *574*, 99.
[34] N. H. Cho, B. C. De Cooman, C. B. Carter, R. Fletcher, D. K. Wagner, *Appl. Phys. Lett.* **1985**, *47*, 879.
[35] D. Cohen, C. B. Carter, *J. Microscopy* **2002**, *208*, 84.
[36] V. I. Vdovin, M. G. Mil'vidskii, T. G. Yugova, *J. Cryst. Growth* **1993**, *132*, 477.
[37] Y. Bogumilowicz, J. M. Hartmann, R. Cipro, R. Alcotte, M. Martin, F. Bassani, J. Moeyaert, T. Baron, J. B. Pin, X. Bao, Z. Ye, E. Sanchez, *Appl. Phys. Lett.* **2015**, *107*, 212105.
[38] O. Rubel, S. D. Baranovskii, *Int. J. Mol. Sci.* **2009**, *10*, 5104.
[39] J. Bai, J.-S. Park, Z. Cheng, M. Curtin, B. Adekore, M. Carroll, A. Lochtefeld, M. Dudley, *Appl. Phys. Lett.* **2007**, *90*, 101902.
[40] J. Yang, H. Deng, J.-S. Park, S. Chen, M. Tang, H. Liu, *Thin Films – Growth, Characterization and Electrochemical Applications*, IntechOpen, London **2024**, 4.
[41] J. Miao, S. Singh, J. Tessmer, M. Shih, M. Ghazisaeidi, M. DeGraef, M. J. Mills, *Microsc. Microanal.* **2018**, *24*, 2202.
[42] J. Miao, *Microsc. Microanal.* **2020**, *26*, 1220.
[43] A. Strömberg, G. Omanakuttan, Y. Liu, T. Mu, Z. Xu, S. Lourdudoss, Y.-T. Sun, *J. Cryst. Growth* **2020**, *540*, 125623.
[44] E. Klimov, A. Klochkov, S. Pushkarev, G. Galiev, R. Galiev, N. Yuzeeva, A. Zaitsev, Y. Volkovsky, A. Seregin, P. Prosekov, *Crystals* **2022**, *13*, 28.
[45] P.-H. Wu, Y.-K. Su, L. Chen, S.-F. Chen, C.-H. Chiou, S.-H. Guo, J.-T. Hsu, W.-R. Chen, *J. Cryst. Growth* **2007**, *298*, 767.
[46] M. Bosi, G. Attolini, C. Ferrari, C. Frigeri, M. Calicchio, F. Rossi, K. Vad, A. Csik, Z. Zolnai, *J. Cryst. Growth* **2011**, *318*, 367.
[47] H. Y. Xu, Y. N. Guo, Y. Wang, J. Zou, J. H. Kang, Q. Gao, H. H. Tan, C. Jagadish, *J. Appl. Phys.* **2009**, *106*, 083514.
[48] S. N. Santalla, C. Kanyinda-Malu, R. M. de la Cruz, *J. Cryst. Growth* **2003**, *253*, 190.