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Prifysgol Abertawe

# Power MOSFET Human Body Model

# Electrostatic Discharge Analysis and Risk Mitigation

Author: - Ian Gilbert BSc (Hons)

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Supervised by

Professor Michael Jennings

Swansea University

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# Abstract

Semiconductor devices are fabricated at Vishay Newport and in particular, power MOSFETs. These power MOSFETS possesses vast income potential for the company now and in the immediate future as the devices are used in numerous electric appliances and gadgets. In the future, the market in Power MOSFETs will be expected, to generate considerable output revenues due to the increase in technologies such as artificial intelligence (AI), robotics, electric appliances, also various electrical gadgets and the growing necessity for hybrid / electric vehicles globally, the power MOSFET market is expected to increase in lucrative opportunities.

However, the devices are susceptible to Electrostatic Discharge (ESD) that can cause undesirable effects and loss of potential revenue to the company due to damage on reticle etc. or loss die on the wafer and damaged die in other company products causing these products to fail.

The intention of this thesis is to minimise the negative impact on productivity caused by static discharge in the production environment by using risk mitigation to lessen or remove the effects of ESD on reticles wafers etc., therefore increasing the “good” die on wafers so improving company output. The research conducted for this thesis is based on an interim report conducted for the company as a basis for this thesis, and also on various papers on the subjects of electrostatic discharge and the human body model.

# Declaration

This work has not previously been accepted in substance for any degree and is not being concurrently submitted in candidature for any degree.

Signed.....  .....

Date.....07/03/2024.....

This thesis is the result of my own investigations, except where otherwise stated. Other sources are acknowledged by footnotes giving explicit references. A bibliography is appended.

Signed.....  .....

Date.....07/03/2024.....

I hereby give consent for my thesis, if accepted, to be available for electronic sharing

Signed.....  .....

Date..... 07/03/2024.....

The University's ethical procedures have been followed and, where appropriate, that ethical approval has been granted.

Signed.  .....

Date..... 07/03/2024.....

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# Acknowledgements

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# Abbreviations

| | |
|---|---|
| **AC** | Alternating current |
| **AI** | Artificial intelligence |
| **ANSI** | American national standards institute |
| **B** | Body terminal |
| **BJT** | Bipolar junction transistor |
| **BT** | British Telecom |
| **CMOS** | Complementary MOS |
| **CRT** | Cathode-ray tube |
| **CDM** | Charged device model ESD. |
| **D** | Drain terminal |
| **DC** | Direct current |
| **D-MOSFET** | Depletion mode MOSFET |
| **DMOS** | Double diffused metal oxide semiconductor |
| **DUT** | Device under test DUT |
| **EMMI** | Emission microscope image |
| **E-MOSFET** | Enhancement mode MOSFET |
| **EOS** | Electrical over stress |
| **EPA** | ESD protected area. |
| **ESD** | Electrostatic discharge |
| **FET** | Field effect transistor |
| **FGMOS** | Floating gate MOSFET |
| **Fop's** | Final operations |
| **G** | Gate terminal |
| **GMe** | General micro electronics |
| **GFCI** | Ground fault circuit interrupters. |
| **HBM** | Human body model |
| **IBM** | International business machines |

| | |
|---|---|
| **IC** | Integrated circuit |
| **ID** | Drain current |
| **IEC** | The international electro technical commission |
| **IGBT** | Insulated gate bi-polar transistor. |
| **IMP** | Interplanetary monitoring platform |
| **I/O** | Input / Output |
| **JEDAC** | Joint electron device engineering council |
| **kV/cm** | Kilovolts per centimetre |
| **L** | Impedance |
| **LDD** | Lightly doped drain |
| **MISFET** | Metal insulator semiconductor field-effect transistor |
| **MOS IC** | MOS integrated circuit |
| **MOSFET** | Metal oxide semiconductor field-effect transistor |
| **MM** | Machine model |
| **MuGFET** | Multi-gate field-effect transistor |
| **NASA** | National aeronautics & space administration |
| **NiCr** | Nickel–chromium |
| **PC** | Personal computers |
| **PCB** | Printed circuit board |
| **P / N** | Positive Negative junction |
| **QFET** | Quantum field-effect transistor |
| **R** | Resistor |
| **RCA** | Radio Corporation of America Laboratories |
| **RC** | Resistor-capacitor |
| **RHBD** | Radiation-hardened-by-design |
| **RH** | Relative humidity |
| **S** | Source terminal |
| **SCR** | Silicon-controlled rectifier |

| | |
|---|---|
| **$SiO_2$** | Silicon dioxide |
| **SOS** | Silicon on sapphire |
| **SRAM** | Static random-access memory |
| **TFT** | Thin-film transistor |
| **TLP** | Transmission line pulse |
| **TV** | Television |
| **TVS** | Diode transient voltage suppressor |
| **USB** | Universal serial Bus |
| **VDS** | Drain-source voltage |
| **VGG** | Gate Positive voltage |
| **WSC** | wafer sort controller |

# Chapter 1 Introduction

The company I work for since 2011 is situated in Newport South Wales, the plant has been running since 1982 since then, the plant has traded under eight different owners since it was built, These being in order INMOS (1982), Thorn EMI (1984), SGS Thomson Microelectronics (1989), European Semiconductor Manufacturing Limited (1999), International Rectifier (2002), Infineon (2015), Newport Wafer Fab (2017), Nexperia (2021), and Vishay acquired the plant in 2023. The fab is run as part of the MOSFET business group. The company currently manufactures a wide range of silicon-based power metal oxide semiconductor field-effect transistor (MOSFET) and insulated gate bi-polar transistors (IGBT's) along with diodes and power management integrated circuits IC's. As well as the manufacturing of these devices. The company also offers wafer level testing of the devices. This ranges from basic parametric test of test structures to functionality testing of gate drivers. The company business of manufacturing power semiconductors is highly focused and is significant for the growth of modern technologies. These technologies include autonomous vehicles, electric vehicles, artificial intelligence (AI), robotics, electric appliances, and various electrical gadgets. Due to this market demand the power MOSFETs that the company produces possesses vast income potential for the company now and in the immediate future due to the devices being used in these technologies.

In the future, the market in power MOSFETs will be expected, to generate considerable output revenues with reasonable investments in research, and development. This due to the increase in necessity for hybrid / electric vehicles globally, therefore the power MOSFET market is expected to increase in lucrative opportunities. These semiconductor devices are susceptible to ESD that can cause undesirable effects such as a loss of potential revenue to the company and reputation due to the damage caused. Also, ESD can cause damage to reticles / masks that lead to defective die on the wafer and damaged semiconductor in other companies' products causing these to fail. This thesis involved from an interim report on the outdated ESD protection practises for within the company.

The intention of this thesis is to minimise the negative impact on productivity caused by static discharge in the production environment by using risk mitigation to lessen or remove the effects of ESD on reticles and wafers. Therefore, increasing the "good" die on wafers so improving company output and to design and construct a Human Body Model (HBM) ESD tester for use with wafers to improve the level of die output and prove that the die is good on each wafer prior to shipping to the customer. Before delving into the HMB we must understand the basic physics of the power MOSFET and its apparent vulnerabilities to ESD. Next an ESD tester is designed and constructed to use on wafers with the results used to show how to prevent ESD events within the workplace etc.

# Chapter 2 Comprehensive overview of MOSFETs

## 2.1 History of the MOSFET

The MOSFET is a semiconductor device that is extensively used for switching functions and for the amplification of electronic signals in electronic designs. Field effect transistors (FET's) have been around the since the early 20th Century, the basic theory of the FET was first suggested by Julius Edgar Lilienfeld an Austro-Hungarian physicist in 1926, when he recorded the first patent for an insulated-gate field-effect transistor [1].

In November of 1959, the MOSFET was successfully invented by Mohamed M. Atalla and Dawon Kahng an inventor and a Korean American electrical engineer when they produced the first working MOSFET device in November 1956 [2]. The patent on the MOSFET was separately filed by both Atalla and Kahng in March 1960 [3] [4], with results published in June of that year at Carnegie Mellon University which held the Solid-State Device Conference [5] also in 1960 Atalla suggested the use of MOSFETs to create MOS integrated circuit chips (MOS IC), documenting the MOSFET's ease of production [6].

From the 1960's onwards MOSET research was led by international business machines (IBM), Radio Corporation of America (RCA) Laboratories, General Microelectronics (GMe) and Fairchild Semiconductors [7]. In 1963, a public statement was made about the technology which displayed the growing interest and awareness of the technology at this time. The first MOSFET to be bought to the public market was made by GMe in May 1964 closely followed by Fairchild Laboratories in October 1964 [7]. GMe worked with suppling MOSFETs that were used in the National aeronautics and space administration (NASA) Explorers programs and Interplanetary Monitoring Platform (IMP). By the middle of the 1960's RCA Laboratories had fabricated MOSFETs to be used in RCA's consumer products such as televisions, FM radios and amplifiers [8]. Even at this time in the 20$^{th}$ century MOSFET technology was underpinning diverse applications across different sectors of society.

In 1968 at Fairchild Laboratories, researchers adapted the Silicon gate MOS transistors for integrated circuits. [9] This caused a development in the semiconductor industry and led to a transformation in electronics technology that fuelled an economic and technological growth of semiconductor manufacturing [10]. These developments were named "*the MOSFET revolution"* [11] from the late 1960's into the early 1970's this revolutionised the wider electronics industry including power electronics, consumer electronics, control systems, and computers. [12].

The MOSFET revolution bought a monumental impact on society and life, which positioned the MOSFET as a cornerstone of modern electronics and a driving force behind the widespread adoption and integration of semiconductor technology across various sectors ensuring its enduring significance in shaping the technological scene. The MOSFET revolution brought about several specific advancements in semiconductor manufacturing that significantly transformed the industry and propelled technological progress.

The development of the MOSFET was therefore the beginning of the modern electronics industry [13] which was pivotal to the microcomputer revolution [14] and is credited with the creation of modern electronics and is the most extensively used semiconductor device in the world today [15]. It is the basis of most modern electronic technology in the late 20th to early 21st centuries. In addition, the MOSFET is the most extensively mass-produced device in history with an approximated total of thirteen sextillion units produced between 1960-2018 accounting for at least 99.9 percent of all transistors made [16].

These innovations had far-reaching implications, for technology influencing various aspects of semiconductor technology and manufacturing. Some of the key developments resulting from the MOSFET revolution were and still are: -

1. Miniaturisation and integration: - The adaptation of Silicon gate MOS transistors for integrated circuits marked a significant leap in the miniaturisation and integration of electronic components. This advancement allowed for the fabrication of increasingly complex and compact integrated circuits, leading to the development of smaller, more powerful, and energy-efficient semiconductor devices. The ability to integrate multiple components on a single chip revolutionised semiconductor manufacturing, enabling the creation of sophisticated ICs and electronic systems.

2. Improved performance and efficiency: - The taking up of MOSFET technology for ICs led to considerable improvements in the efficiency and performance of semiconductor devices. Because MOSFETs offered a reduction in power consumption with enhanced speed, and improved reliability compared to earlier transistor technologies. These improvements paved the way for the development of faster and more efficient electronic devices, contributing to advancements in computing, telecommunications, consumer electronics, and various other applications.

3. Mass production standardisation: - The MOSFET revolution promoted mass production standardisation in semiconductor manufacturing. By placing MOSFET technology in integrated circuits, semiconductor companies were able to establish standardised fabrication processes for producing large volumes of ICs with consistent performance and quality. This scalability and standardisation enabled the mass production of semiconductor devices, meeting the increasing demand for electronic components across all sectors of industry.

4. Cost reduction and accessibility: - The MOSFET revolution advancements contributed to significant cost reductions in semiconductor manufacturing. The ability to fabricate ICs with higher levels of integration and enhanced yields led to cost efficiencies, making electronic devices more affordable and accessible to consumers. Moreover, the widespread adoption of MOSFET-based ICs in various applications drove down the economies of scale, further driving down production expenses and expanding the availability of electronic products to the customers.

5. Technological innovation and diversification: - The MOSFET revolution generated a wave of technological diversification and innovation within the semiconductor industry. The increased resources offered by MOSFET-based ICs stimulated the development of new electronic products, ranging from advanced computing systems and telecommunications equipment to consumer electronics and industrial automation devices. This wave of innovation and diversification broadened the scope of semiconductor applications, directing the development of the electronics industry.

Overall, the MOSFET revolution produced a change in thinking in semiconductor manufacturing, ushering in a new era of advanced, miniaturised, and integrated electronic components. The ensuing advancements in performance, efficiency, standardisation, cost reduction, and technological innovation have had a profound and enduring impact on the evolution of semiconductor technology and its widespread integration into modern electronics within the latter half of the 20$^{th}$ century and into the 21$^{st}$ century.

The US Patent and Trademark Office is cited as saying that the MOSFET is a [17]: -

*"Ground-breaking invention that transformed life and culture around the world."*

In addition, the Computer History Museum acknowledges the MOSFET with [18]: -

*"Irrevocably changing the human experience."*

While no Nobel Prize as ever been given for the MOSFET itself, (Woodall, J.M. 2010) the MOSFET is the foundation for several breakthroughs that have won the Nobel Prize such as the Quantum Hall effect (Lindley, D. 2015) plus the Charge-Coupled Device (CCD). (Williams, J. B. 2017). The Royal Swedish Academy of Sciences explicitly declared that the MOSFET and the microprocessor as significant inventions in the development of microelectronics. (Nobel Prize. 2018) The operating principles of modern MOSFETs have remained the same as the original MOSFET first demonstrated by Mohamed Atalla and Dawon Kahng in 1960. ((Schwierz, F; Wong, H; Liou, J. J.2010) & (Ye, Peide; Ernst, T; Khare, M. V. 2019)).

## 2.2 Structure of a MOSFET

A MOSFET is either a single semiconductor device or can be integrated into a circuit. The device is designed and fabricated in assorted sizes and packages. The MOSFET is operated in both depletion and enhancement modes of operation. Figure 2.1 shows what a practical MOSFET looks like: -

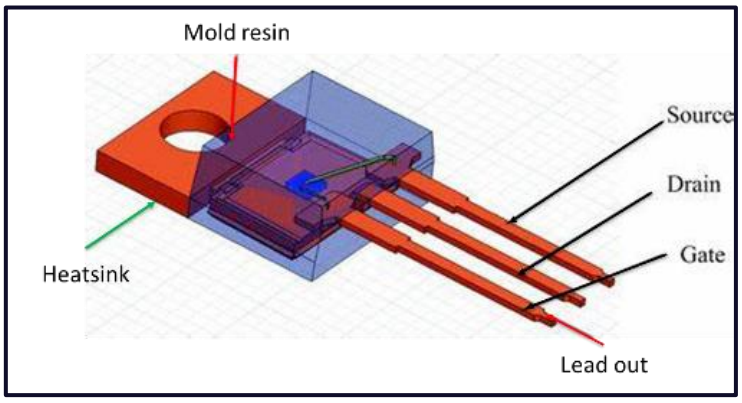


*Figure 2.1 Structure of a T0220 MOSFET package [76]*

A MOSFET is a four-terminal device which consists of source (S), gate (G), drain (D) and body (B) terminals, the gate is detached from the body by an insulating layer. In typical MOSFET's, the body relates to the source terminal creating a three-terminal device i.e., a field-effect transistor. A MOSFET is normally deemed as a transistor and utilised in both analogue and digital circuits. The structure of a MOSFET can be seen in figure 2.2: -

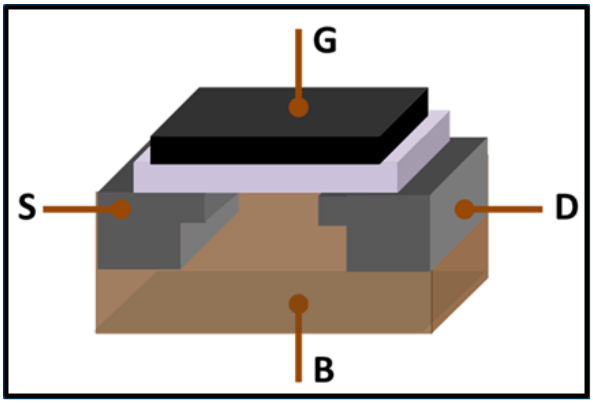


*Figure 2.1 Structure of a MOSFET [77]*

In the MOSFET structure, the functionality the device depends on the electrical changes occurring in the channel width along with the flow of carriers, these being either holes or electrons. The charge carriers enter the channel via the source terminal and exit through the drain terminal. The gate controls the width of the channel by controlling the voltage at its electrode and it is positioned between the source and the drain.

Insulation from the channel is provided by a very thin layer of metal oxide. The MOS capability in the device is the critical segment where the entire operation is across this. MOSFET's operate in two ways these being Depletion Mode or Enhancement Mode and is discussed in the next section.

## 2.3 Working Theory of a MOSFET

In theory, the MOSFET works as a switch, which controls the voltage and current flow between the source and drain. The operation of a MOSFET is depended on the MOS capacitor, which is the semiconductor surface below the oxide layers between the source and drain terminal.

It can be inverted from p-type to n-type, simply by applying positive or negative gate voltage, respectively. Figure 2.3 shows the block diagram of a MOSFET.

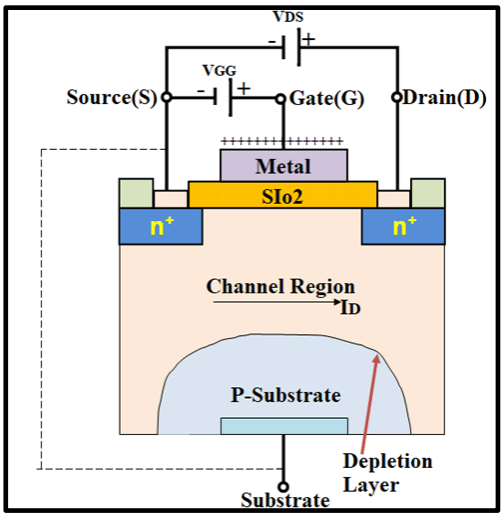


*Figure 2.2 Block diagram of a MOSFET [77]*

When a drain-source voltage (VDS) is connected between the drain and source, a positive voltage is applied to the Drain, and the negative voltage is applied to the Source. Therefore, the PN junction at the Drain is reverse biased and the PN junction at the Source is forward biased. thus, there will not be any current flow between the Drain and the Source.

If a positive voltage, (VGG) is applied to the gate terminal, then the minority charge carriers (electrons) in the P substrate will start to accumulate on the gate contact, which forms a conductive bridge between the two n+ regions this due to electrostatic attraction. Thus, the number of free electrons accumulated at the gate contact is therefore dependent on the intensity of positive voltage applied. The higher voltage applied then the larger the width of the n-channel formed due to electron accumulation, this eventually increases the conductivity, and the drain current (ID) will start to flow between the Source and Drain. When there is no voltage applied to the gate terminal, there will not be any current flow apart from a small amount of current due to minority charge carriers. The minimum voltage at which the MOSFET starts conducting is the threshold voltage. MOSFETs can be classified into two types these being Depletion mode MOSFETs (D-MOSFET) and Enhancement mode MOSFETs (E-MOSFET) based on its operations, the operations of the device are below.

## 2.4 Operation of a D-MOSFET

D-MOSFETs are typically called normally on devices because they are normally in the conductive state when there is no bias voltage at the gate terminal. If the applied voltage to the gate is positive, the channel width will be increased in depletion mode. Therefore, increasing the drain

current (ID) through the channel. If the applied gate voltage is negative, then the channel width will be less and the MOSFET will enter the cut-off region.

## 2.5 Voltage – Current characteristics of the D-MOSFET

The Voltage – Current characteristics of the D-MOSFET is drawn between the drain-source voltage (VDS) and drain current (ID). The small amount of voltage at the gate terminal will control the current flow through the channel. The channel formed between the Drain and the Source will act as a good conductor with zero bias voltage at the Gate terminal. The channel width and drain current will increase if the positive voltage is applied to the Gate and will decrease when applied with a negative voltage to the Gate. As seen in figure 2.4: -

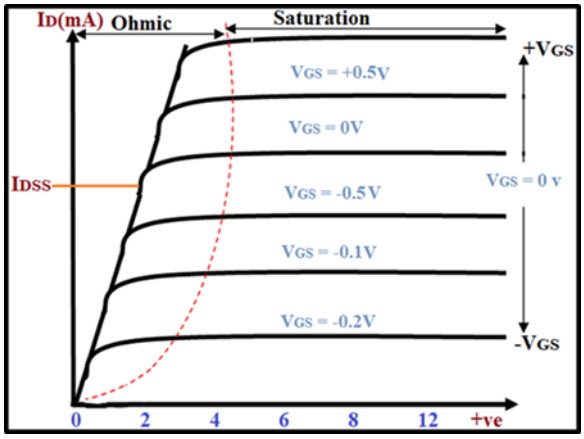


*Figure 2.3 I – V Characteristics of a generic D-MOSFET [78]*

In figure 2.4 the MOSFET drain current vs. drain-to-source voltage for several values of the overdrive voltage, $V_{GS}$ - $V_{th}$ the boundary between linear (ohmic) and saturation (active) modes is indicated by the upward curving parabola.

## 2.6 Operation of an E-MOSFET

E- MOSFET operation is like an open switch, the device will start to conduct only if the positive voltage (VGS) is applied to the gate terminal and the drain current starts to flow through the device. When the bias voltage increases the channel width and drain current will increase. However, when the applied bias voltage is zero or negative the E-MOSFET will remain in the off state.

## 2.7 Voltage – Current characteristics of the E-MOSFET

The Voltage – Current characteristics of the E-MOSFET are drawn between the drain current (ID) and the drain-source voltage (VDS). The Voltage – Current characteristics are segregated into three different regions and is showed in Figure 2.5: -

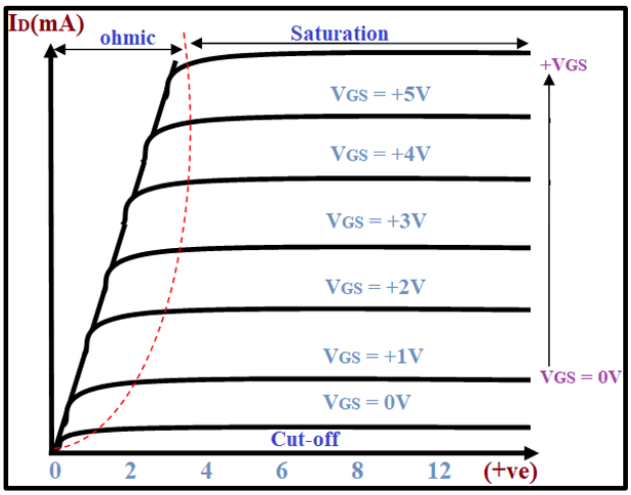


*Figure 2.4 I – V Characteristics of a generic E-MOSFET [78]*

- Ohmic region: - When the bias voltage is applied, the MOSFET slowly moves towards conduction mode, and the slow increase in conductivity takes place in the ohmic region.

- Saturation region: - The saturation region is where the positive voltage is applied constantly, and the device will stay in the conduction state.

- Cut-off regions: - The cut-off region is the region where the MOSFET will be in the OFF state where the applied bias voltage is zero.

The main distinction between the D-MOSFET and E-MOSFET is that the Gate voltage applied to an E-MOSFET is switched on with the forward biasing of the gate and it has a threshold voltage above which it turns on completely. For a D-MOSFET the gate voltage can either be positive or negative and it never turns on completely. Also note that an E-MOSFET can work only in enhancement mode while a D-MOSFET can work in enhancement and depletion mode.

## 2.8 Classification of a MOSFET

As stated above a MOSFET can be classified into two types based on its operations, namely Enhanced mode MOSFET (E-MOSFET) and Depletion mode MOSFET (D-MOSFET), these categories can then be further sub-divided based on the material used for manufacturing them i.e., n-channel and p-channel. Therefore, in general, there are four distinct types these being: -

- N-Channel D-MOSFET and N-Channel E-MOSFET
- P-Channel D-MOSFET and P-Channel E-MOSFET

The N-channel MOSFETs are called NMOS, and they are represented by the following symbols in figure 2.6: -

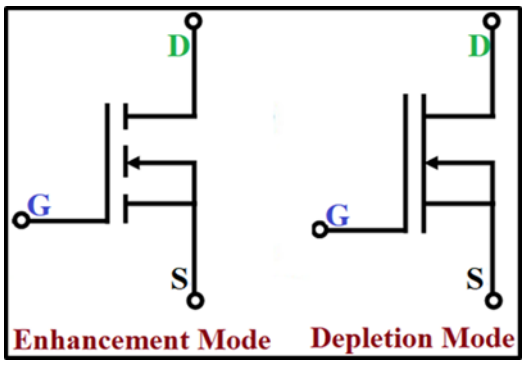


*Figure 2.5 N-Channel MOSFET [78]*

The P-Channel MOSFETs are called PMOS, and they are represented by the following symbols in figure 2.7: -

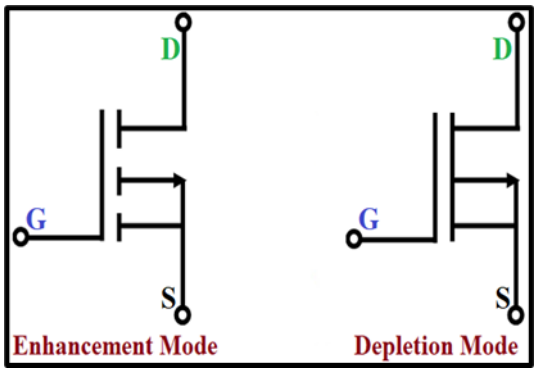


*Figure 2.6 P-channel MOSFET [78]*

The main difference between NMOS and PMOS is that in an NMOS device, the channel will remain open until a gate voltage is provided. When the gate pin senses the voltage, the switch between Drain and Source will be closed and in PMOS the switch will remain closed until a gate voltage is provided which will open the switch.

## 2.9 Types of MOSFET

There are numerous types of MOSFETs available to buy from electronic device suppliers. These are: -

- PMOS and NMOS logic
- Complementary MOS (CMOS)
- Metal‑insulator‑semiconductor field-effect transistor (MISFET)
- Floating-Gate MOSFET (FGMOS)
- Power MOSFET
- Double-diffused metal‑oxide‑semiconductor (DMOS)
- Thin-film transistor (TFT)
- Bipolar‑MOS transistor
- Multi-gate field-effect transistor (MuGFET)
- Quantum field-effect transistor (QFET)
- Radiation-hardened-by-design (RHBD)

These MOSFETs are available in different names, sizes, and packages namely: -

- Surface mount i.e., TO-263 etc.
- Thru Hole i.e., TO-247 etc.
- Power Quad Flat No-Lead (PQFN) i.e., PQFN 2x2 etc.
- Direct FET i.e., Direct-FET M4 etc.

As stated earlier the MOSFET is the most commonly used device in the field of electronics today. However, MOSFETs and other electronic components are vulnerable to ESD from various sources that can cause immediate damage or latent defects and will be discussed in later sections. So, what is ESD and why is so important to the semiconductor industry and the company to reduce the impact of it?

# Chapter 3 ESD in Semiconductor manufacturing

## 3.1 History of Electrostatic Discharge

Countless individuals around the world have experienced electrostatic discharge (ESD), static electricity or “shocks", when touching a metal doorknob after walking across a carpeted floor or after sliding across a car seat. Therefore, the act of walking across a carpet charges the person’s shoes through triboelectric charging and produces a charge on their body [19]. When they touch a conductive object i.e. a metal doorknob, the developed charge balances, causing a current spike that can be felt. This event encompasses several hundred Nano joules of energy and generates about three thousand volts [20]. It can destroy all but the most robust semiconductor devices. Also, a cold and dry winter day is perfect for such an ESD event. This ESD event is the shock felt when the event has substantial energy to excite nerve endings, causing pain.

ESD has been viewed and explored for centuries. Ancient civilisations were aware of static electricity and its effects, and the earliest description of electricity was by a Greek scientist, Thales of Miletus (624BC -546BC) [21]. He declared that after amber was rubbed, dust and leaves were attracted to it. The word "triboelectric", comes from the Greek words, tribo – meaning "to rub" and elektros – meaning "amber" (fossilized resin from prehistoric trees) but systematic investigation began in the 17th century.

One of the earliest documented records of static electricity experiments dates to the work of English scientist William Gilbert in the late 16th or early 17th centuries in his publication De Magnete [22] [23]. He extensively studied magnetism and electricity and coined the term “electricity” from the Greek word “elektros,” [24] [25] meaning amber, which exhibits static electricity when rubbed. When flowing electricity properties were discovered in the early 18$^{th}$ century, static electricity became the term for the old form of electricity, which distinguished it from the new forms of electricity. Also in the 18th century, Benjamin Franklin conducted ground-breaking experiments with electricity, including his famous kite experiment in 1752 [25] [26], which demonstrated the connection between lightning and electricity. Franklin’s work laid the foundation for understanding the nature of electricity and “sparked” further interest in the study of electrostatic phenomena.

Nevertheless, ESD and static electricity have generated severe industrial problems for centuries. As early as the 14$^{th}$ century, European militaries were using static control procedures and grounding devices trying to prevent inadvertent ESD ignition of gunpowder stores within military forts. By the 1860s, paper mills around the world. employed basic grounding, flame ionisation

techniques, and steam drums to dissipate static electricity from the paper web as it travelled through the drying process (techniques still in use today).

It was during the late 19th and 20th centuries, scientists and inventors made considerable progress in understanding and harnessing electricity. Every imaginable business and industrial process has issues with an electrostatic charge and discharge at one time or another. Munitions and explosives, petrochemical, pharmaceutical, agriculture, printing and graphic arts, textiles, painting, and plastics are just some of the industries where control of static electricity has significant importance. Also, during this time that the effects of electrostatic discharge on sensitive electronic devices became more apparent with the increasing use of telegraphy, telephone systems, and early electronic equipment.

However, it was during the latter half of the 20$^{th}$ century and into the 21$^{st}$ century that new problems with static electricity and ESD become more apparent within the electronics field and in particular the semiconductor industry as electronic devices become quicker and the circuitry got smaller, sensitivity to ESD in general increased, this led to the modern era of ESD research and prevention as electronic devices, and integrated circuits have become more widespread. The introduction of solid-state electronics and microelectronics brought about the need for measures to protect sensitive components from ESD damage.

ESD impacts productivity and product reliability in virtually every aspect of the global semiconductor industry. Despite a great deal of effort in the past years, ESD still affects semiconductor yields, manufacturing cost, product quality, product reliability, and profitability. The cost of damaged devices ranges from a few pence for a simple diode to thousands of pounds for complex integrated circuits. The related costs of labour, repair / rework, shipping, and overheads when included can add up to an expensive bill for companies. Nearly all the companies and industries involved in semiconductor and electronics manufacturing pay awareness to the basic elements of static control. It is very unlikely that any organisation which ignores ESD monitoring will be able to manufacture and deliver undamaged semiconductor parts successfully the opportunities exist for significant improvements.

## 3.2 Understanding Electrostatic Charge and Discharge

ESD can modify the electrical attributes of a semiconductor device, degrading or destroying it. ESD may also upset the normal operation of an electronic system, causing equipment breakdown or malfunction. Charged surfaces can attract and hold contaminants, making elimination of the

particles problematic. When attracted to the surface of a silicon wafer or electrical circuitry, air-borne particulates can cause random wafer defects and reduce product yields.

Electrostatic charge is defined as: -

*"Electric charge at rest".*

Static electricity is an imbalance of electrical charges within or on the surface of a material. This imbalance of electrons produces an electric field that can be measured and that can influence other objects. ESD is defined as: -

> *"The rapid, spontaneous transfer of electrostatic charge induced by a high electrostatic field the charge flows through a spark between two conductive bodies at different electrostatic potentials as they approach one another"*

or in other words when one object, typically with a high electric charge, comes into contact or gets close to another object with a lower charge. This rapid transfer of electrons can cause a visible spark or discharge.

To understand ESD we must comprehend how electrostatic charge happens. Electrostatic charge is created by the contact and separation of two materials. The materials may be alike or different, although varied materials tend to release greater levels of static charge. While the degree of electrostatic charge may be different in the examples below, electrostatic charge is formed in each one. Examples of electrostatic charge are a person walking across the floor, generating electrostatic charge as their shoe soles contact and then separate from the floor surface. An electronic device sliding into or out of a bag, magazine, or tube generates an electrostatic charge as the device's housing and metal leads make multiple contacts and separations with the surface of the container.

Creating electrostatic charge by the interaction of materials is known as triboelectric charging. It involves the relocating of electrons between materials. The atoms of a material with no static charge have an equal number of positive (+) protons in the nucleus and negative (-) electrons orbiting the nucleus. In figure 3.1, Material "1" consists of atoms with equal numbers of protons and electrons. Material “2” also consists of atoms with equal numbers of protons and electrons. Both materials are electrically neutral.

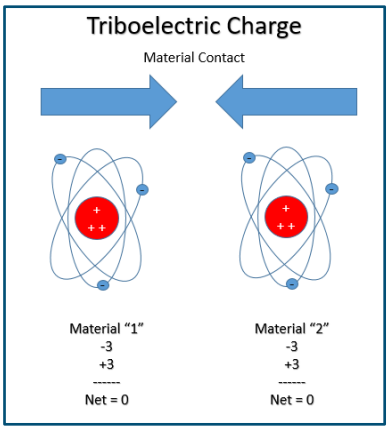


*Figure 3.1 Triboelectric charge. Materials make intimate contact [79]*

When the two materials are placed in contact and then separated, negatively charged electrons are transferred from the surface of one material to the surface of the other material. Which material loses electrons, and which gains electrons will depend on the nature of the two materials. The material that loses electrons becomes positively charged, while the material that gains electrons is negatively charged as below in figure 3.2: -

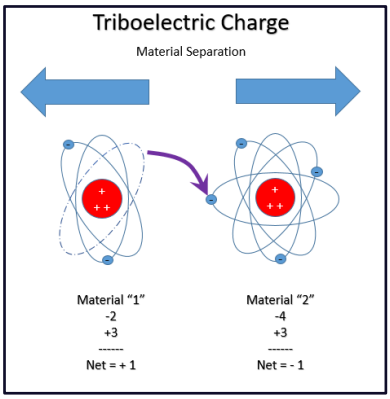


*Figure 3.2 Triboelectric Charge – Separation [79]*

Static electricity is measured in coulombs. The charge (q) on an object is determined by the product of the capacitance of the object (C) and the voltage potential on the object (V): -

$$q = CV \qquad (3.1)$$

Nevertheless, we speak of the electrostatic potential on an object, as voltage. The process of material contact, electron transfer, and separation is a much more complicated system than depicted

here. The amount of charge created by triboelectric generation is affected by the area of contact, the speed of separation, relative humidity, the chemistry of the materials, surface work function, plus additional factors, such as the resistance of the actual discharge circuit and the contact resistance at the interface between contacting surfaces affect the actual charge that is released. Once the charge is created on a material, it becomes an electrostatic charged material or object only if the charge remains on the material or object. This charge may be transferred from the material, creating an ESD event.

Typical charge generation scenarios and the resulting voltage levels are shown in table 3.1. Also, the contribution of humidity to reducing charge accumulation is shown. However, it should be noted that static charge generation still occurs even at high relative humidity (RH). An electrostatic charge may be created on the material by other means, such as by ion bombardment, induction, and or contact with another charged object. However, triboelectric charging is the most common.

*Table 3.1 Examples of typical static generation voltage levels [84]*

| Means of Generation | 10-25% RH | 65-90% RH |
|---|---|---|
| Walking across carpet | 35000V | 1500V |
| Walking across vinyl tile | 12000V | 250V |
| Employee at bench | 6000V | 100V |
| Polybag picked up from the bench | 20000V | 1200V |
| Chair with urethane foam | 18000V | 1500V |

Material characteristics can affect the static charge When two materials interact, the magnitude and polarity of the charge are specified by the materials' positions in a triboelectric series. The triboelectric series can be seen in table 3.2 this shows how charges are generated on various materials. When two materials interact, the one nearer the top of the series takes on a positive charge, the other a negative charge. Materials farthest apart on the table in general generate a higher charge than ones close by.

*Table 3.2 Typical Triboelectric Series [79]*

| Positve ( + ) | Rabbit fur |
|---|---|
| | Glass |
| | Mica |
| | Human hair |
| | Nylon |
| | wool |
| | Fur |
| | Lead |
| | Silk |
| | Aluminum |
| | Paper |
| | cotton |
| | Steel |
| | wood |
| | Amber |
| | Sealing wax |
| | Nickel |
| | Copper |
| | Brass |
| | Sliver |
| | Gold |
| | Platinum |
| | Sulfur |
| | Acetate |
| | Rayon |
| | Polyester |
| | Celluloid |
| | Silicon |
| Negative ( - ) | Teflon |

These tables, nevertheless, should only be used as a general guide because there are many variables involved that cannot be controlled well enough to ensure repeatability. Fundamentally all materials, including water and dirt particles in the air, can be triboelectrically charged. How much charge is generated, where that charge goes, and how quickly, are functions of the material's chemical, electrical, and physical characteristics. Materials can be broken down into have one of three states these being insulate, conductive and dissipative: -

**Insulate materials: -** A material that prevents or limits the flow of electrons across its surface or through its volume, due to having an extremely high electrical resistance, is called an insulate material and is defined as [27]: -

*" A material with a surface resistance or a volume resistance of equal to or greater than 1.0 × $10^{11}$ ohms".*

A considerable amount of charge can be generated on the surface of an insulator. Since an insulating material does not readily allow the flow of electrons, both positive and negative charges can reside on an insulating surface at the same time, however at different points. The excess electrons at the negatively charged point might be sufficient to satisfy the absence of electrons at the positively charged point. However, electrons cannot easily flow across the insulating material's surface, and both charges may remain in place for an exceedingly long time.

**Conductive material: -** A material that allows electrons to flow easily across its surface or through its volume is called a conductive material and is defined as [27]: -

*"A material with a surface resistance or volume resistance of less than 10,000 ohms".*

When a conductive material becomes charged, the deficiency or surplus of electrons “the charge” will be uniformly distributed across the surface of the material. If the charged conductive material contacts another conductive material, the electrons will be shared between the materials quite easily. If the second conductor is attached to equipment ground or another grounding point, the electrons will be grounded, and the surplus charge on the conductor will be neutralised.

Electrostatic charge can be created on conductors in the equivalent way to how it is created on insulators triboelectrically. If the conductor is separated from other conductors or ground, the charge will remain on the conductor. If the conductor is grounded, the charge will go to ground. or, if the charged conductor contacts another conductor of different electrical potential, the charge will flow between the two conductors.

**Dissipative materials: -** A material that has properties of between insulative and conductive materials i.e., has an electrical resistance and is defined as [27]: -

*"A material with a surface resistance or a volume resistance between 10,000 ohms and 100 billion ohms”.*

There can be electron flow across or through the dissipative material, but it is controlled by the surface resistance or volume resistance of the material. As with the other two types of materials, a charge can be generated triboelectrically on static dissipative material. Therefore, like the conductive material, the dissipative material will allow the transfer of charge to ground or other conductive substances. The transfer of charge from a dissipative material will generally take longer than from a conductive material of corresponding size. Charge transfers from dissipative materials are significantly faster than from insulators and slower than from conductive material. In table 3.3 the resistance classifications for these materials can be seen.

*Table 3.3 Resistance Classifications [80]*

| Material | | Resisitance ( Ohms ) | Exponent format |
|---|---|---|---|
| Conductive < 1 x $10^4$ | | 10 | $10^1$ |
| | | 100 | $10^2$ |
| | | 1,000 | $10^3$ |
| Dissipative > 1 x $10^4$ to < 1 x $10^{11}$ | | 10,000 | $10^4$ |
| | | 100,000 | $10^5$ |
| | | 1,000,000 | $10^6$ |
| | | 10,000,000 | $10^7$ |
| | | 100,000,000 | $10^8$ |
| | | 1,000,000,000 | $10^9$ |
| | | 10,000,000,000 | $10^{10}$ |
| Insulative > 1 x $10^{11}$ | | | |
| | | 100,000,000,000 | $10^{11}$ |
| | | | |

Charged materials have an electrostatic field and lines of force associated with them. Conductive items brought into the locale of this electric field will be polarised by a process known as induction. A positive electric field will attract electrons near the surface, thus leaving other areas positively charged. A negative electric field will repel electrons on the surface of the conducting item that is exposed to this field. No change in the actual charge on the item will occur in polarisation. But, if the material is conductive or dissipative, and is connected to ground while polarised, the charge will flow from or to ground due to the charge difference. If the ground contact is detached and then the electrostatic field is removed, the charge will remain on the material. If a nonconductive item is carried into the electric field, the electrical dipoles will tend to align with the field creating apparent surface charges. An insulative material cannot be charged by induction. Figure 3.3 below illustrates induction in progress: -

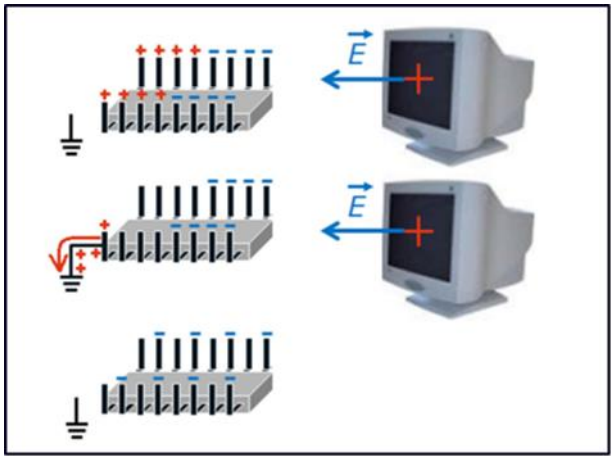


*Figure 3.3 Induction in progress [80]*

The charge / discharge that cause ESD will also cause the following effects within a wafer fab such as: -

- Contamination: - Wafers sitting in a charged wafer carrier will attract airborne particles, causing them to stick to the surface of the wafer.

- Mask / reticle damage: - Discharges to masks / reticles can damage the chrome pattern used to define the circuit. Then each circuit is printed with this damage.

- Direct discharge damage: - Direct discharge to the wafer or die which ruptures the oxides and damages junctions.

- Process interruptions: - ESD can cause electromagnetic interference (EMI) on equipment or damage to equipment by a direct discharge.

The above effects are discussed in the next section.

## 3.3 ESD within a wafer-fabrication facility

ESD events occur throughout the life span of a semiconductor. Firstly, the semiconductor being produced is affected early in the wafer-fabrication process. Cleanrooms can be an excellent source for materials generating charge because of the wide-ranging use of synthetic materials in containers and tools [28]. For example, the wafer boxes that are used to carry groups of wafers between tools can charge to twenty thousand volts. This emphasises the first problem related with ESD being produced - particle pollution caused by electrostatic bonding. In a charged box, the wafers attract airborne particles, causing them to attach to the wafers [29]. The attachment force of a particle on a wafer can be as much as 830 000 psi [30].

A way that particle corruption decreases yield is by modifying the patterns produced on the semiconductor circuit. Thus, the altered patterns can produce shorts or open circuits, causing the die on the wafer to be non-functional. Therefore, further cleaning of the wafer is required to eliminate the particles. Thus, adding more expense to the wafers, and these extra steps in the process can reduce the yield produced.

Another consequence is the reduction in yield caused by an ESD event in wafer fabrication. The ESD discharge reduces yield by two methods. Firstly, a discharge to the mask impairs the design used to outline the circuit [28], [31]. A wafer is manufactured by a sequence of masking steps that define the circuit on the individual die. The masks have the required circuit outlined in chrome. A photolithography process transfers the image of the circuit to the wafers. The ESD event erodes the image outlined on the mask. Therefore, if the mask is impaired by ESD, then each die is printed with this damaged circuit. The second mode of ESD damage is a direct discharge to the wafer. This can burst oxides and can also cause destruction of junctions [28], [32].

The next phase in semiconductor manufacture is the assembly operation, where further ESD threats can exist. The film utilised during the sawing process can charge up to voltages larger than ten thousand volts. This film stops the wafer moving while it is divided to split up the die. The die attaches to the film. When the die is removed, the film charges up. The die is then inspected and located in packages. Wires are attached to allow signals to travel from the outside pins to the die. Lastly, the package is formed around the die (See figure 3.7 for a simple IC construction). These processes are all capable of creating ESD events [33].

Prior to a product's shipping to a customer and after assembly, some level of additional testing is required. This assures the customer of a superior product. It could be a simple electrical test at room temperature or a series of burn-in operations and electrical tests over the full temperature range. These are additional opportunities for ESD to occur. The more a wafer is handled, the higher the probability that an ESD event will occur. The personal and equipment used during the testing operation generate the ESD events.

Any company manufacturing devices will seldom produce a perfect circuit, die, wafer, semiconductor. Numerous electrical tests are required to eradicate the flawed devices from the product to be shipped. Flaws in the design or manufacture of a semiconductor also decrease the ESD protection limit. It is difficult to spot these flaws with regular electrical testing since they may only be operating at the tremendous stress situations forced by an ESD event. These flaws during an ESD event act as concentrators for the energy or electric field. These flaws relate to manufacturing faults. For example, crystal faults in the substrate matrix or oxide pinholes plus design non-conformities. The flaws make the design of the device more susceptible by concentrating the detrimental energy toward a particular point instead of uniformly over the entire semiconductor.

The risk of an ESD event does not stop once the unit leaves the manufacturing plant. In fact, it can increase. The home and office also contain charge-generation sources [34], [35]. For example, synthetic carpets, seat covers, plus clothes provide ample voltage to damage semiconductors [36] as

can any electrical equipment within a home or office for example any old television sets or computer monitors use cathode-ray tubes (CRT) that can be an additional hazard [36]. A large static voltage can be produced from these sources.

A manufacturing plant handles sensitive parts continuously and invests in equipment and procedures to make sure sensitive parts do not become damaged. On the other hand, the customer may not understand the risk and not invest the resources necessary to ensure safe handling of these parts. This is especially true for end users such as electronic hobbyists.

## 3.4 Cost of ESD damage

The expense associated with ESD failure can be difficult to measure. One way of measuring this is to analyse all the field returns to the company this can be done by presenting the failure causes in a pareto chart as seen in figure 3.4. In the chart ESD represents a sizable percentage. Wagner et al. [37] reported ESD as being the cause of greater than 25% of the failures encountered. These data show a fantastic opportunity for improvement with respect to ESD/EOS related failures.

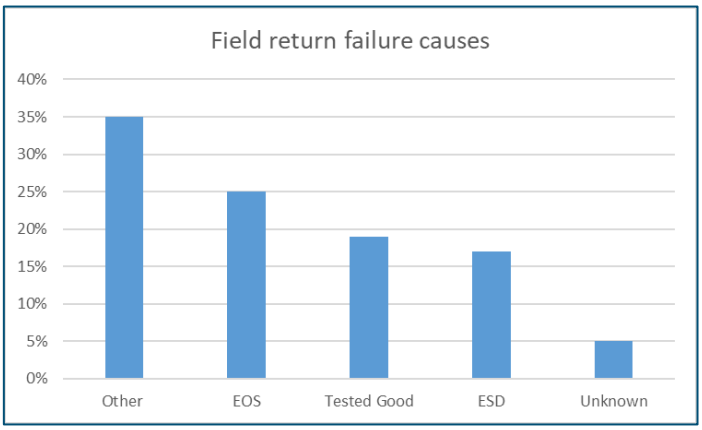


*Figure 3.4 Field return failure causes [81]*

The demonstrable expenses of ESD events are material losses, recycle expenses, and protection expenses. Each of these expenses can be assigned a value. The more difficult expenses to measure are the substantial expenses connected to delays plus the loss of customer confidence in the failed semiconductor or end user product. Of the three demonstrable expenses, material losses are the most straightforward to identify since these are the costs related to the parts that have failed. The expenses include raw materials and the manufacturing processes prior to the semiconductor failing.

This expense also includes the analysis effort and support linked with finding the source of the ESD event and correcting this source of the ESD event. It should be noted that for a small number of failures (Typical less than twenty percent) the expense, does not justify the expenditure of identifying the cause, so the ESD source is not corrected, and a continual stream of small failures occurs. If the failure rate is greater than twenty percent (typical wafer yield rates are above ninety percent) then the whole group of die on the wafer must be scrapped from being manufactured. Wafer yield can be determined by the ratio of all the wafers that are manufactured by the fab to the number of wafers that were introduced to it. It should be noted that a typical single wafer can cost from around one thousand US dollars to three thousand US dollars upwards depending on the wafer construction [38]. Therefore, a typical two-hundred-millimetre wafer cassette holds twenty-five wafers then the expensive is anywhere from twenty-five thousand US dollars to seven hundred and fifty thousand US dollars and above. This situation is extremely expensive for the company.

If reprocessing is allowed, then the wafer may be reprocessed and recycled through some or all of the manufacturing process. Also, the rescreening may require testing and burn-in or may be a simple electrical test. It is critical that the cause of the ESD event be rectified so that further failures during the recycle attempt do not occur again.

The expense linked with recycling incorporates not only the labour and equipment expenses but also the expense of the schedule slipping behind, reduction in capacity, and the lost opportunity of other material not being ran. The price of labour and equipment is a direct expense of the wages, company overheads (i.e. electricity, gas etc.) and equipment declining in value. These are documented numbers within the company and should be available, these factors are used to determine the price of a wafer or semiconductor.

However, the expense of a schedule slipping behind is more difficult to calculate the cost unless the contract between the manufacturer and client has rewards for speedy delivery and or consequences (penalties) for being late. The capacity of the fab to produce wafers decreases because each wafer will have to be processed numerous times. An example, of this is if every ninth lot has to be recycled, it contributes the consequence of a ten percent decrease in production because only nine lots of manufactured wafers are shipped for every ten lots produced.

The expense of protecting semiconductor devices is shared by all wafers manufactured within the fab. Each wafer produced benefits from these procedures. These procedures are: -

- The protective equipment used in production (ionizers, monitors, uniforms, etc.).

- Packaging and transport materials.

- Training and administrative systems.

- Development systems.

These items together provide an ESD-safe environment within the manufacturing environment (and will be discussed later), also ensuring that improved ESD designs are funded within the company.

The first part of the insubstantial expense incurs when a manufacturer must explain to a client why a lot /lots have not been shipped due to ESD failures occurring. Clients, confidence can be lost in a company when this occurs. Thus, the relationship between the client and company becomes strained. This can be due to the schedule slipping behind as well as a view of low-quality semiconductors from all of the failures. Therefore, the client will start to look for other companies to supply similar semiconductors and to only purchase the original manufacturer semiconductors when there are no other substitutes.

The second part of the insubstantial expense is when failures occur, the company must find out the source of the ESD event and then prevent this ESD event from recurring corrective actions must be put into place by the company. If these ESD events are ignored and not corrected, then there is a risk that the ESD event will happen again. Also, the company time for producing new semiconductors is wasted due to preventing these ESD events when it is easier to stop the ESD events in the first place. The damage to the semiconductors being produced is discussed in the next section.

## 3.5 ESD Damage to Semiconductors

ESD events can happen to semiconductors at any time, from production to PCB soldering to end-user interactions. The prevalence of ESD events goes all the way back to the dawn of semiconductors, however it did not become a frequent problem until around the 1970s with the beginning of thin-gate-oxide FETs for highly integrated ICs and the microchip. In the 21$^{st}$ century the power MOSFET market is estimated to be worth $5.90 billion USA dollars in 2019 projected to rise to $9.90 billion USA dollars by 2027 [37]. The company at the time this thesis was written produces power MOSFETS for this market. The company as an overall group recorded a revenue of $25M USA dollars in 2021 projected to rise to $300M USA dollars by 2027 [39]. Annually in the semiconductor / electronics industries ESD failures costs companies $84 billion USA dollars per year [38]. The annually cost to the organisation due to ESD events is on average $442,000 dollars per year.

Therefore, the company cannot afford to allow this to continue. ESD damage can be defined as [40]: -

***"Change to an item caused by an electrostatic discharge that makes it fail to meet one or more specified parameters".***

It can strike at any time in the semiconductor lifetime, from production to in use in the field. In general, damage ensues from handling the semiconductors in uncontrolled environments or when poor ESD control practices are employed. Generally, ESD is characterised by fast rise times and high peak voltages and currents up to thirty amps which can melt silicon and conductor traces. But ESD effects can be subtler. There are three types of damage: -

1. Soft Failures: - ESD can change electrical currents that can change the state of internal logic, causing systems to latch up or cause unpredictably behaviour, or cause corruption of a data stream. While this is temporary, it may slow down communications, or require a system reboot in the case of lockup. An example of this is a temporary change in logic function (i.e., flip-flop or changed state), Soft failures will not be addressed in this thesis because soft failures occur on powering up.

2. Catastrophic Failures: - Also, ESD can damage a component to the point where it does not function as intended or does not work. thus, causing device function to fail. Devices in the test identified as faulty causing cost of reworking due to the device being removed and replaced. ESD damage is responsible for seventy percent of component failures.

3. Latent Defects: - A component or circuit may be damaged by ESD, and its function degraded though the system will continue to work. However, this type of defect often leads to a premature failure. Latent (time dependent) failures can be caused by an excess current leading to partial fusing, stress cracks etc. and excess voltage which will lead to partial breakdown, increased leakage, and short circuits etc. Shorten lifetime of products from the effects of gradual degradation over time latent catastrophic failure of products resulting from electrical, thermal stresses etc., while in use.

The type of damage can be broken down into typical system damage thermal breakdown that is due to ESD current density that causes material fusing / vaporization and dielectric breakdown, which is due to ESD voltage surge causing insulation puncture / rupture. It should be noted that time dependent damage does not advance to a breakdown just by electrical means; a number of other causes can lead to damage from the result of physical shock, thermal shock, etc. The most expensive

ESD failures are those that go unobserved through component testing. These devices are typically categorized as those that break down and degrade which will then later fail while being used externally in the outside world.

Examples of ESD damage can be seen in figures 3.5 and 3.6. Figure 3.5 shows a static random-access memory (SRAM) device with 5-micron structures that was deliberately exposed to an eight-thousand-volt pulse from a 100-ρF capacitor. This produced a 5.3-ampere peak current pulse lasting just under one microsecond. The melting of conductive traces is typical of such ESD damage and creates an open circuit path. Figure 3.6 shows an undefined semiconductor with one-micron line width that failed in service after being exposed to a pulse of approximately five hundred volts. This caused a breakdown of the silicon dioxide ($SiO_2$) layer and a short circuit in the semiconductor.

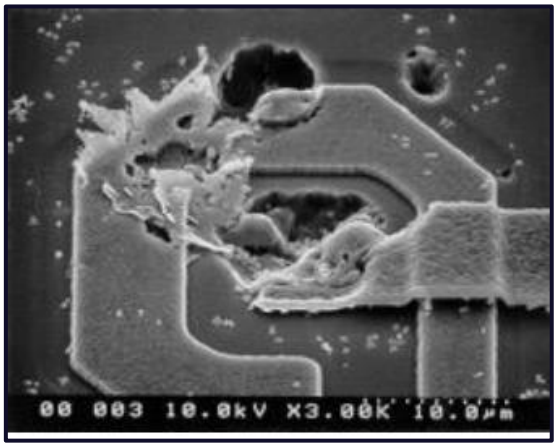


*Figure 3.5 ESD damage to a SRAM device [82]*

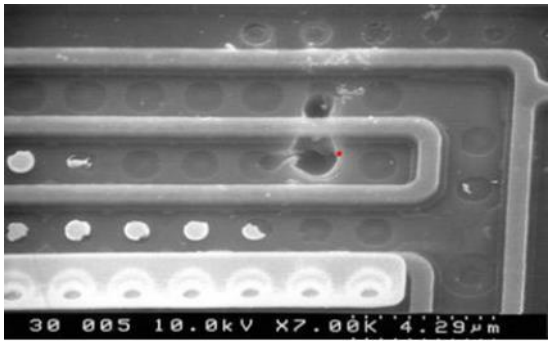


*Figure 3.6 ESD Damage to an unknown semiconductor device [82]*

It should be noted that ESD can originate from a range of sources, both natural and manufactured. Common sources of ESD are below: -

- Human body: - The human body can accumulate static charges through movement or friction with certain materials. When a person touches an electronic component or device, the accumulated charge can discharge and potentially damage sensitive electronics.

- Clothing: - Certain types of clothing made from synthetic materials such as polyester can generate static electricity as they rub against other surfaces. When wearing such clothing in an environment with sensitive electronic equipment, ESD risks increase.

- Machines and equipment: - Industrial machines and equipment can generate static charges during their operation, especially in processes involving moving parts or friction. If these charges come into contact with sensitive electronic components, ESD damage can occur.

- Packaging materials: - Materials used for packaging electronic components or devices, such as plastic or foam, can accumulate static charges. If not designed with proper antistatic properties, these materials can cause ESD issues during handling and transportation.

- Electronic devices: - Operating electronic devices can generate static electricity, especially when the devices are turned on or off. This is particularly relevant for devices that use high voltages or have fast switching circuits.

- Environmental factors: - Certain environmental conditions, such as low humidity, can promote the build-up of static charges on surfaces and objects. Dry air facilitates the accumulation of static electricity, increasing the risk of ESD events.

- Lightning: - Lightning is a natural and powerful source of ESD. A lightning strike in the vicinity of electronic equipment can induce elevated levels of electromagnetic interference and potentially damage the devices.

- Cables and wires: - Cables and wires carrying electric currents can generate static charges due to their insulation materials and movement. If these charges are not effectively managed, it can cause ESD events in connected electronic equipment.

ESD as noted occurs when differently charged objects are brought close together or when the dielectric between them breaks down. Electrical discharges can be broken down into five types: -

- Spark: - Sparks occur between objects at different electric potentials. Electric sparks require a field strength above approximately 40 kV/cm in air, as notably occurs in lightning strikes good grounding of all parts of the equipment and precautions against charge build ups on equipment and personnel are used as prevention measures.

- Brush discharge: - This occurs from a nonconductive charged surface or highly charged nonconductive liquids. The energy is limited to roughly 10 – 20 mJ. To be hazardous, the voltage involved must be above about 20 kV, the surface polarity must be negative, a flammable atmosphere must be present at the point of discharge, and the discharge energy must be sufficient for ignition. Further, because surfaces have a maximal charge density, an area of at least one hundred $cm^2$ has to be involved. This is not considered to be a hazard for dust clouds.

- Propagating brush discharge is high in energy and dangerous. Occurs when an insulating surface of up to 8 mm thick (e.g., a Teflon or glass lining of a grounded metal pipe or a reactor) is subjected to a large charge build-up between the opposite surfaces, acting as a large-area capacitor.

- Bulking brush discharge, also known as cone discharge, occurs over surfaces of charged powders with resistance above $10^{10}$ ohms, or also deep through the powder mass. The energy involved depends on the grain size of the powder and the charge magnitude and can reach up to twenty mJ. Larger dust volumes produce higher energies.

- Corona discharge is an electrical discharge caused by the ionisation of air surrounding a conductor carrying a high voltage. It represents a local region where the air has undergone electrical breakdown and become conductive, allowing charge to continuously leak off the conductor into the air. A corona discharge occurs at locations where the strength of the electric field (potential gradient) around a conductor exceeds the dielectric strength of the air. It is often seen as a bluish glow in the air adjacent to pointed metal conductors carrying high voltages and emits light.

Of the five types of electrical discharge above, three can be classed as forms of ESD event. Such as a discharge that can create spectacular electric sparks (lightning, for example is an ESD event on

a large scale). In addition, less striking forms, which cannot be seen or heard yet, can be enough to cause damage to sensitive semiconductor devices this includes corona discharge from sharp electrodes and brush discharge from blunt electrodes. In addition, three key factors have furthered the increased in ESD vulnerability of today's semiconductors these being: -

- Smaller manufacturing geometries - As manufacturing geometries for today's most advanced ICs decrease to 90 nm and less, the voltage and current levels that can cause ESD related failures for these devices also decrease. ESD damage can occur due to excessive voltage, high current levels, or a combination of both. High voltages can cause gate oxide punch-through, while excessive I2 R levels can cause junction failures and metallisation traces to melt. Therefore, as manufacturing geometries decrease, the voltage and current levels that can cause these failures also decrease. This has made it difficult to provide even relatively low levels of on-chip ESD protection.

- A reduction in on-chip protection as increased susceptibility to ESD damage has been widely publicised. The industry council on ESD target specifications announced a move to reduce the standard level of on-chip ESD protection, making external ESD protection circuits even more critical for adequate system reliability. The focus of the industry council's efforts is to reduce the level of on-chip ESD protection, primarily aimed at providing adequate levels of ESD protection for manufacturing environments. The council are not suggesting reducing system level ESD protection, which must remain at existing levels.

- The changing application environment as evolved due to the proliferation of laptops, mobile phones, MP3 players, digital cameras, and other hand-held mobile devices, used in uncontrolled environments (i.e., no wrist-grounding straps or conductive and grounded table surfaces). In these environments, people touch I/O connector pins while connecting and disconnecting cables. Devices are subjected to constant ESD stress as users plug cameras, games, and other devices into their USB and video ports. A portable device can also build up a charge during normal usage and discharge that energy when connected to another device, such as a computer or a TV. The simple act of walking across a synthetic carpet and touching an exposed port on the outside of a digital TV can result in an ESD discharge greater than 35 kV. ESD discharges can occur directly at the port or can be discharged through a cable. This scenario is particularly dangerous to electronics equipment because the entire charge bypasses the connector's ground shield (if it has one) and is discharged directly into the system's electrical circuits.

The above charge / discharge shows how a charge imbalance is developed and how the ESD event is transferred when charged (There are three models one of these the human body model is discussed in the next section). The next phase of an ESD event in a semiconductor is how a device responds to this pulse of charge.

Once an ESD event is instigated, charge begins to rearrange in the device. This movement of charge induces voltage and generates currents. An ESD event is simply a restructuring of charge and thus the mechanism for this is charge driven. The degree at which charge transfers specifies the currents within, and the capacitance of the structure they move into specifies the final voltage. The voltage developed also has a momentary component specified by the result of the current and the impedance of the conducting pathway.

How a device survives these voltages and currents determines if the operation of the device continues properly. The following considers the discharge paths taken through an IC. A challenge in designing a device is comprehending the various current paths that are being designed and also their thermal, parasitic, and electrical characteristics.

Therefore, the starting point for comprehending the response to an ESD event is to consider the construction of a typical IC package as shown in figure 3.7: -

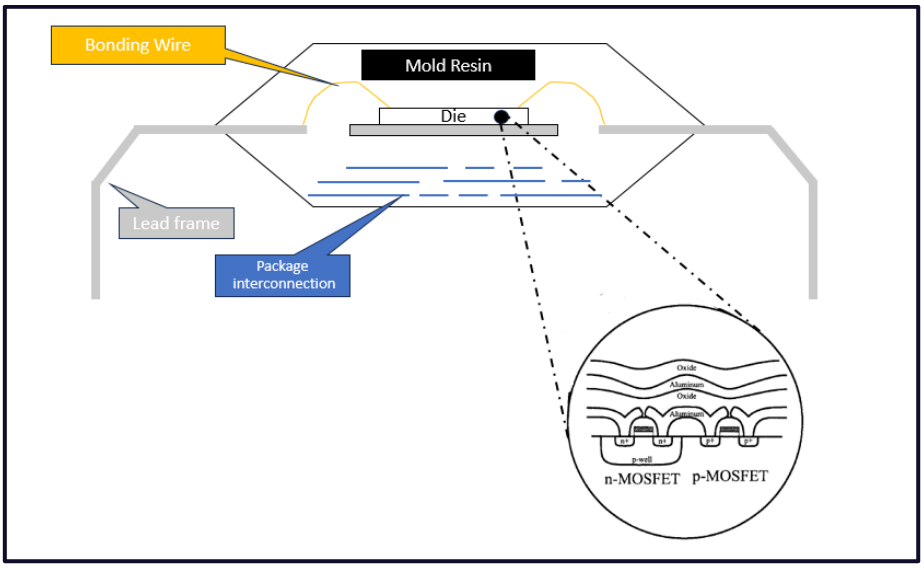


*Figure 3.7 Typical IC package construction [76]*

A die is located in a package and connected to the external world through bond wires and the interconnection of the package. The ESD event conducts through these pins. Firstly, the ESD event charge from an ESD pulse moves through the package interconnection and then the die. The package interconnection operates as a supplementary impedance between the ESD event and the die.

The resistance, inductance and impedance are important because the higher the resistance more of the energy from the ESD pulse is dissipated before it reaches the die, and the rising current pulse is slowed by the higher resistance. Also, more protection is given to the circuit with a higher impedance.

Therefore, the ESD pulse is affected by these factors, however, these factors also affect the incoming electrical inputs in the same way. In a high-performance package to get the best operation from the circuit, impedance is minimised. The equivalent circuit in a package as perceived by an ESD event is shown in figure 3.8: -

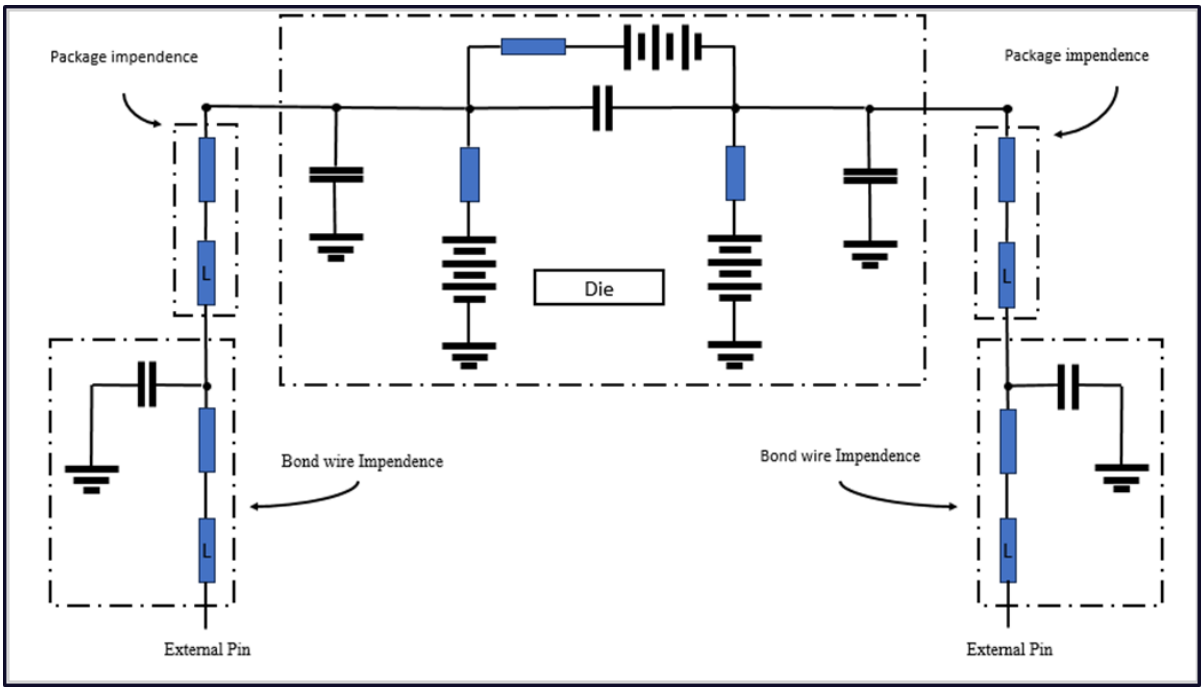


*Figure 3.8 Equivalent circuit in an ESD event for an IC package [83].*

The stored charge in the package is amongst the various conducting planes. The largest plane is in the die connected to the surface. At this point, the charge is amassed in the different isolation technique being used these are junction isolation, dielectric isolation, or silicon on insulator used by the circuit to separate each transistor.

Reducing the capacitance at die-level lowers the amount of charge amassed and increases the charged device tolerance. This can be seen by higher charged device thresholds for smaller devices as opposed to larger packages with similar technologies.

Therefore, the next location is the die for the charge's path. In the IC the functioning, part of the device is enclosed in a slender layer at the top of the silicon die, as shown in figure 3.7. This slender area has conductive layers connecting each circuit component to form the functioning circuit. As the charge moves through the die, it sees both passive and active elements.

Figure 3.9 shows an uncomplicated ESD protection system. Considering with the case of an unshielded input, the resistor and diodes would be eliminated, therefore allowing the exposed gate oxide to soak up the ESD event and in this case the threshold would be exceptionally low. The ESD charge travels throughout the circuit sections used to execute its function and the parasitic factors that exist in circuit operations but are not operational normally.

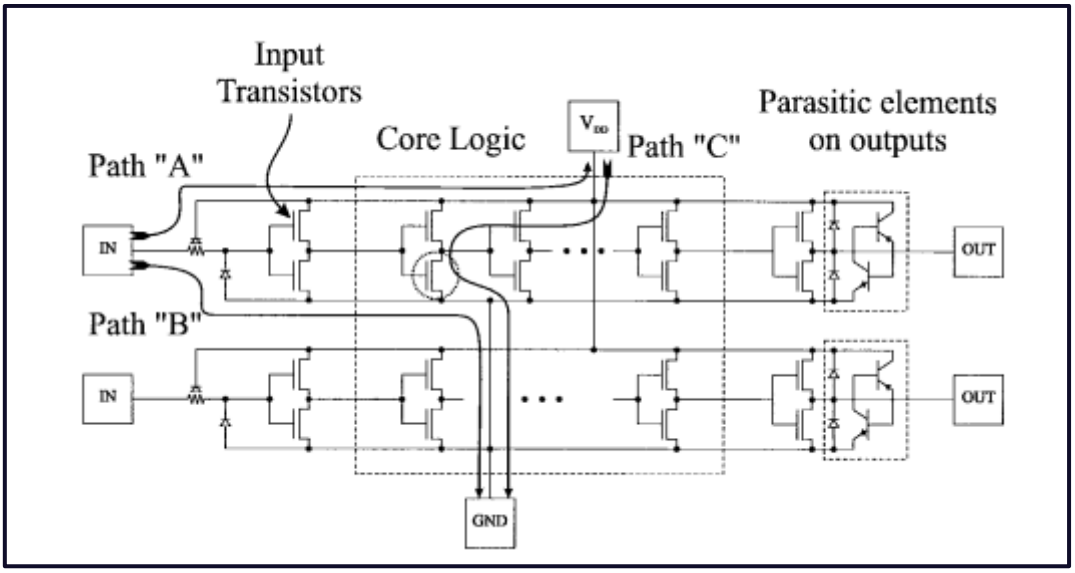


*Figure 3.9 Uncomplicated ESD protection system. [83].*

The parasitic factors are enabled by the conduction path. when a set of voltage or current situations is established. Thus, the parasitic factors are identified during unusual activities in ESD testing. An example of this is that in particular devices constantly degrade at five hundred volts with the HBM ESD test, but the same design always succeeds at one thousand volts. This inexplicable result arises because separate conduction channels are operational, and based on the level of the ESD event it can produce different internal voltages and power dissipation within.

Figure 3.9 also shows instances of some parasitic mechanisms. The parasitic bipolar transistor in the NMOSFET is an example of this. This device helps dissipate the charge by going into snapback (snapback will be discussed later) during breakdown. Once snapback is entered the terminal voltage is decreased, thus reducing the power dissipated. This protection model is similar for all protection systems. Therefore, allocating a low impedance discharge protection route around the circuit. However, the problem with this, is in creating a useful ESD protection circuit that does not impede normal device process.

In HBM, the charge inputs at one pin on the IC and outputs via another pin. Therefore, pins are stressed in pairs. Thus, all through ESD testing, each pair of pins arrangement is under strained condition with both positive / negative currents. It should be noted that a machine model (MM) ESD event as the same conditions as HBM ESD event. However, in contrast, a charged device model (CDM) ESD event, the charge exists within the circuit; therefore, the discharge is via one pin at a time [41]. Thus, all combinations of pins must be protected for acceptable shielding of the circuit, [42].

The magnitude of the current pulse defines which path or paths conduct the charge therefore making the conduction path transferred in a circuit difficult to predict. In figure 16 three potential current paths for an HBM ESD event can be seen these are paths A, B, C. Path “A” presumes that a positively charged body interacts with an input pin. The return path is presumed to be the positive supply pin. In this case, the input protection diode is in forward conduction. Consequently, the voltage and power dissipation drop across the diode is low. The power dissipated is high and is virtually all of the capacity of the diode. Dissipation of the power is over a region, spreading away from the metallurgic junction towards the anode and cathode connections. Therefore, the power density is low for a device. This is the most robust conduction mode for the diode.

In path “B” the diode would be in its worst conduction mode when the conduction path is changed to the ground pin in its place of the supply pin. In this situation, the diode is acting in reverse-bias avalanche breakdown mode, and the diode’s breakdown voltage is far higher than the forward voltage, therefore the dissipated power is incredibly high in the element. Generally, all of this voltage is released throughout the narrow depletion region positioned around the metallurgic junction. This translates to a high-power density and a small dissipation volume. Therefore, a bigger diode is desirable to dissipate this energy in an ESD event that triggers a reverse breakdown conduction mode.

The conduction mode in path “C” (figure 16) is the capacitive coupling of an event to an internal element this is often overlooked. Applying an ESD event pulse to $V_{DD}$ triggers the voltage on $V_{DD}$ to change quickly. A large p-channel MOSFET gate capacitance transmits the fast *dv / dt*

signal to an internal logic node. Therefore, the smaller transistor (circled) is destroyed by the resulting current $I = C\,dv / dt$.

Damage comes from high current intensities' shorting the drain to source of the transistor. The previous paragraph demonstrates three conduction methods that can occur during an ESD event in an IC. The linear conduction methods are easily understood these being: -

- $V = IR.$ (3.2)
- $I = C\,dv / dt.$ (3.3)
- $v = L\,di / dt.$ (3.4)

and needs not to examined in this thesis. There are also nonlinear conduction methods / processes, and every single one is showed with its typical I–V characteristic these are: -

- Forward conduction (Figure 3.10): - [83]
  - Power dissipated over entire region of the device.
  - Parasitic resistance controls power dissipation.
  - Total power dissipation is low to medium.
  - Full recover of device is possible.

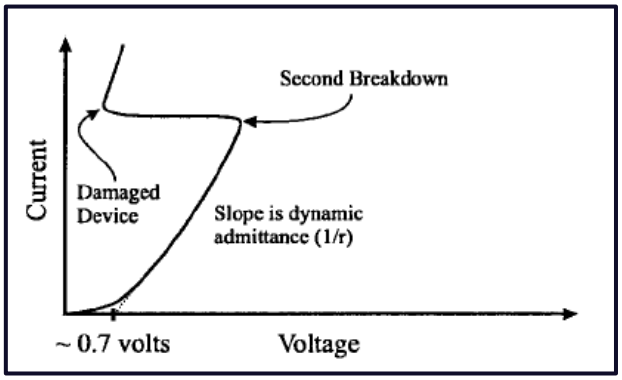


*Figure 3.10 Forward conduction [83]*

- Junction breakdown (Figure 3.11): - [83]
  - Power dissipated in depletion region.
  - High power dissipation.
  - High power density (small volume).
  - Parasitic resistance controls current capability
  - Full recover of device is possible.

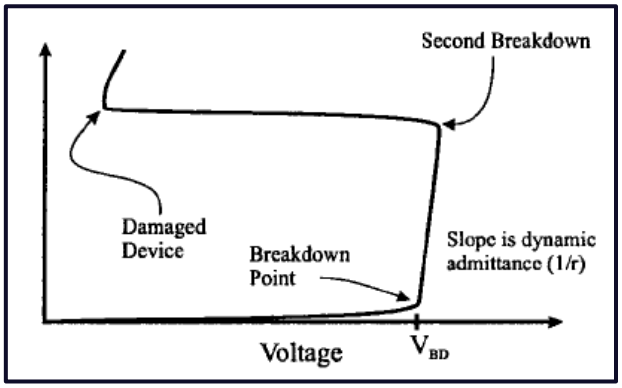


*Figure 3.11 Junction breakdown [83]*

- Junction avalanche dielectric charge injection (Figure 3.12): - [83]
    - Electric field at surface controls injection.
    - Oxide charge generated by current flow.
    - Physical change in microstructure of oxide.

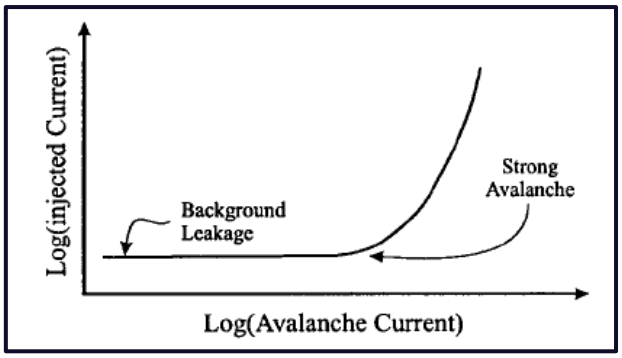


*Figure 3.12 Junction avalanche dielectric charge injection [83]*

- Dielectric breakdown (Figure 3.13): - [83]
    - Electrical field causes current flow in oxide.
    - Field intensity exceeds dielectric strength causing a short.
    - Energy stored in capacitor discharged into a small site causing rupture.
    - Physical change in microstructure of oxide.

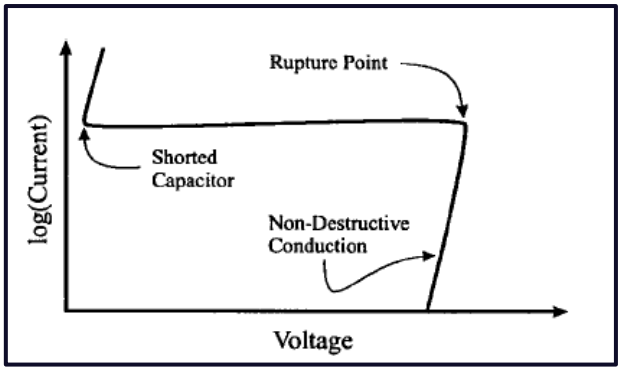


*Figure 3.13 Dielectric breakdown [83]*

- Snapback (Figure 3.14): - [83]
    - Bias voltage exceeds trigger voltage, $V_{T.}$
    - Terminal voltage decreases to sustaining voltage, $V_{s.}$
    - Lowering voltage reduces power dissipation.
    - Parasitic resistance controls terminal voltage and power dissipation.
    - Full recovery of device possible.

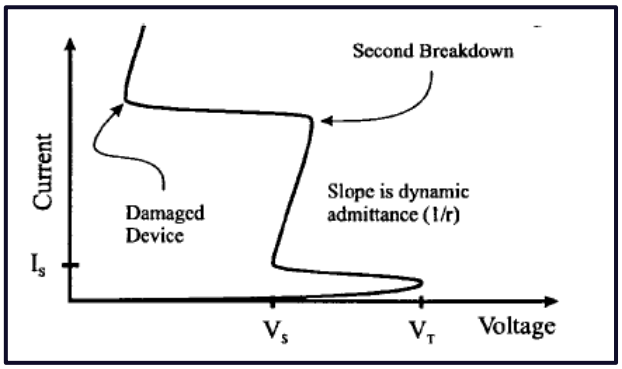


*Figure 3.14 Snapback [83]*

- Silicon controlled rectifier (Figure 3.15): - [83]
    - Conduction triggered by displacement or avalanche current.
    - Terminal voltage extremely low.
    - Good protection component.
    - Full recovery of device possible.

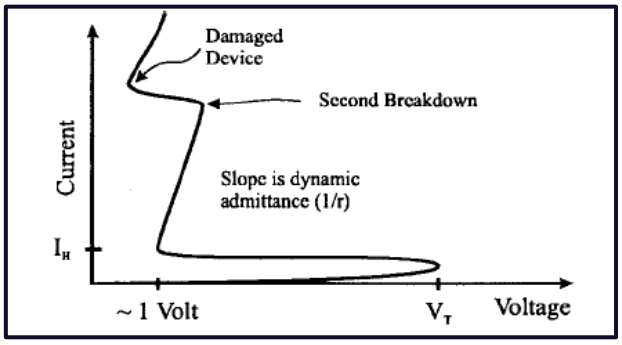


*Figure 3.15 Silicon controlled rectifier [83]*

Each conduction method above has a total amount of current (upper limit) that is permitted without damage being done. Charge injection and dielectric breakdown are two methods that can cause physical changes to the dielectric stratum that are problematic if not difficult to anneal out. Therefore, damage to the circuit results if one of these methods is active.

The two best conduction methods are forward conduction and silicon-controlled rectifier (SCR) action because these generate the lowest power and spreading it over the largest volume. Note that with SCR protection, the risk of latch-up increases. Then snapback is next, with junction breakdown as described earlier being the worst. With each protection method there are trade-offs to be considered.

Figures 3.16 and 3.17 show from an ESD event perspective two types of design and or geometry layout flaws. Figure 3.16 shows a device layout that causes a non-symmetric current density along its width [43].

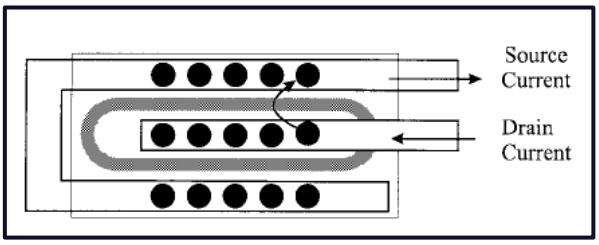


*Figure 3.16 No symmetric current density showing a Drain to Source short [83].*

In the drain and source regions the resistance reduces the bias in the remaining width, thus the transistor conducts a lot of the current at one end. This results in damage near to the entering metal. Therefore, so that no single spot carries all the current it is vital that the entire width conduct evenly [44] [46]. In this stress condition a short develops in the drain-to-source. A better design is showed in figure 3.17 this permits a symmetric current flow.

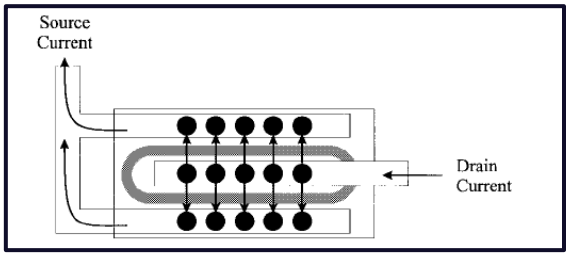


*Figure 3.17 Symmetric current density allows better current flow [83]*

Figure 3.18 shows a transistor made of silicon on sapphire (SOS) sectioned across the channel width. Where the polysilicon steps down the side of the mesa are regions of high field points. When an ESD event occurs voltage transients can rupture the oxide at these points prior to the normal gate being damaged.

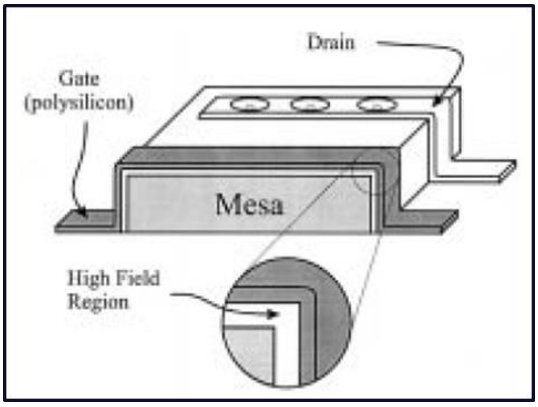


*Figure 3.18 Silicon on sapphire sectioned. [83]*

Transistors exposed to ESD voltage transients should feature a circular design, as seen in figure 3.19. This circular design eliminates the high field points and manufactures a more durable arrangement against ESD damage. Processing defects can severely affect the ESD performance of device structures.

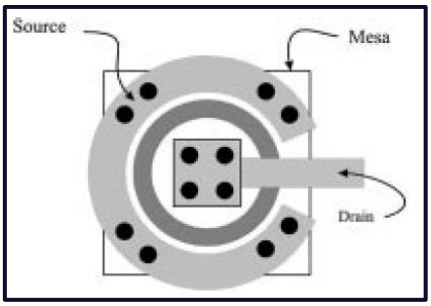


*Figure 3.19 Circular designed transistor to eliminate high field points [83]*

Figure 3.20 shows a picture of a transistor taken with an emission microscope image (EMMI) as the drain voltage comes close to breakdown. This tool can be used to perceive low levels of light that accompany five electrical incidents these being: -

1. Avalanche luminescence.
2. Dielectric luminescence.
3. Forward bias emission,
4. Thermal radiation.
5. Saturated luminescence.

The light released shows that the junction is in breakdown at this spot. What is here is a crystal defect that reduces the area breakdown voltage at this spot. Therefore, at this point attracts nearly all if not most of the energy during a ESD event.

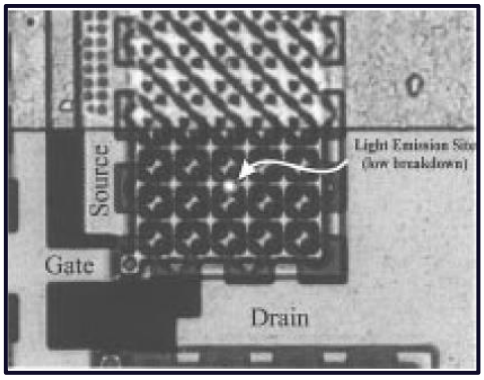


*Figure 3.20 Transistor with drain breakdown. [83]*

Figure 3.21 displays the damage after an electrical over stress (EOS) event caused by an ESD event. Evidently, the defect site reduced the tolerance of this component. It is problematic, if not incredible hard, to design around defects within the process. Because of the random nature with which defects happen testing is also not a viable option and the necessary stress conditions to detect them.

The only actual technique is to decrease their numbers by continuous improvement methods of the process of wafer-fabrication. This can be done by designing experiments, test configurations and test systems that are able to detect the important defects.

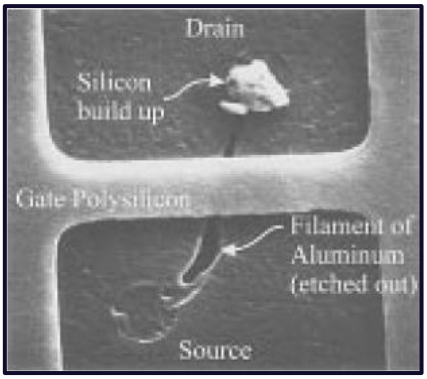


*Figure 3.21 Damage from EOS. [83]*

In the methods above, enhancements in wafer processing are vital to decrease the defect concentration, but some enhancements in wafer processing also reduce the ESD tolerance. Examples of this are lightly doped drain (LDD) structures and silicide junctions. LDD structures minimise the threshold of devices and silicide junctions reduce contact resistance [43], [44], [47].

LDD structures have an effect by expanding the resistance across a transistor and changing the conduction attributes during the ESD event in the transistor. These changes can create extreme power dissipation, causing damage to the transistor at lesser threshold points as seen below in figure 3.22: -

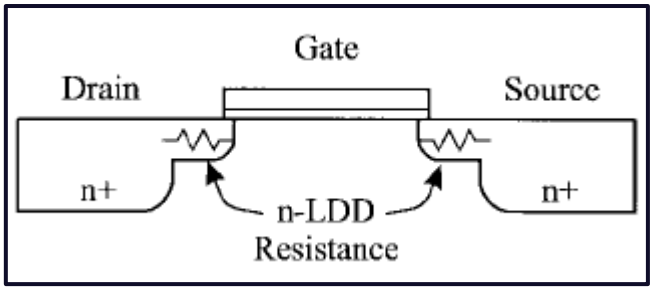


*Figure 3.22 Lightly doped drain structures. [83]*

The silicide material resistance is low and laid on top of the normal drain / source diffusion see figure 3.23. Therefore, the comparative resistance of silicon to silicide is high, nearly all of the current is carried in the incredibly thin silicide area. The minimal resistance of the silicide also lowers the natural balance of the current across the breadth of the transistor. Therefore, with the silicide present, all the current may flow in a tiny section of the total transistor. Subsequently this can cause the current intensity to increase, therefore causing damage to be produce easier.

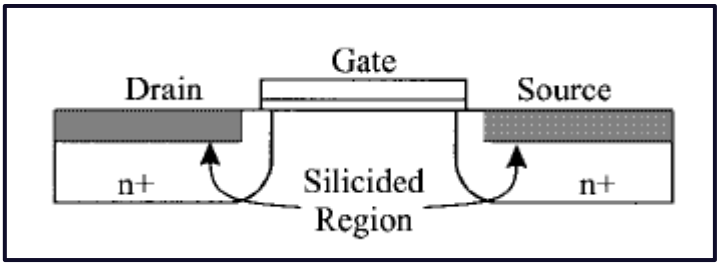


*Figure 2.23. Silicide junctions. [83]*

These sophisticated techniques should be cautiously used in components designed to absorb ESD events. These examples demonstrate that all viewpoints of a process must be assessed against how it effects the ESD ability of a completed product.

## 3.6 The Outcome of ESD event on a Semiconductor

The last step of an ESD event is evaluating the failure after an ESD event is over. The first question that must be asked is, “Did the circuit, die, wafer, survive?” To evaluate this a clear explanation of the malfunction is required. To define the point of malfunction the electrical test requirement is used. The test requirement classifies the leakage, drive current, timing tests, and functional tests that must be effectively completed to be deemed reliable. A parameter for the test will have limits on how much the test is allowed to change. Delta limits are considered during this. When making appraisals between numerous parts or technologies, it is imperative to know the ESD tester specification and the test criteria used [48] [49].

This guarantees that the outcome can be evaluated. It would be inappropriate to compare the ESD thresholds of different semiconductors within this thesis because this thesis concentrates on power MOSFETs. As discussed, previously, there are three types of failure: -

1. Soft failure.
2. Catastrophic failure.
3. Latent failure.

As stated, previous soft failures are not discussed in this thesis. Catastrophic failure will be discussed in this section. Latent failure will be addressed later on. The maximum voltage applied without failure is used for all of the failure classifications in use based on voltage levels. These voltages are the open circuit voltage of the charged capacitor in the previous discharge models.

The classifications are used as a benchmark for individuals holding components. The lower the rating, the more susceptible the component is to an ESD event, and the more safeguards are needed to be put in place to protect the components from an ESD event.

The following is a classification standard used worldwide there are others, and these are listed in appendix 1. Table 3.4 lists the classification standard for ESD failure threshold classifications for HBM based on ANSI / ESDA / JEDEC JS001-2023 revised from ANSI / ESDA / JEDEC JS001-2017- ESD Association Standard Test Method for the Protection of Electrostatic Discharge Sensitive Items - Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) Testing - Device Level.

*Table 3.4 ESD failure threshold classifications for HBM based on JEDEC-JS001. [94]*

| Classification | Voltage Threshold |
|---|---|
| Class 0Z | 0 to 49 volts |
| Class 0A | 50 to 124 volts |
| Class 0B | 125 to 249 volts |
| Class 1A | 250 to 499 volts |
| Class 1B | 500 to 999 volts |
| Class 1C | 1,000 to 1,999 volts |
| Class 2 | 2,000 to 3,999 volts |
| Class 3A | 4,000 to 7,999 volts |
| Class 3B | 8,000 volts and above |

Class 0Z is a component / part that is most sensitive and thus requires further safeguards beyond what is typically used in production of semiconductors. These safeguards can include dedicated people, dedicated work areas, and dedicated packaging materials. Because of the cost, these dedicated safeguards would be used for only the parts that require it. However, these safeguards can be used for all parts.

Circuit-level breakdowns are apparent as a change in a measurable parameter. For example, these can be: -

- Input leakage.
- Supply current.
- Bias current.
- Offset voltage.

In extreme cases, the total loss of functionality occurs. The function and circuit design dictate the susceptible limits. For example, in op-amps, the susceptible limits are: -

- Offset voltage.
- Offset current.
- Open loop gain.
- Common mode rejection ratio.

The weak points in the design are the input stage and compensation capacitors. When the input stage is broken, it becomes shorted or pulls more current. When a compensation capacitor fails, the output is fixed at a voltage and the component becomes non-operational. These two regions are complex to protect because they are exceedingly difficult to guard without reducing the components

operation. The compensation capacitor is tied to a supply pin on one side. Therefore, causing it to be immediately open to the outside. The input cell is constructed for low capacitance (small size) and a high impedance (large power dissipation). Together this allows an ESD event to cause damage easily. Digital circuits fail with rises in input or output leakage and additional supply current. It should be noted that analogue parts are more difficult to protect than digital parts as a rule. ESD failures are caused by at least one of three sources: -

- Localised heat generation.
- High current densities.
- High electric field intensities.

An ESD pulse is modelled as a time variable current source. When the current passes within an IC, an internal current path is created. The conduction routes liable for this path define the current densities observed and the voltages developed.

The product of voltage and current density expresses the power density produced. Heating (Joule) instigates locally rising temperatures. The thermal resistance and thermal mass in the region of power dissipation specify the final temperature reached.

For protection circuits, it is preferred to keep the current density in a circuit element uniform so no position sources of power dissipation happen, Silicon has a negative resistance association with temperature, therefore an incredibly high-power dissipation in a small area will result in greater temperatures and thermal runaway.

For MOS circuits, the electric field intensity denotes the voltage developed throughout the junctions and dielectric in the circuit. The most susceptible dielectric is the gate oxide because it is the thinnest. The most likely positions for focusing the electric field are the sharp corners in layouts and structural defects, making breakdown more likely at these points.

Each ESD event can be tracked by five fundamental damage processes. It should be noted that one or more of these can happen at any time. The processes are as follows with a schematic and failure model for each: -

- Filamentation (Figure 3.24) is caused by: - [83]
    - Current flows in localised regions creating a melt filament.
    - Redistribution of dopant atoms plus crystal damage cause high field and leakage currents.
    - Shorted junctions occur in worst case situations.

- Correction of filamentation is done by reducing defect densities and ensuring that there is uniform current flow across junctions.

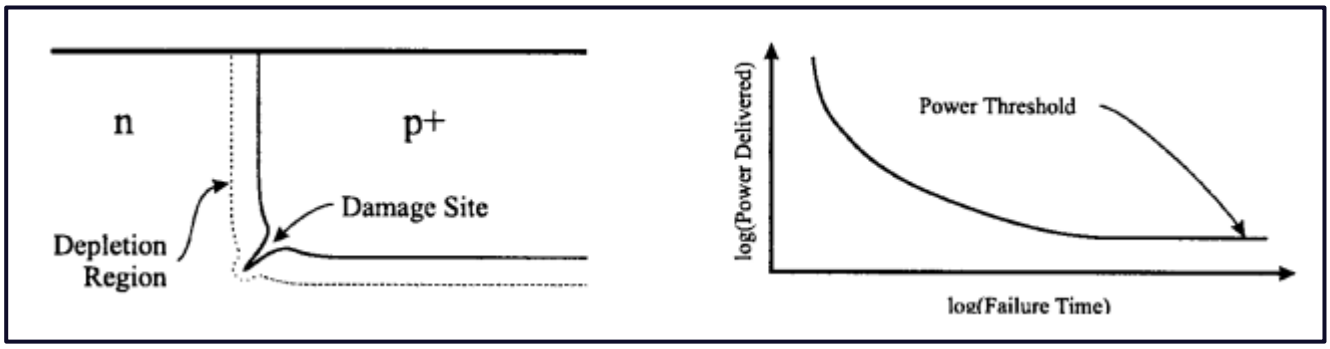


*Figure 3.24 Filamentation [83]*

- Charge injection (Figure 3.25) is caused by: - [83]
  - Avalanche breakdown of junction injecting hot carriers into oxide layers.
  - Shift in surface threshold affects $V_T$ in MOSFET, $h_{fe}$ in Bipolar Junction Transistor (BJT) and breakdown voltages in diodes.
  - Correction of charge injection is done by minimising electric fields at junction surface.

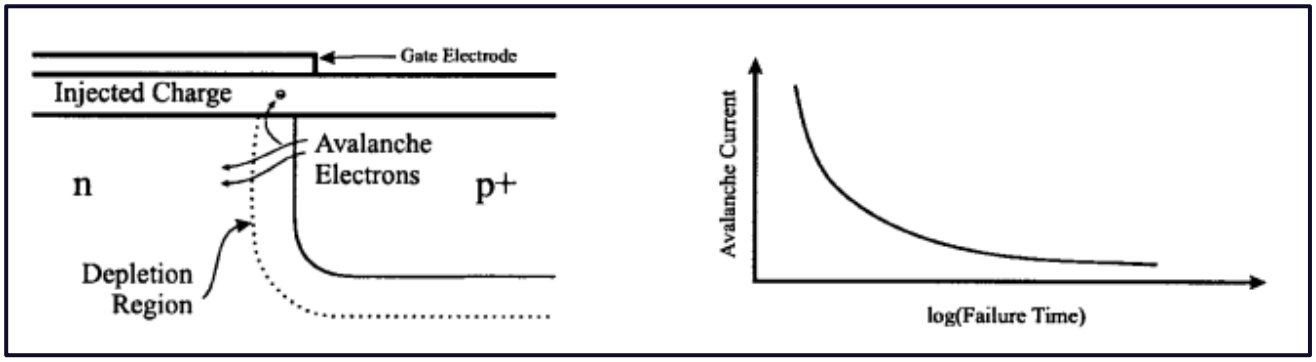


*Figure 3.25 Charge injection. [83]*

- Oxide rupture (Figure 3.26) is caused by: - [83]
  - ESD current induces voltages.
  - Developed electric fields exceed dielectric strength resulting in a rupture of the dielectric.
  - Correction of oxide rupture is done by minimising sharp corners.

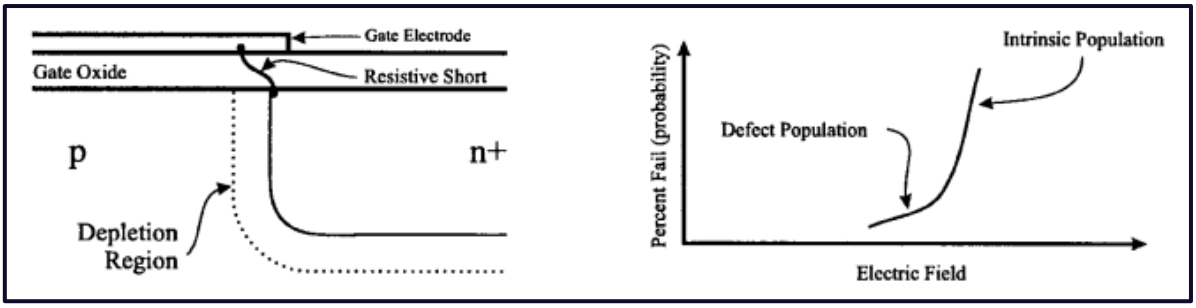


*Figure 3.26 Oxide rupture. [83]*

- Thin film burn-out (Figure 3.27) is caused by: - [83]
    - Power density un the film exceeds its capability.
    - Heating (Joule) causing film to melt resulting in fusing.
    - Correction of thin film burn-out is done by increasing cross sectional area and using film with a higher melting temperature.

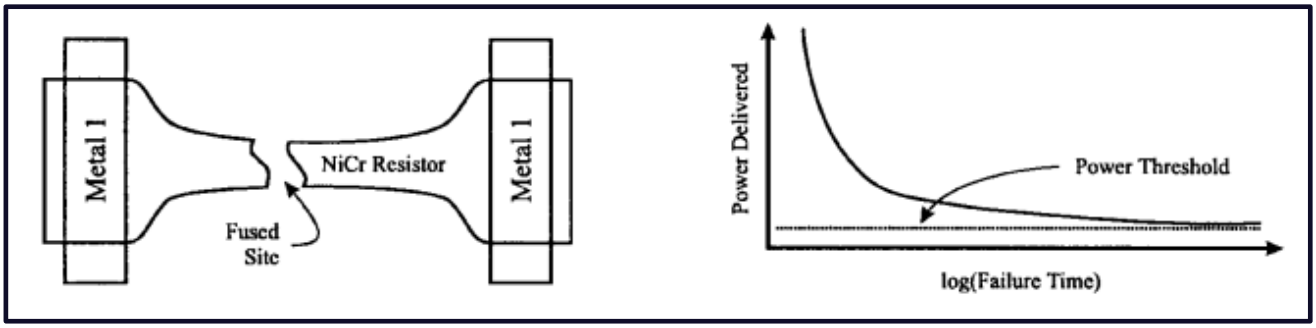


*Figure 3.27 Thin film burn-out. [83]*

- Contact spiking (Figure 3.28) is caused by: - [83]
    - Failure mode is similar to filamentation.
    - After second breakdown a melt filament intersects an aluminium contact.
    - An interchange of aluminium and silicon takes place shorting the junction.
    - Correction of contact spiking is done by spacing contacts away from the junction and insuring uniform current flow across the junction.

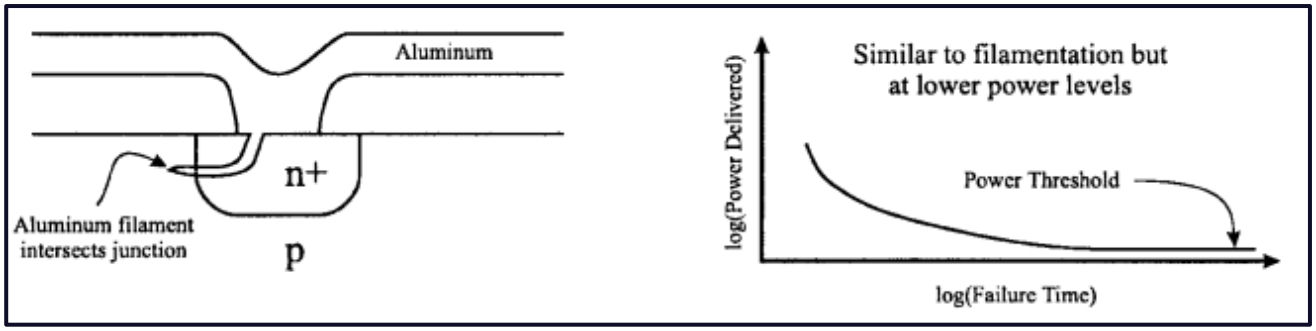


*Figure 3.28 Contact spiking. [83]*

The most common damage processes are filamentation and oxide rupture. Contact spiking is related to filamentation. Thin film burn-out is most common in circuits with thin film resistors composed of a nickel–chromium (NiCr) alloy. The least common is charge injection, which is oxide charging by avalanche injection of carriers into the oxide. In most instances, the charging conduit results in an oxide rupture instead of trapping charge in the oxide layers.

Oxide rupture is prevalent in MOS technologies [50]. Thus, the induced voltage surpasses the dielectric strength of the oxide, causing a rupture. For example, in figure 3.9 typically, the input transistors gate oxides are those that get damaged by ESD events. Therefore, the protection circuit does not clamp the induced voltage caused by the ESD event to a sufficient low level to prevent rupture from the gate to the source, drain or body, of the transistor. Under the gate material a tiny crater is formed where a conductive track is established in the dielectric.

In ICs, the gate oxide is not the only problem. MOSFET and bipolar procedures are capable of having dielectric ruptures in oxides overcharged circuitry. This could be the oxide growing in an isolation area or over a diffused resistor. If a conductor occurs on top of an oxide, a rupture could happen.

Junction filamentation causes a surge in the reverse bias leakage of a p-n junction. So, in these, situations the junction is shorted. In the junction the ESD event causes current to flow. Therefore, in the junction the dissipated power rises the temperature until an area of silicon dissolves. When silicon dissolves, its resistance decreases by a factor of 30 [51]. The increasing current in the dissolved area, will promote rising temperatures leading to further heating in the area, conducting to thermal runaway. This occurrence is a secondary breakdown [52]. The dopant material rearranges along the dissolved path. Once the event is over, the power dissipation stops, and the silicon solidifies. The electric field is greater at this point, increasing junction leakage. The site will grow to a shorted junction if the current level stays high, or the junction is in secondary breakdown for a prolonged

time. In bipolar junction transistors (BJT's) the base emitter junction is vulnerable to filamentation damage.

A similar process is contact spiking, but the dissolved area grows until it interrupts a metal contact, therefore causing the aluminium and silicon to switch. The aluminium contacts damage thresholds are lower level because the aluminium-silicon mixture is a eutectic mixture that develops at 577° C instead of silicon's melting point which is 1415° C or aluminium's melting point which is 660.3° C [44], [53].

Thin-film fusing involves every film in a circuit. These include the polysilicon interconnects, metal interconnect, plus diffused and thin-film resistors. The most susceptible circuits are ones with thin film resistors. Many circuits use nickel–chromium (NiCr) alloy resistors as a precision, resistance element. These resistors have exceptionally low thresholds for fusing and are thin (~200 Å) [54] [60]. Davidson et al describes the fusing mechanism in [54]. During designing of the resistor, it is especially important that the resistor is designed sufficiently wide to handle an ESD event for the level of protection required. NiCr power densities greater than 3875 W/mm2 fuse in less than 10 µm with a fusing threshold of 2325 W/mm2 [54].

Oxide charge injection by avalanche breakdown is the last mechanism to be discussed. Oxide charge injection by avalanche breakdown transpires when an ESD event triggers a reverse-biased junction to conduct by avalanche multiplication. The carriers have sufficient energy to overcome the energy barrier that oxide-silicon forms. The barrier is smaller for electrons so are more likely to be injected than holes [61].

In a MOSFET If the junction is the drain, then, a change in the threshold voltage results [50]. But there is an insignificant range where parts are damaged by charge injection however oxide rupture does not result [60], [62]. The amount of degradation in oxide reliability is also connected to the current density of the injected charge plus the total charge injected [61] [65]. During a drain avalanche a localised injection of charge for the period of an ESD transient produces more damage than uniform conduction from the gate junction to the body of the transistor [65].

Also, this process can affect bipolar transistors. When the emitter-base junction is affected, the low current $h_{fe}$ shifts. The space charge region at the junction surface, is distorted by the injected charge therefore the leakage current increases from base to emitter. In the next part of this section Latent (time dependent) failures is discussed

There is and has been concern over latent failures as a result of ESD damage for many years within the semiconductor and electronics industries and continues to be a controversial subject in the

21st century. This may have been because of the low testability of semiconductors in general in the 20th century. Latent damage is still being discussed between manufacturers and clients when malfunctions are assigned to ESD events after a period of time. The company wants to produce components that are reliable, but the company has invested a lot of time and money in the components so needs to ship the components or start to lose revenue. The client wants a guarantee that the manufactured components will not have additional faults if the client decides to use the component which could affect the products of the clients. So, to understand what latent failures the company needs to understand the following.

Latent (time dependent) failures can have numerous meanings in the perspective of ESD events. For latency to be understood, it is imperative that the company bear in mind that an ESD event is a casual event at a set point in time. This event is comprised of a limited amount of energy delivered to a component in a limited amount of time. Also, the company must remember that when the event is finished, that event can no longer cause damage to the component. When damage happens, it is by a degrading chemical process. This event is outside the normal operational range of the component and is a form of EOS. Therefore, successive ESD events are further modes of EOS and should not be thought of in terms of latent damage.

The dependability of the component is regarded as the ability of the component to operate for a stated amount of time given a fixed set of operational circumstances. Therefore, if the component fails to operate under these circumstances, then it is a reliability failure. These malfunctions are caused by chemical processes which can alter the device specifications. Examples of this is that the component may become non-operational, or the current leakage may rise increase. Also examples of the failure processes are mobile ionic contamination and oxide rupture.

During wafer processing or assembly when the component was produced, these failure points were manufactured into the component. If the problem was instigated at a point caused by ESD damage, then the component failed because of “ESD damage latency” understanding this, the following descriptions can be made: -

1. Latent ESD failure: - An ESD event that is time-dependent failure that causes damage but not detected after the event as happened and causes a stable noticeable failure with successive use in normal operational conditions. If the component damage is discovered preceding its use, then, the component is rejected.

2. ESD threshold: - The ESD event voltage level referenced to a particular ESD discharge model that is able to produce detectable damage with a quantified set fixed number of tests.

3. Testability: - A measure of the capability of a set of tests to detect defects, damage, and changes in function of a component. These tests can incorporate any AC tests such as timing measurements, DC tests such static parameters, and supply current, input leakage, etc., and functional tests. Data-analysis processes are also categorised in this section as well.

Latent (time dependent) damage can be seen as dielectric rupture, junction breakdown, and polysilicon resistor damage. Therefore, a component that is subjected to an ESD event may be partly damaged but may keep on performing its expected function. Nonetheless, the operational life of the component may be decreased considerably.

So manufactured goods or systems incorporating components with latent failures may experience an untimely malfunction after the client inserts the component in a product that the client has manufactured (For example an electric car). These failures are typically expensive to repair and, in some products, could cause hazards dangerous to people etc.

With the correct test equipment, it is easy to prove that a component has suffered a catastrophic failure or that a component has started to break down and fail test limits. Simple performance tests will prove component damage. But latent failures are practically impossible to verify or discover using the present test technology, particularly after the component is inserted into a completed product. Latent failures may require new test techniques to be created.

If testing concerns are incorporated into the design, of the semiconductor then it makes identifying and eliminating failures easier, enhancing both the quality and dependability of the component. The design of the semiconductor can make tests more efficient if the design minimises the use of current sources and free running oscillator circuits within the semiconductor.

Selecting the proper test condition can also be an important aspect of increasing the testability of the device. For example, the temperature of a SOS component under test. A SOS component can be more sensitive to revealing gate oxide defects to temperatures as low as - 55° C or below. The SOS material within the component was found to have leakage current dependent on temperature. But at normal temperature in this case 15° C to 25° C (room temperatures), the SOS material component leakage concealed every gate oxide defect. Therefore, low temperature testing eliminated, the SOS leakage and gate oxide defects were observed in the component. Also, the detection limit on power MOSFET is much higher on the tests used within the company because of the substantial amounts of current consumed. The ESD threshold level within the tests is reliant on its previous history.

As stated above ESD events not only lessen yields but can also create a component that is damaged but goes unnoticed by testing, and in the future, becomes the cause of a latent failure. These component with latent ESD defects can be considered to be “walking wounded” because they have been degraded, but not damaged enough to be destroyed, by an ESD event. As stated above this happens when an ESD pulse is not strong enough to damage a component, but nonetheless causes damage.

Frequently, the component experiences junction degradation through increased leakage or a decreased reverse breakdown, but the component continues to function and is still within data limits. The component can be exposed to numerous weak ESD pulses, while operational with each consecutive pulse further damaging a component until, finally, there is a catastrophic failure. As stated, there is no known common practical tests to screen for these components. To avoid this type of damage, devices must be given continuous ESD protection, as explained later.

The situation between manufacturers and clients over latent failures can be solved by rectifying the source of the ESD event. This can be fixed with personal being trained to handle components correctly also the grounding requirements on equipment within the company. After this is done, the components can be retested with tighter leakage and limits removing components that was damaged but were not discovered in previous testing. The component limits should come from a statistical assessment of each parameter and the outliers are to be eliminated from the component circuits.

It should be noted that, most studies are at odds with one another as to what degree of ESD damage can be credited to latent failures. On one hand some research papers argue that the quantity of components dispatched to clients with latent failures surpasses the amount that fail catastrophically due to ESD in production. On the other hand, other research papers argue that no failure process exists to demonstrate the existence of latent failures.

Of all the sources stated above the common source for ESD damage for a semiconductor manufacturer is the human body generating ESD and is discussed in the next section.

# Chapter 4 Human Body Model Electrostatic Discharge

## 4.1 History of the Human Body ESD Model

The Human body model developed in early days in the mining industry in the 1950s. Research reports discussed the issue of ESD within the mining industry. The first report was the Bureau of Mines, Report of Investigation 4833, U.S. Department of Interior, January 1952 by P.G. Guest, V.W. Sikora, and B.L. Lewis. A second article of interest was published by D. Bulgin. Static Electrification. British Journal of Applied Physics, Supplemental 2, 1953. Further pieces on this subject were published during the 1950s / 1960s.

Initial researchers of issues with the HBM standard were T.M. Madzy and L.A. Price II of IBM in 1979. They debated a test method titled "Module Electrostatic Discharge Simulator". This article showed that the simulator was used since 1974 in IBM. In 1980, H. Calvin, H. Hyatt, H. Mellberg, and D. Pellinen recommended amounts for the capacitance and resistance for the HBM ESD event for the fingertip and field-enhanced discharges in "Measurement of Fast Transients and Application to Human ESD," published in the 1980 proceedings of the EOS/ESD conference. The proposed capacitance of 110 pF and a resistance for the fingertip was averaged 1920 ohm, where the field-enhanced discharge was 120 pF and a resistance of 550 ohms.

In 1981, H. Hyatt, H. Calvin, and H. Mellberg investigated the human ESD event, published in the 1981 proceedings of the EOS/ESD conference, entitled "A Closer Look at the Human ESD Event." In January 1982 one of the first standards proposed for the HBM was military standard MIL-STD 883B Method 3015.1 referred to as "Electrostatic Discharge Sensitivity Classification,".

In 1983, R.N. Shaw and R.D. Enoch of British Telecom (BT) research laboratories printed one of the first publications on test equipment at the EOS/ESD Symposium, titled "A Programmable Equipment for Electrostatic Discharge Testing to Human Body Models." The system shown in the journal consist of a high-voltage power source, a series charging resistor for charging the 100-pF capacitor, a 1500-ohm series resistor, and a single mercury wetted relay switch that will eliminate switch bounce.

HBM commercial systems were first established for qualification and release of semiconductor components in the 1980s. However, there was no HBM wafer level commercial test system for semiconductor development, ESD library test and verification at this time. HBM ESD wafer level classification was feasible by lengthening the wires from the test socket to a workstation for wafer level and wafer probes. In the 21$^{st}$ century, HBM ESD wafer level test systems now exist

for development. To decrease turnaround time of semiconductor design and development, wafer level classification was introduced. HBM ESD wafer level testing can be used for device classification of passive and active elements in a technology library for HBM ESD technology benchmarking. HBM ESD wafer level testing can be done on ESD networks that will be introduced into a technology ESD library. In addition, HBM ESD testing of components can be done on a wafer to provide an initial observation before the first design pass.

## 4.2 Human Body Model ESD

The semiconductor industry has defined three basic models to describe how charge is transmitted during an ESD event. These are the Human Body Model (HBM), Machine Model (MM), and Charge Device Model (CDM).

- Human Body Model: - This standard is intended to simulate a person becoming charged and discharging from a bare finger to ground through the circuit under test.

- Machine Model: - This model is intended to simulate a charged manufacturing machine, discharging through the device to ground.

- Charged Device Model: - This model simulates an IC becoming charged and discharging to a grounded metal surface.

The models are based on the component holding the charge and the discharge impedance. These models define the equivalent circuit model and how testing and calibration will be done. These models intend to mimic reality but do not cover all conceivable variables that affect a real ESD event. Therefore, the models should be used only to compare robustness of unique design schemes and thus not an outright measure of a design's ESD capacity [65], [66].

In this section I will discuss the HBM model as it is the most popular ESD model tester used in organisations [67], and as stated in the previous section the human body is a source of ESD events that can damage semiconductor devices while being manufactured and cause damage to working systems.

As the name implies, it is designed to model the ESD event coming from a person's fingertip touching a thin i.e. semiconductor or wafer. Therefore, the human body in electrostatic terms is a conductor with a variable capacitance of around 500ρF, and a skin resistance under clean dry conditions of 1500 ohms. However substantially larger capacitances have been measured and

recorded. For example, the voltage from a human body walking on a synthetic flooring can rise from zero volts up to fourteen kilovolts over a period of just twenty seconds due to the voltage building up on the body just like a capacitor see below for this in Figure 4.1: -

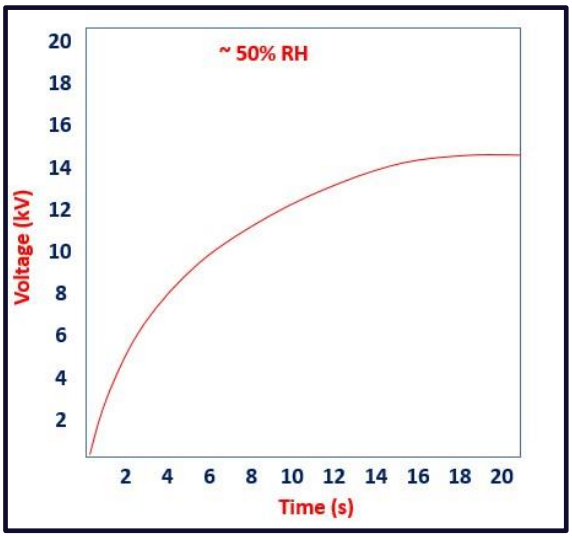


*Figure 7 Voltage builds up on a person over time. [84]*

It should be noted that these conditions will fit the equation for a charging capacitor which is: -

$$Vc(t) = Vo\ (1 - e^{-t/RC}) \qquad (4.1)$$

Where $V_c$ is the voltage charge and $V_o$ is the charging circuit. However, due to the human body having significant resistance the current is limited and the peak current discharged is normally around 0.1 amps to 10 amps over a period of 100 nanoseconds to 200 nanoseconds. The human body capacitance is dependent on the closeness of other items or bodies these can be such things as furniture, flooring, and walls also when standing / moving around, the characteristics of clothing, and footwear are important causes. The example in figure 4.2 shows how an operator without a wrist strap working in a laboratory can generated human body voltage spikes just by moving around within a lab. Please note the effect of just resting shoes on the footrest plus what occurs as the operator stands in figure 4.2.

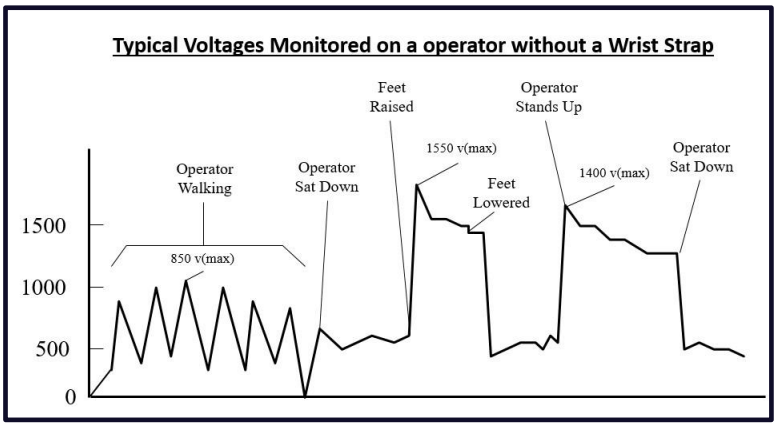


*Figure 4.2 Typical voltages monitored on an operator without a wrist strap. [84]*

The HBM is considered as an ESD event, not an electrical overstress (EOS) event because it is a charge transfer-related source, with a short pulse event. The HBM is intended to represent the interface of the electrical discharge from a charged human being, with a component, or an object. The HBM assumes that the human individual is the start condition. The charged human then touches a wafer or die using a fingertip. Note that ESD damage from humans to semiconductor components can be at lower voltages such as two hundred volts.

The HBM is modelled with the schematic in figure 4.3. Figure 4.4 demonstrates the current waveform assuming zero device under test (DUT) impedance. As stated above the HBM is the most popular ESD model in organisations and the one most will use to evaluate ESD threshold levels between semiconductors [67]. The HBM presumes that a person is standing upright and as stated above touching the wafer with a fingertip [69].

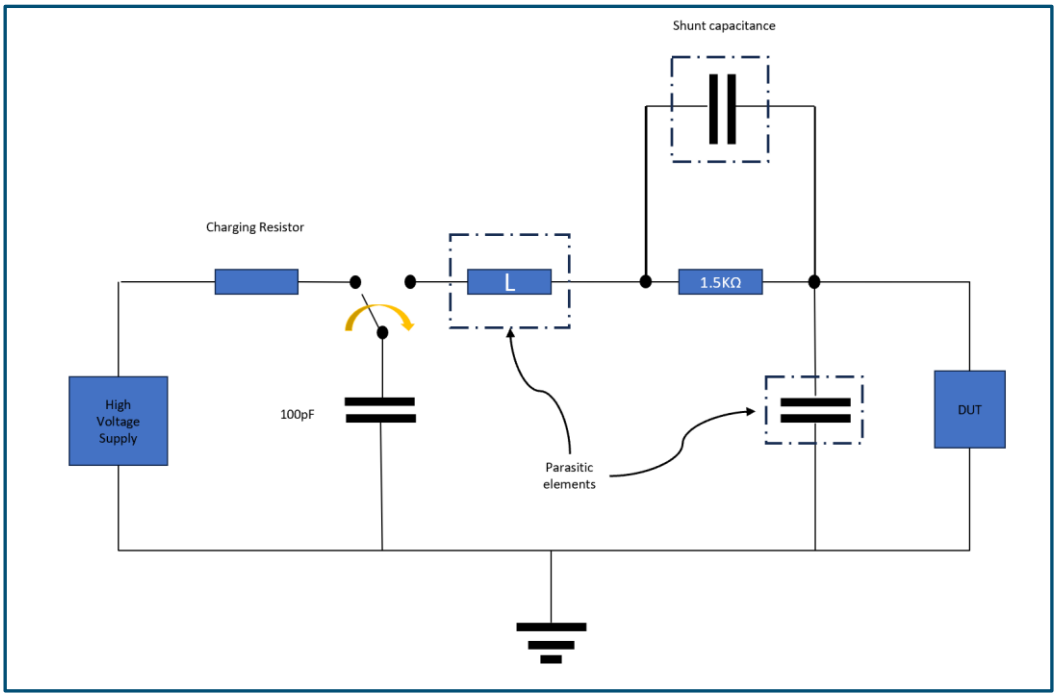


Figure 4.3 Human Body Model schematic.[85]

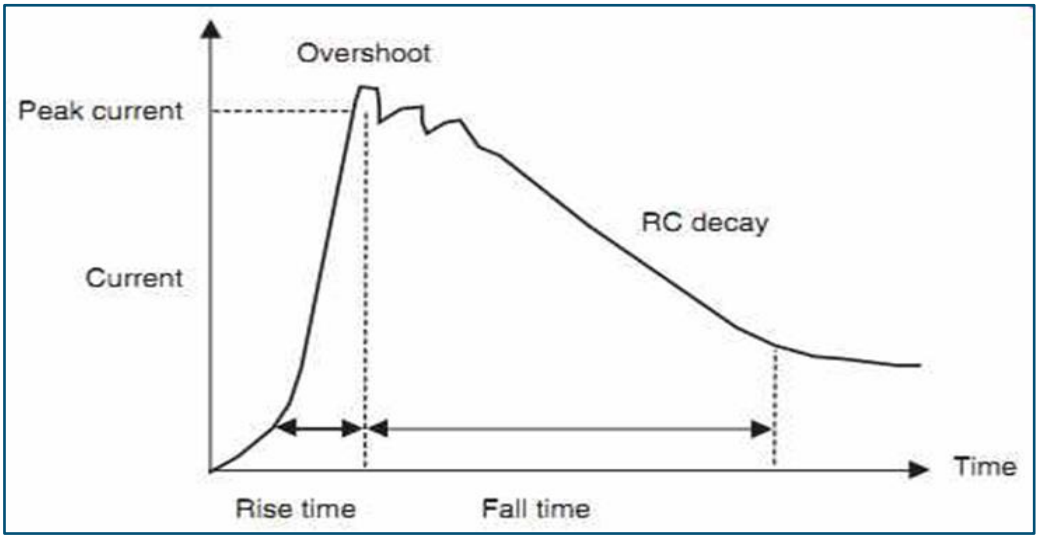


*Figure 4.4 Human Body Model current wave form. [86]*

The differences seen between the models used with the semiconductor industry (HBM, CDM, MM) are due to the parasitic impedance shown in figure 4.3 [50], [51]. Because of the large series resistance in the HBM, this ESD event can be modelled as a current source with the current waveform shown in Fig. 4.4 [65], [69]. The characteristic time of the HBM event is associated with the electrical components used to emulate the human being. In the HBM standard, as stated before the circuit components used to simulate the charged human being is a 100-pF capacitor in series with a 1500-

Ohm resistor. This network has a characteristic rise time and decay time. The rise time is in the range of 17 nanoseconds to 22 nanoseconds. The characteristic decay time is associated with the time of the network, which is 150 nanoseconds. The pulse event is a single polarity event. The test is performed in both positive and negative polarity events this is to address HBM ESD qualification. The energy content in a HBM event follows the energy accumulated in a capacitor: -

$$U = 1/2\ C\text{-}V2 \qquad (4.2)$$

At 4000 V, a total charge of 0.4C and 800 J of energy is available, but only a small portion of this is absorbed by the device under test [69]. For the HBM, most of that energy is dispersed in the source resistance. The critical factors in the HBM are stray capacitance, series resistance and series inductance. An example of a positive polarity HBM pulse event is seen in figure 4.4.

In a real-world condition, a person will have a capacitance and resistance that varies from the HBM. The charge accumulates in the shoes of the person and induces a charge on the body [64], [72]. Chase and Unger [71] showed capacitance from 167pF rising to 514pF depending on the type of footwear worn. The footwear sole material type and thickness determine the capacitance and triboelectrification characteristics. Also, peoples skin resistance also differs depending on the amount of perspiration and the skin levels of oiliness. The resistance can vary from 1000 ohms rising to 100 000 ohms. Also, if f a metal object is held while touching the DUT, the resistance is lowered, causing faster rise times and higher peak currents [72].

The HBM standard is used to measure the sensitivity or susceptibility of these wafers / die to damage or degradation to the defined HBM standard. The test is executed with the die or wafers in an unpowered state. Therefore, the HBM test is the established standard for the qualification and release of semiconductor components in the semiconductor industry. The HBM standard is integrated into the qualification and release process of the quality and reliability teams for wafers / die in semiconductor organisations. There are a number of standards used around the world. These standards are in appendix 1. The standards that are used in this thesis is below in table 5: -

*Table 4.1 Standards for ESD test models. [94]*

| Model | Standard | Rs (Ω) | C ESD (ρF) |
|---|---|---|---|
| Human Body Model (HBM) | IEC 60749-26 ANSI/ESD/JEDEC JS-001 | 1500 | 100 |
| Machine Model (MM) | IEC 60749-26 ANSI/ESD/JEDEC STM 5.2 | | 200 |
| Human Metal Model (HMM) | IEC 61000-4-2 ANSI/ESD 55.6 | 330 | 150 |

A HBM tester can be built and then used on semiconductor wafers, die and IC's this is discussed in the next section.

## 4.3 Human Body Model ESD Tester

From the HBM schematic in figure 4.3 a simple electrical ESD circuit can be modelled such as the one below in Figure 4.5: -

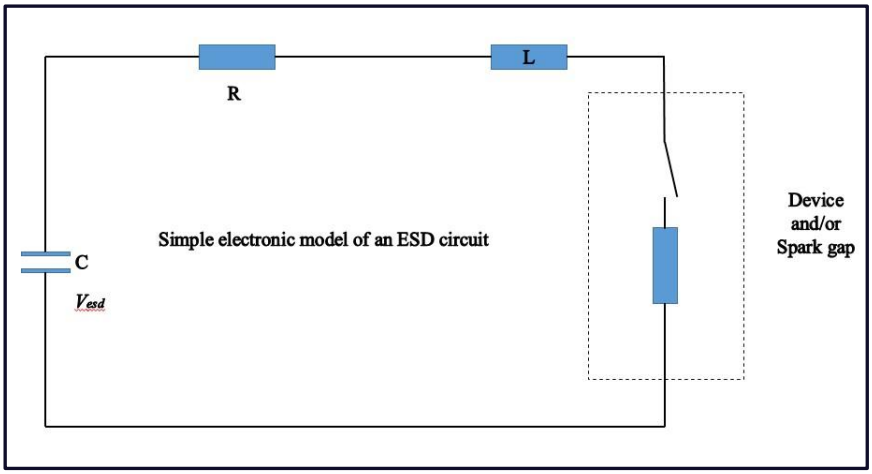


*Figure 4.5 Simple electrical ESD circuit. [87]*

From the simple electronic circuit above, a simple HBM tester circuit was designed as in Figure 4.6 below: -

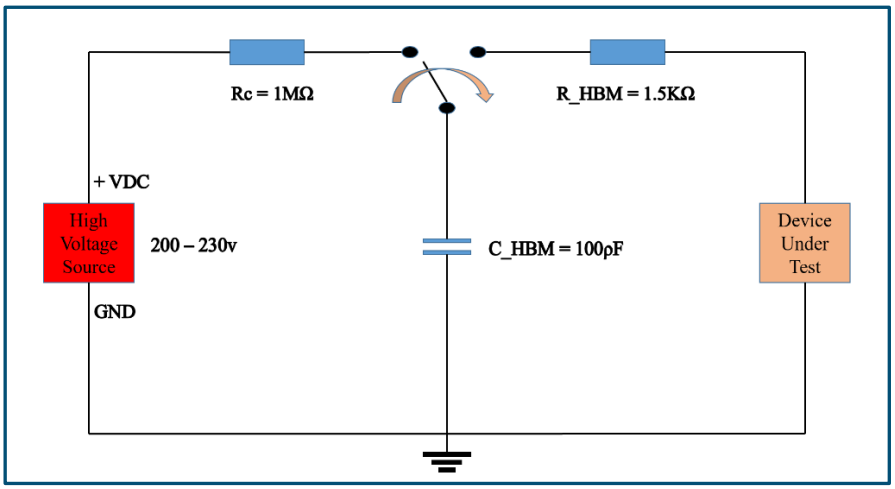


*Figure 4.6 Simple Human Body Model tester circuit. [87]*

The final circuit design of the HBM ESD tester is below in figure 4.7 from this diagram a HBM tester can be designed and built using the parts from the resource list in appendix 3: -

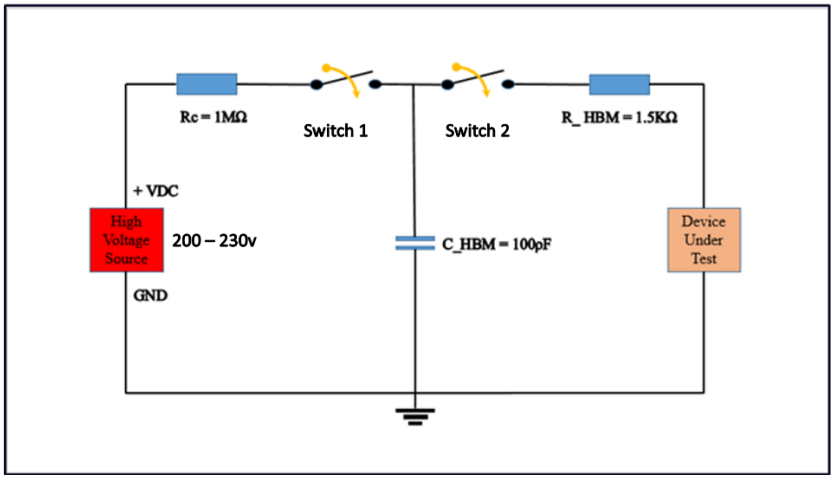


*Figure 4.7 Final circuit design of the Human Body Model ESD tester. [88]*

Also, a simple PCB can be designed from the circuit in figure 4.7. This is below in figure 4.8 and can be done at a later date due to time constraints and an absence of an electronics lab within the company also government restrictions due to the company being owned by Nexperia at the time this thesis was written.

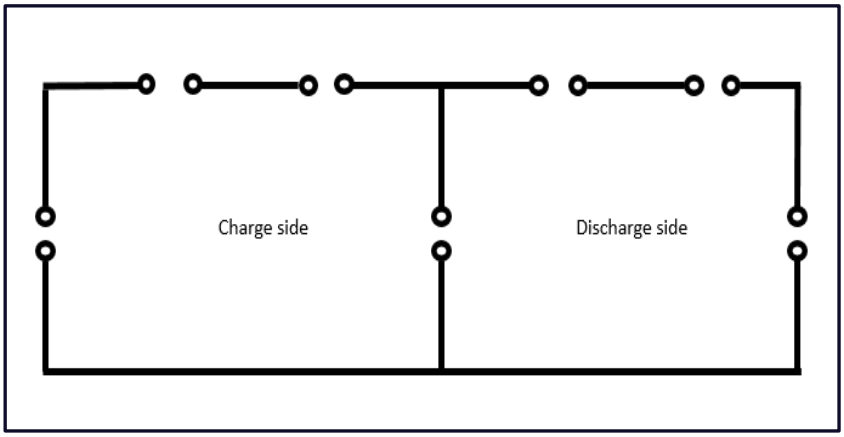


*Figure 4.8 A simple PCB for the Human Body Model ESD tester. [88]*

The initial budget for the project would be set at £19,198.15 with twenty percent as a precautionary guard band. However, due to the cost of some parts i.e., the power supply (the red band in the resource list). The company will supply the parts in for the project via the final analysis (FA) department. Therefore, the initial cost for the tester is set at £104.79 with the twenty percent precautionary guard band still in place. The project costing is based on the initial research already done by the author in an interim report.

As well as the items listed in appendix 3, time from the company and wafers to be tested would be required. This has been arranged with the company via the FA department. Defective wafers will be used for the HBM ESD test because of the cost of each wafer. The cost of the FA department and their time will be covered by the company and will not be directly applied to the thesis.

# Chapter 5 Testing and Results of the HBM ESD Tester

## 5.1 Testing of the Human Body ESD Model Tester

Primarily, safety is the priority while conducting these tests. During the initial set up (see figure 5.3), the HBM ESD tester shall be inspected in its operating location to ensure that the tester is not operating in a combustible (hazardous) environment. All personal **before** operating the tester shall receive training in system and electrical safety training. The procedures and equipment described within this thesis could expose people to hazardous electrical conditions. I have selected equipment that complies with applicable laws and regulatory codes plus both internal and external policies where needed. Any requirements for personal safety will not be superseded.

Safety protection must be considered where personnel could come into contact with electrical sources such as ground fault circuit interrupters (GFCI). Also, electrical hazard reduction practises should be implemented, and proper grounding instructions for equipment will be followed.

As stated, before the HBM standard is ANSI / ESDA / JEDEC JS001-2023 revised from ANSI / ESDA / JEDEC JS001-2017- ESD Association Standard Test Method for the Protection of Electrostatic Discharge Sensitive Items - Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) Testing - Device Level.

The scope of HBM ESD test is for testing, evaluation, and classification of components and micro to nano-electronic circuitry. The test is to quantify the sensitivity or susceptibility of these components to damage or degradation to the defined HBM test. The test is performed with the component in an unpowered state. However, the standard also defines wafer level testing and how to implement it, and this is what will be used to test the die.

The purpose of the HBM ESD test is to establish a testing method that evaluates the consistency and reliability of wafers when exposed to a defined pulse event in order to classify or compare ESD sensitivity levels. The pulse waveform is a representative time of the HBM ESD event and is related with the electrical components used to mimic the human body. In the HBM standard, the circuit has been discussed in previous sections and has a distinctive a rise, and decay times.

The HBM test equipment will discharge an HBM pulse to the device under test (DUT). As shown figure 4.7 the test equipment requires a high-voltage source to charge the HBM circuit. Switch 1 is closed and switch 2 is open within the test system when the high-voltage source charges the circuit. After the circuit is charged the high voltage will be switched off via switch 1. It is especially important that during the charging of the HBM source circuit the second switch must be remain open.

When the operator of the tester is ready switch 1 is opened and switch 2 is closed then the HBM circuit current is discharged into the load or DUT.

The standard JEDEC-JS001 specifies that a sample of three devices (A, B, C) for each voltage level shall be characterised for the device ESD failure threshold using recommended voltage steps at 50 V, 125 V, 250 V, 500 V, 1 kV, 2 kV, 4 kV. Each sample of three die shall be stressed at one voltage level using one positive and one negative pulse with a minimum of 100 milliseconds between pulses. Longer intervals are allowed and must be used if the die is expected to be vulnerable to increasing effects. In the testing of wafers, there is a defined test sequence and procedure. Figure 5.1 provides a test sequence flow for the HBM test systems.

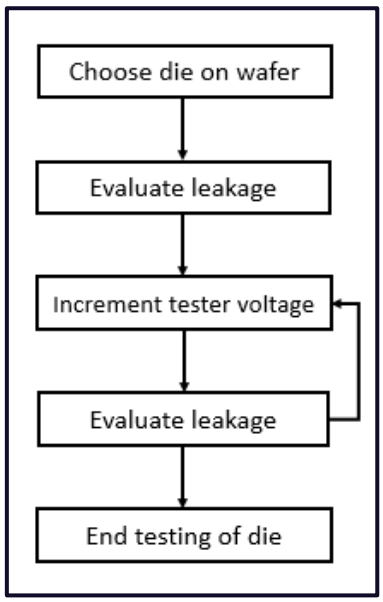


*Figure 5.1 Human body model test sequence. [86]*

In the testing of wafers to larger voltages for semiconductor die classification, a reference for grounded is determined this is normally the chuck of the tester. A preliminary reading of the output voltage is implemented prior to any applied voltage on the tester. A first step voltage is defined on the capacitor element. All selected die are pulsed with an ESD event, individually relative to the grounded reference. In a final test situation  all die are selected. However for this thesis only selected die are pulsed. Each die is gauged based on a failure condition (e.g., voltage shift, leakage). If the die then "passes," it remains in the test sequence for the next voltage. Die that "fail" are isolated from the test order, the surviving die remain in the test run. The voltage is increased on the high voltage source to the next step level, and testing resumes for the surviving die. For this test, after the desired steps

are complete, the tester is stopped, and the failed, and surviving die on the wafer are recorded. The MOSFET die that are to be tested look similar to the one pictured in figure 5.2.

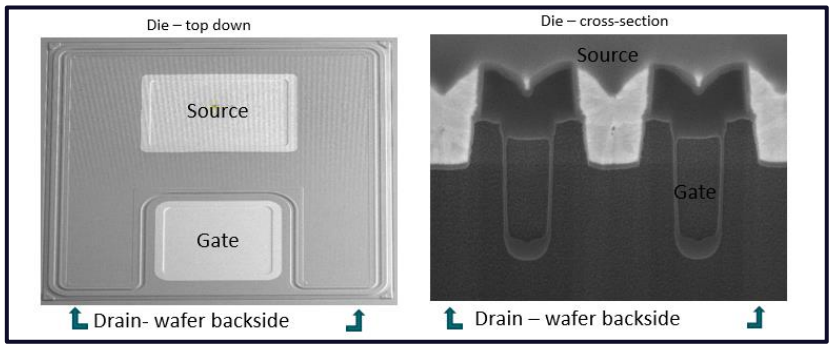


*Figure 5.2 Top-down view of a die with a cross section of the same die. [76]*

It should be noted that the voltage generator in the FA department can only generated voltages up to 230 volts DC, while the HBM ESD tester circuit can tolerate up to 650 volts DC (due to the components used). All three wafers were tested on a Cascade Microtech Alessi REL-6100 200mm 8" Wafer Probe Station, this probe station is rated up to 200 volts AC and is more than suitable for the required testing. The probe station is sat upon a vibration table. The setup of the equipment is seen in figure 5.3.

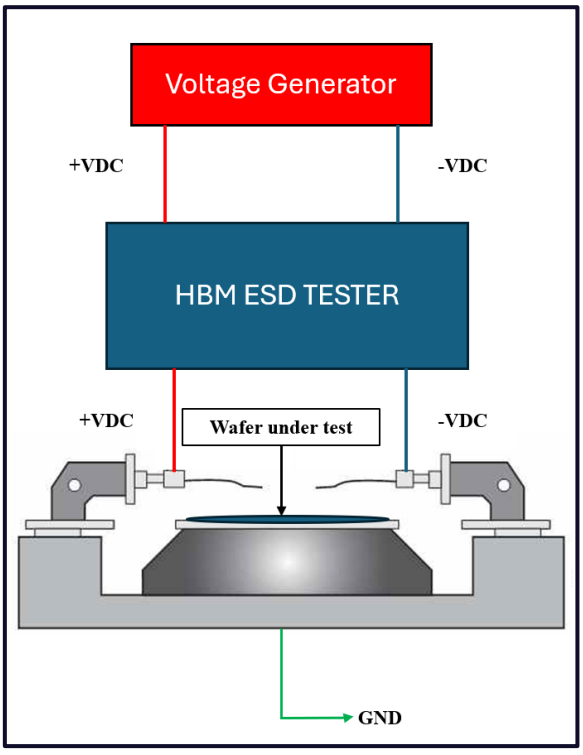


*Figure 5.3 HBM ESD tester equipment set up [87]*

The samples were stressed at voltage levels of 10V, 20V, 30V, 40V, 50V, 60V, 100V, 100V, 150V, and 200V applied in 22˚C, 25% RH with a current of 114 μA applied between the Gate-Source. In the first round of testing the probes was placed above the samples (2 mm maximum) and in the second / third round of testing touching the wafer. The samples A, and C, are products of the company. Sample B was a product that the company created for a client.. Each sample was tested on known "good" die of each wafer as seen in figure 5.3.

Figure 5.5 shows a wafer sort controller (WSC) map with the good die being represented by the colour green. The rest of the colours are defective die and need not be explained here. A microscope was used to check for visible damage done to the die. The results for each sample tested are in the next section.

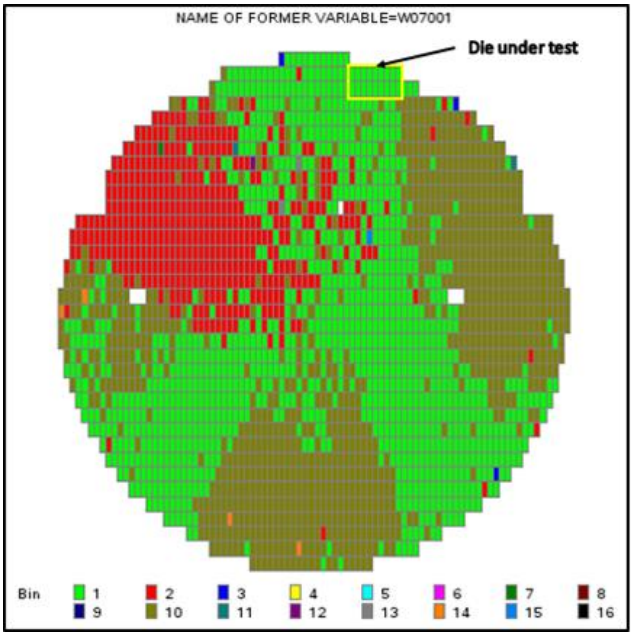


*Figure 5..5 Wafer sort controller map. [89]*

## 5.2 Results of Testing the Human Body ESD Model Tester

As stated above the first round of testing was done with the probes placed above the sample's at a maximum height of 2mm, with the positive probe placed above the gate and the negative probe placed above the source. The drain (back of the wafer) was earthed though the chuck.

The first sample (A) was a power MOSFET (company name Roach) with a breakdown voltage of between 25.5 volts to 30.1 volts. The sample was stressed with voltage levels as stated above increasing from ten volts up to two hundred volts. Each time the sample was checked underneath a microscope to check for visible damage to the die under test. No visible damage was seen.

The second sample (B) was a low voltage IC (produced for another company) with a breakdown voltage of 3.6 volts to 5 volts. Again, the sample (B) was stressed with the same voltage levels as sample (A). Again, the sample was checked under a microscope for any visible damage none was found.

The third sample (C) was a power MOSFET (company name Yemen) with a breakdown voltage of 42.5 volts to 46.7 volts. As with the previous samples the sample (C) was stressed with the same voltage levels as the other samples and checked under the same microscope. As previous no damage was seen with the sample.

As stated previously the second round of testing was done with the probes touching the samples. The positive probe was placed touching the gate pad with the negative probe touching the source pad. Again, the drain (back of the wafer) was earthed though the chuck.

Again, the first sample (A) was a power MOSFET (company name Roach) with a breakdown voltage of between 25.5 volts to 30.1 volts. The sample was stressed with voltage levels as stated above increasing from ten volts up to two hundred volts. Again, each time the sample was checked underneath a microscope to check for visible damage to the die under test. Again, no visible damage was seen. The second and third samples were evaluated under the same conditions with the same results seen.

Because no damage was seen on the samples. The connections between the ESD tester and the DUT was checked to make sure that the connections was secure and properly made. This was done because loose connections could prevent the ESD tester from delivering the voltage to the DUT.

Than the HBM ESD tester was removed from the set up then the circuit within the HBM ESD tester was checked and continuity checks was performed on the tester using a multi meter to verify

continuity within the tester after this, the tester was placed back in to the setup and continuity checks was performed along the test setup, including the leads and connections between the ESD tester and the DUT. This was done to ensure that there was no breaks or shorts in the circuit none was found. For the future a oscilloscope can be used to monitor the pulse in real time.

Then we checked the O/P voltage from the tester and along the test leads / connections and finally at the probe tips using a multi meter. Various voltages were assessed at each stage of the tester, these voltages being the same as the voltages used to stress the samples. The voltage was seen at each point of the set up including the probe tips.

After checking the above, we tried a third round with the same wafers and voltages with the probes touching down on the wafers and after stressing the wafers we checked with a microscope again no damage was seen. It was expected that the devices would breakdown at or around fifty volts due to the known breakdown of the die, however as stated none was seen.

So, the question now is why the HBM ESD tester is not damaging the samples as expected. As the following was done to check why the tester was not producing the desired results. The probes were cleaned and checked before the testing started. The probes were checked for dirt or damaged because this could prevent proper sparking.

Both the tester and DUT was properly grounded because poor grounding can affect the performance of the ESD tester and prevent it from delivering the required discharge. The DUT was properly connected in the test setup and there were no protective components attached to the DUT i.e. diodes. The settings on the voltage generator and HBM ESD tester were double checked to ensure that it was configured correctly for the test voltage range that was used.

One of the problems could be the environmental conditions, within the test area the FA department is “dry” but very warm with a humidity level of 25% RH (This was checked) this could have affected the testing. A dry cold environment is best to produce ESD

The ESD tester may not be properly configured for the test conditions. The standards used within this thesis quote a range of voltages to be used. However, most papers cited within this thesis use a voltage range of 1kV to 4kV for power MOSFETs. Also a factor could be due to the breakdown voltage for air. The breakdown voltage for air is the minimum voltage required to cause a dielectric breakdown in air, leading to electrical discharge, such as a spark. This value depends on factors like pressure, temperature, and the distance between the electrodes. Under standard conditions (at sea level, with a gap of 1 cm between electrodes), the breakdown voltage of air is approximately 30 kV/cm. For example: -

- For a 1 mm gap: The breakdown voltage is around 3 kV.
- For a 1 cm gap: The breakdown voltage is about 30 kV.

This value can vary depending on the conditions, but 30 kV/cm is a commonly referenced approximation for standard conditions. So this could have been the main factor. It is possible that the ESD tester may have technical limitations because the tester as a maximum discharge threshold of 650 volts due to the components used. Also power MOSFETs are known to be sensitive to ESD events due to their design and structure. However, the failure of the ESD tester to generate sparks could indicate that the power MOSFETs wafers used have adequate protection against ESD at the various voltage levels used for the tests.

Due to the nature of HBM testing, the device is subjected to controlled ESD pulses generated by the tester. These pulses simulate human touch induced ESD events and the ESD pulses are extremely short in duration (nanoseconds), minimising the energy transfer to the device this could be a cause for no damage being seen. Switch “bounce” could have also been a factor in this.

Switch “bounce” could have been a factor due to the rise time taking nanoseconds. Switch bounce is when a switch in this case a rocker switch see appendix 3 is pushed, two metal parts make contact. it might seem that the contact is made immediately for the operator. This is incorrect. Inside the switch there are two contacts plus moving parts. When the switch is pushed, it primarily makes contact with the other metal part. However within a microsecond the contact is made a bit longer, and once again a little longer. The switch is fully closed in the end. The switch is moving or “bouncing” between in-contact, and not in-contact. "When the switch is closed, the two contacts actually separate and reconnect, typically 10 to 100 times over a period of about 1ms." [95] So the ESD “spark” is gone but the voltage remains to be tested at various points in the HBM ESD set up.

The testing of the HBM ESD tester revealed unexpected results, as none of the samples showed visible damage under the stressed voltage conditions. Despite thorough checks of the test setup, including the grounding, probe integrity, continuity of the circuit, and voltage levels, the tester did not produce the anticipated breakdown in the DUT. Several factors may have contributed to these results, including environmental conditions like humidity, potential limitations of the ESD tester, the inherent design resilience of the tested power MOSFETs and ICs, and possible issues like switch bounce. The discrepancy between expected and observed outcomes suggests that for future improvements that further investigation into the tester’s configuration, the specific environmental conditions, and possibly using a different voltage range or more sensitive detection methods might be necessary to better understand the ESD resistance of the samples.

# Chapter 6 Mitigation of ESD in Semiconductor manufacturing

## 6.1 Mitigation of ESD in semiconductor Manufacturing

As stated above, damage to semiconductors (power MOSFET included) by ESD events are governed by the semiconductor's ability to disperse the energy of the ESD event and / or to withstand the voltage level in the event. The sensitivity of semiconductors to ESD events is determined by ESD models test methods. Thus, the semiconductor device's ability to withstand ESD voltage can be defined as [37]: -

*"The highest voltage level that does not cause device failure and the device passes all lower voltage tests."*

Most semiconductor devices are vulnerable to ESD damage at moderately low voltage levels typical less than one hundred volts with some semiconductors being damaged below ten volts. If current trends in product design and development continue as in the past, then future semiconductors will have much more circuity packed onto them. Therefore, increasing the sensitivity to ESD damage and making the scale of this problem even more critical. Thus, ESD protection is of vital significance during circuit design, component handling, and final consumer usage from circuit designers, manufacturers, suppliers, and end users.

This problem can be reduced by the company using risk mitigation and risk mitigation can be defined as: -

"*The process of reducing risk exposure and minimising the likelihood of an incident."*

It involves constantly dealing with the companies' top risks and concerns to ensure that the company is fully protected.

Therefore, ESD protection measures involving ESD protection structures are utilised within the semiconductor (On chip protection). Also, ESD enhanced fabrication processes are usually the first line of defence. Whilst ESD protection circuit development (on-chip) has been an important part of every single IC, additional protection on the majority of discrete components has been deemed discretionary by many manufacturers and clients using these components in their products. ESD protected versions of discrete components are available from the company.

Consequently, the company uses these two factors for ESD improvements as follows: -

1. Produce robust devices through design, process, and circuit improvements.

2. Minimise the ESD event exposure by providing systems and safeguards within the production environment.

## 6.2 On chip protection from ESD in Semiconductors

As stated above the probability of electronic circuit damage is intensifying as semiconductor dimensions are reducing in size to nanometre scales. Most semiconductors operate at low voltages and thus have structures plus conductive paths that cannot endure the high voltages and currents associated with ESD transients. However, it is during the production of these components that ESD events can happen.

The company's semiconductor designers include a controlled amount of ESD suppression to the semiconductor being produced to help prevent damage during manufacturing and assembly processes. However, the level of protection that is added may not be sufficient to protect the devices from ESD during actual usage. Many electronic products, especially portable ones, are used in uncontrolled environments. Portable devices can experience a charge increase as they are carried by people in their pockets or in a bag etc. Therefore, this energy will then be discharged to another piece of equipment when the two are attached, usually when a person touches Input / Output pins on a cable connector. Thus, product designers should consider ESD suppressors being added additional to their circuits.

Appropriate utilisation of ESD circuit protection will help to prevent these failures. However, selection of a suppression device by the designer must recognise that ESD events have noticeably short rise and fall time typical less than one nanosecond (1ns) in most cases. The International Electro Technical Commission (IEC) have developed specifications (See Appendix 1) for ESD testing that helps determine if products are susceptible to ESD events.

The company use these specifications to design ESD suppressors with the speed, clamping voltage, and residual current levels that will protect sensitive semiconductors / devices and electronic circuitry now and in the future. Many of these designs have the low internal capacitance needed for high bandwidth communications. Therefore, when selecting ESD suppressors, the company designers will need to consider potential coupling paths that would allow ESD events to enter their circuits and end user products. These identify area weak points will need to be considered for ESD suppressor installation. Finally, the company designers need to select ESD suppressors with characteristics

appropriate for their type of semiconductor being used in equipment, the sensitivity of the semiconductor, and the environment where it will be used.

Therefore, ICs are protected by an approach to discharge the ESD events that might occur on any pin of the package that is exposed to its environment. The protection approach involves consideration of HBM and other model events for every pin, it should be noted that the protection strategy against IEC events are considered for selected pins based on end equipment system requirements and is not discussed here.

For every innovative technology, the company wishes to produce, then the protection circuits / sections are first depicted through test ICs, then suitable protection structures are formulated. These structures are analysed for their effectiveness through another round of test ICs before applying the approaches in the production die. The protection sections and their variations for the different ICs power pins, and signal are based on the required applications.

Simulations are often used, to ensure the efficiency of the protection sections and their compatibility with the IC pin/s they are designed to protect. Before fully applying the completed design of the protection circuits and releasing it for production, an ESD software program tool can be run. The circuit connections and layout of a product can be extremely complicated and can lead to various unexpected faults even for simple ESD designs. The tool is a high-tech software program developed to detect ESD design errors and enforce compliance to the company's ESD rules. However due to company intellectual property the title of the software cannot be named in this thesis. The point of the program is to discover design and layout errors that might lead to ESD events. This program ensures that, before a component is released for production, that all potential ESD infringements are detected. The software also gives designers guidance to correct any errors that are detected.

In a semiconductor, as stated before the current from an ESD event seeks the path with the lowest impedance to ground. These currents are categorised as 0.1-10 amps, dissipating power can be categorised as 10 – 100W with a time as short as $10e^{-6}$ seconds. The purpose of ESD protection circuits / components is to shunt ESD currents along a planned discharge path and dissipate the energy in ESD components whilst clamping the voltage safely to protect components in the circuit.

We can now look at methods for protection against ESD events as stated above this is the first line of defence. ESD protection components can be split into two groups, voltage suppression and current limiting. Voltage limiters are placed between a precise point and a low impedance voltage, normally ground. Throughout normal operation of the circuit the voltage limiting component should have high impedance. Beyond operational voltages the voltage limiting component should switch to

a low impedance to divert current stress to ground, therefore restraining the voltage to the precise point. Current limiting components are placed in line with the signal. Current limiting components should have low resistance during operational conditions but switch to a high impedance condition during a stress state.

Most ICs pins have a range of voltage and current in which they are intended to be operational. Beyond the operational voltage is an area of safe overvoltage, which will not damage the circuit. At voltages beyond this the IC will be damaged. These regions are seen in figure 6.1.

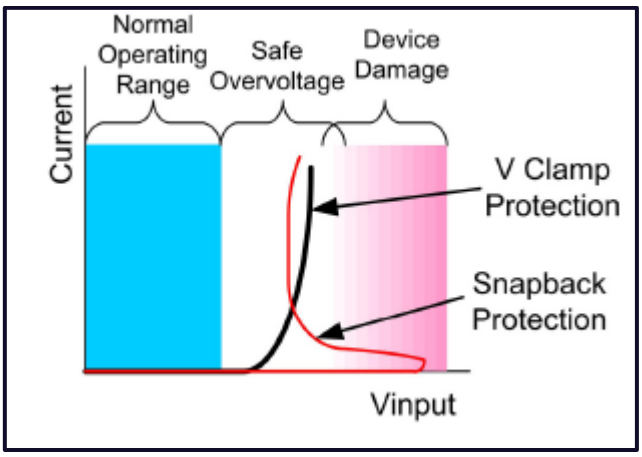


*Figure 6.1 I–V Curves for Voltage Clamping and Snapback Voltage Limiting Devices. [90]*

The border between safe overvoltage and device damage is not defined. Damaging voltages can be endured if the voltage spike is of a duration that is short. Voltage suppressors must work in the area of safe overvoltage of the circuit they are protecting by preventing voltage from entering the device damage area, however system performance must not be degraded and within the range of normal operation.

Voltage suppressors are categorised by their directionality and by protection performance. The behaviour of the protection distinguishes between voltage clamping and snapback, whilst the directionality distinguishes between bidirectional and unidirectional. Voltage suppressor components fall into two classes of behaviour, voltage clamping, and snapback protection as seen in figure 6.1.

A voltage clamping device has high resistance up to the turn on voltage, beyond which the resistance drops considerably. For a voltage clamping device it is essential that the turn on voltage is beyond the operational voltage of the system but still small enough to guarantee the clamping voltage

is considerably below the damage voltage for the point under protection. The on-state resistance must be extremely small to ensure low clamping voltages across a variety of situations that the ESD event can pose to the circuit.

The behaviour of a snapback device is different. A snapback device like a voltage clamping device has high resistance at low voltage and turns on at a voltage beyond the normal operational voltage of the circuit being protected. But a snapback device, turn on voltage instigates a new conduction procedure which creates a low resistance, and the voltage drops below the turn on voltage. Sometime the voltage may in fact drop into the operational range. Snapback devices may pass briefly into the device damage region prior to reverting to the safe voltage range as seen in figure 6.1. For many circuits, such brief periods are tolerable since the start of damage is often very time dependent.

Voltage limiting devices can be categorised as bidirectional or unidirectional. Sample I–V curves for bidirectional and unidirectional voltage clamping protection components are seen in Figure 6.2.

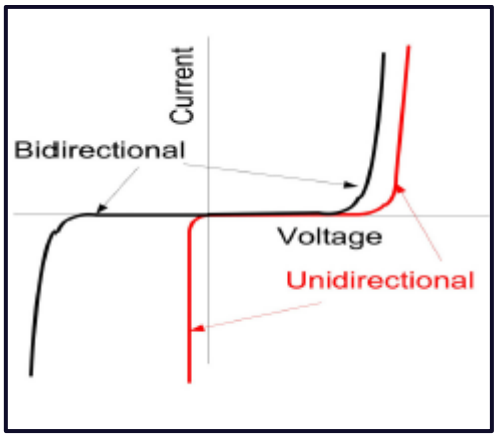


*Figure 6.2 Sample I–V curves for bidirectional and unidirectional voltage clamping protection components. [90]*

A bidirectional protection device has equal protection focused at zero volts. As seen in figure 6.3 a bidirectional protection structure is ideal for protecting nodes whose voltage normally extends symmetrically above and below zero volts.

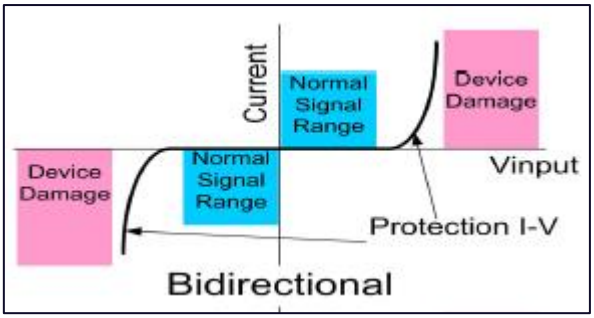


*Figure 6.3 Bidirectional Devices with the Range of Safe and Unsafe Conditions for the Circuit Being Protected. [90]*

A unidirectional device has an uneven behaviour around zero volts. A typical unidirectional protection device is a Zener diode. In the forward direction the Zener begins to conduct strongly at about 0.7 V. In the reverse bias direction, the Zener begins to conduct at its reverse bias breakdown voltage. As seen in figure 6.4.

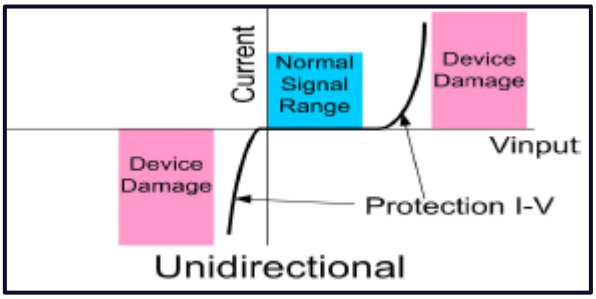


*Figure 6.4 Unidirectional Devices with the Range of Safe and Unsafe Conditions for the Circuit Being Protected. [90]*

A unidirectional protection device is perfect for protecting voltage points whose voltage is always positive or negative. It should be noted that, both unidirectional and bidirectional protection products can protect stress with either polarity.

Diode transient voltage suppressors (TVS) are diodes with two terminal circuit parts which conduct current easily in one polarity and have a high resistance, up to breakdown voltage, in the other polarity. Most diodes in the 21$^{st}$ century are solid state devices made from silicon.

Silicon diodes are formed at a boundary between n doped and p doped areas of silicon as seen in figure 6.5.

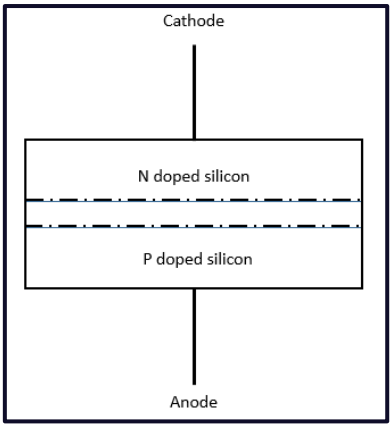


*Figure 6.5 Silicon diode construction. [88]*

At the intersection, the electric fields between the n and p doped areas create a depleted area without n or p carriers when there is no applied external voltage. If a negative voltage is directed from the cathode to the anode both n and p carriers are driven in opposite directions across the junction and current begins to flow at around 0.7 volts. If a positive voltage is directed from the cathode to the anode the n and p carriers are drawn further apart and exceedingly current flows.

When a higher voltage is reached it will result in either avalanche breakdown or Zener tunnelling in high currents. A basic diode's I−V curve is shown in figure 6.6.

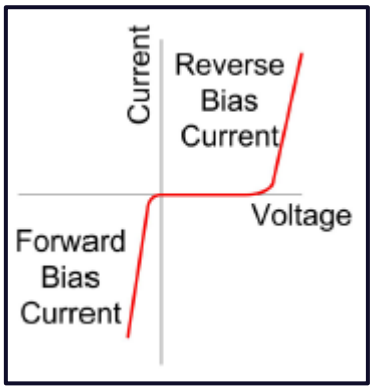


*Figure 6.6 Diode's I−V curve. [90]*

Diodes protect by voltage clamping and are fundamentally unidirectional components. The properties of the diode differ on the doping levels of the n and p areas both near the junction and further from the junction. A wide range of diode properties can be created by varying the doping profiles in the diode structure.

Designed diodes for protection have benefited from all of the developments in silicon technology. One of the diode properties is the breakdown voltage. Reverse bias diode breakdown voltages can range from a few volts up to hundreds of volts. Most silicon-based diodes with a well-defined breakdown voltage are referred to as Zener diodes. The circuit symbols for standard diode and Zener diodes are shown in figure 6.7.

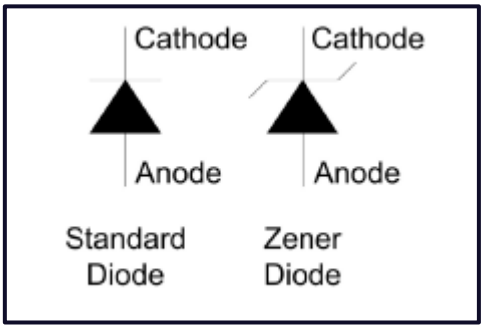


*Figure 6.7 solid state diode symbols. [90]*

Zener tunnelling causing reverse bias conduction is only noteworthy for diodes with breakdowns of six volts and less. Diodes with breakdown voltages over six volts normally begin to conduct in the reverse bias direction by avalanche breakdown. However, it should be noted that the term Zener diode for these higher breakdown voltage devices is standard in the semiconductor and electronics industries.

Earlier silicon based TVS devices had a drawback protecting products with high-speed signal lines and low voltage. Reducing the turn on voltage of a protection diode involves higher doping levels in the silicon resulting in a high capacitance, making them unsuitable for high-speed applications. The latest technology advances in the 21$^{st}$ century have eliminated this problem. New products combine the advantages of silicon-based protection with the low capacitance. New components behave if these components were a simple Zener diode. Most new devices combine a low breakdown Zener diode and a pair of standard diodes which have high breakdowns, and therefore low capacitance, as seen in figure 6.8.

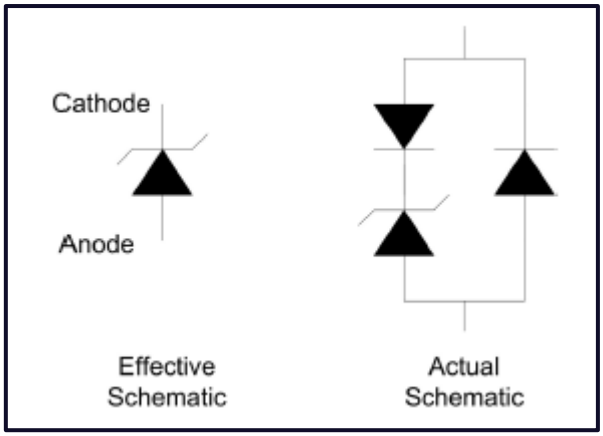


*Figure 6.8 Effective and Actual Schematic of an Ultra-Low Capacitance Diode Based TVS Device. [90]*

The DC I−V characteristics of these devices are the same as for a low voltage Zener diode. In the actual schematic the single diode in the right branch provides forward bias diode conductivity. For a negative cathode to anode voltage. For positive cathode to anode voltages the left branch will have a breakdown voltage equal to the Zener diode's breakdown plus a forward bias diode drop. However, the right branch of the device carries little current. These devices acquire its low capacitance from the low capacitance of the standard diodes. The left branch the series diodes will have a capacitance no higher than the capacitance of the low capacitance high breakdown diode and the right branch of the circuit has the low capacitance characteristic of the high breakdown diode.

Zener diode TVS are very efficient devices for protection. Zener diode TVS have high conductivity in the on state, the turn on voltage can be regulated correctly, and they do not degrade with recurring ESD events under their maximum current limits. Zener diode TVS can be produced in a variety of designs on a single silicon substrate using IC processing techniques.

As stated above at low voltages, the snapback ESD device also has high resistance and turns on at a voltage greater than normal operational states of the protected circuit. The difference is that after it starts to conduct with a low resistance, the voltage drops below the turn on voltage and in some circumstances, falls into the operational voltages of the protected circuit. Therefore, the device could remain in the on state, conducting current when the ESD event is over. This state is called "latch-up".

A latch-up is a kind of short circuit which can happen in an IC. specifically, it is the unintentional making of a low-impedance channel between the power supply rails of a MOSFET circuit, triggering a parasitic construction which interrupts proper operation of the

device, possibly even destroying the device due to overcurrent. To cure latch up the device must be powered cycled.

Therefore, ESD protection devices should be selected such that the voltage at which it triggers is not above operational voltage that it can damage sensitive components of the circuit to be protected. Similarly, the lower hold voltage should not be lower than the normal operating voltage of the circuit so that the device switches off after the ESD event ends.

For several reasons, the company as required the addition of ESD protection designed into their systems on their discrete components. ESD protection of some components can be a challenge just as with ICs. For MOSFETs, the gate oxide between the gate and channel using current CMOS processes is exceptionally thin this subsequent results in variable degrees of ESD. The electric field $E_{ox}$ across the gate oxide of thickness $t_{ox}$ when voltage V is applied is: -

$$Eox = V / tox \qquad (6.1)$$

For exceedingly small $t_{ox}$, the electric field $E_{ox}$ can surpass the breakdown field $E_{bk}$ for fairly small voltages.[73] ESD failure of the MOSFET happens when the gate-to-source voltage is sufficiently high to damage the gate dielectric. A leakage path across the gate oxide can cause a catastrophic failure.

The scale of sensitivity is also reliant on the input value of the capacitance. Power MOSFETs with considerable chip regions are characterised by input capacitances that are high. As a general rule, the proportionality between the die area and ESD threshold of the component, is obvious based on the capacitance ratio between the MOSFET and the forcing capacitor in the ESD circuit. Damage happens when the voltage throughout the gate oxide drives enough current to disrupt the gate oxide. HBM threshold can improve because of thinner gate oxide in some circumstances because input capacitance rises and decreases the stress on the oxide by rising its magnitude in contrast to the forcing capacitor.

To safeguard a MOSFET from ESD events or any other additional gate voltage, the main goal is to keep the gate-to-source voltage from surpassing the breakdown voltage. In order to achieve this the follow may be needed: -

- ESD protection may be required at all gates to prevent damage during fabrication.
- ESD Protection may also be required at all input/output pads connected to a sensitive region.

- ESD protection may include shorting the gate to the source or applying Zener protection gate-to-source.
- ESD protection may be a function of gate-to-gate spacing's. [74].
- ESD protection usually increases gate leakage.
- ESD protection can increase die size by up to 10%.

ESD protection can be as simple as reversed biased diodes where the diode network prevents $V_{GS}$ from exceeding the oxide breakdown voltage. Diodes should be tied to voltages according to the MOSFET $V_{gs}$ and large voltages across the gate oxide should be avoided. [75]

As stated previously power MOSFETs use a thin oxide to separate the gate electrode from the active area of the transistor. A lot like normal MOSFETs used in the production of microprocessors, a power MOSFET gate oxide is just as vulnerable to damage from ESD events as its smaller counterparts. Causing the same ESD failures as previous stated such as gate-oxide breakdown which is catastrophic failure etc.

Some discrete power MOSFETs and power-block MOSFETs include incorporated ESD protection circuits to prevent unnecessary damage caused by ESD events. There are three types of protection that the company and most manufacturers of discrete power MOSFETs use these being: -

- No ESD protection.
- Single-ended ESD protection.
- Back-to-back ESD protection.

The majority of power MOSFET and power-block MOSFET components produced by the company are in the first type these have no ESD protection. While these power MOSFET, do not have an incorporated gate ESD circuit, they still have a characteristic ESD capacity that ranges from 150 volts to 3,000 volts. Larger die sizes have higher ESD capacities because the ESD capacity is related to device density and charge.

Therefore, the client must constantly confirm that the MOSFET's ESD capacity meets the prerequisites in their products and therefore the client must also, take into consideration adding external ESD protection if it does not. N-channel and P-channel MOSFETs with no integrated ESD protection schematics are showed in figure 6.9.

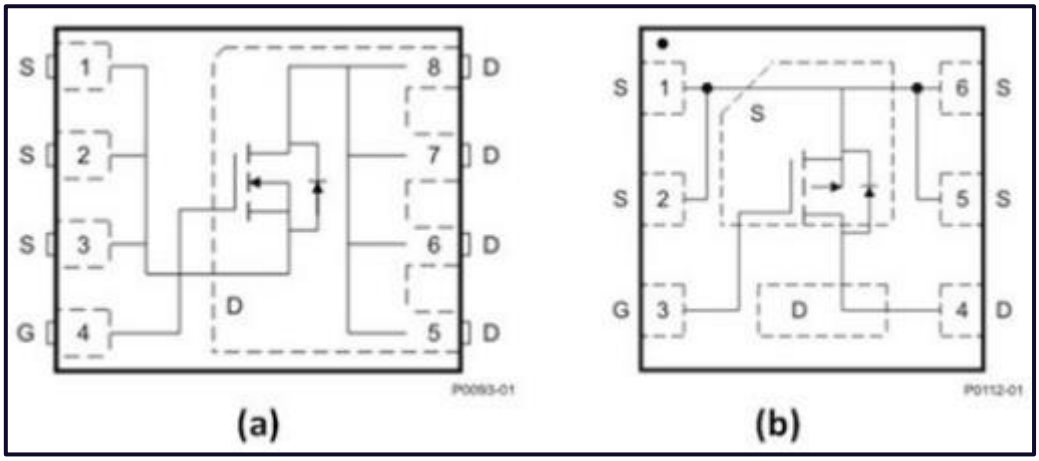


*Figure 6.9 MOSFETs with no ESD protection: (a) N-channel; and (b) P-channel. [91]*

The next type of protection for power MOSFETs are single-ended ESD protection. This has an incorporated, single-ended ESD protection diode from gate to source in N-channel and P-channel MOSFETs. Components of this type can attain ESD ratings of greater than 4,000 volts. In the past, ESD protection of a power MOSFET gate caused a high gate leakage current. However, some components, can now attain leakage specifications as low as twenty-five nA; these components are an improvement over other component with no gate ESD protection.

For example, due to their low gate leakage, these components are ideal for applications which use battery-power where runtime and standby power are crucial. The client must weigh up operational situations to confirm that the ESD diode is not forward biased, or it will conduct current. However, if forward-biasing is necessary, it will be essential to include an external, current-limiting gate resistor in the circuit. Figure 6.10 shows the single-ended ESD protection diode highlighted with N-channel and P-channel schematic symbols.

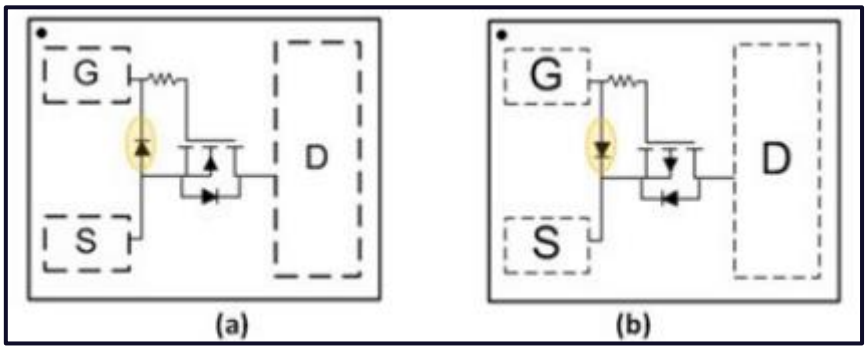


*Figure 8 MOSFETs with single-ended ESD protection (a) N-channel; and (b) P-channel. [91]*

Back-to-back ESD protection circuits are the final type and includes N-channel and P-channel MOSFETs. The ESD capacity of these components goes from four hundred volts up to 3,250 volts. With the back-to-back ESD structure there is no need to be concerned about forward-biasing.

However, back-to-back ESD protection MOSFETs have higher gate leakage current than single-ended ESD protection MOSFETs. For example, a drawback in battery-powered products is the higher gate leakage. Figure 6.11 shows the back-to-back ESD protection diodes highlighted with N-channel and P-channel schematics symbols.

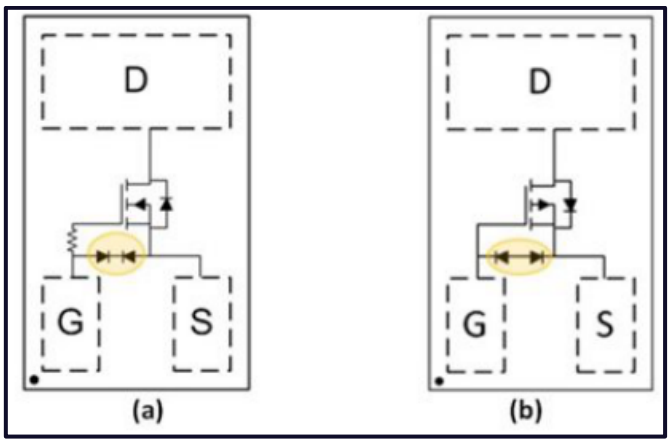


*Figure 6.11 MOSFETs with back-to-back ESD protection :(a) N-channel; and (b) P-channel. [91]*

A protection plan can be made by designers, the protection plan considers all current paths to prevent thermal damage to silicon, either in the internal circuits or in the protection circuit, also every voltage build-up situation is taken into consideration, in an attempt to prevent gate oxide failure. For example, a simplified plan is shown in figure 6.12, and the clamps are described.

- Clamp 1: - Is the main protection design that protects against ESD events by clamping the voltage at the I/O pad and permitting the ESD current to be terminated safely to the ground point. The design of the clamp is selected on the application specifications and the technology of the I/O signal circuitry. This clamp is essential for HBM, and other methods.

- Clamp 2: - Is isolated by resistor R and its main function is to protect the gate oxide of the input NMOS buffer. Clamp 2 triggers before primary Clamp 1. At the same time, resistor R is chosen carefully to limit current to the output buffer and protect the buffer transistors, as well as to satisfy the output buffer operational requirements. This clamp is essential and is particularly critical for the CDM method.

- Clamp 4 and 5: - Protect all of the internal circuits between any power supply and ground. For different VDD supplies, a clamp is placed at every site to ensure that all core and internal logic circuits are protected from an ESD event on the VDD pads. The design of this clamp must take into consideration the burn-in voltage requirements, latch up requirements, and in general must ensure that electrical overstress (EOS) events do not cause failure.

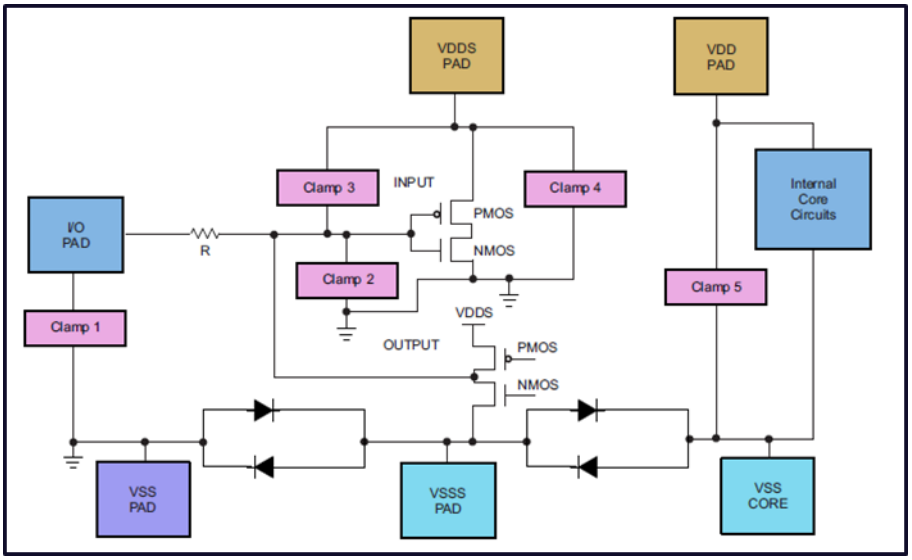


*Figure 6.12 Simplified protection plan. [92]*

The ESD design must make certain that the current path is accessible for all ESD event combinations between an I/O pad and internal grounds. The diode functioning between the grounds thus allows effective ESD current flow.

In principle, the diodes, along with the correct clamps to ground, offer operational protection for HBM, and other methods. A further example of clamping is seen in figure 6.13.

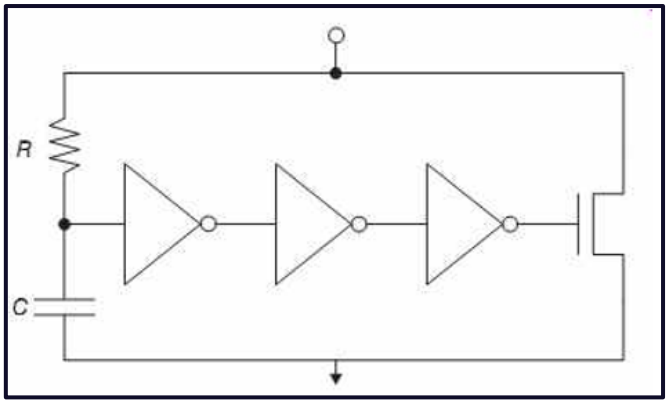


*Figure 6.13 HBM ESD protection device. Power rail to power rail protection. [86]*

This is an example of an ESD network that is placed between two power rails where the first power rail is a VDD power rail, and the second power rail is a VSS power rail. These types of networks are also ESD power clamps. The most frequently used ESD networks are resistor-capacitor (RC)-triggered MOSFET ESD power clamps. This involves a frequency trigger, a MOSFET drive stage, and an O/P MOSFET clamp device. The most commonly used network has a RC discriminator that is modified to react to an HBM ESD pulse event. The MOSFET drive stage contains a series of inverter switches, with intensifying width, to "turn-on" the O/ P MOSFET clamp device. These networks in recent years have been adapted to have a smaller area and respond to faster impulses with lower leakage, plus means to avoid false triggering.

Designers of semiconductor ESD protection must verifying the effectiveness of an ESD device by considering the I-V characterization curves for ESD devices and can be used to verify their proper operation in circuits. The I-V characterization curves are created by using a method called transmission line pulse (TLP) these precise timed square waves are running in the device and a number of measurements are taken. However, software simulation can be inadequate for demonstrating the snapback operation. The result is the negative differential resistance influencing the convergence of the DUT. Incorrectly analysing snapback or discounting it will create results that can lead to ESD events and ESD damage during use. Thus, efficient ESD protection devices will fulfil the following factors: -

- The device as a low leakage current.
- The snapback region is high when there is an ESD current.
- The device response time is fast.
- The device can constantly conduct high voltages and currents over short periods.

As discussed above, the company designs and manufactures devices with ESD protection as a first step towards preventing ESD events within their devices. The second step is to minimise the ESD event exposure by providing systems and safeguards within the manufacturing environment and this will be discussed below.

## 6.3 Precautions Against ESD in the Semiconductor Manufacturing Area

In the semiconductor manufacturing environment, there is four fundamental principles of ESD control. These being: -

- Principle 1: - ESD Technical Elements. All conductors, including personnel, shall be bonded, or electrically connected and attached to a known good ground.
- Principle 2: - Static generators. Non-conductors in the environment cannot lose their electrostatic charge by connection to ground because of stored charge. Devices must be kept thirty centimetres away from static generators to ensure discharge does not occur through the product.
- Principle 3: - Packaging and marking. Transportation of items outside an ESD area requires enclosure in static protective materials.
- Principle 4: - ESD Administrative Elements. Checking Compliance. A regular audit programme is in place to check compliance to the specified requirements.

The corporation has company policies for ESD this to establish all appropriate measures to prevent damage of our devices due to ESD by responding appropriately in relevant areas such as design and development, manufacturing, packaging, testing, packing, handling, and transportation while ensuring the safety of colleagues and visitors.

ESD protection requirements are based on JEDEC standard JESD625B, ANSI/ESD S20.20 and additional requirements as specified by our clients. Also, all colleagues with access to ESD protected areas (EPA) will be trained and awareness training will be conducted regularly, and this is part of the recertification of all trained personal. This is verified by annual audits of the EPA.

The first principle in environmental ESD protection is the ESD technical elements these include areas that are ESD protected and have been established to allow the safe handling of ESDS devices. when personal is entering into an EPA, a warning sign indicates that they have entered into the area and that they have to work inside the area complying to the special ESD rules. The EPA normally for a fab is probe, test, FOPs, and packing. Preceding the probe area, the ESD standards require precautions where appropriate, but do not require the whole area to be ESD protected. It should be

noted that personnel are exposed to hazardous electrical voltages whilst working in an EPA are exempt from ESD guidelines for reasons of safety.

Within the EPA there are work surfaces and workbenches. All work surfaces must be constructed from clean room compliant material and grounded. Certain work surfaces / workbenches have blue matting on the benches. The blue matting is conductive and grounded via the underlying work surfaces / workbenches. The work surfaces / workbenches are designed for ESD protection depending on, how a material will be charged positively or negatively depends on the material with which it contacts and then separates from.

Also, it is important to understand that the amount of charge that accumulates on any surface is reliant on the contacting material, intimacy of contact, speed of separation, cleanliness of surfaces also other physical and chemical factors. It should be noted that all stainless-steel workbenches that house any electrical equipment (including PC benches) must be individually hardwired to ground. This is again for safety reasons and all other stainless-steel work surfaces / workbenches that do not contain equipment used for product, must have conductive feet or an adequate controlled dissipation to ground through the conductive flooring which is throughout the EPA.

At some work surfaces / workbenches there will be seating. Seating within EPA are connected to ground through conductive wheels and drag chains or both. Also, within the EPA there are shelves and trolleys these must be constructed from conductive clean room compliant material for all wafers storage locations and transport trolleys. Shelving must have aluminium conductive collars on every corner plus have aluminium conductive feet and an ESD label on the equipment. Trolleys must have aluminium conductive collar and conductive wheels ensuring grounding through the flooring and ESD labelled. It is important that wafer boxes / lots must not be opened on shelves but taken to a workstation in the EPA and opened there.

Personnel grounding within the EPA consists of fab clean room suits and shoes and over boots. The suits are made of a material which minimises static and are connected together to provide an electrical path to ground through the boot soles this is done by having visible conductive threads. To maintain the integrity of the garments special laundering processes are in place. Damage to the suit must be reported to the supervisors and to the suit vendor. Also, fab clothing must be comfortable; the suit must be zipped up to the top and the press studs must be fastened at wrist, neck, and calf. The total resistance of the fab clean room suits shall be less than $1 \times 10^{9}\Omega$.

The clean room shoes and over boots (footwear systems within the company) have soles that are made from a conductive material. When personal is correctly gowned up, the shoes and boots provide

a path to ground should a charge be generated on the suit. It should be noted that when the clean room shoes / over boots with the conductive floor is used as the primary grounding system for personal then either of the following condition's must be met.

The total resistance of the system is less than 3.5 x $10^7\Omega$ or the total resistance of the system is less than 3.5 x $10^7\Omega$ and less 1 x $10^9\Omega$ with a voltage less than one hundred volts on personal.

In the EPA are areas, where the manual handling of wafers is required then grounded vac pens are used. This is equivalent to wearing a wrist strap because wafers including dummies should not be touched by hand. It is important that limited manual handling is only performed using a conductive vac pen / wand.

The second principle in environmental ESD protection is static generators within the EPA these are any static generator material generating ±1000V must be controlled or eliminated. Control of these static generators requires these materials to be kept at least 30cm away from product. Examples of static generators in a wafer fab are: -

- Work instruction wallets.
- Old CRT monitors.
- Bin bags that are not ESD compliant, so bins have designated areas that have defined areas throughout the fab and within the EPA where bins are to be permanently located.

Also within EPA are air ionisers that can neutralise the static charges on insulated and isolated objects, however it is not a replacement for grounding methods but an addition. Air ionisers are located in probe, test, FOPs, packing, and also included within individual machines.

The ioniser height is based on a balance of comfort versus effectiveness over work surfaces / workbenches. Also, all packing and unpacking of wafers is done under ionisation in designated EPA throughout the fab.

The third principle in environmental ESD protection is packaging and marking, the company shall define ESD protective packaging requirements, both inside and outside the EPA. Protective packaging is necessary to store, transport and protect ESD sensitive devices during production phases. The selection of an ESD protective packaging is done regarding: -

- The sensitivity of the devices: -
    - Damage models and testing methods are used to determine the sensitivity.

    - If the device is robust and less sensitive to ESD, the level of protective packaging can be reduced. If it is extremely sensitive, maximum protective properties should be used.
    - If the sensitivity is unknown, the maximum level of protective packaging should be used.
- The threats that a package will be exposed to: -
    - EPA where ESD is controlled. Even though ESD control exist, some potential for ESD damages remains.
    - Uncontrolled area where the packaged devices will be subjected to ESD from people, machines, and other many sources.
- The ways that packaging can protect sensitive devices.
    - ESD protective packaging has properties to prevent static electricity from damaging the packaged devices.
    - The three key properties are low charging, resistance (insulative, dissipative or conductive) and shielding.

Inside the EPA the packaging must be, at least, low charging, and have dissipative or conductive materials in close contact with ESD sensitive items. Outside the EPA the packaging must provide, low charging, have dissipative or conductive materials in intimate contact in ESD sensitive items, and provide static shielding protection.

While transporting the devices outside after ESD protection is tackled, the choice of package should be based on the need for physical protection and how the package interfaces with the production and transportation processes.

Inside the EPA the packing of wafers in wafer tubs are protected by liners / covers manufactured in ESD foam which is pink, and the wafers are only protected when inside the wafer tubs. The wafers are at risk during the packing / unpacking process as wafers will come in close proximity of the wafer tub. Also, all unpacking / packing of wafers is be done under ionisation and on ESD safe work surfaces / workbenches.

Tubs are packed in shielded bags and should be removed under ionisation. Outside the EPA incoming silicon wafer boxes are normally manufactured from polypropylene which are not ESD safe. It should be noted that wafers in black wafer boxes and black shells require no additional protection.

Marking for ESD sensitive assemblies and equipment as well as packaging materials is not optional and should be documented in the ESD control program. If this symbol is on any packaging, then it shows it is ESD safe. As seen in figure 6.14.


*Figure 9 label showing ESD safe. [93]*

Symbols for ESD safe packing- material with an indication of the type of protection:

- S-Electrostatic discharge shielding
- D-Electrostatic dissipative
- L-Low charging
- C-Electrostatic conductive

If no symbol is present, then assume that the material is not ESD safe. The ESD susceptibility symbol in figure 6.15 is applied directly to ICs, PCBs, and assemblies that are static sensitive. It indicates that handling or use of this item may result in damage from ESD if proper precautions are not taken.

*Figure 6.15 ESD susceptibility symbol. [93]*

The symbol in figure 6.16 indicates ESD protective material. It is applied to mats, chairs, garments, packaging, and other items that provide ESD protection.

*Figure 6.16 ESD protective material. [93]*

The fourth principle in environmental ESD protection is administrative elements these are where the company will prepare training for personal and compliance documents that deal with each of the requirements of the ESD environmental protection these being: -

- Training.
- Compliance verification.
- Grounding / equipotential bonding systems.
- Personnel grounding.
- EPA requirements.
- Packaging systems.
- Marking.

A training plan for all personnel handling or otherwise coming into contact with ESD sensitive devices. The initial training of personal will be required before entering an EPA and before first handling any ESD sensitive devices. Retraining of personal is recommended every two years. The training plan shall define the type and frequency of ESD training for personnel. It shall also include training records and the methods used to verify comprehension and training competence of the trainee.

The compliance verification plan shall be established to ensure the fulfilment of the technical requirements of the ESD control program plan and will include the technical requirements of ESD control these being below and modifying training and plans statement if needed: -

- Frequency.
- Measurements limits.
- Test method.

Audit each operation involving the processing, handling, or storage of ESD sensitive devices, at least annually to verify compliance with the specified requirement. The objective of the audit process is to demonstrate that the company conform to the standard’s laid out, and to highlight plus fix any problems. This audit process will follow a defined company checklist.

# Chapter 7 Conclusion and Future developments

## 7.1 Conclusion

I am disappointed that the HBM ESD tester did not produce the results that I was expecting. I suspect it is due to the reasons stated in the results section. The voltage generator was unable to produce the voltage that was needed, and it was the only one available to me within my company. The probe station as stated is rated up to 200 - 230 volts and was suitable for the voltage range used. As for my HBM ESD tester the voltage output was limited due to the components used. For example, the push buttons were rated up to 700 volts DC and was mechanical in operation therefore switch "bounce" could be a factor. Solid state relays would remove this but again is limited because of the specifications of the components.

Another way of designing the HBM ESD tester to remove switch bounce is to replace the charging switch with a relay and the discharge switch with a mercury relay switch coupling both to a driving circuit to perform the same functions as the switches already in the tester.

Also going to the electronics laboratory in Swansea University would help because there is no electronics laboratory within my company and the tester had to designed and constructed during my shift's, permission was granted by my company and also on my days off. Also, the FA department is only accessible during the day.

However disappointed I am with the results of the HBM ESD tester, ESD events are real as stated in this thesis and various papers / sources and therefore are unavoidable in semiconductor production and also when clients use the components in manufacturing their own products i.e. automotive. The results of ESD events in this thesis are costly in company resources and personal as well as the companies time and not forgetting that the client will have problems from ESD events that could occur from within the company. The most challenging part of this thesis overall was dealing with the government restrictions imposed on Nexperia at the time this was written.

The continual development of better protection circuits and understanding of ESD protected environments is still needed as stated as semiconductor technology continues to develop now and into the future. However, this thesis was not intended to be an all-inclusive report on all events involving ESD within the semiconductor technology areas. But was intended to stimulate interest in working towards the mitigation of ESD events within the various production areas of the company.

In conclusion, the susceptibility of power MOSFETs to ESD events, as replicated by the HBM, could cause significant challenges in ensuring the reliability and performance of

semiconductors. Throughout this thesis, I have examined the characteristics of Power MOSFETs, the mechanisms of ESD damage, and the implications of HBM testing on device integrity.

To effectively mitigate the risk of ESD event failures in power MOSFETs, a multi-layered approach is still necessary now and, in the future, as stated above this still consists of engineers having a deep and comprehensive understanding of the physical principles underlying ESD events and the specific vulnerabilities of power MOSFETs to help to design robust protection approaches.

These approaches still need to use the utilisation of advanced simulation tools and methods, such as SPICE simulations and finite element analysis, can assist in predicting and analysing the behaviour of power MOSFETs under ESD stress. Also, the addition of innovative designing, including layout optimisation, ESD protection circuitry, and selection of materials, can increase the resilience of power MOSFETs against ESD events.

Also, the company will still need to adhere to the protocols and industry standards for ESD testing and mitigation of these events. This is essential to ensure the reliability and compliance of power MOSFET applications and the company will need to continue to monitor ESD events within the production areas, by analysing the failure modes and refining mitigation strategies used in the company. This will be critical for staying up to date with the evolving ESD challenges and advancing the reliability of power MOSFET technologies to the clients that the company produces wafers for.

By applying these methods, the company's researchers, engineers, can tackle the complicated relationship between power MOSFETs, HBM ESD events, and risk mitigation strategies, thereby promoting the enhancement of resilient power MOSFETs, capable of withstanding the challenges of modern operating environments. This thesis promotes the wider body of knowledge in power MOSFETs, reliability and ESD protection, paving the way for enhanced performance and longevity of power MOSFET-based applications in diverse sectors.

## 7.2 Future improvements and developments

In spite of the disappointing results from the HBM ESD tester, the insights I have gained have provided a well-defined pathway for future improvements and developments. Several important factors have been identified for further research and development these being:-

- Enhanced voltage generation:-
    - To address the limitations of the current voltage generator within the FA department, a future improvement would be purchasing a high-precision voltage generators that meet the testing requirements for HBM ESD testers. This system should be able to constantly generate the required voltage levels for the HBM ESD testing. Other measures that the company could develop in the future are forming a collaborative development with manufacturers to develop custom voltage generation solutions tailored to the needs of HBM ESD testing.
- Improved switching mechanisms: -
    - The mechanical push buttons currently used in the HBM ESD tester create problems such as switch bounce. To overcome this, further designs should integrate better switching mechanisms such as utilising solid state relays to replace the push buttons, thus removing switch bounce and improving reliability and implement mercury relay switches for the discharge process to ensure stable and consistent switching operation. Also developing and integrating driving circuits to control the new switching operations, to ensure they function effectively within the tester.
- Access to advanced testing facilities: -
    - The limitations imposed by the lack of an electronics laboratory within the company highlight the need for better testing infrastructure this can be done by re-establishing partnerships with universities such as Swansea University to access their electronics laboratories. Therefore, providing the necessary resources and environment for accurate and reliable testing, and the company should invest in an in-house electronics laboratory equipped with the necessary tools and instruments for ESD testing and research.
- Comprehensive ESD event analysis: -
    - To further the understanding of ESD events and their impact on power MOSFETs, and semiconductors a multi-faceted approach should be used such as utilising tools like SPICE simulations and finite element analysis to predict and analyse the behaviour of power MOSFETs and semiconductors under ESD stress. Also, the

company can perform detailed analyses of failure modes in power MOSFETs due to ESD events to improve protection strategies within the company.

- Optimised design and materials: -
    - To increase the resilience of power MOSFETs against ESD events, future developments within the company design departments should focus on innovative design and material selection therefore optimising the layout of power MOSFETs to enhance their ESD resilience. Also designing and integrating advanced ESD protection circuits to protect sensitive components and investigating and using materials with superior ESD protection properties.
- Adherence to Industry Standards: -
    - Maintaining compliance with industry standards is crucial for ensuring the reliability and performance of ESD protection strategies this can be done by regularly reviewing and updating ESD testing and mitigation protocols to evolve with emerging industry standards. Also, the company must ensure strict adherence to established protocols to maintain high reliability and compliance.
- Ongoing Research and Development: -
    - Continued research and development efforts are essential for staying ahead of ESD challenges presented by advancing semiconductor technology this can be done by promoting relationships between researchers, engineers, and industry experts to drive innovation in ESD protection. Also, the company can share findings and advancements through publications, conferences, and industry forums to contribute to the broader body of knowledge.

Also, dealing with the issues related to the breakdown voltage of air as I found out, is crucial for accurate and reliable testing. The following can be considered for future improvements and developments:-

- Enhancing Test Environment Control: -
    - Develop more sophisticated systems to monitor and control the environmental conditions (temperature, humidity, air pressure) in the testing chamber. Air's breakdown voltage varies with these factors, so precise control and real-time adjustment can minimize their impact on testing outcomes.
    - Implement automated calibration systems that adjust the HBM tester parameters based on real-time environmental data to maintain consistent testing conditions.

- Advanced Shielding Techniques: -
    - Research and integrate advanced materials for better shielding against environmental interference, thereby reducing the likelihood of unwanted discharges that can occur due to the breakdown of air.
    - Incorporate electromagnetic shielding to reduce the influence of external electric fields, which can contribute to air breakdown during testing.
- Refining Discharge Models: -
    - Develop models that account for varying breakdown voltages due to environmental changes. These models could adjust the expected discharge levels dynamically, providing more accurate results across different conditions.
    - Use machine learning to analyse test data and predict environmental conditions that may lead to premature breakdown. This predictive capability could help pre-emptively adjust testing protocols.
- Enhanced Tester Design: -
    - Redesign the tester's probe tips to minimize the air gap or create controlled environments within the probes themselves. This can help manage the breakdown voltage more effectively.
    - Design testers that can switch between conventional air-gap discharge and a controlled environment mode, allowing for testing in varied scenarios.
- Improved Software Algorithms: -
    - Develop algorithms to compensate for variations in breakdown voltage due to environmental factors. These could adjust the applied voltage or correct the measured data, ensuring that the results reflect the true ESD characteristics of the device under test.
    - Create advanced data analysis tools that can detect patterns related to environmental changes, allowing testers to differentiate between genuine ESD events and those influenced by air breakdown.
- Standardisation and Testing Protocols: -
    - Work with standards organisations to refine testing protocols that consider the variability in air breakdown voltage, possibly by incorporating more stringent environmental controls or standardised compensation techniques.
    - Multi-Condition Testing: Introduce testing protocols that require devices to be tested under a range of environmental conditions to ensure reliability across different real-world scenarios.

- Alternative Testing Methods:-
    - Explore and develop alternative ESD testing methods that do not rely on air as a medium, such as liquid or solid dielectric environments, where the breakdown voltage is more predictable and controllable.
    - Develop virtual testing environments that simulate the effects of different environmental conditions on ESD testing, allowing for comprehensive analysis without physical limitations.

By tackling the breakdown voltage of air in HBM ESD testers a multi-faceted approach, combining hardware, software, and procedural improvements can be used, so that future testers can provide more accurate and reliable measurements, even under varying environmental conditions, and by identifying the imperfections in the current HBM ESD tester and pursuing these in future developments, significant improvements can be made in the testing, design, and protection of power MOSFETs against ESD events. These efforts will enhance the reliability, performance, and longevity of semiconductor devices, ultimately benefiting the company and its clients.

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# Appendix 1 Standards for Electrostatic Discharge Testing

**USA standards**

- **ANSI/ESD S20.20** this replaces the following standards: -
  - MIL-STD 1686
  - ANSI/EIA-625 ESD Control Standards.
- **ANSI/ESD ESD-STM 5.1 - 2007** - ESD Association Standard Test Method for the Protection of Electrostatic Discharge Sensitive Items - Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) Testing - Component Level. Standard Test Method (STM) document, 2007.
- **ANSI C63.14:1998**—American national standard dictionary for technologies of electromagnetic compatibility (EMC), electromagnetic pulse (EMP), and electrostatic discharge (ESD)—Dictionary of EMC/EMP/ESD terms and definitions.
- **ANSI C63.16:1993**—American national standard guide for electrostatic discharge test methodologies and criteria for electronic equipment.
- **ASTM D2679-95 (2005)**—Standard test method for electrostatic charge; Reapproved: 2005.
- **ASTM D3509:1982** - Electrostatic field strength due to static charge
- **ASTM F150:2006**—Standard test method for electrical resistance of conductive and static dissipative resilient flooring.
- **IEC/PAS 62162 Ed. 1.0 en:2000** - Field-induced charged-device model test method for electrostatic discharge withstand thresholds of microelectronic components.
- **ASTM D4470-97(2004)** - Standard Test Method for Static Electrification

**European Standards**

- **BS 6667 P2:1985** - Method of evaluating susceptibility to electrostatic discharge.
- **BS 7506 P1** - Methods for measurement in electrostatics - Part 1 - Guide to basic electrostatics
- **BS 7506 P2** - Methods for measurement in electrostatics - Part 2 - Test methods
- **BS EN ISO 21179:2006** - Light conveyor belts—Determination of the electrostatic field generated by a running light conveyor belt.
- **CECC 00015 P1:1992**—Basic specification for protection of electrostatic sensitive devices. Part 1 - General requirements.
- **EN 55024:1989** - Electrostatic discharge requirements

## IEC Standards

- **IEC 60050 Ed 1.0, 1990** - International Electro Technical Vocabulary
- **IEC 60801-2:1991**—Electromagnetic compatibility for industrial-process measurement and control equipment—Electrostatic discharge requirements.
- **IEC 61340-2-1:2002**—Electrostatics—Part 2-1: Measurement methods—Ability of materials and products to dissipate static electric charge.
- **IEC 61340-2-2:2000**—Electrostatics—Part 2-2: Measurement methods—Measurement of chargeability.
- **IEC 61340-3-1, Ed 2.0, 2006**—Electrostatics—Part 3-1: Methods for simulation of electrostatic effects—Human body model (HBM) electrostatic discharge test waveforms
- **IEC 61340-3-2, Ed 2.0, 2006**—Electrostatics—Part 3-2: Methods for simulation of electrostatic effects—Machine model (MM) electrostatic discharge test waveforms
- **IEC 61340-5-1, Ed 1.0, 2007**—Electrostatics—Part 5-1: Protection of electronic devices from electrostatic phenomena—General requirements.
- **IEC TR61340-5-2, Ed 1.0, 2007**—Electrostatics—Part 5-2: Protection of electronic devices from electrostatic phenomena—User Guide
- **IEC/PAS 62179:2000**—Electrostatic discharge (ESD) sensitivity testing human body model (HBM).
- **IEC/PAS 62180:2000**—Electrostatic discharge (ESD) sensitivity testing machine model (MM).
- **IEEE C62.38-1994**—IEEE guide on electrostatic discharge (ESD)—ESD withstand capability evaluation methods (for electronic equipment subassemblies).

## IEEE Standards

- **IEEE C62.47:1992**—IEEE guide on ESD—Characterization of the ESD environment; Reaffirmed: 1997.
- **IEEE C63.14-1998** - American National Standard dictionary for technologies of Electromagnetic Compatibility (EMC), Electromagnetic Pulse (EMP) and Electrostatic Discharge (ESD)
- **IEEE C63.16-1993** - American National Standard Guide for electrostatic discharge test methodologies and criteria for electronic equipment.

# Appendix 2 Time Frame for Thesis

| Thesis: - Power MOSFET ESD Analysis and Risk Mitigation | | | | | | |
|---|---|---|---|---|---|---|
| Thesis Start Date: | 04/04/2022 | | | | | |
| Thesis Author: | Ian. Gilbert. | | | | | |
| WBS | Task | Start | End | Days | % Done | Work Days |
| 1 | Research and interim report | 04/04/2022 | 07/08/2022 | 126 | 100 | 85 |
| 1.1 | Design thesis to Nexperia needs | 04/04/2022 | 10/04/2022 | 7 | 100 | 5 |
| 1.2 | Research of MOSFET. | 11/04/2022 | 01/05/2022/ | 21 | 100 | 13 |
| 1.3 | Research of Electrostatic Discharge (ESD) | 02/05/2022 | 22/04/2022 | 21 | 100 | 14 |
| 1.4 | Research of Human Body Models (HBM) | 22/05/2022 | 12/06/2022 | 21 | 100 | 13 |
| 1.5 | Research Risk migration | 13/06/2022 | 03/06/2022 | 21 | 100 | 15 |
| 1.6 | Gantt Chart | 04/07/2022 | 17/07/2022 | 7 | 100 | 5 |
| 1.7 | Risk Assessment | 11/07/2022 | 17/07/2022 | 7 | 100 | 5 |
| 1.8 | Complete Report | 18/07/2022 | 07/08/2022 | 21 | 100 | 15 |
| 2 | Design Stage | 08/08/2022 | 25/08/2022 | 49 | 0 | 34 |
| 2.1 | Design PCB | 08/08/2022 | 28/08/2022 | 21 | 0 | 15 |
| 2.2 | Order components | 29/08/2022 | 11/08/2022 | 14 | 0 | 9 |
| 2.3 | Ask Swansea university to product PCB | 12/08/2022 | 25/08/2022 | 14 | 0 | 10 |
| 3 | Assembly and initial testing | 26/09/2022 | 22/02/2020 | 105 | 0 | 72 |
| 3.1 | Assembly HBM ESD tester | 26/09/2022 | 16/102022 | 21 | 0 | 15 |
| 2.6 | Debug HBM ESD tester | 17/10/2022 | 06/11/2022 | 21 | 0 | 15 |
| 3.2 | Initial testing HBM ESD Tester | 07/11/2022 | 27/11/2022 | 21 | 0 | 15 |
| 3.3 | Evaluate capability HBM ESD Tester | 28/11/2022 | 08/01/2023 | 42 | 0 | 27 |
| 4 | Qualification | 09/01/2023 | 02//04/2023 | 84 | 0 | 60 |
| 4.1 | Reliability Testing | 09/01/2023 | 19/02/2023 | 42 | 0 | 30 |
| 4.3 | Further testing of HBM ESD tester | 20/02/2023 | 26/06/2022 | 35 | 0 | 25 |
| 4.4 | Production Release | 27//03/2023 | 02//04/2023 | 7 | 0 | 5 |
| 5 | Future | 03/04/2023 | 03/04/2023 | 28 | 0 | 18 |
| 5.1 | Evaluate potential improvements | 03/04/2023 | 30/04/2023 | 28 | 0 | 18 |
| 6 | Writing up of thesis | 03/04/2024 | 01/04/2024 | 0 | 0 | 0 |
| 6.1 | Produce thesis | 03/04/2023 | 01/04/2024 | 0 | 0 | 0 |

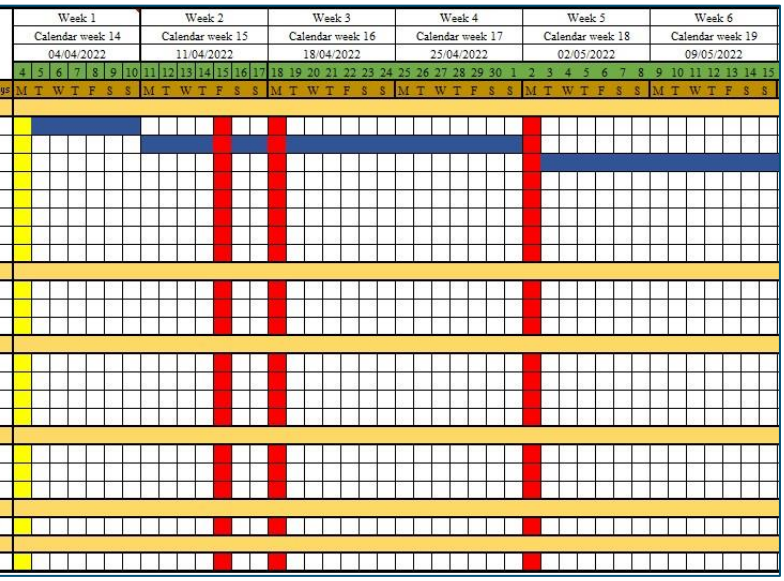


*Chart 1*

| Thesis: - Power MOSFET ESD Analysis and Risk Mitigation | | | | | | |
|---|---|---|---|---|---|---|
| Thesis Start Date: | 04/04/2022 | | | | | |
| Thesis Author: | Ian. Gilbert. | | | | | |
| WBS | Task | Start | End | Days | % Done | Work Days |
| 1 | Research and interim report | 04/04/2022 | 07/08/2022 | 126 | 100 | 85 |
| 1.1 | Design thesis to Nexperia needs | 04/04/2022 | 10/04/2022 | 7 | 100 | 5 |
| 1.2 | Research of MOSFET. | 11/04/2022 | 01/05/2022/ | 21 | 100 | 13 |
| 1.3 | Research of Electrostatic Discharge (ESD) | 02/05/2022 | 22/04/2022 | 21 | 100 | 14 |
| 1.4 | Research of Human Body Models (HBM) | 22/05/2022 | 12/06/2022 | 21 | 100 | 13 |
| 1.5 | Research Risk migration | 13/06/2022 | 03/06/2022 | 21 | 100 | 15 |
| 1.6 | Gantt Chart | 04/07/2022 | 17/07/2022 | 7 | 100 | 5 |
| 1.7 | Risk Assessment | 11/07/2022 | 17/07/2022 | 7 | 100 | 5 |
| 1.8 | Complete Report | 18/07/2022 | 07/08/2022 | 21 | 100 | 15 |
| 2 | Design Stage | 08/08/2022 | 25/08/2022 | 49 | 0 | 34 |
| 2.1 | Design PCB | 08/08/2022 | 28/08/2022 | 21 | 0 | 15 |
| 2.2 | Order components | 29/08/2022 | 11/08/2022 | 14 | 0 | 9 |
| 2.3 | Ask Swansea university to product PCB | 12/08/2022 | 25/08/2022 | 14 | 0 | 10 |
| 3 | Assembly and initial testing | 26/09/2022 | 22/02/2020 | 105 | 0 | 72 |
| 3.1 | Assembly HBM ESD tester | 26/09/2022 | 16/102022 | 21 | 0 | 15 |
| 2.6 | Debug HBM ESD tester | 17/10/2022 | 06/11/2022 | 21 | 0 | 15 |
| 3.2 | Initial testing HBM ESD Tester | 07/11/2022 | 27/11/2022 | 21 | 0 | 15 |
| 3.3 | Evaluate capability HBM ESD Tester | 28/11/2022 | 08/01/2023 | 42 | 0 | 27 |
| 4 | Qualification | 09/01/2023 | 02//04/2023 | 84 | 0 | 60 |
| 4.1 | Reliability Testing | 09/01/2023 | 19/02/2023 | 42 | 0 | 30 |
| 4.3 | Further testing of HBM ESD tester | 20/02/2023 | 26/06/2022 | 35 | 0 | 25 |
| 4.4 | Production Release | 27//03/2023 | 02//04/2023 | 7 | 0 | 5 |
| 5 | Future | 03/04/2023 | 03/04/2023 | 28 | 0 | 18 |
| 5.1 | Evaluate potential improvements | 03/04/2023 | 30/04/2023 | 28 | 0 | 18 |
| 6 | Writing up of thesis | 03/04/2024 | 01/04/2024 | 0 | 0 | 0 |
| 6.1 | Produce thesis | 03/04/2023 | 01/04/2024 | 0 | 0 | 0 |

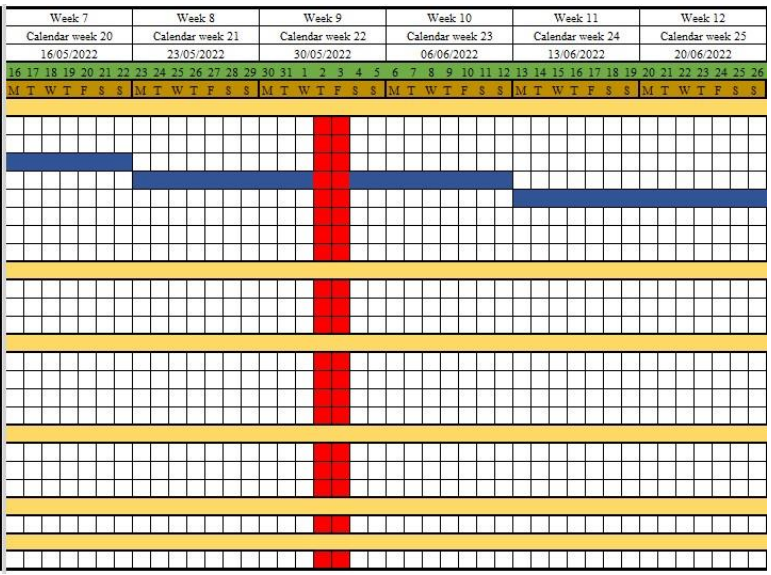


*Chart 2*

| Thesis: - Power MOSFET ESD Analysis and Risk Mitigation | |
|---|---|
| Thesis Start Date: | 04/04/2022 |
| Thesis Author: | Ian. Gilbert. |

| WBS | Task | Start | End | Days | % Done | Work Days |
|---|---|---|---|---|---|---|
| 1 | Research and interim report | 04/04/2022 | 07/08/2022 | 126 | 100 | 85 |
| 1.1 | Design thesis to Nexperia needs | 04/04/2022 | 10/04/2022 | 7 | 100 | 5 |
| 1.2 | Research of MOSFET. | 11/04/2022 | 01/05/2022/ | 21 | 100 | 13 |
| 1.3 | Research of Electrostatic Discharge (ESD) | 02/05/2022 | 22/04/2022 | 21 | 100 | 14 |
| 1.4 | Research of Human Body Models (HBM) | 22/05/2022 | 12/06/2022 | 21 | 100 | 13 |
| 1.5 | Research Risk migration | 13/06/2022 | 03/06/2022 | 21 | 100 | 15 |
| 1.6 | Gantt Chart | 04/07/2022 | 17/07/2022 | 7 | 100 | 5 |
| 1.7 | Risk Assessment | 11/07/2022 | 17/07/2022 | 7 | 100 | 5 |
| 1.8 | Complete Report | 18/07/2022 | 07/08/2022 | 21 | 100 | 15 |
| 2 | Design Stage | 08/08/2022 | 25/08/2022 | 49 | 0 | 34 |
| 2.1 | Design PCB | 08/08/2022 | 28/08/2022 | 21 | 0 | 15 |
| 2.2 | Order components | 29/08/2022 | 11/08/2022 | 14 | 0 | 9 |
| 2.3 | Ask Swansea university to product PCB | 12/08/2022 | 25/08/2022 | 14 | 0 | 10 |
| 3 | Assembly and initial testing | 26/09/2022 | 22/02/2020 | 105 | 0 | 72 |
| 3.1 | Assembly HBM ESD tester | 26/09/2022 | 16/102022 | 21 | 0 | 15 |
| 2.6 | Debug HBM ESD tester | 17/10/2022 | 06/11/2022 | 21 | 0 | 15 |
| 3.2 | Initial testing HBM ESD Tester | 07/11/2022 | 27/11/2022 | 21 | 0 | 15 |
| 3.3 | Evaluate capability HBM ESD Tester | 28/11/2022 | 08/01/2023 | 42 | 0 | 27 |
| 4 | Qualification | 09/01/2023 | 02//04/2023 | 84 | 0 | 60 |
| 4.1 | Reliability Testing | 09/01/2023 | 19/02/2023 | 42 | 0 | 30 |
| 4.3 | Further testing of HBM ESD tester | 20/02/2023 | 26/06/2022 | 35 | 0 | 25 |
| 4.4 | Production Release | 27//03/2023 | 02//04/2023 | 7 | 0 | 5 |
| 5 | Future | 03/04/2023 | 03/04/2023 | 28 | 0 | 18 |
| 5.1 | Evaluate potential improvements | 03/04/2023 | 30/04/2023 | 28 | 0 | 18 |
| 6 | Writing up of thesis | 03/04/2024 | 01/04/2024 | 0 | 0 | 0 |
| 6.1 | Produce thesis | 03/04/2023 | 01/04/2024 | 0 | 0 | 0 |

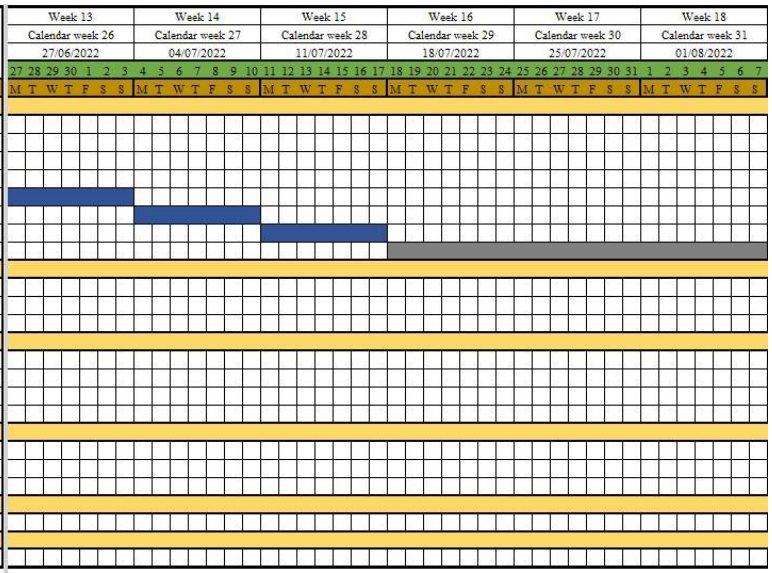


*Chart 3*

| Thesis: - Power MOSFET ESD Analysis and Risk Mitigation | |
|---|---|
| Thesis Start Date: | 04/04/2022 |
| Thesis Author: | Ian. Gilbert. |

| WBS | Task | Start | End | Days | % Done | Work Days |
|---|---|---|---|---|---|---|
| 1 | Research and interim report | 04/04/2022 | 07/08/2022 | 126 | 100 | 85 |
| 1.1 | Design thesis to Nexperia needs | 04/04/2022 | 10/04/2022 | 7 | 100 | 5 |
| 1.2 | Research of MOSFET. | 11/04/2022 | 01/05/2022/ | 21 | 100 | 13 |
| 1.3 | Research of Electrostatic Discharge (ESD) | 02/05/2022 | 22/04/2022 | 21 | 100 | 14 |
| 1.4 | Research of Human Body Models (HBM) | 22/05/2022 | 12/06/2022 | 21 | 100 | 13 |
| 1.5 | Research Risk migration | 13/06/2022 | 03/06/2022 | 21 | 100 | 15 |
| 1.6 | Gantt Chart | 04/07/2022 | 17/07/2022 | 7 | 100 | 5 |
| 1.7 | Risk Assessment | 11/07/2022 | 17/07/2022 | 7 | 100 | 5 |
| 1.8 | Complete Report | 18/07/2022 | 07/08/2022 | 21 | 100 | 15 |
| 2 | Design Stage | 08/08/2022 | 25/08/2022 | 49 | 0 | 34 |
| 2.1 | Design PCB | 08/08/2022 | 28/08/2022 | 21 | 0 | 15 |
| 2.2 | Order components | 29/08/2022 | 11/08/2022 | 14 | 0 | 9 |
| 2.3 | Ask Swansea university to product PCB | 12/08/2022 | 25/08/2022 | 14 | 0 | 10 |
| 3 | Assembly and initial testing | 26/09/2022 | 22/02/2020 | 105 | 0 | 72 |
| 3.1 | Assembly HBM ESD tester | 26/09/2022 | 16/102022 | 21 | 0 | 15 |
| 2.6 | Debug HBM ESD tester | 17/10/2022 | 06/11/2022 | 21 | 0 | 15 |
| 3.2 | Initial testing HBM ESD Tester | 07/11/2022 | 27/11/2022 | 21 | 0 | 15 |
| 3.3 | Evaluate capability HBM ESD Tester | 28/11/2022 | 08/01/2023 | 42 | 0 | 27 |
| 4 | Qualification | 09/01/2023 | 02//04/2023 | 84 | 0 | 60 |
| 4.1 | Reliability Testing | 09/01/2023 | 19/02/2023 | 42 | 0 | 30 |
| 4.3 | Further testing of HBM ESD tester | 20/02/2023 | 26/06/2022 | 35 | 0 | 25 |
| 4.4 | Production Release | 27//03/2023 | 02//04/2023 | 7 | 0 | 5 |
| 5 | Future | 03/04/2023 | 03/04/2023 | 28 | 0 | 18 |
| 5.1 | Evaluate potential improvements | 03/04/2023 | 30/04/2023 | 28 | 0 | 18 |
| 6 | Writing up of thesis | 03/04/2024 | 01/04/2024 | 0 | 0 | 0 |
| 6.1 | Produce thesis | 03/04/2023 | 01/04/2024 | 0 | 0 | 0 |

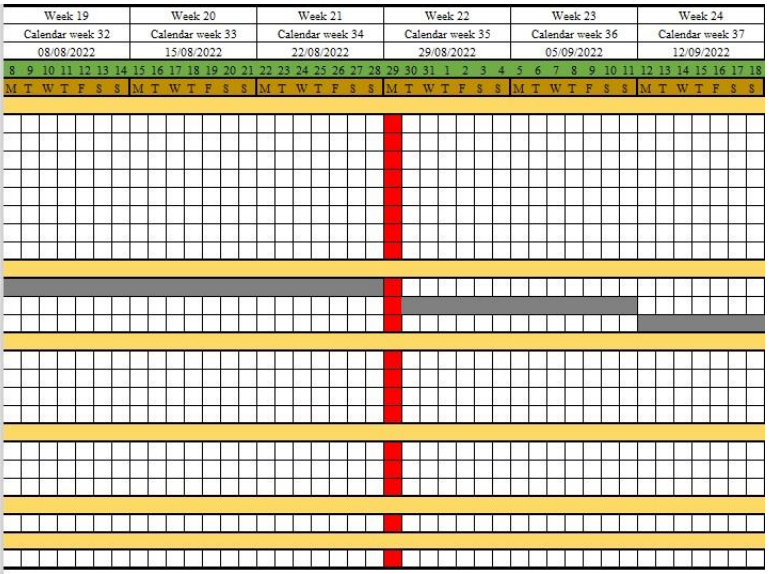


*Chart 4*

| Thesis: - Power MOSFET ESD Analysis and Risk Mitigation | |
|---|---|
| Thesis Start Date: | 04/04/2022 |
| Thesis Author: | Ian. Gilbert. |

| WBS | Task | Start | End | Days | % Done | Work Days |
|---|---|---|---|---|---|---|
| 1 | Research and interim report | 04/04/2022 | 07/08/2022 | 126 | 100 | 85 |
| 1.1 | Design thesis to Nexperia needs | 04/04/2022 | 10/04/2022 | 7 | 100 | 5 |
| 1.2 | Research of MOSFET. | 11/04/2022 | 01/05/2022/ | 21 | 100 | 13 |
| 1.3 | Research of Electrostatic Discharge (ESD) | 02/05/2022 | 22/04/2022 | 21 | 100 | 14 |
| 1.4 | Research of Human Body Models (HBM) | 22/05/2022 | 12/06/2022 | 21 | 100 | 13 |
| 1.5 | Research Risk migration | 13/06/2022 | 03/06/2022 | 21 | 100 | 15 |
| 1.6 | Gantt Chart | 04/07/2022 | 17/07/2022 | 7 | 100 | 5 |
| 1.7 | Risk Assessment | 11/07/2022 | 17/07/2022 | 7 | 100 | 5 |
| 1.8 | Complete Report | 18/07/2022 | 07/08/2022 | 21 | 100 | 15 |
| 2 | Design Stage | 08/08/2022 | 25/08/2022 | 49 | 0 | 34 |
| 2.1 | Design PCB | 08/08/2022 | 28/08/2022 | 21 | 0 | 15 |
| 2.2 | Order components | 29/08/2022 | 11/08/2022 | 14 | 0 | 9 |
| 2.3 | Ask Swansea university to product PCB | 12/08/2022 | 25/08/2022 | 14 | 0 | 10 |
| 3 | Assembly and initial testing | 26/09/2022 | 22/02/2020 | 105 | 0 | 72 |
| 3.1 | Assembly HBM ESD tester | 26/09/2022 | 16/102022 | 21 | 0 | 15 |
| 2.6 | Debug HBM ESD tester | 17/10/2022 | 06/11/2022 | 21 | 0 | 15 |
| 3.2 | Initial testing HBM ESD Tester | 07/11/2022 | 27/11/2022 | 21 | 0 | 15 |
| 3.3 | Evaluate capability HBM ESD Tester | 28/11/2022 | 08/01/2023 | 42 | 0 | 27 |
| 4 | Qualification | 09/01/2023 | 02//04/2023 | 84 | 0 | 60 |
| 4.1 | Reliability Testing | 09/01/2023 | 19/02/2023 | 42 | 0 | 30 |
| 4.3 | Further testing of HBM ESD tester | 20/02/2023 | 26/06/2022 | 35 | 0 | 25 |
| 4.4 | Production Release | 27//03/2023 | 02//04/2023 | 7 | 0 | 5 |
| 5 | Future | 03/04/2023 | 03/04/2023 | 28 | 0 | 18 |
| 5.1 | Evaluate potential improvements | 03/04/2023 | 30/04/2023 | 28 | 0 | 18 |
| 6 | Writing up of thesis | 03/04/2024 | 01/04/2024 | 0 | 0 | 0 |
| 6.1 | Produce thesis | 03/04/2023 | 01/04/2024 | 0 | 0 | 0 |

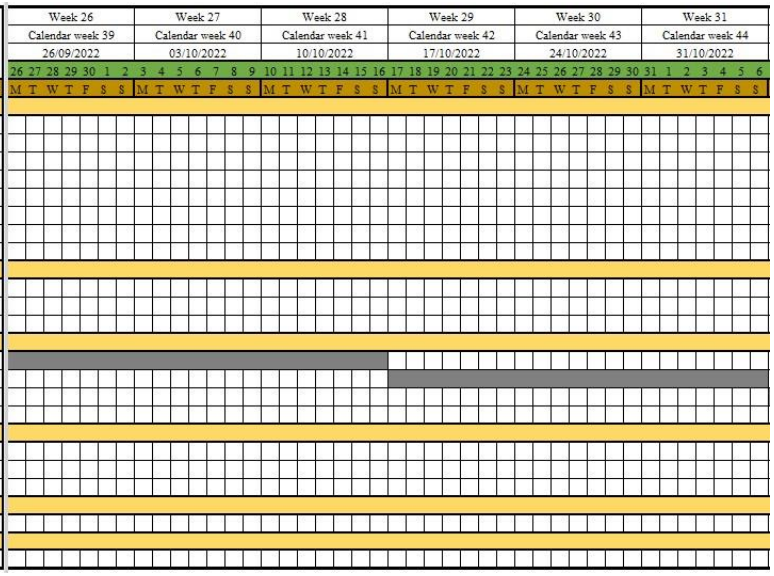


*Chart 5*

| Thesis: - Power MOSFET ESD Analysis and Risk Mitigation | |
|---|---|
| Thesis Start Date: | 04/04/2022 |
| Thesis Author: | Ian. Gilbert. |

| WBS | Task | Start | End | Days | % Done | Work Days |
|---|---|---|---|---|---|---|
| 1 | Research and interim report | 04/04/2022 | 07/08/2022 | 126 | 100 | 85 |
| 1.1 | Design thesis to Nexperia needs | 04/04/2022 | 10/04/2022 | 7 | 100 | 5 |
| 1.2 | Research of MOSFET. | 11/04/2022 | 01/05/2022/ | 21 | 100 | 13 |
| 1.3 | Research of Electrostatic Discharge (ESD) | 02/05/2022 | 22/04/2022 | 21 | 100 | 14 |
| 1.4 | Research of Human Body Models (HBM) | 22/05/2022 | 12/06/2022 | 21 | 100 | 13 |
| 1.5 | Research Risk migration | 13/06/2022 | 03/06/2022 | 21 | 100 | 15 |
| 1.6 | Gantt Chart | 04/07/2022 | 17/07/2022 | 7 | 100 | 5 |
| 1.7 | Risk Assessment | 11/07/2022 | 17/07/2022 | 7 | 100 | 5 |
| 1.8 | Complete Report | 18/07/2022 | 07/08/2022 | 21 | 100 | 15 |
| 2 | Design Stage | 08/08/2022 | 25/08/2022 | 49 | 0 | 34 |
| 2.1 | Design PCB | 08/08/2022 | 28/08/2022 | 21 | 0 | 15 |
| 2.2 | Order components | 29/08/2022 | 11/08/2022 | 14 | 0 | 9 |
| 2.3 | Ask Swansea university to product PCB | 12/08/2022 | 25/08/2022 | 14 | 0 | 10 |
| 3 | Assembly and initial testing | 26/09/2022 | 22/02/2020 | 105 | 0 | 72 |
| 3.1 | Assembly HBM ESD tester | 26/09/2022 | 16/102022 | 21 | 0 | 15 |
| 2.6 | Debug HBM ESD tester | 17/10/2022 | 06/11/2022 | 21 | 0 | 15 |
| 3.2 | Initial testing HBM ESD Tester | 07/11/2022 | 27/11/2022 | 21 | 0 | 15 |
| 3.3 | Evaluate capability HBM ESD Tester | 28/11/2022 | 08/01/2023 | 42 | 0 | 27 |
| 4 | Qualification | 09/01/2023 | 02//04/2023 | 84 | 0 | 60 |
| 4.1 | Reliability Testing | 09/01/2023 | 19/02/2023 | 42 | 0 | 30 |
| 4.3 | Further testing of HBM ESD tester | 20/02/2023 | 26/06/2022 | 35 | 0 | 25 |
| 4.4 | Production Release | 27//03/2023 | 02//04/2023 | 7 | 0 | 5 |
| 5 | Future | 03/04/2023 | 03/04/2023 | 28 | 0 | 18 |
| 5.1 | Evaluate potential improvements | 03/04/2023 | 30/04/2023 | 28 | 0 | 18 |
| 6 | Writing up of thesis | 03/04/2024 | 01/04/2024 | 0 | 0 | 0 |
| 6.1 | Produce thesis | 03/04/2023 | 01/04/2024 | 0 | 0 | 0 |

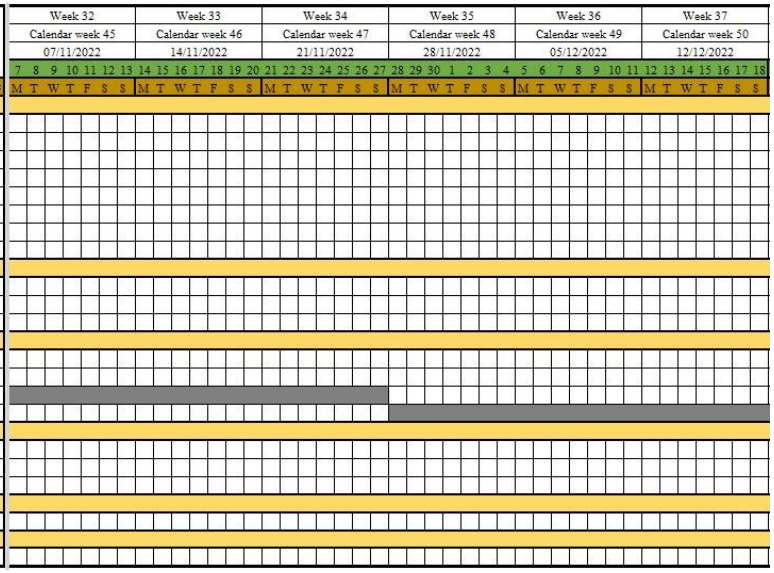


*Chart 6*

| Thesis: - Power MOSFET ESD Analysis and Risk Mitigation | |
|---|---|
| Thesis Start Date: | 04/04/2022 |
| Thesis Author: | Ian. Gilbert. |

| WBS | Task | Start | End | Days | % Done | Work Days |
|---|---|---|---|---|---|---|
| 1 | Research and interim report | 04/04/2022 | 07/08/2022 | 126 | 100 | 85 |
| 1.1 | Design thesis to Nexperia needs | 04/04/2022 | 10/04/2022 | 7 | 100 | 5 |
| 1.2 | Research of MOSFET. | 11/04/2022 | 01/05/2022/ | 21 | 100 | 13 |
| 1.3 | Research of Electrostatic Discharge (ESD) | 02/05/2022 | 22/04/2022 | 21 | 100 | 14 |
| 1.4 | Research of Human Body Models (HBM) | 22/05/2022 | 12/06/2022 | 21 | 100 | 13 |
| 1.5 | Research Risk migration | 13/06/2022 | 03/06/2022 | 21 | 100 | 15 |
| 1.6 | Gantt Chart | 04/07/2022 | 17/07/2022 | 7 | 100 | 5 |
| 1.7 | Risk Assessment | 11/07/2022 | 17/07/2022 | 7 | 100 | 5 |
| 1.8 | Complete Report | 18/07/2022 | 07/08/2022 | 21 | 100 | 15 |
| 2 | Design Stage | 08/08/2022 | 25/08/2022 | 49 | 0 | 34 |
| 2.1 | Design PCB | 08/08/2022 | 28/08/2022 | 21 | 0 | 15 |
| 2.2 | Order components | 29/08/2022 | 11/08/2022 | 14 | 0 | 9 |
| 2.3 | Ask Swansea university to product PCB | 12/08/2022 | 25/08/2022 | 14 | 0 | 10 |
| 3 | Assembly and initial testing | 26/09/2022 | 22/02/2020 | 105 | 0 | 72 |
| 3.1 | Assembly HBM ESD tester | 26/09/2022 | 16/102022 | 21 | 0 | 15 |
| 2.6 | Debug HBM ESD tester | 17/10/2022 | 06/11/2022 | 21 | 0 | 15 |
| 3.2 | Initial testing HBM ESD Tester | 07/11/2022 | 27/11/2022 | 21 | 0 | 15 |
| 3.3 | Evaluate capability HBM ESD Tester | 28/11/2022 | 08/01/2023 | 42 | 0 | 27 |
| 4 | Qualification | 09/01/2023 | 02//04/2023 | 84 | 0 | 60 |
| 4.1 | Reliability Testing | 09/01/2023 | 19/02/2023 | 42 | 0 | 30 |
| 4.3 | Further testing of HBM ESD tester | 20/02/2023 | 26/06/2022 | 35 | 0 | 25 |
| 4.4 | Production Release | 27//03/2023 | 02//04/2023 | 7 | 0 | 5 |
| 5 | Future | 03/04/2023 | 03/04/2023 | 28 | 0 | 18 |
| 5.1 | Evaluate potential improvements | 03/04/2023 | 30/04/2023 | 28 | 0 | 18 |
| 6 | Writing up of thesis | 03/04/2024 | 01/04/2024 | 0 | 0 | 0 |
| 6.1 | Produce thesis | 03/04/2023 | 01/04/2024 | 0 | 0 | 0 |

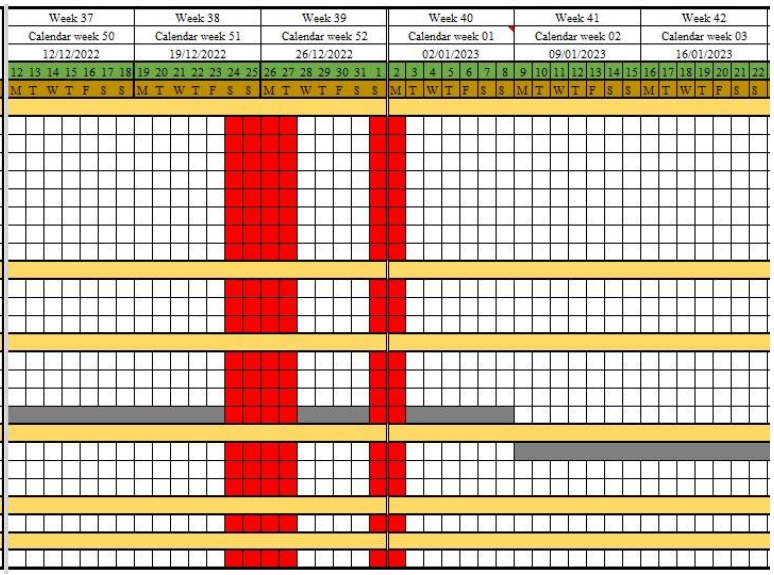


*Chart 7*

# Appendix 3 Thesis Project Cost

| Human Body Model ESD Tester Part list | Part No | Approx Cost | Quantity | Total Cost | Possible source |
|---|---|---|---|---|---|
| Resistor - High Volt Axial Resistor 10W 40KV 1MΩ | RS No 146-9496 | £22.11 | 1 | £22.11 | Supplied by RS |
| Arcol, 1.5kΩ 100W Aluminium Chassis Mount Resistor HS100F 1K5 F ±1% | RS No 186-0120 | £15.00 | 1 | £15.00 | Supplied by RS |
| Capacitor - Radial polyprop cap, 100pF 2KV 15mm | RS No 616-7799 | £0.72 | 1 | £0.72 | Supplied by RS |
| Vero Board-SRSP strip board, 111.76mm x 176.76mm x 1.6mm | RS No 043-4217 | £12.69 | 1 | £12.69 | Supplied by RS |
| Plug - Mueller Electric Red Female Banana Socket - Solder termination 2000 V dc 15A | RS No 888-4594 | £3.41 | 2 | £6.82 | Supplied by RS |
| Plug - Mueller Electric Black Female Banana Socket - Solder termination 2000 V dc 15A | RS No 888-4590 | £3.57 | 2 | £7.14 | Supplied by RS |
| Enclosure-TK Enclosure w/o KO, PC, 180mm x 130mm x 90mm | RS No 881-9776 | £25.54 | 1 | £25.54 | Supplied by RS |
| Switch - Rocker Switch, On / Off, SPST, Illuminated, Panel Mount, Green, R13 | Farnell No 1634664 | £6.43 | 2 | £12.86 | Supplied by Farnell |
| RS PRO Slot Cheese Nylon Machine Screws DIN 84, M3x6mm | RS No 232-6930 | £0.24 | 4 | £0.96 | Supplied by RS |
| RS PRO Nylon Hex Standoff, Male/Female, 10mm, M3 x M3 | RS No 325-0687 | £0.24 | 4 | £0.94 | Supplied by RS |
| EA Elektro-Automatik Bench Power Supply, 3W, 1 output,750V dc, 12A with UKAS calibration | RS No 886-6959 | £2,869.00 | 1 | £2,869.00 | Supplied by Nexperia Newport/ Swansea University |
| Mueller Electric, 20A, 3kV, Red, 1m Lead Length | RS No 888-4005 | £19.28 | 1 | £19.28 | Supplied by Nexperia Newport/ Swansea University |
| Mueller Electric, 20A, 3kV, Black, 1m Lead Length | RS No 888-4001 | £19.32 | 1 | £19.32 | Supplied by Nexperia Newport/ Swansea University |
| Tektronix DP07104 Digital Oscilloscope, 4 channel, 1Ghz, | Discontinued | £3,000.00 | 1 | £3,000.00 | Supplied by Nexperia Newport/ Swansea University |
| Tektronix, THD Series THDP0100cOscilloscope Probe, Differential, High Voltage Type, 1:100, 1:1000 6kV | RS No 752-7353 | £4,632.00 | 2 | £9,264.00 | Supplied by Nexperia Newport/ Swansea University |
| Probe Positioner - MSA 100 3D Probe Positioner | Farnell No 1903978 | £980.44 | 4 | £3,921.76 | Supplied by Nexperia Newport/ Swansea University |
| Total initial budget | | | | £19,198.15 | |
| Total initial budget + 20% precautionary measure | | | | £23,037.77 | |
| Total initial budget minus the total of the parts in red | | | | £104.79 | |
| Total initial budget minus the total of the parts in red + 20% precautionary measure | | | | £125.74 | |