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A family of High Boost Active-Switched Impedance Networks with Low Shoot-Through Current Using Coupled-Inductor

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Abstract — This paper proposes a novel class of impedance source networks based on coupled inductors and an active switch. Due to the turn ratio of the coupled inductors, these networks offer unique features, such as high voltage gain and flexibility in design. The proposed networks effectively reduce the voltage spikes and current stresses, which are common drawbacks of most coupled inductor-based networks. They also offer continuous input current and ultra-high voltage gain, minimizing shoot-through duty cycles (*D*) and resulting in many practical advantages. Reduced current stresses, specifically the shoot-through (*ST*) current, have reduced the total power losses of the elements and the capacity of the passive elements. These features demonstrate the converters' superior efficiency and higher power density. Theoretical performance analysis and comparisons with similar topologies are presented. Finally, experimental tests on a 300W DC-DC converter confirm the theoretical results.

***Index Terms* — impedance network, coupled inductor, active-switched, high gain, shoot-through (*ST*) current, voltage spikes.**

I. Introduction

Voltage source converters are used in various applications, such as renewable energy systems and electric vehicles (EVs). However, they encounter challenges, including input short circuits due to EMI interferences, which reduce reliability. Furthermore, when both buck and boost operations are needed, these converters require multi-stage power conversion, resulting in increased volume, higher cost, and reduced efficiency [1].

Impedance source or Z-source converters were introduced as an appealing solution to overcome the limitations of traditional converters [2]. In Z-source converters, the voltage increase is done in a single stage with high reliability. They do not have the shoot-through problem, and by eliminating the dead time, the quality of the converter's output waveform usually improves. The traditional converters have some limitations, including high voltage and current stresses, high inrush currents, no common ground between the input source and the switching stage, and low voltage gain. In recent years, numerous impedance networks have been presented using different techniques. One of the recent developments in this field is the utilization of coupled inductors and transformers, providing ultra-high voltage gain with a reduced component count. These networks are called magnetically coupled impedance networks (MCINs). The main structures are T-Z-source, Trans-Z-source, Γ-Z-source, Y-source, and Δ-source [3]-[7]. A common drawback of these networks is the presence of leakage inductors, resulting in voltage and current spikes. Cascade networks and snubber circuits are proposed in [8]-[10] to minimize this problem. Another class of impedance networks is active-switched networks. The first active-switched network (SBN) was introduced in [11], incorporating a transistor switch. This leads to a significant reduction in volume and weight and an increase in the converter's power density. To overcome the limitations of the SBN network, the ESBN topology was introduced in [12], fixing issues such as discontinuous input current and non-common ground between the input and the output. However, it still does not have a high voltage gain. By integrating these networks with switched-inductor cells, ASC/SL-ZSN and ASC/SL-QZSN structures are obtained, improving the voltage gain and the converter efficiency [13], [14]. To reduce voltage and current stresses and achieve higher efficiency, the SC-QZSN network was presented in [15], and then the EB-AS-QZSN was proposed in [17]. However, besides the fact that these complex topologies have a large number of elements, in high-voltage applications, the ST duty cycle (*D*) needs to be too high, which is considered a major drawback. The latest advancements combine active-switched impedance networks with MCINs to achieve maximum performance with a minimal number of components. One successful topology is proposed in [16], which effectively limits the leakage inductor's effects. Due to the use of an active switch, it has a small volume and weight, enhancing efficiency and power density. However, the three-winding coupled inductor can have a complex design and construction. Also, the DC-link voltage of this converter fluctuates between two different levels, which is a disadvantage.

This paper presents a class of impedance source networks based on coupled inductors and an active switch. The proposed networks offer an ultra-high voltage gain with a small *D*. This directly translates to reduced voltage and current stresses. Furthermore, the effects of the leakage inductor have been effectively reduced. This leads to decreased power losses, increased efficiency, and higher power density. Theoretical analysis and operating principles of the proposed networks are provided in Section II. Section III details the design considerations. In Section IV, various comparisons between the topologies and counterparts are conducted. The experimental

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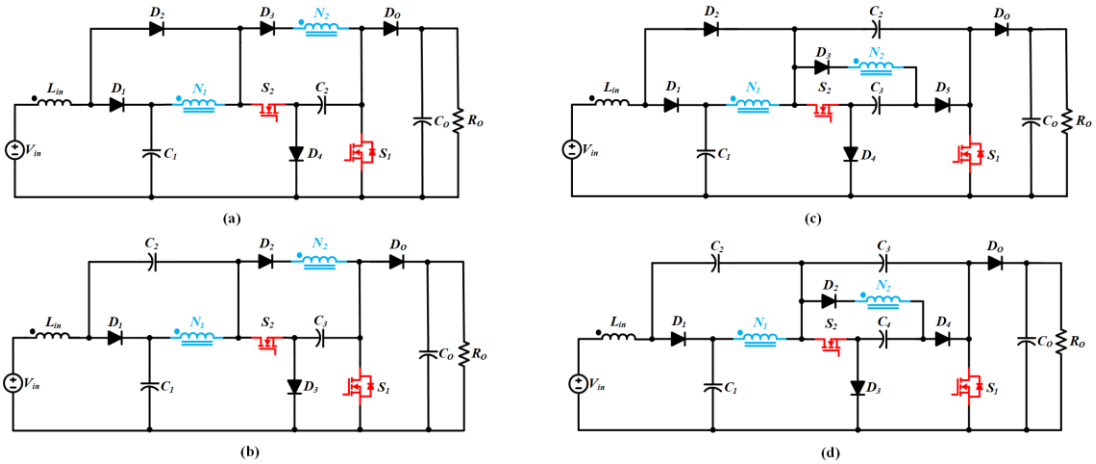

Fig. 1. Proposed Impedance Networks: (a) Type I, (b) Type II, (c) Type III, and (d) Type IV.

verification on a DC-DC prototype converter is presented in Section V. It should be noted that there is no limitation on the application of the proposed networks beyond a simple DC-DC converter.

II. Proposed Impedance Networks

All of the proposed impedance networks have a two-winding coupled inductor and two transistor switches and are grouped into four types, as shown in Fig. 1. Type I topology has an input inductor, two capacitors, and four diodes. Type II is obtained by replacing diode D_2 with a capacitor in Type I. Type III is acquired by adding a diode and capacitor to Type I. Finally, Type VI is obtained by replacing diode D_2 in Type III with a capacitor. The coupled inductor employed in the topologies is modeled by an ideal transformer with magnetizing inductance (L_M) transferred to the primary side. Leakage inductors are assumed small and ignored in modeling and calculations.

A. Performance Analysis

Similar to all Z-source converters, the proposed topologies have two operating modes: shoot-through (ST) and non-shoot-through (NST) states. The equivalent circuit of the proposed topologies in ST and NST modes is shown in Fig. 2. For simplicity, the output diode and the load are considered as a current source in parallel with the switch S_1.

1) *Proposed Network (Type I)*

a) ST state:

Fig. 2(a). shows the ST state equivalent circuit of topology Type I. In this state, switches S_1 and S_2 are on simultaneously. Diodes D_1, D_3, and D_4 are reverse-biased and block, and diode D_2 is forward-biased and conducts. Therefore, the coupled inductors are charged by capacitors C_1 and C_2. The voltage equations are:

$$\begin{cases} V_{Lin}^{ST} = V_{in} + V_{C2} \\ V_{N1}^{ST} = V_{C1} + V_{C2} \end{cases} \tag{1}$$

b) NST state:

During this state, switches S_1 and S_2 are turned off, diodes D_1, D_3 and D_4 conduct, while diode D_2 blocks, shown in Fig. 2(b). In this state, capacitor C_1 charges through D_1. The voltage equations are:

$$\begin{cases} V_{Lin}^{NST} = V_{in} - V_{C1} \\ V_{N1}^{NST} + V_{N2}^{NST} = V_{C1} - V_{C2} \end{cases} \tag{2}$$

The output voltage of Type I is obtained by applying the volt-second balance on the windings N_1 and L_{in}, where D is the ST duty cycle.

$$G = \frac{V_{out}}{V_{in}} = \frac{1+ND}{1-(2(2-D)+N)D} \tag{3}$$

2) *Proposed Network (Type II)*

a) ST state:

According to the equivalent circuit, as depicted in Fig. 2(c), both switches are on, and diodes D_1 to D_3 are reverse-biased. In this state, L_{in} and L_M are charged by the capacitors and the input source. The voltage equations can be written as follows:

$$\begin{cases} V_{Lin}^{ST} = V_{in} + V_{C2} + V_{C3} \\ V_{N1}^{ST} = V_{C1} + V_{C3} \end{cases} \tag{4}$$

b) NST state:

Referring to Fig. 2(d), both switches are off while the diodes are forward-biased and conduct, and capacitor C_1 charges through D_1. Equations can be expressed as:

$$\begin{cases} V_{Lin}^{NST} = V_{in} + V_{C1} \\ V_{N1}^{NST} = -V_{C2} \\ V_{N2}^{NST} = V_{C1} + V_{C2} - V_{C3} \end{cases} \tag{5}$$

Type II voltage gain can be then concluded as:

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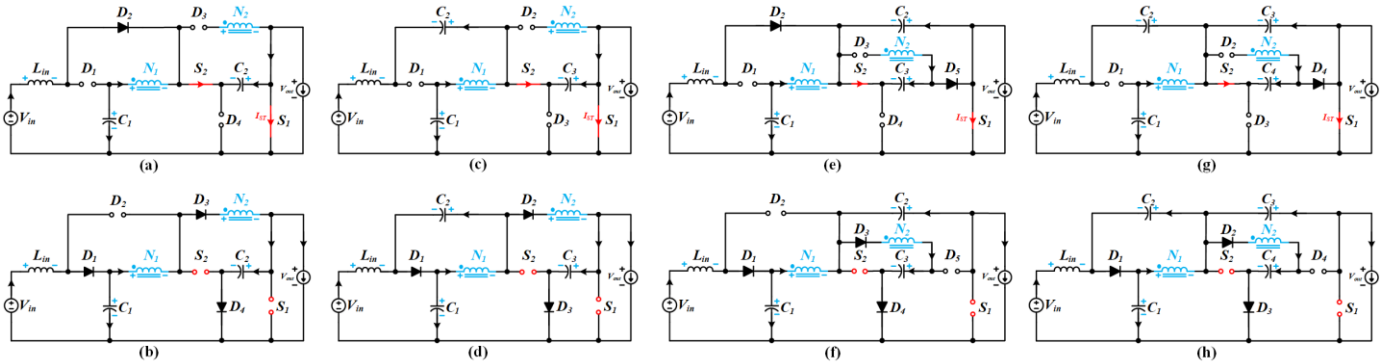

Fig. 2. Operating Sates: (a) ST and (b) NST of Type I, (c) ST and (d) NST of Type II, (e) ST and (f) NST of Type III, and (g) ST and (h) NST of Type IV.

$$G=\frac{V_{out}}{V_{in}}=\frac{1+ND}{1-(4+N)D} \tag{6}$$

3) *Proposed Network (Type III)*

a) ST State:

The operation of this converter, illustrated in Fig. 2(e), is similar to the previous topologies. By applying the KVL to the equivalent circuit, one gets:

$$\begin{cases} V_{Lin}^{ST}=V_{in}+V_{C2} \\ V_{N1}^{ST}=V_{C1}+V_{C2} \end{cases} \tag{7}$$

b) NST State:

This state is indicated in Fig. 2(f), Readily, one can write:

$$\begin{cases} V_{Lin}^{NST}=V_{in}-V_{C1} \\ V_{N1}^{NST}+V_{N2}^{NST}=V_{C1}-V_{C2} \end{cases} \tag{8}$$

Similar to the previous topologies, by considering equations (7), and (8), and using the volt-second balance for inductors, the output voltage is :

$$G=\frac{V_{out}}{V_{in}}=\frac{2}{1-(2(2-D)+N)D} \tag{9}$$

4) *Proposed Network (Type IV)*

The equivalent circuits of Type IV ST and NST states are presented in Fig. 2(g) and (h). Using the same method as the previous converters, the output voltage of the converter can be easily calculated:

$$G=\frac{V_{out}}{V_{in}}=\frac{2}{1-(4+N)D} \tag{10}$$

The voltage gain curves are then plotted in Fig. 3(a). All the proposed converters exhibit ultra-high voltage gains in different turn ratios. It can be observed that a higher turn ratio (N) leads to an increase in the gain. In Fig. 3(b), the gains of the proposed networks are compared with other successful networks. Even with a unity turn ratio, the proposed class has higher voltage gain than most topologies. The EGS-ZSN network has the highest voltage gain compared to other networks. However, at higher values of D, its gain is lower than Types III and IV. Increasing the turn ratio significantly improves the proposed network's gain compared to others. Therefore, if the proposed networks are implemented in the DC-AC application at the same voltage gain as other topologies, they can use a higher modulation index (M), reducing the distortion of the output waveform of the converter. The parameter K represents the turn ratios of the coupled inductors, which is given in Table I for all topologies.

III. Component Parameters Design

Generally, the size, cost, and power losses of ZSNs are mainly determined by the reactive elements, including input inductors, magnetizing inductors, and capacitors, which need to be designed carefully.

A. *Input inductor*

The input inductors' current of the proposed networks is continuous. L_{in} can be defined in terms of the current ripple as:

$$L_{in}=\frac{V_{Lin}^{ST}DT}{\Delta I_{in}} \tag{11}$$

Where ΔI_{in} is the input current ripple, V_{Lin} is the voltage across L_{in} during the ST state, and T is the switching period. Therefore, the input inductor can be optimally designed by considering ΔI_{in} as ($\alpha\%$) of the input current, which gives:

$$\begin{cases} L_{in}^{I,III}=L_{in}^{Base}\times\dfrac{2D(1-D(2-D))}{1-(2(2-D)+N)D} \\ L_{in}^{II,IV}=L_{in}^{Base}\times\dfrac{2D(1-D)}{1-(4+N)D} \\ L_{in}^{Base}=\dfrac{V_{in}^{2}T}{\alpha\%P_{O}} \end{cases} \tag{12}$$

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TABLE I
VOLTAGE AND CURRENT STRESSES

Converter	Prop. Type I	Prop. Type II	Prop. Type III	Prop. Type IV
K	$N=N_2/N_1$	$N=N_2/N_1$	$N=N_2/N_1$	$N=N_2/N_1$
δ	2(2-D)+N	4+N	2(2-D)+N	4+N
B	1+KD/(1-(2(2-D)+K)D	1+KD/(1-(4+K)D)	2/(1-(2(2-D)+K)D	2 /(1-(4+K)D
V_{C1}/V_{in}	B(1-D(2+N))/(1+ND)	B(1-D(2+N))/(1+ND)	B(1-D(2+N))/2	B(1-D(2+N))/2
V_{C2}/V_{in}	B	2BD/(1+ND)	B(1+ND)/2	BD
V_{C3}/V_{in}	NA	B	B(1+ND)/2	B(1+ND)/2
V_{C4}/V_{in}	NA	NA	NA	B(1+ND)/2
I_m/I_{in}	(B(3-2D)+1)/2B	(3B+1)/2B	(N+2(1-D))/2	(N+2)/2
I_{D1}/I_{in}	1	1 /(1-D)	1	1 /(1-D)
I_{D2}/I_{in}	1	(B+1)/(2B(1-D))	1	1 /2(1-D)
I_{D3}/I_{in}	(B+1)/(2B(1-D))	(B-1)/(2B(1-D))	1 /2(1-D)	1 /2(1-D)
I_{D4}/I_{in}	(B-1)/(2B(1-D))	NA	1 /2(1-D)	1/2D
I_{D5}/I_{in}	NA	NA	1/2D	NA
I_{S1}/I_{in}	(B-1)/(2BD)	(B-1)/(2BD)	(B-2)/(2BD)	(B-2)/(2BD)
I_{S2}/I_{in}	(B-1)/(2BD)	(B-1)/(2BD)	1/2D	1/2D
V_{D1}^{BR}/V_{in}	2B(1-D)/(1+ND)	2B/(1+ND)	B(1-D)	B
V_{D2}^{BR}/V_{in}	2BD/(1+ND)	B(1+N(2-D)) /(1+ND)	BD	B(1+N(2-D))/2
V_{D3}^{BR}/V_{in}	B(1+N(2-D))/(1+ND)	B	B(1+N(2-D))/2	B(1+ND) /2
V_{D4}^{BR}/V_{in}	B	NA	B	B(1-ND) /2
V_{D5}^{BR}/V_{in}	NA	NA	B(1-ND) /2	NA
V_{S2}^{BR}/V_{in}	B(1-ND) /(1+ND)	B(1-ND) /(1+ND)	B(1-ND) /2	B(1-ND) /2
Converter	**SDL-YSN [16]**	**HS-YSN [8]**	**LH-YSN [9]**	**LCD-QYSN [10]**
K	$(N_1+N_3)/(N_2-N_3)$	$(N_1+N_3)/(N_3-N_2)$	$(N_1+N_3)/(N_3-N_2)$	$(N_1+N_3)/(N_2-N_3)$
δ	2(K+1)	K+2	K+1	K+1
B	1/(1-(2(K+1))D)	1/(1-(K+2)D)	1/(1-(K+1)D)	1/(1-(K+1)D)
I_m/I_{in}	0	$(N_1+N_3)/N_1$	$(N_1+N_3)/N_1$	0
I_{LO}/I_{in}	NA	1	NA	$(BD^2)/(L_o f_{sw} I_{in})$
I_{D1}/I_{in}	(D+K(1+D))/K(1-D)	(K+1)/K(1-D)	K/(K-1)(1-D)	1 /(1-D)
I_{D2}/I_{in}	(D+K(1+D))/(1-D)	(K+1)/(1-D)	K/(1-D)	$(K/(1-D))+ ((BD^2)/(L_o f_{sw} I_{in}))$
I_{D3}/I_{in}	K+1	NA	NA	$(BD^2)/(L_o f_{sw} I_{in})$
I_{S1}/I_{in}	K+1	K+2	K+1	K+1
I_{S2}/I_{in}	K+1	NA	NA	NA
V_{D1}^{BR}/V_{in}	2KB	KB	(K-1)B	KB
V_{D2}^{BR}/V_{in}	B	B	B	B
V_{D3}^{BR}/V_{in}	B	NA	NA	B(1-D)
V_{S2}^{BR}/V_{in}	B	NA	NA	NA

Where P_o is the output power. The energy stored in the input inductor and the peak current can be calculated from (13) and (14), respectively.

$$W_{Lin} = 0.5 \times L_{in} \left(I_{in}^{\max} \right)^2 \tag{13}$$

$$I_{in}^{M\,ax} = \left(1 + \frac{\alpha\%}{2} \right) \times I_{in} \tag{14}$$

B. Magnetizing Inductor

Similar to L_{in}, the magnetizing inductors can be optimally designed from the tolerable magnetizing current ripple (ΔI_M):

$$L_m = \frac{V_{Lm}^{ST} DT}{\Delta I_M} \tag{15}$$

In Equation (15), V_{Lm}^{ST} is the voltage across the windings N_1 during the ST state. ΔI_M can be assumed to be ($\beta\%$) of the magnetizing current. Eventually, one can conclude:

$$\begin{cases} L_m^{I,III} = L_m^{Base} \times \dfrac{2D(1-D)}{1-(2(2-D)+N)D} \\ L_m^{II,IV} = L_m^{Base} \times \dfrac{2D(1-D)}{1-(4+N)D} \\ L_m^{Base} = \dfrac{V_{in} T}{\Delta I_M} \\ W_{Lm} = 0.5 \times L_m \left(I_m^{\max} \right)^2 \end{cases} \tag{16}$$

C. Capacitors

For the proper selection of the capacitors, their maximum voltage ripple and the current through it should be considered. Therefore:

$$C = \frac{I_C^{ST} DT}{\Delta V_C} \tag{17}$$

Assuming ΔV_C as ($\gamma\%$) of the capacitor voltage or maximum tolerable voltage ripple for capacitors, the capacitors for the proposed networks are derived as follows:

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$$\begin{cases} C_1^I = \dfrac{D(1-D)(1+N)}{B(1-(2+N)D)} \times C_{Base}, C_2^I = \dfrac{D(2+N-D)}{B(1+ND)} \times C_{Base} \\ C_1^{II} = \dfrac{D(1+N(1-D))}{B(1-(2+N)D)} \times C_{Base}, C_2^{II} = \dfrac{1+ND}{2B} \times C_{Base}, \\ C_3^{II} = \dfrac{D(2+N)}{B(1+ND)} \times C_{Base} \\ C_1^{III} = \dfrac{D(2(1-D)+N)}{B(1-(2+N)D)} \times C_{Base}, C_2^{III} = \dfrac{B}{2} \times C_3^{III} = \dfrac{2}{B^2(1+ND)} \times C_{Base} \\ C_1^{IV} = \dfrac{D(2+N)}{B(1-(2+N)D)} \times C_{Base}, C_2^{IV} = \dfrac{1}{B} \times C_{Base}, \\ C_3^{IV} = \dfrac{B}{2} \times C_4^{IV} = \dfrac{2}{B^2(1+ND)} \times C_{Base} \\ C_{Base} = \dfrac{P_O T}{\gamma \% V_{in}^2} \end{cases} \quad (18)$$

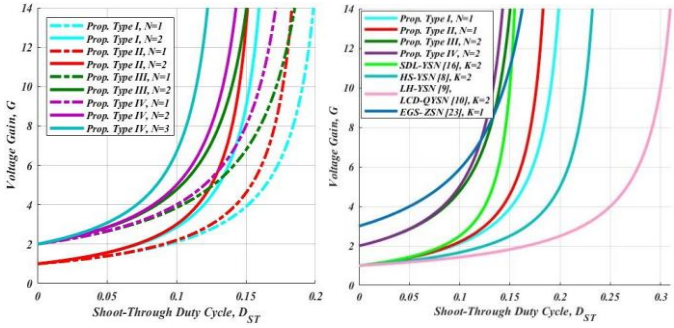
IV. Comparison

In this section, the proposed networks are compared with each other and other counterparts in various aspects.

A. Comparison between proposed networks

Each of the proposed converters exhibits distinct features. They are compared from different aspects and the results are summarized in Fig. 4. Types III and IV are superior to Types I and II in some major indicators such as voltage gain, power density, etc. However, Types I and II also offer advantages, such as low semiconductor current stress, fewer components, and higher efficiency.

B. Comparison with other networks



(a) (b)

Fig. 3. Comparison of (a) voltage gains of the proposed ZSNs, (b) and the competitors

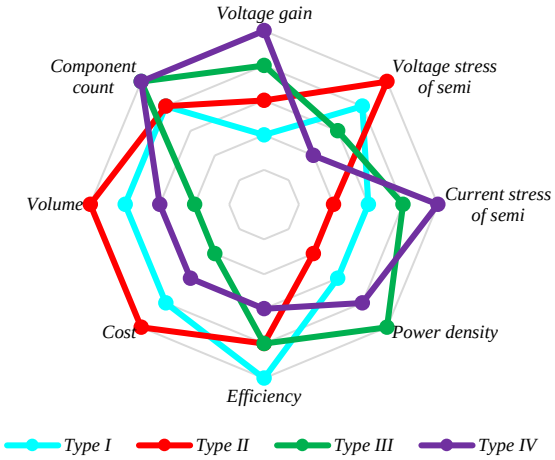


Fig. 4. Comparison of proposed networks.

The proposed networks are compared with recent counterparts. The following subsections present results and discussions, including the shoot-through current, the maximum

TABLE II
NUMERICAL DESIGN OF THE INDUCTORS FOR ALL NETWORKS

Network	Inductors	Part num.	Turn ratio	Volume and weight				K_u (%)	MLT (mm)
				mm^3		gr			
				Core	Win.	Core	Win.		
Type I	L_{IN}	77616	164	51800	23760	340	183	27	94
	L_M	77439	41:41	21300	7400	130	57	21.7	67
Type II	L_{IN}	77616	192	51800	28090	340	216	31.5	95
	L_M	77439	43:43	21300	9720	130	71	26	70
Type III	L_{IN}	77192	122	28600	13903	180	107	30.7	74
	L_M	77083	35:35	10600	5090	65	50	18.8	54
Type IV	L_{IN}	77192	121	28600	13790	180	106	30.5	74
	L_M	77083	34:34	10600	4950	65	38	18	54
SDL-YSN [16]	L_{IN}	77735	397	91400	72750	570	565	33.2	120
	L_M	77083	55:83:28	10600	20740	65	160	61	67
HS-YSN [8]	L_{IN}	77212	243	20700	24700	130	190	33.2	66
	L_M	77192	32:32:64	28600	23176	180	182	38	77
	L_O	77212	246	20700	25000	130	193	33.6	66
LH-YSN [9]	L_{IN}	77212	245	20700	24900	130	192	33.5	66
	L_M	77192	46:23:46	28600	29400	130	225	57.8	83
LCD-YSN [10]	L_{IN}	77735	390	91400	71471	570	550	32.6	119
	L_M	77083	63:42:21	10600	21125	65	163	62	67
EGS-ZSN [23]	L_{IN}	77192	90	28600	15130	180	117	33	75
	L_M	77934	18:18:18	4150	2846	26	22	34.8	44

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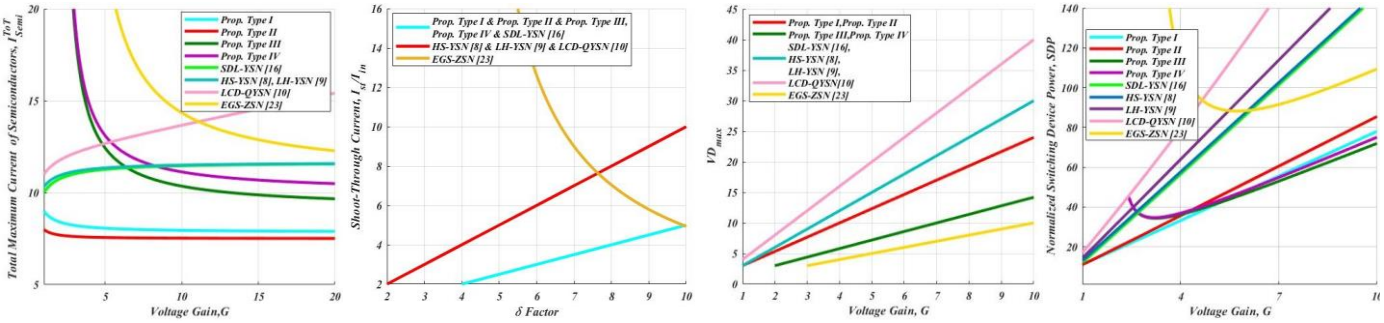
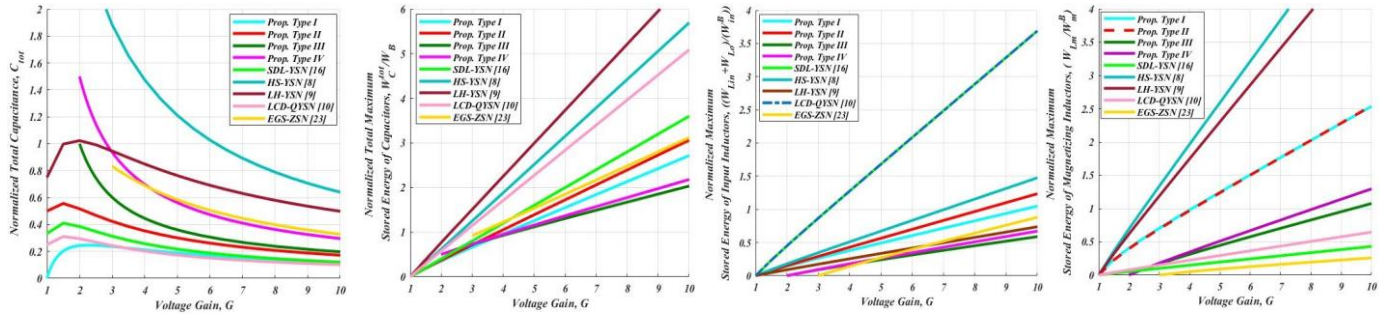


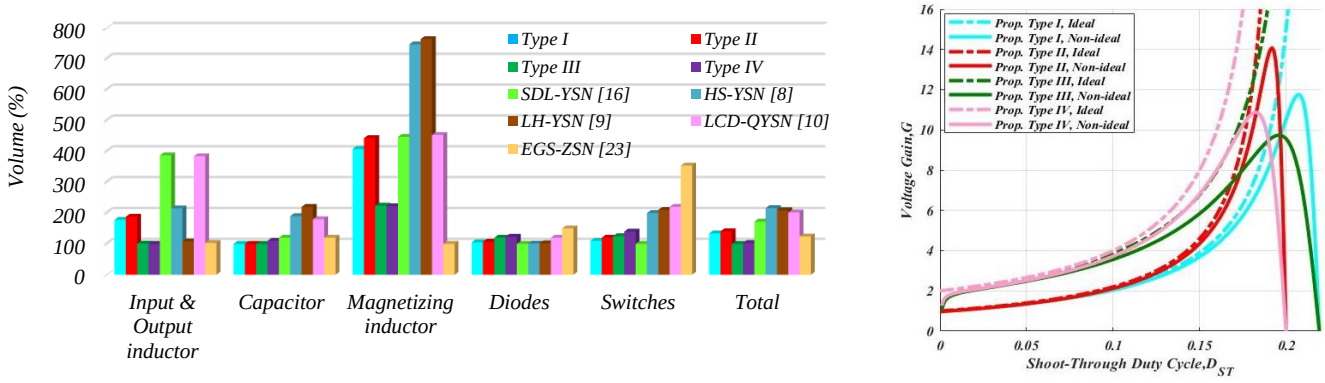
(a) (b) (c) (d)

Fig. 5. Normalized (a) total maximum current of semiconductors, (b) shoot-through (*ST*) currents, (c) VD_{MAX} for δ=5, and (d) SDP_{MAX}.



(a) (b) (c) (d)

Fig. 6. Normalized (a) total capacitance, (b) total maximum stored energy of the capacitors, (c) total maximum stored energy of the input & output inductors, and (d) magnetizing inductors.



(a) (b)

Fig. 7. (a) Comparison of volume among the proposed and competitor networks, (b) practical voltage gains.

voltage stress of semiconductors, the maximum switching device power, the stored energy of capacitors, and the stored energy of inductors. Table I summarizes the voltage and current expressions for the networks. A parameter called δ, as already defined in [16], is utilized to assess the topologies. To ensure a fair comparison, all the converters are assumed to operate in similar conditions. So, the output power, input voltage, and voltage gain (δ=5) are assumed to be the same for all.

1) *Semiconductors*

a) Total current stress of semiconductors

In most impedance networks, the elements experience high current stress, which is a significant drawback. The total maximum current stress of active devices is depicted in Fig. 5(a). As can be seen, this parameter for the proposed networks, especially Types I and II, is significantly lower than their counterparts. As the voltage gain increases, the superiority of the proposed networks becomes more evident. Among the studied ZSNs, the current stresses of the EGS-ZSN network are the highest.

b) Shoot-Through Current

One concern among all Z-source converters is the ST current that flows through the output switches. The proposed networks offer the advantage of a low ST current. The normalized ST current of the networks is compared versus δ, as shown in Fig. 5(b). The ST current of the proposed networks and SDL-YSN is significantly lower than the others. In this comparison, the ST current of the EGS-ZSN network is significantly larger than that of its competitors, particularly at a small δ. If the ST current assumed the same, in an equal voltage gain, δ is derived much larger than counterparts, resulting in a significant reduction of *D*. These features can be also translated as lower voltage stresses and improved output waveform quality.

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c) Maximum Voltage of Semiconductors

In active networks, the main parameters determining the power losses are the voltage and current stresses, summarized in Table I. In most ZSNs, the maximum voltage stress among semiconductors happens across D_1. However, in the proposed ZSNs, the maximum voltage drops across the series diode with winding N_2. In Fig. 5(c), the maximum voltage stress among the semiconductors (VD_{max}) in $\delta=5$ is plotted versus voltage gain, showing that VD_{max} of the EGS-ZSN network is the lowest, followed by Type IV, Type III, Type II, and Type I, respectively. In this comparison, the proposed networks have a fair value.

d) Maximum Switching Device Power

The maximum switching device power, abbreviated as SDP_{Max}, is introduced in [1]. It is a fair index for evaluating the ratings of the converter's semiconductors:

$$SDP_{MAX} = \sum_{i=1}^{n} V_i^{peak} I_i^{peak} \tag{19}$$

where V_i^{peak} and I_i^{peak} are the peak voltage and peak current of the semiconductor elements, respectively. This index is calculated for all the converters and plotted in Fig. 5(d). These plots confirm that the normalized SDP_{Max} of the proposed networks, especially Types III and IV, is lower than that of others. Although EGS-ZSN components have low voltage stresses, its high current stresses result in a higher SDP_{Max} than its counterparts. So, even though the number of semiconductors in the proposed circuits is high, their overall voltage and current requirements are low. Therefore, semiconductors with a lower rating can be used at equal voltage gains, which reduces the overall cost and power losses of the switching devices.

2) *Reactive Elements*

a) Capacitors

According to [18], the volume of capacitors is directly related to their maximum stored energy. Using the energy relation ($W_C=0.5\times C\times(V_{max})^2$), the maximum stored energy of capacitors for the proposed converters and competitors can be calculated. Assuming the voltage ripple is the same for all converters, the capacity and maximum normalized stored energy of the capacitors are plotted in Fig. 6(a) and (b), respectively. The normalized total capacitance of Type I, LCD-QZSN, and SDL-YSN is the lowest, while for the HS-YSN is the highest. The other proposed networks exhibit fair values compared to competitors. Regarding Fig. 6(b), the capacitors' volume of the proposed networks is the smallest.

b) Inductors

Magnetic elements are one of the parameters that determine the power density and volume of the converter. Based on [18], the maximum energy stored in inductors $(L(I_{L,Max})^2)$ is an important parameter for selecting the magnetic core. The proposed converters and the SDL-YSN use two magnetic components, while the other converters use three, which is an advantage for the proposed networks.

The normalized maximum energy stored in inductors is calculated for all under-study ZSNs, and results are plotted in Fig. 6(c) and (d). It is important to note that for a fair comparison, the current ripple of the magnetic elements is assumed to be the same for all networks. From Fig. 6(c), the input inductor of Types III and IV has the lowest maximum stored energy. From Fig. 6(d), the networks can be ranked in order of the maximum energy of their magnetizing inductor, from lowest to highest: EGS-ZSN, SDL-YSN, LCD-QYSN, Type III, Type IV, and other networks.

For a better comparison with actual parameters, i.e. core size and winding turn numbers, the values of maximum stored energy of the inductors are calculated for the under-study ZSNs. As mentioned before, this parameter is then used to select the minimum core size to avoid core saturation. For a fair comparison of the core volume, winding, etc., all magnetic elements are designed using Magnetics® toroid cores, and the required index values are calculated according to the method detailed in [24]. In this comparison, ΔI_M is assumed to be the same for all networks. The numerical design results are summarized in Table II. As expected, the volume of L_{IN} for SDL-YSN and LCD-QYSN is the largest, while it is the smallest in Types III and IV. In the case of L_M, the maximum energy stored for the SDL-YSN and LCD-QYSN is the lowest due to zero magnetization current. However, having three windings with a high flowing current lead to a larger size of the coupled inductor compared to the proposed networks. In other words, the volume of the coupled inductor is the lowest for EGS-ZSN, followed by the proposed networks. It should be noted that the HS-YSN and LH-YSN not only require larger maximum stored energy but also have a high coupled inductor volume compared to the competitors due to the use of three windings with high current stresses.

3) *Power density and non-ideal voltage gain*

a) Power density

Power density depends on several parameters, such as the volume of inductors, maximum energy of capacitors, and power loss of semiconductors as an indicator of their cooling system. They have been normalized to the minimum value in each case for easier comparison. Referring to Fig. 7(a), it can be seen that the proposed networks outperform competitors in terms of the volume of capacitors and power switches. Among the proposed networks, Type III and HS-YSN have the smallest and largest overall volumes, respectively. Compared to others, the other proposed networks are also relatively small in size. The EGS-ZSN inductor volume is smaller than all networks, while in terms of other indicators, especially the volume of active elements, it is larger than other converters. The high volume of magnetic elements of SDL-YSN, HS-YSN, LH-YSN, and LCD-QYSN is one of the main reasons for their lower power density than the proposed networks. In addition, all the proposed networks are superior to competitors in terms of the required cooling system.

b) Non-ideal voltage gain

The proposed networks can ideally change the output voltage from zero to infinity, while it is limited when the parasitic

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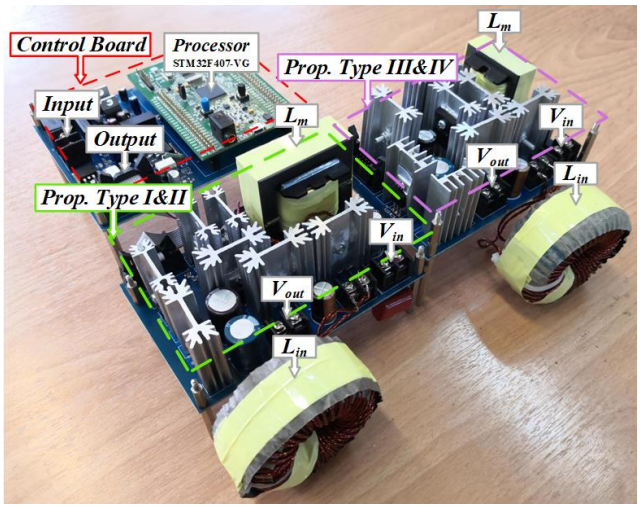
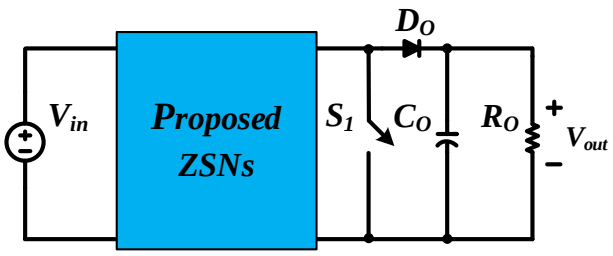
elements are considered. These parasitic elements include the equivalent series resistance (ESR) of the inductors and the capacitors, forward voltages of diodes, and the resistance of the diodes and MOSFETs. The non-ideal voltage gain of the proposed networks is obtained according to the method presented in [20]. For a more detailed analysis, the voltage gain curves of the proposed networks versus D under ideal and non-ideal conditions are compared in Fig. 7(b). When D increases beyond a practical threshold, the converters become unstable and the gain starts to fall suddenly, which is expected behavior for all boost converters.

TABLE III
SYSTEM PARAMETERS

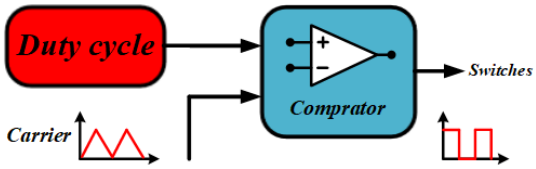
Parameters		Values
Output power, P_O		300W
Output voltage, V_O		200VDC
Input voltage, V_{in}		50VDC
Switching frequency, f_{sw}		40kHz
L_{in}	Type I, II	1800µH & 180mΩ
	Type III, IV	900µH & 140mΩ
L_m	Type I, II	250µH (60:80mΩ), (N=1)
	Type III, IV	140µH (50:70mΩ), (N=1)
Magnetic cores of L_m		EE55/28/21, EE42/21/20
Capacitors	C_1, C_2, C_3, C_4	47μF, 63μF,100μF,160μF & 40$m\Omega$
MOSFET	S_1 & S_2	IPP410N30N, IXFH/IXFT58N20
Diodes	$D_1 \sim D_5$	IDW30G65C5, MSC030SDA070K VS-60APU02, RF1501TF3SFH, TST30L100CW



(a)



(b)



(c)

Fig. 8. (a) Photo of the experimental setup, (b) DC-DC ZSN configuration, and (c) PWM generation of gating signals.

V. EXPERIMENTAL RESULTS

An experimental DC-DC converter test rig is developed using the proposed ZSNs, shown in Fig. 8(a). The parameters are summarized in Table III. The gate signals are generated by an STM32F407-VG microcontroller. As shown in Fig. 8(c), a simple PWM signal is generated for the switches by comparing the duty cycle signal with a triangular carrier waveform. The coupled inductors are wound on an EE ferrite core with very low core losses. Also, multi-strand Litz wire is employed for the magnetizing inductor, which is also wound in a bi-filar method to reduce the leakages [19]. For the input inductors, a toroidal magnetic core with the KoolMµ® material from Magnetics® is selected, whose windings are constructed with multi-strand Litz wires. To achieve the desired voltage gain of $G=4$, the value of D for Types I to IV is 0.152, 0.144, 0.107, and 0.10, respectively. Fig. 9-12 show the experimental waveforms of the converters. Based on the relations in the previous sections, the calculated and measured values for the output voltage, capacitor voltage, input current, and magnetizing current are compared in Table III, which closely match. A practical voltage gain slightly lower than the ideal value is due to two main reasons, which have been investigated in [20]. Passive components have parasitic resistance, and the semiconductors are not ideal. Fig. 9-12. (a) show the input and output voltages and currents. As expected, the output voltage is slightly smaller than the nominal value and is between 192V to 194V, instead of 200V. Moreover, the input currents are continuous, making them suitable for renewable energy applications. The voltages of the capacitors are shown in Fig. 9-12 (b). The ripples are less than 2%, complying with the design expectations. Focusing on Type I, the internal voltages are reported in Fig. 9(b) and (c). As already expected, the voltage stresses are in agreement with the theoretical values. These figures show that in the ST state, the switches are on, and diode D_2 conducts, while diodes D_1, D_3, and D_4 are reverse-biased. On the contrary, in the NST mode, the semiconductors' status is completely reversed, which means switches are turned off, and D_2 blocks, whereas D_1, D_3, and D_4 are forward-biased. For Type II, as shown in Fig. 10(c) and (d), both switches conduct in the ST state, and the diodes are reverse-biased. In the NST state, the diodes conduct, and the switches are turned off. Types III and IV, as shown in Fig. 11-12 (b), (c), and (d), respectively, Operate similarly to Types I and II. In all networks, the parasitic capacitors and leakage inductance of the coupled inductor have the potential to resonate, resulting in ringing across the diode in series with the winding N_2. Although, it can be effectively mitigated by a small snubber [7]. In all the proposed networks, DC-link voltage spikes are effectively limited, which can reduce switching losses and

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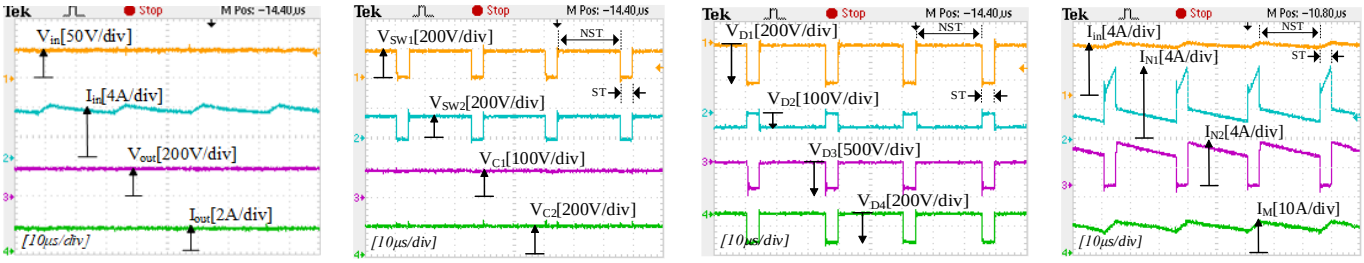

Fig. 9. Experimental waveforms of Type I proposed network (a) input and output voltages and currents, (b) voltages across switches SW_1 and SW_2 and capacitors, (c) voltages across diodes, and (d) input, and coupled inductor currents.

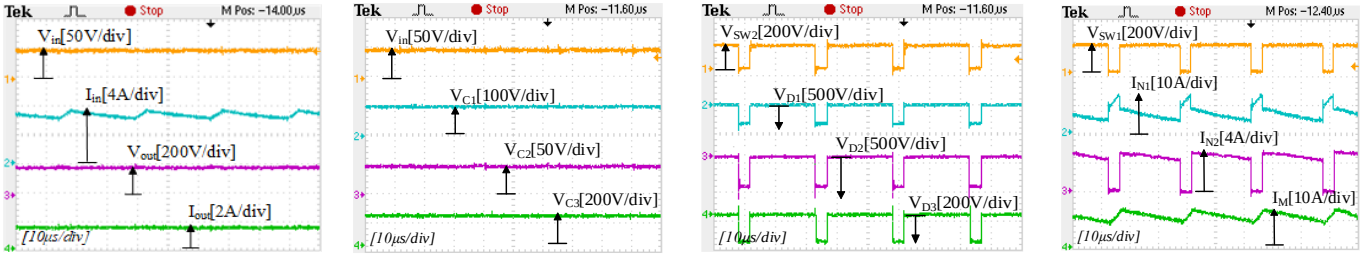

Fig. 10. Experimental waveforms of Type II proposed network (a) input and output voltages and currents, (b) input and capacitors voltages, (c) voltages across switches SW_1 and diodes, and (d) voltage across switch SW_2, coupled inductor currents.

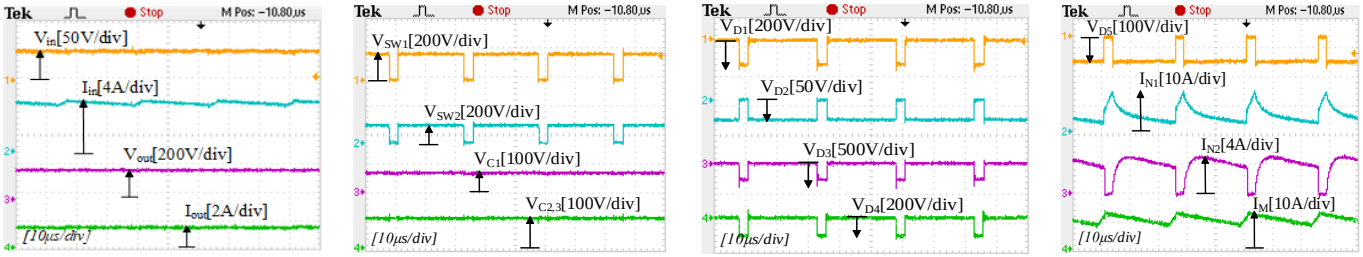

Fig. 11. Experimental waveforms of Type III proposed network (a) input and output voltages and currents, (b) voltages across switch SW_1 and SW_2 and capacitors, (c) voltages across diodes, and (d) voltages across D_5, coupled inductor currents.

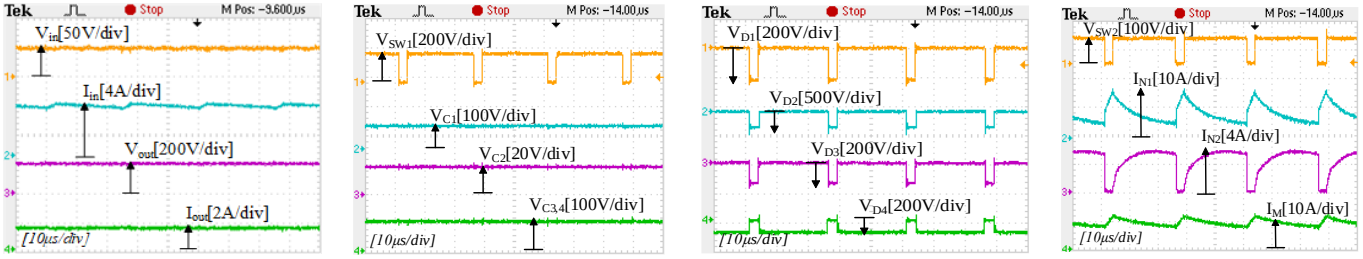

Fig. 12. Experimental waveforms of Type IV proposed network (a) input and output voltages and currents, (b) voltages across switch SW_1 and capacitors, (c) voltages across diodes, and (d) voltage across SW_2, and coupled inductor currents.

increase power density. To confirm the relations of the Magnetizing current (I_M) of the converters, the current waveforms of the windings and I_M at the primary side are measured and given in Fig. 9-12 (d). It is important to mention that to obtain the magnetizing current in practice, the equation $N_1I_M=N_1I_1+N_2I_2$ is used. Considering that the turn ratio is unity, this equation simplifies to $I_M=I_1+I_2$. According to Table IV, the measured values of I_M are in good agreement with the theory. In addition, to demonstrate the potential merits of the proposed networks, some experimental tests were carried out at the voltage gain of G=8. Referring to Fig. 13-16, it can be seen that the proposed networks maintain their superior performance even at high voltage gain. At a voltage gain of G=8, the spikes in the circuit are still effectively limited. Based on these experimental waveforms, it can be concluded that the proposed networks can be utilized without any limitations in applications requiring high voltage gain. Finally, a comparative analysis is performed in terms of efficiency. All under-study ZSNs are simulated in PSIM. In this simulation, thermal model of the active elements, the ESR of the passive components, and the leakage inductance of the coupled inductors are considered. For the sake of fairness, the passive components are designed with the same current and voltage ripples for the inductors and the capacitors, respectively. The semiconductors reported in Table III are used similarly for all converters. Power losses and efficiency are evaluated using the method presented in [21] and [25]. In this comparison, D is manually adjusted to keep the output voltage constant at 200V while P_o changes from 50W to 350W. The results are depicted in Fig. 17(a). As anticipated, the proposed converters exhibit higher efficiency than the competitors, and at higher power levels, their efficiencies slightly decrease. In comparison to their competitors, only SDL-YSN

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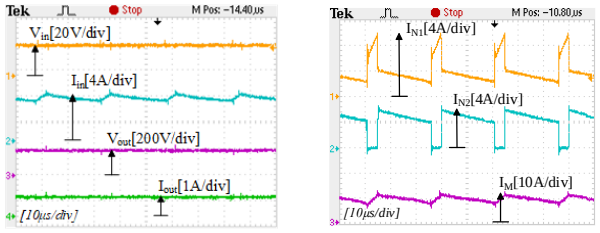
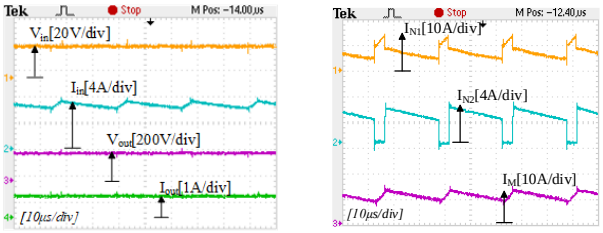


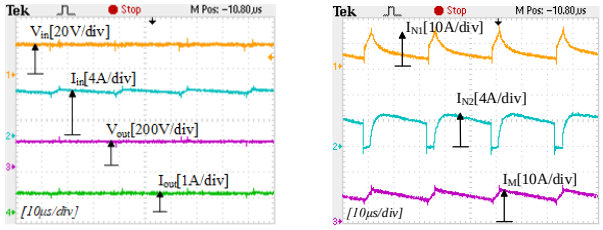
(a) (b)

Fig. 13. Experimental waveforms of Type I proposed network in G=8 (a) input and output voltages and currents, (b) coupled inductor currents.



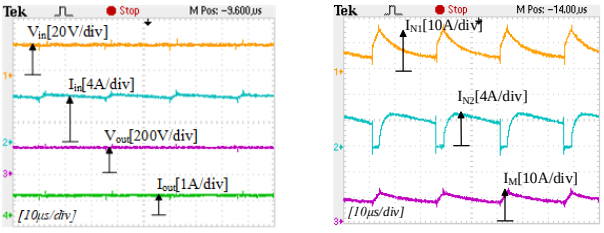
(a) (b)

Fig. 14. Experimental waveforms of Type II proposed network in G=8 (a) input and output voltages and currents, (b) coupled inductor currents.



(a) (b)

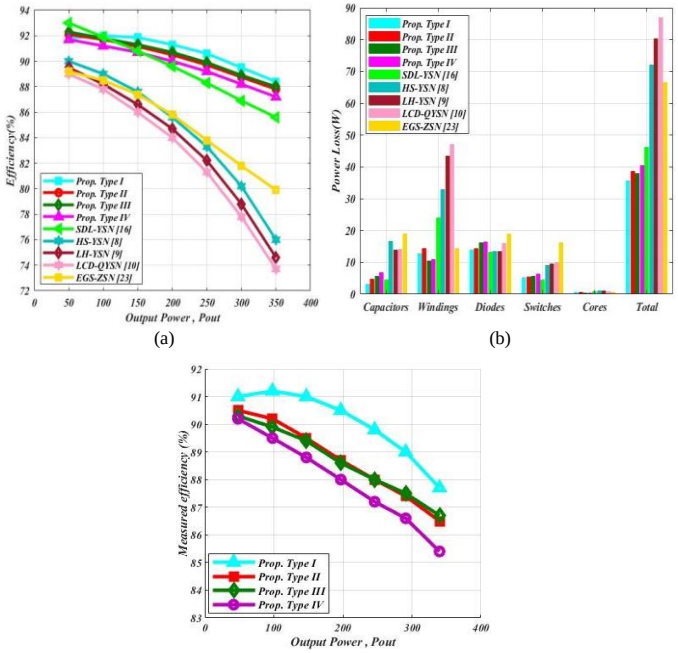
Fig. 15. Experimental waveforms of Type III proposed network in G=8 (a) input and output voltages and currents, (b) coupled inductor currents.



(a) (b)

Fig. 16. Experimental waveforms of Type IV proposed network in G=8 (a) input and output voltages and currents, (b) coupled inductor currents.

offers relatively good efficiency, which is also outperformed by the proposed topologies at higher powers. Generally, the improvement in the efficiency of the proposed converters can be attributed to very low current stresses and voltage spikes. For a more detailed analysis, Fig. 17(b) reports the power loss distributions at 300W. The power losses in the windings of the proposed converters are significantly lower than other converters. In terms of other elements, such as the power losses of capacitors, diodes, etc., the proposed topologies perform better than competitors in most parts. To validate the simulation results, the experimental efficiencies for the proposed networks are measured and plotted in Fig. 17(c). The measurements closely match the theoretical results of Fig. 17(a). Evidently, the practical efficiency is slightly lower than the values derived from simulations. This is mainly due to losses ignored in simulations such as losses of the board (PCB), the skin effects of windings, and the wires used for connections [22]. Eventually, it can be asserted that, at high power levels, the proposed ZSNs offer significant advantages, including high efficiency, low current stresses of elements, and low volume of inductors and capacitors, compared to other ZSNs.



(a) (b)

(c)

Fig. 17. (a) Efficiency comparison, (b) loss distribution at 300W, and (c) measured efficiency.

TABLE IV
MEASURED AND CALCULATED PARAMETER VALUES

Parameters		Type I	Type II	Type III	Type IV
V_{out}	Meas.	194 V	193 V	193 V	192 V
	Calc.	200 V	200 V	200 V	200 V
V_{C1}	Meas.	92 V	97 V	66 V	69 V
	Calc.	95.5 V	99 V	68 V	70 V
V_{C2}	Meas.	195 V	48.5 V	103 V	19 V
	Calc.	200 V	50 V	110 V	20 V
V_{C3}	Meas.	-	193.5 V	104 V	105 V
	Calc.	-	200 V	100 V	110 V
V_{C4}	Meas.	-	-	-	103 V
	Calc.	-	-	-	110 V
I_{in}	Meas.	6.54 A	6.62 A	6.61 A	6.65 A
	Calc.	6 A	6 A	6 A	6 A
I_M	Meas.	10.1 A	11.2 A	9.85 A	10.15 A
	Calc.	8.84 A	9.75 A	8.35 A	9 A

VI. CONCLUSION

This paper introduces a novel class of impedance source networks based on coupled inductors and an active switch for DC-DC applications. The proposed converters offer significant advantages, including ultra-high voltage gain, low current stress of elements, low volume of inductors and capacitors, continuous input current, high efficiency, and power density.

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These features make them suitable for renewable energy sources and high voltage gain applications such as distributed power generation. Also, these networks effectively mitigate the DC-link voltage spikes caused by leakage inductance. Although the proposed converters have a higher number of components, their current and voltage ratings are low. The theoretical steady-state operation analysis is presented and successfully verified by extensive experimental waveforms.

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