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A Grid-Forming Converter with MVDC Supply and Integrated Step-Down Transformer: Modeling, Control Perspectives, and Control Hardware-in-the-Loop (C-HIL) Verification

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Abstract: A grid-forming voltage source converter with an integrated step-down transformer could be a promising solution for supplying low-voltage alternating current loads from a medium-voltage direct current supply. However, it may require a control system that gathers feedback signals from both the primary and secondary sides of the transformer, which in turn complicates the derivation of a standard form linear model. The absence of such a model complicates control tuning, as well as the assessment of dynamics and stability of the converter system. The objective of this paper is to address this gap in knowledge. For the case study, a conventional *H*-bridge converter with a step-down transformer and an $\alpha\beta$-frame dual-loop grid-forming controller is considered. Initially, comprehensive guidelines on deriving a standard form linear model for this converter system are presented. Then, the impact of controlling the VSC in a *dq* frame and the changes in the transformer vector group on the small-signal model of the VSC are analyzed. The aspects of control tuning are also discussed in detail, and the model's accuracy and efficacy are validated both theoretically and through control hardware-in-the-loop (C-HIL) tests using a Typhoon HIL setup.

Keywords: control hardware-in-the-loop (C-HIL); control tuning; grid-forming control; low-voltage alternating current (LVAC); medium-voltage direct current (MVDC); small-signal modeling; transformer; voltage source converter (VSC); voltage control

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1. Introduction

The expansion of MVDC networks, ranging from 1.5 to 55 kV, presents a crucial solution for creating a cleaner energy landscape by addressing and mitigating challenges encountered in the transition towards transportation electrification, integrating renewable energy sources such as photovoltaic (PV) and wind, and implementing energy storage systems [1–5]. For example, it is known that the transportation industry, responsible for nearly 36% of total energy expenditure, is shifting towards electric vehicles (EVs) to reduce emissions of harmful greenhouse gases [6]. This shift, marked by a significant increase in EV production and the expansion of the global EV fleet, highlights the urgent need for an enhanced EV charging infrastructure to match the growing demand. Figure 1 illustrates the role of an MVDC network in addressing this challenge, notably through the integration of the railway system, renewable energy, energy storage resources, and EV charging stations, among others [1]. One innovative aspect involves capturing and repurposing the kinetic energy generated during train braking—a process that would otherwise waste this energy—by providing supplemental power to EV charging stations located near railway stations [7–10]. This approach not only conserves energy but also promotes the adoption of EVs and the integration of renewable energy sources into the electrical grid, thereby

creating a more flexible and resilient energy system capable of adjusting to varying supply and demand conditions.

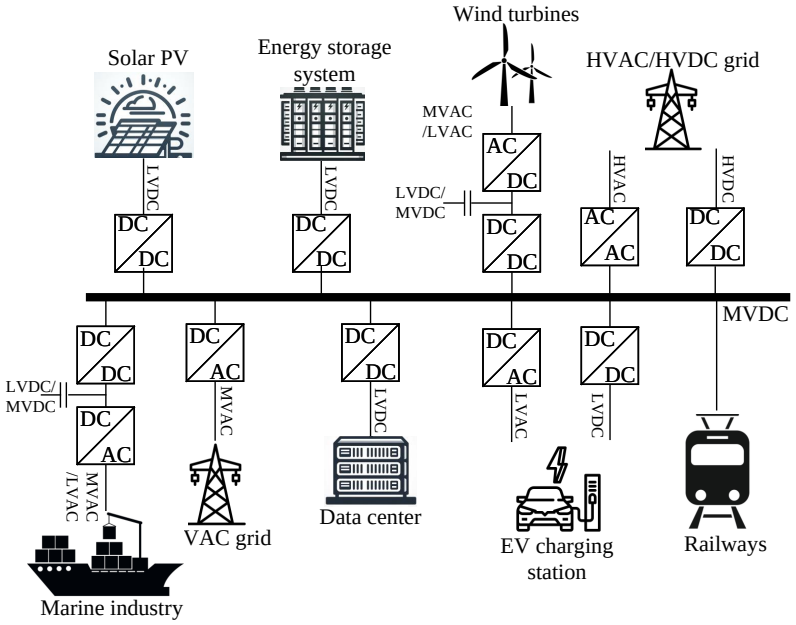

Figure 1. Highlighting the role of an MVDC grid in supporting EV charging stations, enhancing renewable energy integration, among other benefits, and reinforcing weak AC grids to ensure power quality.

To supply power to low-voltage AC (LVAC) equipment and loads, such as an AC EV charging station, from an MVDC source (e.g., a DC railway traction system), several topological options are available. Thanks to rapid advancements in power electronics components and systems, which have enabled the development of efficient MV converters, employing high-power MV DC-AC converters emerges as a practical alternative [11]. The choice of converter—whether a conventional *H*-bridge or multilevel power converters including the neutral point clamped inverter, the flying capacitor multilevel inverter, or cascaded *H*-bridge inverters—depends on the MVDC voltage level and several key factors, including power quality, efficiency, and system complexity [12–14]. Regardless of the chosen topology, a step-down transformer is beneficial at the converter's output to lower the voltage to an LVAC level. With an appropriate design and vector group selection, this transformer can also block zero sequence currents from passing through, prevent DC injection by the converter, provide single-phase loading on the secondary side, and also serve as the output filter inductor for the converter. Furthermore, to complete the LC filter for the converter, a capacitor is necessary on the secondary (LV) side of the transformer. Using the capacitor on the LV side offers several advantages: it eliminates the need for expensive high-voltage sensors, reduces insulation requirements, and minimizes overall cost. Figure 2 illustrates this configuration for clarity, with three-phase AC EV chargers as the load.

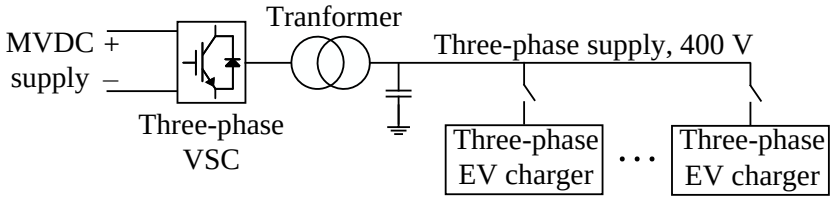

Figure 2. Three-phase EV charging from an MVDC supply (e.g., a DC railway traction system).

To stabilize the voltage and frequency at the load terminal, the voltage source converter (VSC) needs to function as a grid-forming converter. To achieve this objective, a range of control strategies has been developed as documented in the literature [15–17]. A class of methods executes grid-forming control by directly manipulating the inverter's terminal voltage. This can be accomplished using methods such as virtual synchronous machine-based methods, which causes the inverter to mimic the operational characteristics of a synchronous generator [18], or virtual oscillator-based methods, which use virtual oscillator control to emulate the dynamics of weakly nonlinear oscillators in inverter control [19,20]. More common approaches utilize a nested control structure that includes an inner current control loop, an intermediate voltage control loop, and an outer layer comprising virtual impedance and power control loops [21,22]. The inner current loop, essential for damping the LC filter resonance, could be either the capacitor current feedback loop or the inverter-side current control loop. The inverter-side current control loop is the more common choice because it not only damps the LC filter resonance but also provides short-circuit and fault current limitation capabilities for the converter, which are necessary to prevent damage to power electronics switches. The intermediate voltage control stabilizes the converter's output capacitor voltage. The power control loops are crucial in adjusting the reference voltage magnitude, phase, and frequency signals for the intermediate voltage control loop, for instance, through the well-known droop control method [23].

A grid-forming converter integrated with a step-down transformer may require feedback signals from both the primary and secondary sides of the transformer due to technical or economic considerations. This necessitates the use of transformation matrices to convert secondary voltages and/or currents to their primary counterparts. The step-down transformer at the converter output and its associated transformation matrices in the control system complicate the derivation of a standard small-signal model for the converter system. The absence of a standard linear model, in turn, challenges the tuning of control parameters, as well as the assessment of the dynamics and stability of the converter system. The existing literature lacks comprehensive studies addressing these complexities. Additionally, the impact of the transformer's vector group and the control system's working frame on the small-signal model is underexplored. This paper aims to address these gaps in knowledge. To this end, a conventional H-bridge converter with a Dyn11 vector group step-down transformer and an $\alpha\beta$-frame dual-loop grid-forming controller is initially considered as the case study. Comprehensive guidelines for developing a standard small-signal model of this converter system are provided. Based on the resulting small-signal model, detailed guidelines for tuning control parameters will also be provided. Additionally, we will discuss the implications of changing the transformer's vector group to Dyn1 and shifting from an $\alpha\beta$-frame to a dq-frame control system on the resulting linear model.

The remainder of this work is organized as follows: Section 2 delves into the architecture of the grid-forming (voltage-controlled) VSC and its dual-sided feedback control within the $\alpha\beta$ frame, with an emphasis on the role of transformation matrices in signal conversion and their derivation based on transformer characteristics. It also describes the process for establishing a primary-side equivalent of the VSC system, deriving and integrating its average model into the control system, and simplifying it into a standard-form small-signal model. Section 3 is dedicated to analyzing the impact of different control frames—$\alpha\beta$ versus dq—on the small-signal model's accuracy. Additionally, this section examines how changes in the transformer's vector group affect the model. Section 4 provides detailed guidelines for tuning the control parameters of the VSC. Sections 5 and 6 address the VSC's performance assessment and model verification through theoretical and C-HIL investigations. Finally, the paper concludes in Section 7.

2. Grid-Forming VSC with a Dual-Sided Feedback Control

Figure 3 illustrates a grid-forming VSC equipped with a dual-sided feedback control in the $\alpha\beta$ frame, where the inner loop regulates the inverter-side current, and the intermediate loop controls the capacitor voltage. Note that measuring current on the primary side, which is in a Delta connection, avoids the complications of zero sequence currents, which can occur on the secondary side due to its Yn connection. Note also that the dynamics of the outer power control loop, which adjusts the reference signals for voltage magnitude, phase, and frequency, are neglected in this paper.

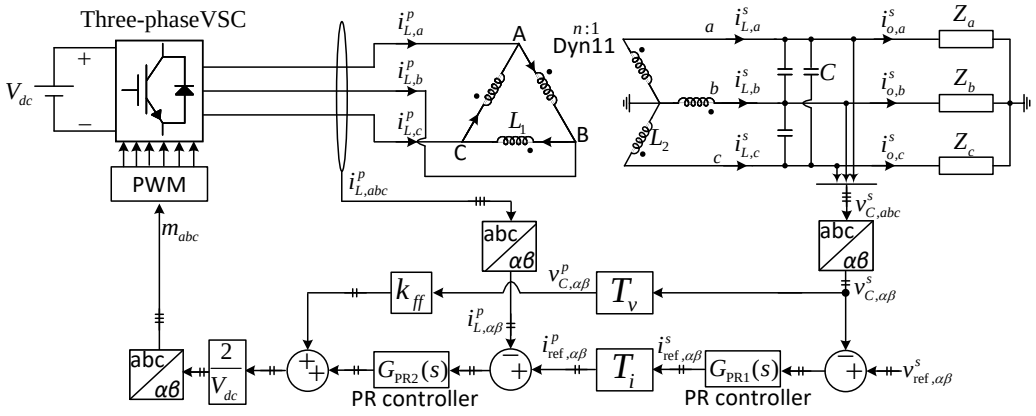

Figure 3. A grid-forming VSC with a dual-sided feedback control in the $\alpha\beta$ frame. This VSC supplies power to an LVAC network, using a transformer to lower voltage, enable single-phase loading, and block zero sequence currents.

The symbols i_L, i_o, and v_C denote the inverter-side current, output (load) current, and capacitor voltage, respectively, while v_{ref} and i_{ref} represent the reference signals for the intermediate voltage and inner current control loops. Additionally, the symbols L_1 (R_1) and L_2 (R_2) indicate the leakage inductances (resistances) of the transformer on the primary and secondary sides, receptively. R_1 and R_2 are not depicted in Figure 3. n represents the turn ratio, which is equal to the ratio of the input phase voltage to the output phase voltage. The term V_{dc} represents the DC-link voltage, and $\frac{2}{V_{dc}}$ in the control system makes the control design independent of the DC-link voltage value. The superscripts p and s denote signals or variables related to the primary and secondary sides of the transformer, respectively.

The control system depicted in Figure 3 resembles a traditional dual-loop controller but with a notable distinction: the transformation matrices $T_{v,\alpha\beta}$ and $T_{i,\alpha\beta}$, which convert the transformer's secondary-side voltage and current signals to their primary counterparts in the $\alpha\beta$ frame, respectively. These transformation matrices, which are determined based on the turn ratio and vector group of the transformer, introduce complexity into the small-signal modeling, thereby complicating the control tuning and stability analysis of the system. The strategies for addressing this challenge are explored in the subsequent sections.

2.1. Transformation Matrices $T_{v,\alpha\beta}$ and $T_{i,\alpha\beta}$

According to the transformer's turn ratio and vector group as shown in Figure 3, the three-phase current signals on the primary and secondary sides of the transformer are related to each other as follows:

$$i^p_{L,abc} = \frac{1}{n}\begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix} i^s_{L,abc}. \tag{1}$$

In the equation above, the three-phase current signal can be expressed as the product of the inverse Clarke transformation ($T_{\alpha\beta\to abc}$) to their $\alpha\beta$ frame counterparts, that is,

$$T_{\alpha\beta\to abc} i^{p}_{L,\alpha\beta} = \frac{1}{n}\begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix} T_{\alpha\beta\to abc} i^{s}_{L,\alpha\beta} \tag{2}$$

where

$$T_{\alpha\beta\to abc} = \begin{bmatrix} 1 & 0 \\ -0.5 & \frac{\sqrt{3}}{2} \\ -0.5 & -\frac{\sqrt{3}}{2} \end{bmatrix}. \tag{3}$$

By multiplying both sides of Equation (2) with the Clarke transformation ($T_{abc\to\alpha\beta}$), we obtain

$$\begin{aligned} &\underbrace{\left(T_{abc\to\alpha\beta} T_{\alpha\beta\to abc}\right)}_{I} i^{p}_{L,\alpha\beta} \\ &= \underbrace{\left(\frac{1}{n} T_{abc\to\alpha\beta}\begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix} T_{\alpha\beta\to abc}\right)}_{T_{i,\alpha\beta}} i^{s}_{L,\alpha\beta} \end{aligned} \tag{4}$$

which can be rewritten as

$$i^{p}_{L,\alpha\beta} = \underbrace{\frac{1}{n}\begin{bmatrix} \frac{3}{2} & \frac{\sqrt{3}}{2} \\ -\frac{\sqrt{3}}{2} & \frac{3}{2} \end{bmatrix}}_{T_{i,\alpha\beta}} i^{s}_{L,\alpha\beta}. \tag{5}$$

Similarly, the transfer matrix $T_{v,\alpha\beta}$, which relates the secondary and primary voltages of the transformer in the $\alpha\beta$, can be obtained as

$$v^{p}_{C,\alpha\beta} = \underbrace{\frac{n}{3}\begin{bmatrix} \frac{3}{2} & \frac{\sqrt{3}}{2} \\ -\frac{\sqrt{3}}{2} & \frac{3}{2} \end{bmatrix}}_{T_{v,\alpha\beta}} v^{s}_{C,\alpha\beta}. \tag{6}$$

2.2. Transformation of Secondary-Side Elements to Primary-Side Equivalents in VSC System

In this section, we delve into a mathematical transformation process that enables the representation of all secondary-side components of the VSC system with transformer—specifically, the capacitor, load, and associated elements—into an equivalent primary-side representation. This equivalent primary-side representation simplifies the process of developing a comprehensive closed-loop model for the VSC, along with its control systems. It aids in streamlining control tuning and in the analysis of the VSC system's dynamics and stability. The key points to consider are as follows:

- The equivalent resistance, inductance, or, more broadly, impedance seen at the primary side of the transformer when a resistor R, an inductor L, or impedance Z is connected to the secondary side, are given by n^2R, n^2L, or n^2Z, respectively.
- The equivalent capacitance seen at the primary side of the transformer, when a capacitor C is connected to the secondary side, is given by $\frac{C}{n^2}$.
- For three identical resistors $R_\triangle$, inductors $L_\triangle$, or generally, impedances $Z_\triangle$ arranged in a Delta configuration, the equivalent resistors, inductors, or impedances in a Wye (Star) configuration can be determined as follows: $R_Y = \frac{R_\triangle}{3}$, $L_Y = \frac{L_\triangle}{3}$, and $Z_Y = \frac{Z_\triangle}{3}$, respectively.
- For three identical capacitors $C_\triangle$ in a Delta configuration, the equivalent capacitors in a Wye configuration are calculated as follows: $C_Y = 3C_\triangle$.

- As the secondary winding of the transformer is in a Wye configuration, elements on the secondary side of the transformer in a Delta configuration should be converted to their equivalent Wye configuration before transferring them to the primary side.
- As the primary winding of the transformer is in a Delta configuration, the elements transferred to the primary side will be in Delta configurations, meaning that a Delta-to-Wye transformation would be needed after transferring elements to the primary side.

Based on the above points, the equivalent primary-side representation of the converter system in Figure 3 can be obtained as depicted in Figure 4.

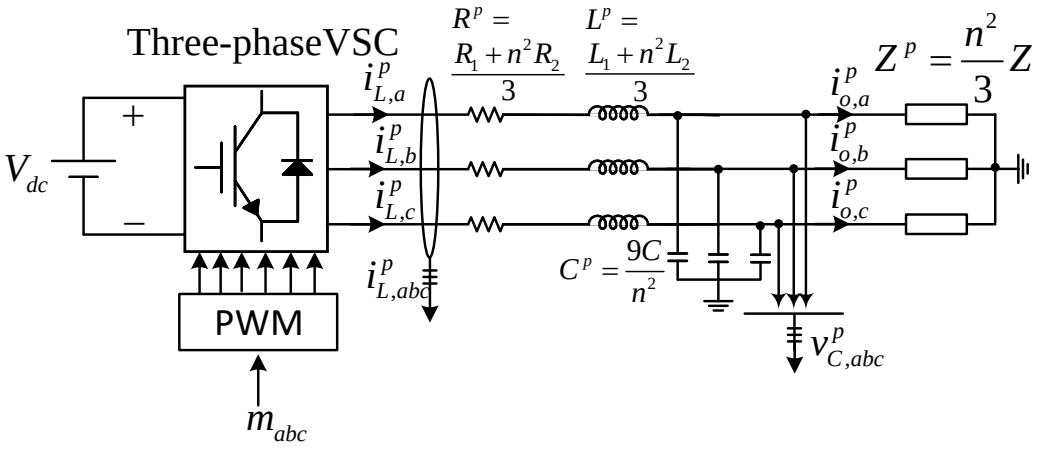

Figure 4. Equivalent primary-side representation of the converter system shown in Figure 3.

2.3. Small-Signal Modeling

The primary-side representation of the converter system as shown in Figure 4 is in a standard form, that is, a converter with an LC output filter and load. This allows for the straightforward derivation of its average model in the $\alpha\beta$ frame as depicted in Figure 5. As illustrated, the output of the average model is $v^p_{C,\alpha\beta}$, which represents the $\alpha\beta$-frame capacitor voltage transferred to the primary side of the transformer. However, the voltage feedback signal to the control system is sourced from the secondary side. Thus, to integrate the average model shown in Figure 5 with the grid-forming control system in Figure 3, the inverse of the transfer matrix $T_{v,\alpha\beta}$ (see (6)) needs to be applied to the voltage feedback signal as highlighted in Figure 6a. Through the application of block diagram algebra, Figure 6a is simply represented by Figure 6b. Within the simplified representation in Figure 6b, the intricate product of $T^{-1}_{v,\alpha\beta} G_{\mathrm{PR1}}(s) T_{i,\alpha\beta}$ can be decoded into a more straightforward expression, as follows:

$$\underbrace{\frac{1}{n}\begin{bmatrix} \frac{3}{2} & -\frac{\sqrt{3}}{2} \\ \frac{\sqrt{3}}{2} & \frac{3}{2} \end{bmatrix}}_{T^{-1}_{v,\alpha\beta}} \begin{bmatrix} G_{\mathrm{PR1}}(s) & 0 \\ 0 & G_{\mathrm{PR1}}(s) \end{bmatrix} \underbrace{\frac{1}{n}\begin{bmatrix} \frac{3}{2} & \frac{\sqrt{3}}{2} \\ -\frac{\sqrt{3}}{2} & \frac{3}{2} \end{bmatrix}}_{T_{i,\alpha\beta}} = \frac{3}{n^2}\begin{bmatrix} G_{\mathrm{PR1}}(s) & 0 \\ 0 & G_{\mathrm{PR1}}(s) \end{bmatrix}. \quad (7)$$

By utilizing the equation above, Figure 6b can be simplified as depicted in Figure 6c.

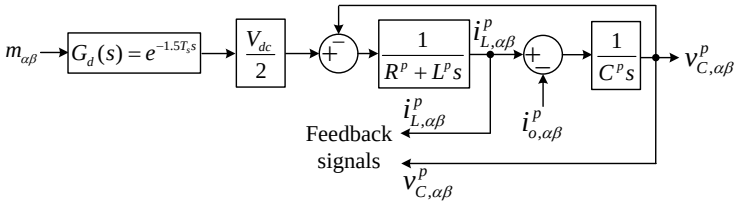

Figure 5. Average model of converter system in Figure 4.

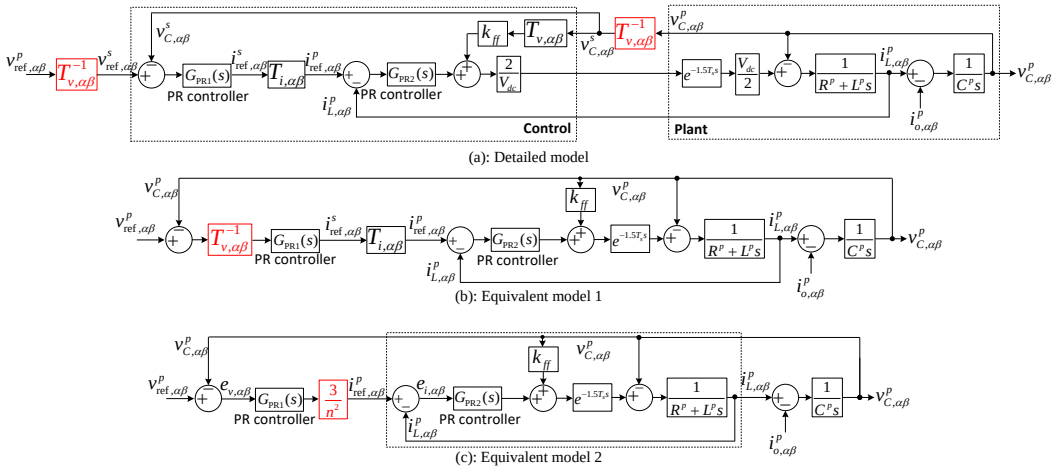

Figure 6. Small-signal model of the grid-forming VSC shown in Figure 3. (**a**) Detailed model. (**b**,**c**) Mathematically equivalent alternative versions.

3. Impact of Transformer's Vector Group and Control Frame on Small-Signal Model

3.1. Impact of Transformer's Vector Group

In the case study depicted in Figure 3, the transformer's vector group is designated as Dyn11. This indicates that the primary winding is connected in a Delta configuration (D), the secondary winding is in a star configuration (Y) with an accessible neutral point (n), and there is a phase shift of 330° between the primary and secondary sides. This section will briefly explore how altering the transformer's vector group impacts the small-signal model of the converter system. It is important to note that a star-connected neutral is required on the secondary side to facilitate single-phase loading. Furthermore, a Delta connection on the primary side is necessary to prevent the passage of third harmonic currents, commonly referred to as earth fault currents, through the transformer. Consequently, Dyn1 will be selected as the illustrative example. However, it should be noted that this may not necessarily represent a superior choice compared to the original Dyn11 configuration in practical applications.

In Section 2.2, it is shown that the equivalent primary-side representation of the converter system is influenced solely by the winding configuration of the transformer (i.e., whether they are connected in Delta or star), while the phase shift between the primary and secondary windings has no impact. Since the Dyn1 and Dyn11 vector groups share the same winding configurations, both result in an identical equivalent primary-side representation of the converter system as illustrated in Figure 4. Consequently, the models illustrated in Figures 6a,b are applicable to the Dyn1 vector group as well. However, to ascertain whether the simplification of Figure 6b leads to Figure 6c for Dyn1, similar to what is demonstrated for Dyn11, it is necessary to derive the transformation matrices $T_{v,\alpha\beta}$ and $T_{i,\alpha\beta}$ specific to the Dyn1 vector group.

Following the procedures described in Section 2.1, the transformation matrices $T_{v,\alpha\beta}$ and $T_{i,\alpha\beta}$ for the transformer vector group Dyn1 can be derived as follows:

$$i^p_{L,\alpha\beta} = \underbrace{\frac{1}{n}\begin{bmatrix} \frac{3}{2} & -\frac{\sqrt{3}}{2} \\ \frac{\sqrt{3}}{2} & \frac{3}{2} \end{bmatrix}}_{T_{i,\alpha\beta}} i^s_{L,\alpha\beta}. \tag{8}$$

$$v^p_{C,\alpha\beta} = \underbrace{\frac{n}{3}\begin{bmatrix} \frac{3}{2} & -\frac{\sqrt{3}}{2} \\ \frac{\sqrt{3}}{2} & \frac{3}{2} \end{bmatrix}}_{T_{v,\alpha\beta}} v^s_{C,\alpha\beta}. \tag{9}$$

By substituting $T_{v,\alpha\beta}$ and $T_{i,\alpha\beta}$ as defined in the above equations into the product $T_{v,\alpha\beta}^{-1} G_{\mathrm{PR1}}(s) T_{i,\alpha\beta}$, which appears in the small-signal model in Figure 6b, we obtain

$$\underbrace{\frac{1}{n}\begin{bmatrix} \frac{3}{2} & \frac{\sqrt{3}}{2} \\ -\frac{\sqrt{3}}{2} & \frac{3}{2} \end{bmatrix}}_{T_{v,\alpha\beta}^{-1}} \begin{bmatrix} G_{\mathrm{PR1}}(s) & 0 \\ 0 & G_{\mathrm{PR1}}(s) \end{bmatrix} \underbrace{\frac{1}{n}\begin{bmatrix} \frac{3}{2} & -\frac{\sqrt{3}}{2} \\ \frac{\sqrt{3}}{2} & \frac{3}{2} \end{bmatrix}}_{T_{i,\alpha\beta}} = \frac{3}{n^2}\begin{bmatrix} G_{\mathrm{PR1}}(s) & 0 \\ 0 & G_{\mathrm{PR1}}(s) \end{bmatrix} \tag{10}$$

which is identical to (7). Therefore, the simplified small-signal model depicted in Figure 6c is also valid for the transformer vector group Dyn1.

The concise conclusion is that the phase shift between the primary and secondary windings has no impact on the small-signal model of the converter system.

3.2. Impact of Control Frame

Figure 7 illustrates a grid-forming VSC equipped with dual-sided feedback control in the dq frame, closely resembling Figure 3, except that the converter's working frame is the dq frame and the proportional–resonant (PR) controllers have been replaced with proportional–integral (PI) controllers. The primary inquiry of this section is to discern how the control frame of the converter influences its small-signal model. To address this query, it is first necessary to ascertain how a change in the control frame affects the transformation matrices T_v and T_i.

Equation (5), as mentioned previously, establishes a relationship between the $\alpha\beta$-frame current signals on the primary and secondary sides of the transformer. For convenience, this equation is reiterated below, where $i_{L,dq}^{p}$ and $i_{L,dq}^{s}$ represent the dq-frame equivalents of $i_{L,\alpha\beta}^{p}$ and $i_{L,\alpha\beta}^{s}$, respectively, and $T_{dq\to\alpha\beta} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{bmatrix}$ is the dq-frame to the $\alpha\beta$-frame transformation.

$$\underbrace{i_{L,\alpha\beta}^{p}}_{T_{dq\to\alpha\beta} i_{L,dq}^{p}} = \underbrace{\frac{1}{n}\begin{bmatrix} \frac{3}{2} & \frac{\sqrt{3}}{2} \\ -\frac{\sqrt{3}}{2} & \frac{3}{2} \end{bmatrix}}_{T_{i,\alpha\beta}} \underbrace{i_{L,\alpha\beta}^{s}}_{T_{dq\to\alpha\beta} i_{L,dq}^{s}} \tag{11}$$

If we multiply both sides of the equation above by the inverse of $T_{dq\to\alpha\beta}$, we obtain:

$$\begin{aligned} i_{L,dq}^{p} &= \underbrace{\left(\frac{1}{n} T_{dq\to\alpha\beta}^{-1} \begin{bmatrix} \frac{3}{2} & \frac{\sqrt{3}}{2} \\ -\frac{\sqrt{3}}{2} & \frac{3}{2} \end{bmatrix} T_{dq\to\alpha\beta}\right)}_{T_{i,dq}} i_{L,dq}^{s} \\ &= \underbrace{\frac{1}{n}\begin{bmatrix} \frac{3}{2} & \frac{\sqrt{3}}{2} \\ -\frac{\sqrt{3}}{2} & \frac{3}{2} \end{bmatrix}}_{T_{i,dq}} i_{L,dq}^{s} \end{aligned} \tag{12}$$

It is observed that $T_{i,dq} = T_{i,\alpha\beta}$. Similarly, it can be demonstrated that $T_{v,dq} = T_{v,\alpha\beta}$. Therefore, the transformation matrices T_v and T_i are identical in both control frames.

It is known that an integrator $\frac{1}{s}$ in the dq frame mathematically corresponds to what is known as a reduced-order generalized integrator, also referred to as a complex integrator $\frac{1}{s-j\omega_o}$ in the $\alpha\beta$ frame [24,25]. Here, j represents the complex operator, and $\omega_o = \frac{d\theta}{dt}$ is the angular frequency of the dq frame's rotating angle. Consequently, a PI controller in the dq frame, expressed as $k_p + \frac{k_i}{s}$, corresponds to a Proportional–Complex–Integrator (PCI) controller $k_p + \frac{k_i}{s-j\omega_o}$ in the $\alpha\beta$ frame. Given this correspondence and the fact that $T_{i,dq} = T_{i,\alpha\beta}$ and $T_{v,dq} = T_{v,\alpha\beta}$, the equivalent $\alpha\beta$-frame representation of Figure 7a can be derived as illustrated in Figure 7b.

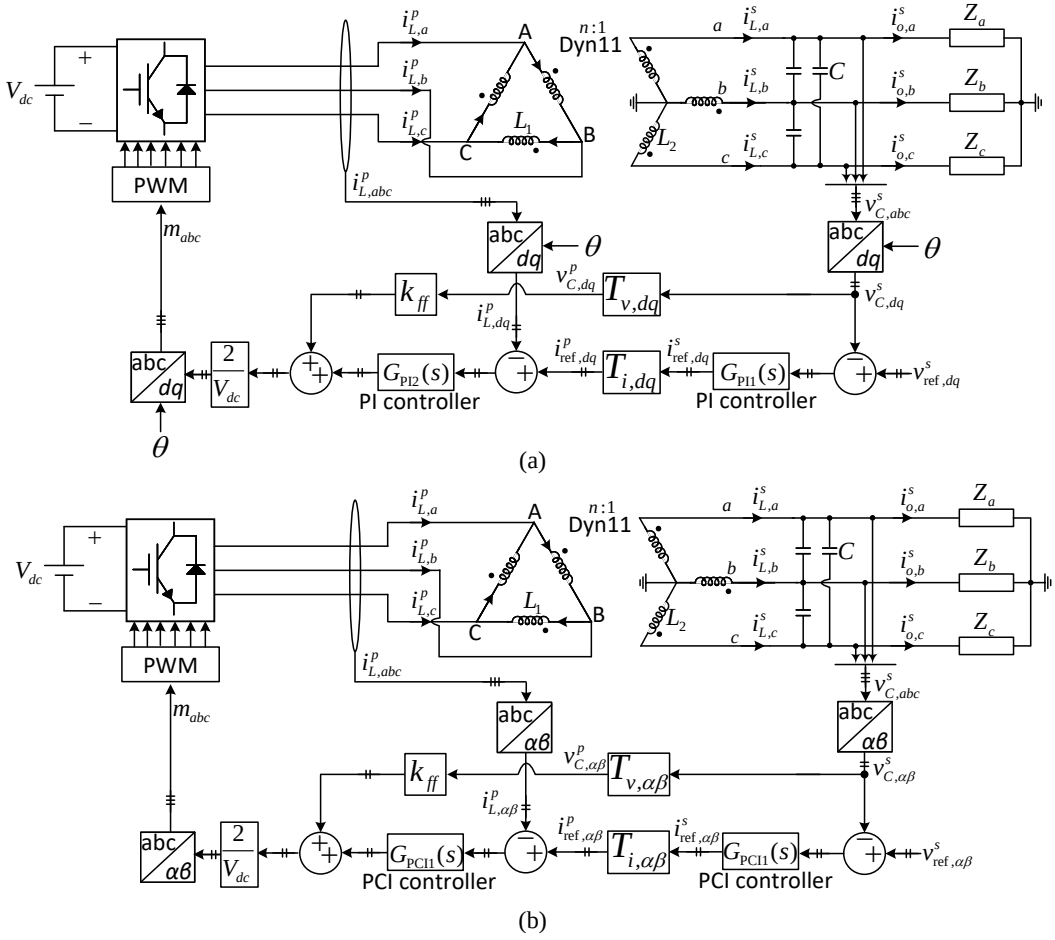

Figure 7. (**a**) A grid-forming VSC with dual-sided feedback control in the *dq* frame. (**b**) Its alternative representation in the $\alpha\beta$ frame. Note that $T_{i,dq} = T_{i,\alpha\beta}$ and $T_{v,dq} = T_{v,\alpha\beta}$.

Upon comparing the converter system depicted in Figure 7b with that shown in Figure 3, it becomes clear that the sole difference lies in the types of control loop regulators: PCI regulators are used in Figure 7b, whereas PR controllers are utilized in Figure 3. Therefore, the small-signal model presented in Figure 6c remains valid for the VSC employing a *dq*-frame control system, provided that the PR regulators within the model are replaced by PCI regulators.

4. Control Tuning

4.1. Inner Current Control and Voltage Feedforward Loops

To tune the control parameters of the inner loop, the focus will be solely on the dashed box in Figure 6c. Here, $i^p_{\text{ref},\alpha\beta}$, $i^p_{L,\alpha\beta}$, and $v^p_{C,\alpha\beta}$ act as the input, output, and noise (disturbance) in the model, respectively. Initially, the disturbance effect of $v^p_{C,\alpha\beta}$ is ignored, and the open-loop transfer function—specifically, the ratio of the output current $i^p_{L,\alpha\beta}$ to the error current—is derived as follows:

$$G_{ol}(s) = \frac{i^p_{L,\alpha\beta}(s)}{i^p_{\text{ref},\alpha\beta}(s) - i^p_{L,\alpha\beta}(s)} = \underbrace{\left(k_{pc} + k_{rc}\frac{s}{s^2+\omega_o^2}\right)}_{G_{\text{PR2}}(s)} e^{-1.5T_s s}\frac{1}{L^p s + R^p} \tag{13}$$

For frequencies higher than the fundamental frequency ω_o, a resonant controller and integral controller have very close frequency response (see Figure 8). Therefore, for the

sake of simplicity, the resonant regulator in the above transfer function can be replaced by a simple integrator. In this case, we obtain:

$$G_{ol}(s) \approx \left(k_{pc} + \frac{k_{rc}}{s}\right) e^{-1.5T_s s} \frac{1}{L^p s + R^p} = \frac{k_{pc} e^{-1.5T_s s}}{L^p s} \frac{s + k_{rc}/k_{pc}}{s + R^p/L^p} \tag{14}$$

If $k_{rc}/k_{pc} = R^p/L^p$ is considered, a pole-zero cancellation is achieved, and the above transfer function can be simplified as follows:

$$G_{ol}(s) = \frac{k_{pc} e^{-1.5T_s s}}{L^p s}. \tag{15}$$

If we define ω_c as the loop gain crossover frequency, we obtain

$$|G_{ol}(j\omega_c)| = \frac{k_{pc}}{L^p \omega_c} = 1 \Rightarrow k_{pc} = L^p \omega_c. \tag{16}$$

Therefore, k_{pc} can be determined by selecting an appropriate value for the loop gain crossover frequency. Typically, it is set to 1/10 of the effective switching frequency, which is 7 kHz (see Table 1). Once k_{pc} is calculated, k_{rc} is set to $k_{rc} = k_{pc} \cdot \frac{R^p}{L^p}$.

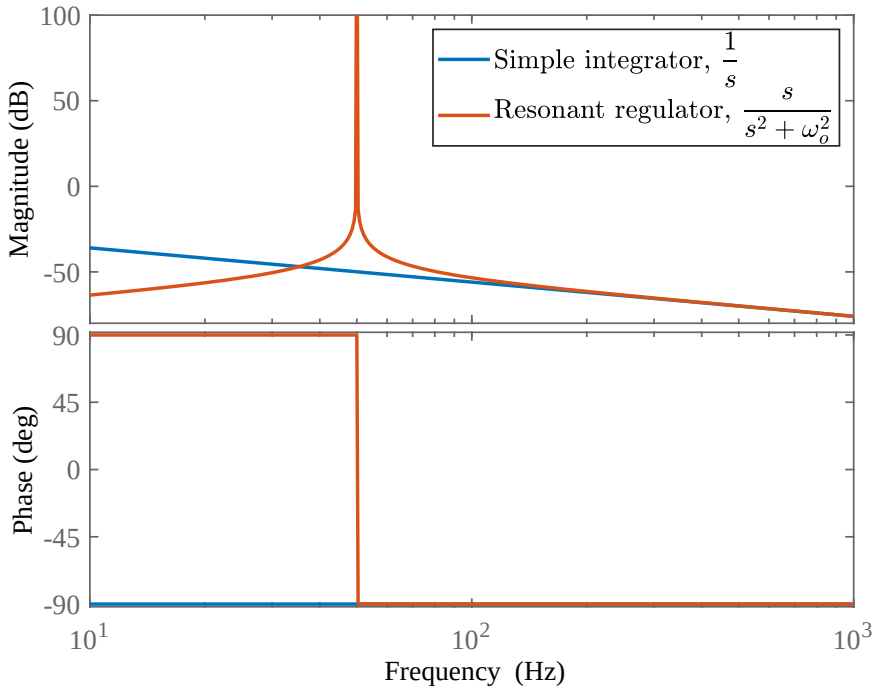

Figure 8. Bode plots of a resonant regulator and a simple integrator, with the resonant regulator's center frequency set at $\omega_o = 2\pi 50$ rad/s.

Table 1. System parameters.

Description	Value
Nominal DC-link voltage, V_{dc}	3300 V
Primary winding resistance, R_1	0.2 Ω
Secondary winding resistance, R_2	0.001 Ω
Primary winding leakage inductance, L_1	3 mH
Secondary winding leakage inductance, L_2	4 µH
Output capacitance, C	240 µF
Transformer's turn ratio, n	$1900/(400/\sqrt{3})$
VSC switching frequency, f_{sw}	7 kHz

Based on the guidelines provided above, and considering the open-loop gain crossover frequency to be 1/10 of the switching frequency, i.e., $\omega_c = 2\pi \times 700\,\text{rad/s}$, the proportional and resonant gains of the inner current control loop can be calculated to be $k_{pc} = 4.79$ and $k_{rc} = 392$.

Figure 9 shows the Bode plot of the open-loop transfer function (13) with the designed control parameters. It is observed that both the Phase Margin (PM) and Gain Margin (GM) of the control loop fall within the recommended ranges of 30–60° and 2 to 10 dB, respectively, and are therefore considered satisfactory. Interestingly, the open-loop gain crossover frequency occurs exactly at the targeted value of 700 Hz, which further confirms that the approximation made for obtaining (14), replacing the resonant controller with an integral one, is accurate.

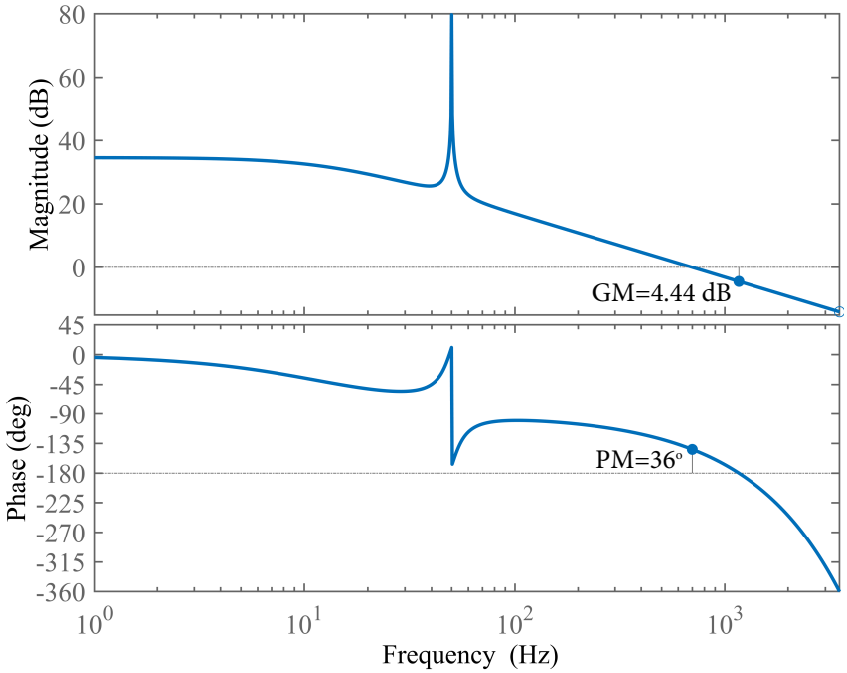

Figure 9. Bode plot of the open-loop transfer function (13) with the designed control parameters, $k_{pc} = 4.79$ and $k_{rc} = 392$.

The next step involves designing the gain of the voltage feedforward loop, denoted as k_{ff}. This gain needs to be designed to ensure that the ratio of the inverter-side current to the capacitor voltage, expressed in (17), demonstrates passivity over the widest possible frequency spectrum. This requirement means that the phase angle should range from $-90°$ to $+90°$ across the broadest achievable frequency range:

$$\left.\frac{i^p_{L,\alpha\beta}(s)}{v^p_{C,\alpha\beta}(s)}\right|_{i^p_{ref,\alpha\beta}=0} = -\frac{1 - k_{ff}G_d(s)}{R^p + L^p s + G_d(s)\left(k_{pc} + \frac{k_{rc}s}{s^2+\omega_o^2}\right)} \tag{17}$$

Figure 10 displays the Bode plot of (17) for different values of the feedforward gain k_{ff}. It is observed that increasing the value of k_{ff} expands the passivity frequency region at high frequencies. However, this results in increased nonpassivity around the fundamental frequency. Therefore, a trade-off decision must be made. In this work, $k_{ff} = 0.7$ is selected. It is noted that $k_{ff} = 1$ leads to significant nonpassivity around the fundamental frequency and is, therefore, not recommended.

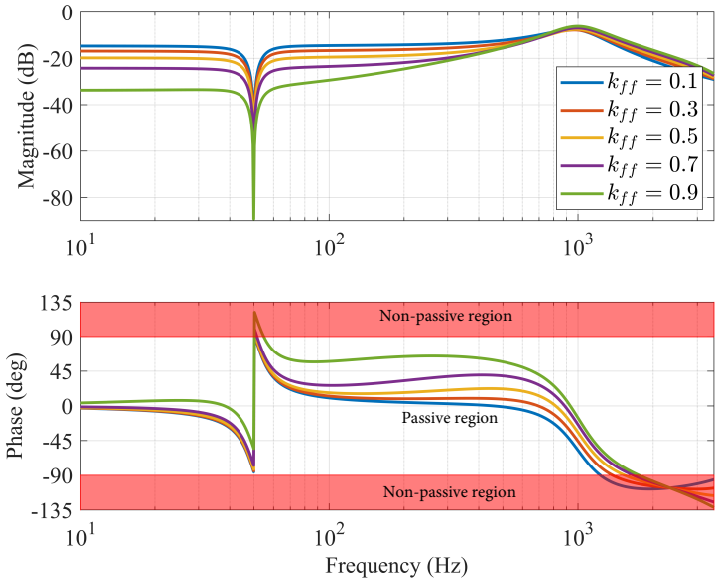

Figure 10. Bode plots of (17) for different values of the voltage feedforward loop's gain.

4.2. Intermediate Voltage Control Loop

By neglecting the disturbance effect of the output (load) current, denoted as $i^p_{o,\alpha\beta}(s)$, the open-loop transfer function of the voltage control loop can be obtained as follows:

$$G_{ol}(s) = \frac{v^p_{C,\alpha\beta}(s)}{v^p_{ref,\alpha\beta}(s) - v^p_{C,\alpha\beta}(s)} = \frac{\frac{3}{n^2} e^{-1.5T_s s} G_{\text{PR1}}(s) G_{\text{PR2}}(s)}{1 + C^p s.(R^p + L^p s) + \left(C^p s.G_{\text{PR2}}(s) - k_{ff}\right) e^{-1.5T_s s}} \quad (18)$$

where $G_{\text{PR1}}(s) = k_{pv} + k_{rv}\frac{s}{s^2+\omega_0^2}$ represents the PR controller within the voltage control loop. The aim of this section is to fine-tune its control parameters for optimal performance.

The resonant gain of the voltage control loop mainly affects the frequencies around the fundamental frequency and has a negligible effect on the high-frequency range. The Bode plots in Figure 11 confirm this fact. Therefore, without affecting the accuracy, the resonant term can be set to zero, and the proportional gain can be determined based on the GM of the voltage control loop.

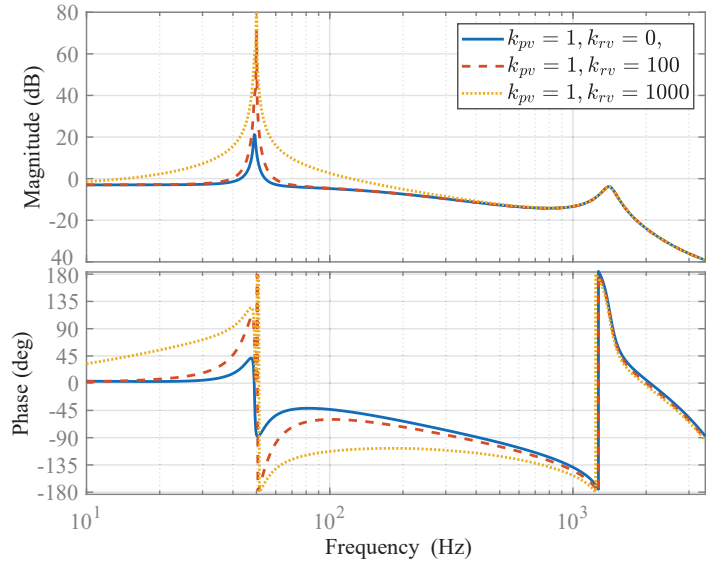

Figure 11. Bode plots of the open-loop transfer function of the voltage control loop, (18), with the proportional gain (k_{pv}) fixed at 1 and varying resonant gains (k_{rv}) of 0, 100, and 1000.

Figure 12 presents the Bode plots for the open-loop transfer function of the voltage control loop as defined in (18), with the resonant gain (k_{rv}) set to 0 and the proportional gains (k_{pv}) adjusted to 0.5, 1, and 1.5. It is observed that increasing the proportional gain enhances the magnitude–frequency response, thereby improving the system's dynamic response speed. Concurrently, it is noted that the high-frequency resonance peak elevates, and the Gain Margin of the converter decreases as the proportional gain increases. If the high-frequency resonance peak nears 0 dB, the converter risks instability. Consequently, to maintain stability, the proportional gain must be chosen to keep the resonance peak well below 0 dB and ensure a sufficiently large GM. Here, a proportional gain (k_{pv}) of 1 is selected, corresponding to a GM of 8 dB.

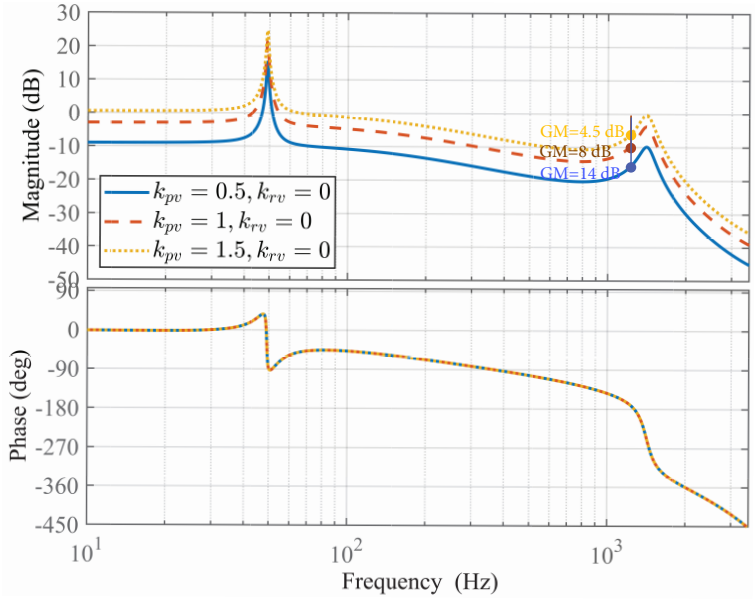

Figure 12. Bode plots of the open-loop transfer function of the voltage control loop, (18), with the resonant gain (k_{rv}) fixed at 0 and varying proportional gains (k_{rv}) of 0.5, 1, and 1.5.

After setting the proportional gain, the resonant gain needs to be determined. As demonstrated in Figure 11, increasing the resonant gain widens the resonance peak around the fundamental frequency, which in turn enhances the system's ability to quickly respond to changes in the grid voltage reference. However, this also leads to a decrease in the PM of the control loop, necessitating a balance between responsiveness and stability. Based on this consideration, a resonant gain of $k_{rv} = 1000$ is identified as the optimal choice. This choice achieves a GM of 9 dB and a PM of 70°. Notably, the achieved GM closely matches the value observed with $k_{pv} = 1$ and $k_{rv} = 0$ in Figure 12, validating the initial decision to consider $k_{rv} = 0$ in the design of k_{pv}.

5. Simulation Results

In this section of the paper, we test the small-signal model shown in Figure 6c to ensure its validity and reliability. Additionally, the performance of the converter when supplying a diode bridge rectifier with an RC load in its DC part is also investigated. This load can resemble most practical nonlinear loads due to its nonlinear characteristics and high harmonic content. The tests are conducted in the MATLAB/Simulink environment (version 8.5).

Using the small-signal model shown in Figure 6c, the output impedance of the grid-forming VSC can be obtained as

$$Z_{out}(s) = \left.\frac{v^p_{C,\alpha\beta}(s)}{i^p_{o,\alpha\beta}(s)}\right|_{v^p_{ref,\alpha\beta}(s)=0} = \frac{\left(Z_L(s) + e^{-1.5T_s s}G_{\mathrm{PR2}}(s)\right)}{1 + C^p s(R^p + L^p s + e^{-1.5T_s s}G_{\mathrm{PR2}}(s)) + e^{-1.5T_s s}\left(\frac{3}{n^2}G_{\mathrm{PR1}}(s)G_{\mathrm{PR2}}(s) - k_{ff}\right)} \quad (19)$$

Figure 13 shows the Bode plot of the output impedance of the VSC, together with the Bode plots for 1 p.u. inductive and capacitive loads. The impedance-based stability criterion mandates that, to ensure the stability of two stable subsystems connected in parallel (here, a grid-forming VSC and a load), the intersection point of their output impedances must demonstrate a positive PM. Specifically, PM $= 180^\circ - |\angle Z_{\mathrm{out}}(j\omega_i) - \angle Z_{\mathrm{load}}(j\omega_i)| > 0$, where ω_i denotes the intersection frequency. The Bode plot in Figure 13 highlights the intersection points between the VSC output impedance and the inductive and capacitive load impedances, as well as the phase of the VSC output impedance at these points. In each case, the phase difference between Z_{out} and Z_{load} is significantly less than 180°, indicating that the VSC maintains a sufficient PM and thereby assures stability under both load conditions.

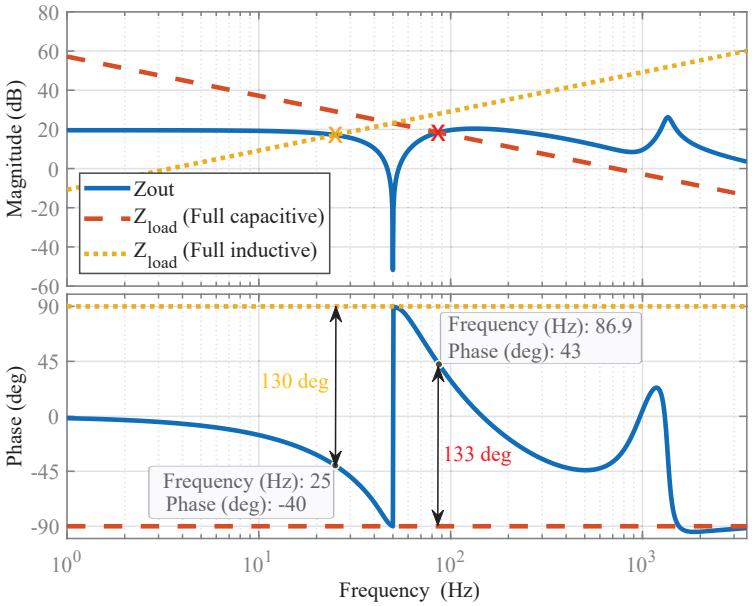

Figure 13. Bode plot of the output impedance of the VSC, along with Bode plots for 1 p.u. inductive and capacitive loads. Crosses indicate intersection points.

Now, an alternative scenario is explored, in which a parallel ideal resonant regulator, centered at the fifth harmonic frequency, is connected in parallel with the PR controller ($G_{\mathrm{PR1}}(s)$) in the voltage control loop in Figure 3. This parallel resonant regulator functions as a harmonic compensator, effectively reducing the THD of the VSC output voltage when powering nonlinear loads. In this case, the Bode plot of the output impedance of the VSC will be as shown in Figure 14. Regarding the inductive load, the situation closely resembles that depicted in Figure 13, suggesting that the incorporation of the fifth harmonic resonant regulator does not affect the VSC stability with a 1 p.u. inductive load. However, with a capacitive load, the dynamics change; we identify three intersection points, with phase differences of 131.1°, 34°, and 189°. Importantly, the phase difference at the third intersection point surpasses 180°, indicating a negative PM and, thus, instability for the VSC when connected to a 1 p.u. capacitive load.

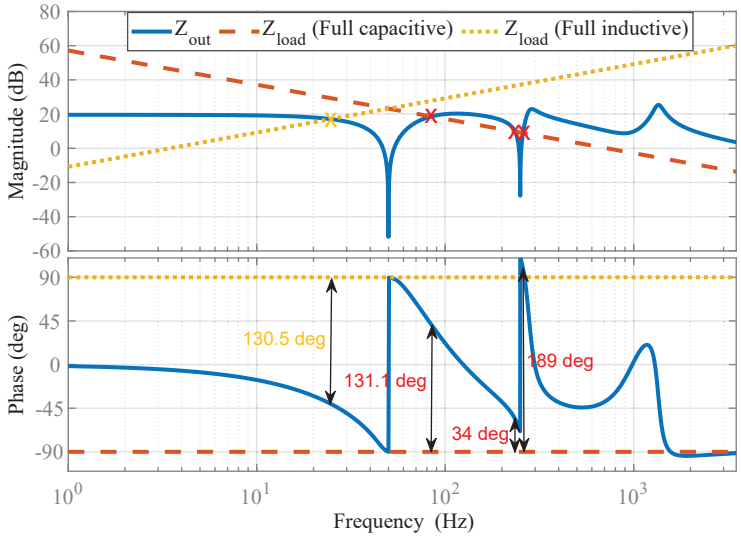

Figure 14. Bode plot depicting the output impedance of the VSC, which includes a fifth-harmonic resonant regulator in its voltage control loop, alongside the Bode plots for 1 p.u. inductive and capacitive loads.

To confirm the aforementioned observation, a 1 p.u. (250 Mvar) capacitive load is connected to the VSC. Initially, the VSC begins to supply power to the load without the fifth Harmonic Resonant Regulator (5th HRR). At a certain point, this harmonic resonant regulator is activated, and after a brief period, it is deactivated. As shown in Figure 15, the activation of the 5th HRR destabilizes the VSC. It is also observed that the VSC regains stability after its deactivation. The above observations confirm the theoretical predictions, which are based on the obtained small-signal model for the VSC. These observations directly validate the model's accuracy and reliability. The validity of the model can also be demonstrated in a similar manner for the case of an inductive load, but to save space, detailed results are not presented.

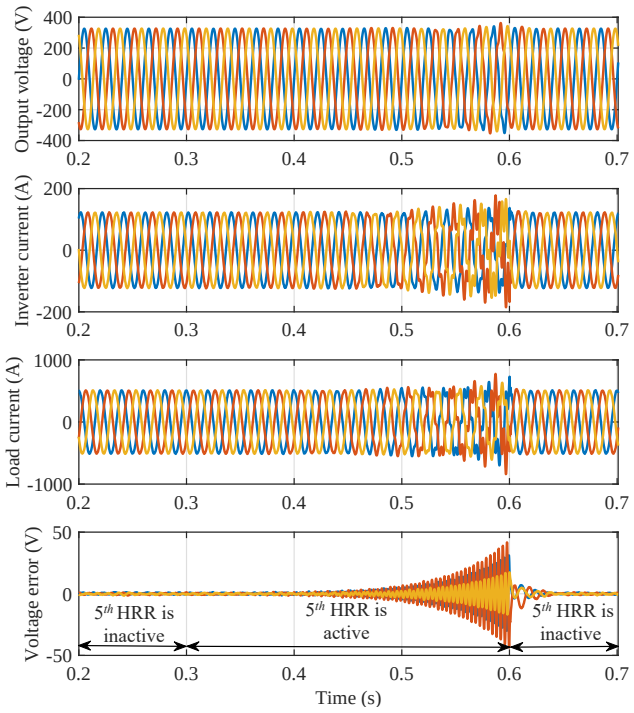

Figure 15. Dynamic response of VSC supplying a 1 p.u. (250 Mvar) capacitive load, illustrating the impact of the fifth harmonic resonant regulator (5th HRR).

Now, the converter performance when supplying a diode bridge rectifier load is investigated. For this test, a full-bridge rectifier load (R = 1.5 Ω and C = 2 mF) is used. As demonstrated earlier, an ideal 5th HRR can result in instability. Therefore, a damped 5th HRR is used in the converter control system hereafter. This ensures that the converter output voltage THD remains low under nonlinear load conditions and that the converter output impedance around the fifth harmonic frequency remains passive. The obtained simulation results are shown in Figure 16, and the converter output voltage spectrum and THD is illustrated in Figure 17. Despite the high harmonic content of the load (around 37%), the output voltage maintains a low harmonic content of around 4%, which confirms the effectiveness of the converter when supplying nonlinear loads.

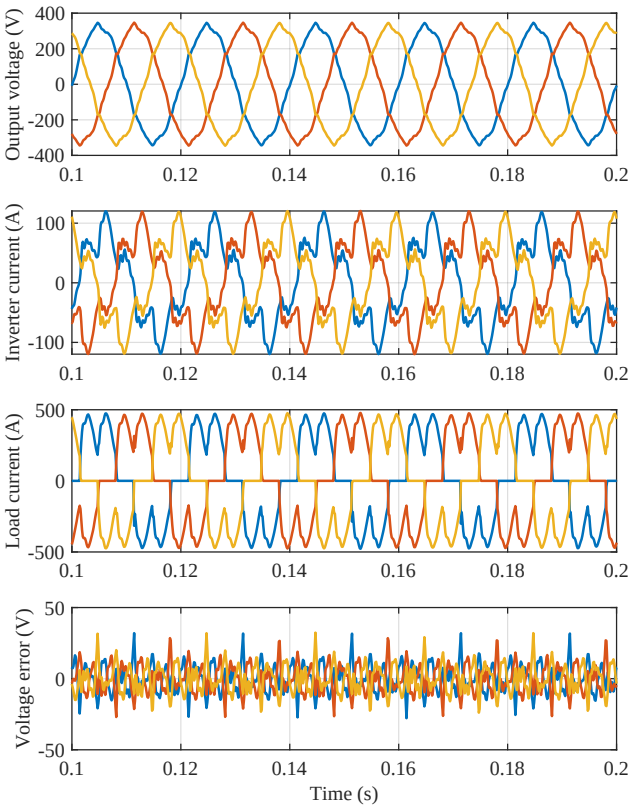

Figure 16. Simulation results illustrating the response of the converter when supplying a full-bridge rectifier load (R = 1.5 Ω and C = 2 mF).

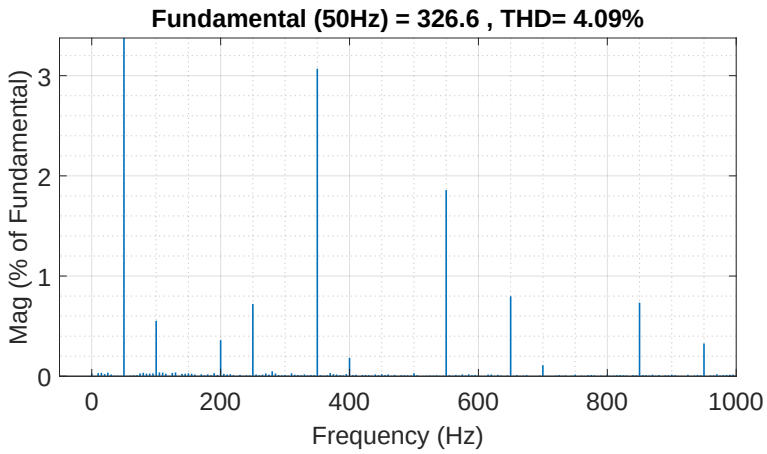

Figure 17. Output voltage spectrum and THD of the converter when supplying a full-bridge rectifier load (R = 1.5 Ω and C = 2 mF).

6. C-HIL Verification

To validate the control strategies developed for the grid-forming VSC shown in Figure 3, the C-HIL test results are presented in this section. This involves examining the system's response to load and reference changes, unbalanced loading conditions, and its ability to maintain stability under various scenarios. The VSC system and its control parameters are detailed in Tables 1 and 2, respectively. First, a description of the C-HIL setup is provided, followed by the presentation of the C-HIL test results.

Table 2. Control parameters.

Description	Value
Current control loop's proportional gain, k_{pc}	4.79
Current control loop's resonant gain, k_{rc}	392
Voltage control loop's proportional gain, k_{pv}	1
Voltage control loop's resonant gain, k_{rv}	1000
Voltage feedforward loop gain, k_{ff}	0.7

6.1. C-HIL Setup

As shown in Figure 18, the C-HIL setup is built using a Typhoon HIL604, which has eight processing cores and a 500 ns update rate. The plant is divided into two sections, the power switches go to one of the HILs cores, while the passive elements (transformer, capacitors, and load) go to the other core. The control feedback signals (inverter current, capacitor voltage, etc.) are sent out of the HIL by the 16-bit DAC, which can generate signals in the range of ±10 V up to 1 MSPS. In this C-HIL configuration, the outputs of the HIL DAC are limited to 0 to 3.0 V to ensure that the ADC of the DSP can measure them properly.

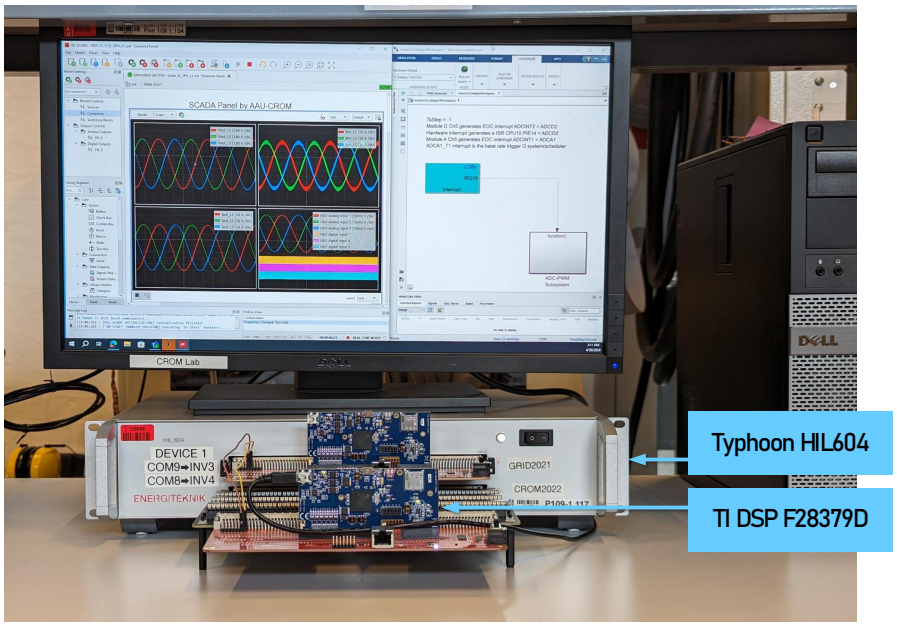

Figure 18. C-HIL setup.

The controller is deployed to a Texas Instrument DSP F28379D using code generation (C2000 Microcontroller Blockset on Matlab Simulink). The DSP runs at 200 MHz and is configured to switch and sample synchronously at 7 kHz. This means that each time the ePWM counter reaches its maximum count, the ePWM1 module triggers a Start of Conversation (SoC) interrupt in one of the ADC blocks. Once the ADC conversion is finalized, the End of Conversion (EoC) interrupt is triggered, and the controller subsystem is executed. To operate the converter, three ePWM modules are needed, where each module

can generate two PWM signals, ePWMA and ePWMB, which are configured to drive the upper and lower switches of one of the converter's three legs. The deadband unit of the three ePWM is set to generate a 10 µs deadtime to avoid short-circuiting the input power supply. Finally, the PWMs are sampled by the HIL ADCs at a 50 MHz rate, which allows testing the controller with high fidelity.

6.2. Transition Dynamics: No-Load to Full-Load

Operating under a no-load condition can pose a challenge for converter control, as the resistive element of the load typically contributes to the passive damping of the LC filter. To ensure that the VSC control system provides sufficient damping in scenarios where natural load damping is missing, testing under no-load conditions, and transitioning between no-load to full-load (250 kW) states is necessary.

Figure 19 presents the results, showing that the output voltage total harmonic distortion (THD) remains low under both no-load and full-load conditions, at 2% and 1.7%, respectively. Furthermore, the VSC exhibits an excellent dynamic response, with the tracking error converging to zero in fewer than two cycles of the fundamental frequency.

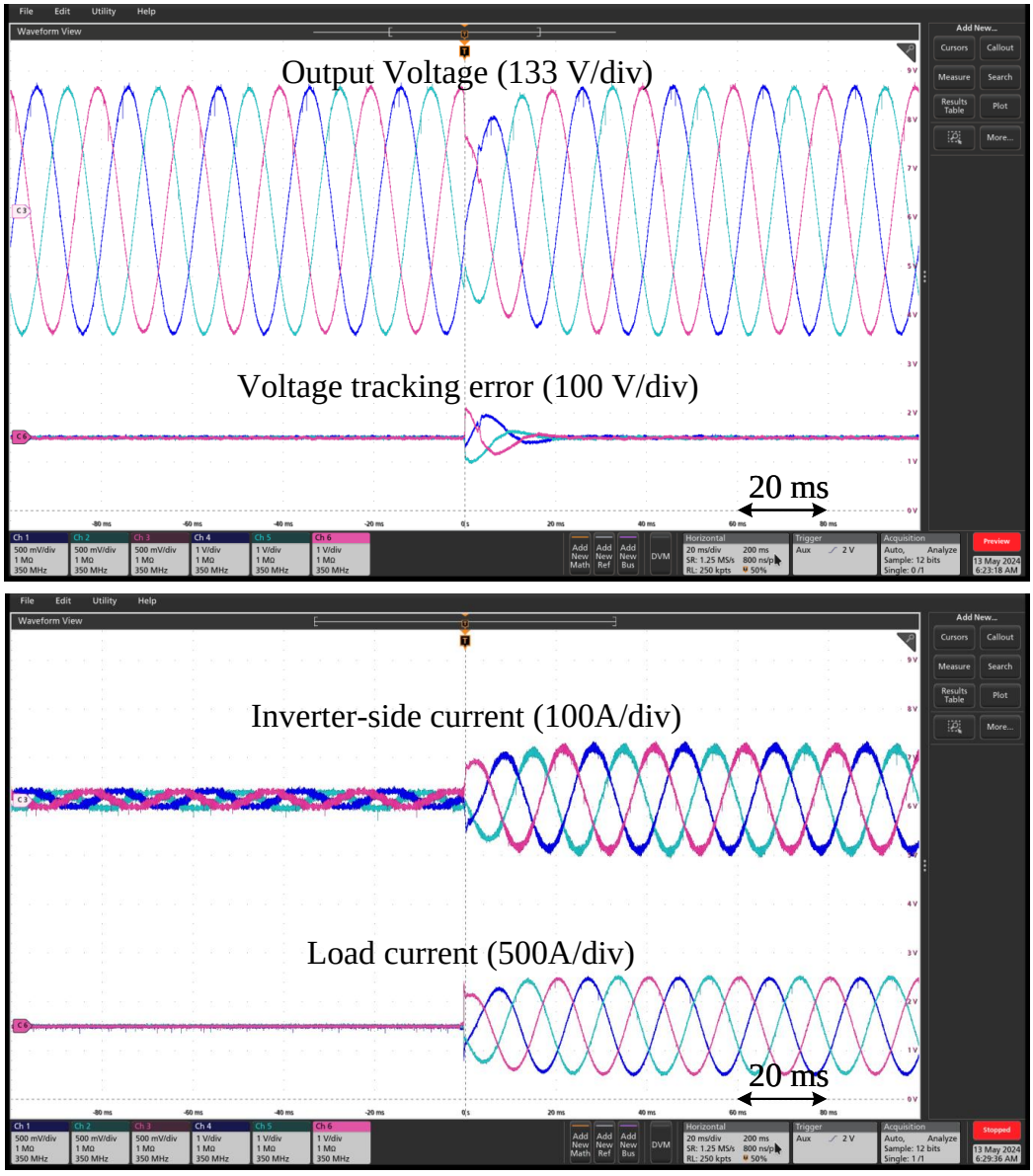

Figure 19. C-HIL test results demonstrating the efficacy of the VSC control system under no-load conditions and during transition from no-load to full-load states.

6.3. Unbalanced Load Conditions

The unbalanced load test for a three-phase grid-forming VSC is essential, as it reflects real-world scenarios where loads are not uniformly distributed across phases. For this purpose, a full load (0.64 Ω) is connected to phase A, while phases B and C carry no load. It is important to note that the Wye point neutral in the transformer's secondary winding serves as a connection point for single-phase loads on the secondary side. The outcomes of this test are presented in Figure 20. Remarkably, the output voltage remains perfectly balanced, and the voltage tracking error is zero, even under such an extremely unbalanced loading condition.

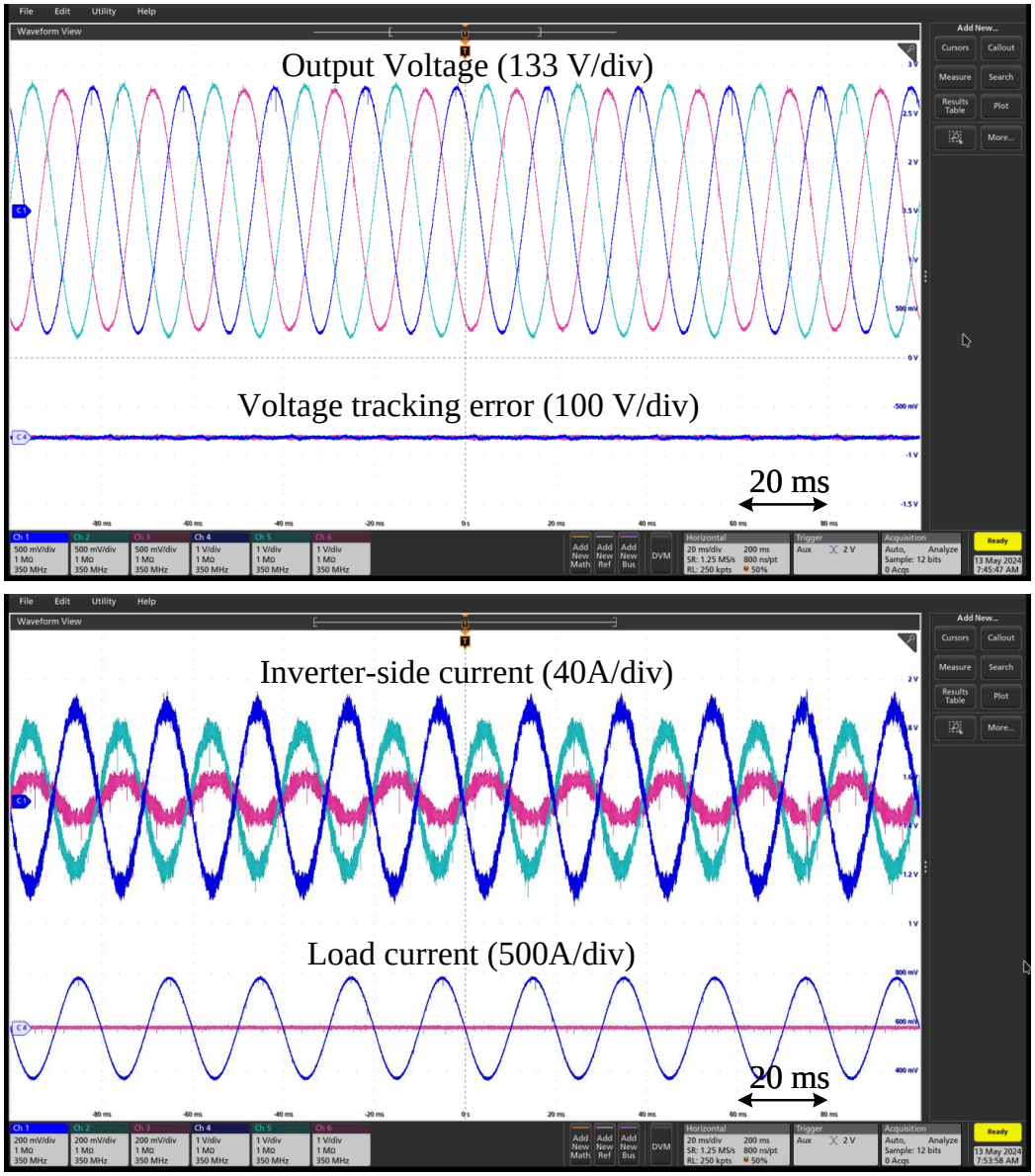

Figure 20. C-HIL test results illustrating the performance of the VSC under an unbalanced load condition.

6.4. Response to Step Change in Reference Voltage Amplitude

In real-world applications, the reference signal for a grid-forming VSC is dynamic and adjusted by sophisticated control loops to achieve specific objectives such as power sharing, power quality enhancement, and optimization. It is crucial, therefore, that the grid-forming VSC demonstrates a robust ability to accurately track changes in its reference voltage. This section is designed to explore this aspect. For this purpose, a deliberate and sudden reduction in the reference voltage amplitude from 400 V (line-to-line RMS) to 320 V

(line-to-line RMS) is implemented to assess the VSC response and tracking accuracy. This test is carried out under a full-load condition. The findings of this test are depicted in Figure 21. Observations indicate that the VSC adeptly follows the altered reference signal, with the voltage tracking error returning to zero in around two cycles, showcasing its rapid and effective response.

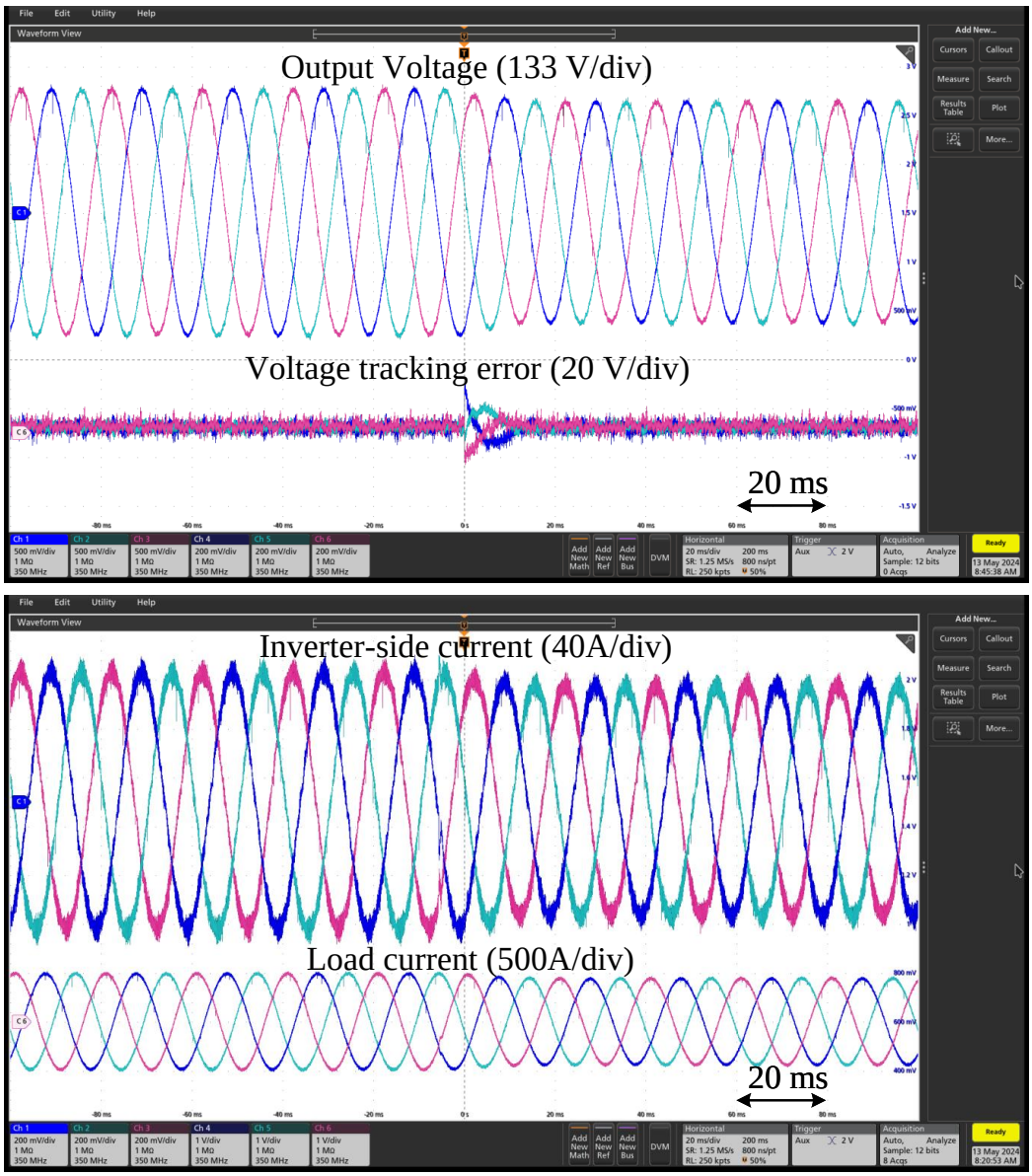

Figure 21. C-HIL test results illustrating the dynamic response of the grid-forming VSC to a controlled step change in the reference voltage amplitude.

7. Discussion and Conclusions

This study has contributed to addressing the complex modeling and control challenges associated with grid-forming VSCs equipped with an MVDC supply and a step-down transformer at their output. The complexity arises from the necessity of dual-sided feedback control—that is, incorporating feedback signals from both the secondary and primary sides of the transformer for effective converter control. This requirement introduces transformation matrices into the converter control process, thereby increasing the complexity of small-signal modeling and control tuning.

The study focused on an $\alpha\beta$ frame grid-forming controller, incorporating an intermediate voltage control loop, an inner current loop, a voltage feedforward loop, and the transfor-

mation matrices $T_{v,\alpha\beta}$ and $T_{i,\alpha\beta}$. These matrices convert the transformer's secondary-side voltage and current signals to their primary counterparts in the control process. Initially, it was briefly demonstrated how these transformation matrices can be determined based on the transformer's vector group and turn ratio. Subsequently, the study illustrated how to obtain an equivalent primary-side representation of the VSC system with a transformer, derive its average model, connect this average model to the control system, and simplify it with some mathematical manipulations to produce a standard-form small-signal model.

The study's investigation into the impact of control frame selection on the VSC small-signal model represents another contribution. It revealed that choosing between $\alpha\beta$ and dq control frames does not compromise the model's validity as long as appropriate adjustments are made to the system's regulators. This discovery expands the model's applicability, ensuring its relevance across various control frameworks. Moreover, the study demonstrated that changes in the transformer's vector group do not affect the small-signal model.

The article also provided detailed step-by-step guidelines for tuning the gains of PR regulators and the voltage feedforward gain within the system's control loops. This considerably simplifies the VSC control design and offers a clear direction for optimizing VSC performance.

Then, extensive simulation and C-HIL tests, along with theoretical investigations, were conducted. These studies not only validated the theoretical model but also confirmed the efficacy of the derived control design principles under a range of operational conditions, including load changes and unbalanced loading scenarios. Specifically, it was shown that the VSC maintained a low THD of 2% at no load, 1.7% at full resistive load, and around 4% under a highly nonlinear load. It exhibited excellent dynamic response, with tracking errors converging to zero in fewer than two cycles, even under extreme load conditions and step changes in reference voltage.

In conclusion, this paper addresses a research gap in the existing literature and contributes to future research in the domain of grid-forming VSCs through the methodologies and insights developed in this study.

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