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ORIGINAL RESEARCH

Interleaved ZVS DC-DC converter with ultrahigh step-down and flexible gain

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Abstract

This paper proposes a novel non-isolated ultrahigh step-down interleaved DC-DC converter with an extremely extended duty cycle based on the series capacitor and coupled-inductor techniques. The proposed converter utilizes a three-winding coupled inductor (TWCI) to enhance the step-down conversion ratio. In contrast to conventional coupled inductor-based step-down converters, its voltage gain improves as the turn ratio approaches unity. Consequently, coupled inductors have significantly lower winding losses. Furthermore, there is no extra constraint on the turn ratio of the TWCI. It results in a highly flexible voltage gain and more design freedom. Other advantages of the employed series capacitor and coupled inductor techniques can be listed as, zero voltage switching (ZVS) condition for all switches, significant reduction of the total switching device power (SDP) and recovery of the energy of leakage inductors. They all reduce power losses and costs. Steady-state analysis, derivation of voltage gain and design considerations are discussed in detail. Finally, a 200 W, 400-to-12 V experimental prototype is implemented to verify the effectiveness and feasibility of the proposed converter.

1 | INTRODUCTION

Nowadays high step-down DC-DC converters are widely used in a variety of industrial applications, such as battery chargers, electric vehicles, uninterruptable power supplies (UPSs), light emitting diode (LED) lamps, telecommunication systems and voltage regulator modules (VRMs) for digital processors [1–3]. When isolation is not required, and cost, volume and loss are the deciding factors, non-isolated structures are preferred [4]. Interleaved buck converters (IBCs) are widely used for non-isolated step-down conversion because they have a simple structure, low current ripple, simple control and low current stresses [5–9]. Despite these, semiconductors are highly stressed by blocking the input voltage. Also, at high conversion ratios, the duty cycle decreases dramatically, resulting in high power losses and control complexity.

To overcome the aforementioned drawbacks of IBCs, various improved topologies have been introduced in the literature. With tapped-inductor (TI) buck converters, improved voltage gain and extended duty cycle can be achieved [10] and [11]. TI buck converters show a voltage spike across the main switch because of the leakage inductance of the coupled inductor. As a step forward, the TI buck converter with a lossless clamped circuit is presented in [12]. Although it recovers the stored energy of the leakage inductor and limits the spike voltage, this converter operates under hard switching and the voltage gain is limited. By adding only one capacitor to IBCs, the interleaved series-capacitor buck (ISC-buck) converter improves the voltage gain to half of the conventional IBC [5]. In addition, this converter reduces the voltage stress across the switches to half of the input voltage. Also, owing to the ampere-second balance principle on the series capacitor, automatic current balancing is achieved. Therefore, the converter efficiency is improved. This idea is utilized in [8, 13] and [14]. In these converters, the voltage conversion ratios are one-third and one-fourth of the IBC. However, the number of elements has been increased, switches commutate under hard conditions and the problem of extremely narrow duty cycles in high step-down applications remains unsolved. By combining the coupled-inductor and the series capacitor techniques, the high step-down converters can extend the duty cycle and eliminate the spike voltage issue [15–20]. The converter in [15] operates under hard

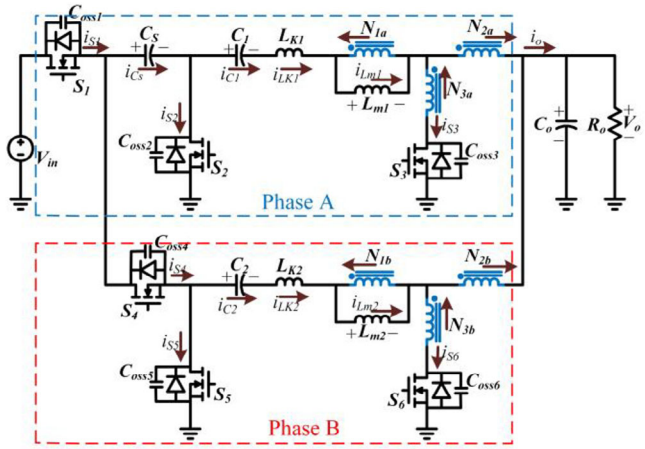

FIGURE 1 Proposed ultrahigh step-down converter.

switching conditions and there is no common ground between the input and the output. The converter in [16] provides ZVS conditions for all switches, but a high number of magnetic cores and semiconductors are utilized, increasing the cost and volume. Moreover, the converters in [17] and [18] can achieve an ultrahigh-step-down gain at the price of high power losses and a high number of components. In addition, the three-winding coupled inductor (TWCI) in [18] must be designed to have equal turn ratios. The converters in [19] and [20], are also proposed to offer high voltage gain, soft-switching operation and simple topology and control. By increasing the turn ratio of the coupled inductor, these converters improve the voltage conversion ratio at the cost of efficiency.

This paper proposes a novel highly efficient interleaved ultrahigh step-down converter. This converter combines the advantages of both the buck converters based on series capacitors and the TI. As the prominent feature of the proposed converter, its voltage gain is improved by moving the turn ratio of the coupled inductor towards unity (trans-inverse). Interestingly, the magnetizing current average value at high voltage gains with a near unity turn ratio is almost zero. In addition, compared to other converters, the two turn ratios of the TWCI can be chosen arbitrarily. In other words, it is not necessary to have equal turn ratios. It provides two benefits. Firstly, additional design freedom to extend the voltage gain and more converter flexibility. Secondly, the easier implementation of the converter than the competitors. Also, the proposed converter offers lower SDPs. It indicates the lower price and losses of the semiconductors. The aforementioned features along with the ZVS operation and recovered energy of the leakage inductance result in a high efficiency and power density of the proposed converter. All of these advantages are experimentally proved through extensive tests on a 200 W, 400-to-12 V laboratory setup.

2 | OPERATION PRINCIPLES

The structure of the proposed converter is shown in Figure 1. The circuit consists of six switches (S_1–S_6), three energy transfer capacitors C_1, C_2 and C_S, and an output filter capacitor C_o. Also, each phase employs a set of TWCI to achieve a trans-inverse ultrahigh step-down conversion. The coupled inductors are modelled as ideal transformers with leakage and magnetizing inductances, L_K and L_m, reflected on the primary side. To simplify the steady-state analysis of the proposed converter, the following assumptions are considered; the converter operates in continuous conduction mode (CCM); except for the parasitic capacitance across the switches, all semiconductors are ideal; both coupled inductors have the same parameters; all the capacitors and magnetizing inductors are large enough to be considered as a voltage and a current source, respectively. The key waveforms of the proposed converter are plotted in Figure 2. The two-phase series capacitor buck converter works interleaved. In this way, each phase works similarly to the other, so, only the second phase operation is analysed. Also, based on the operation concept of the series capacitor converter, capacitor C_S acts as an energy-transfer capacitor as well as a voltage source for phase B. The operation over one sampling period consists of nine distinct modes as illustrated in Figure 3.

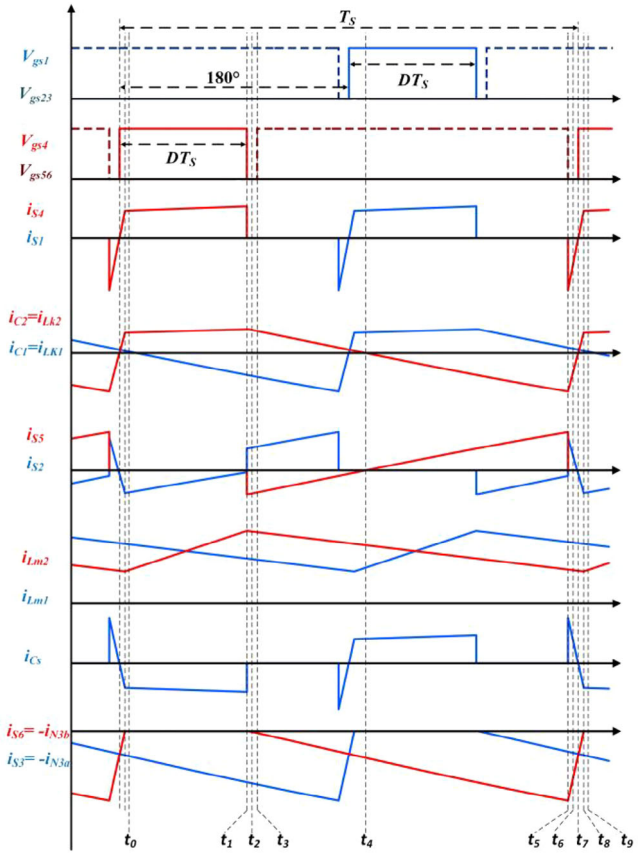

FIGURE 2 Key theoretical waveforms of the proposed converter.

Mode 1 [t_0–t_1]: During this mode, S_4 conducts while S_5 and S_6 are off, as depicted in Figure 3a. Hence, no current flows through the tertiary winding. During this mode, capacitor C_S charges capacitor C_2. In addition, voltages across L_{m2} and L_{K2} are positive, so the magnetizing

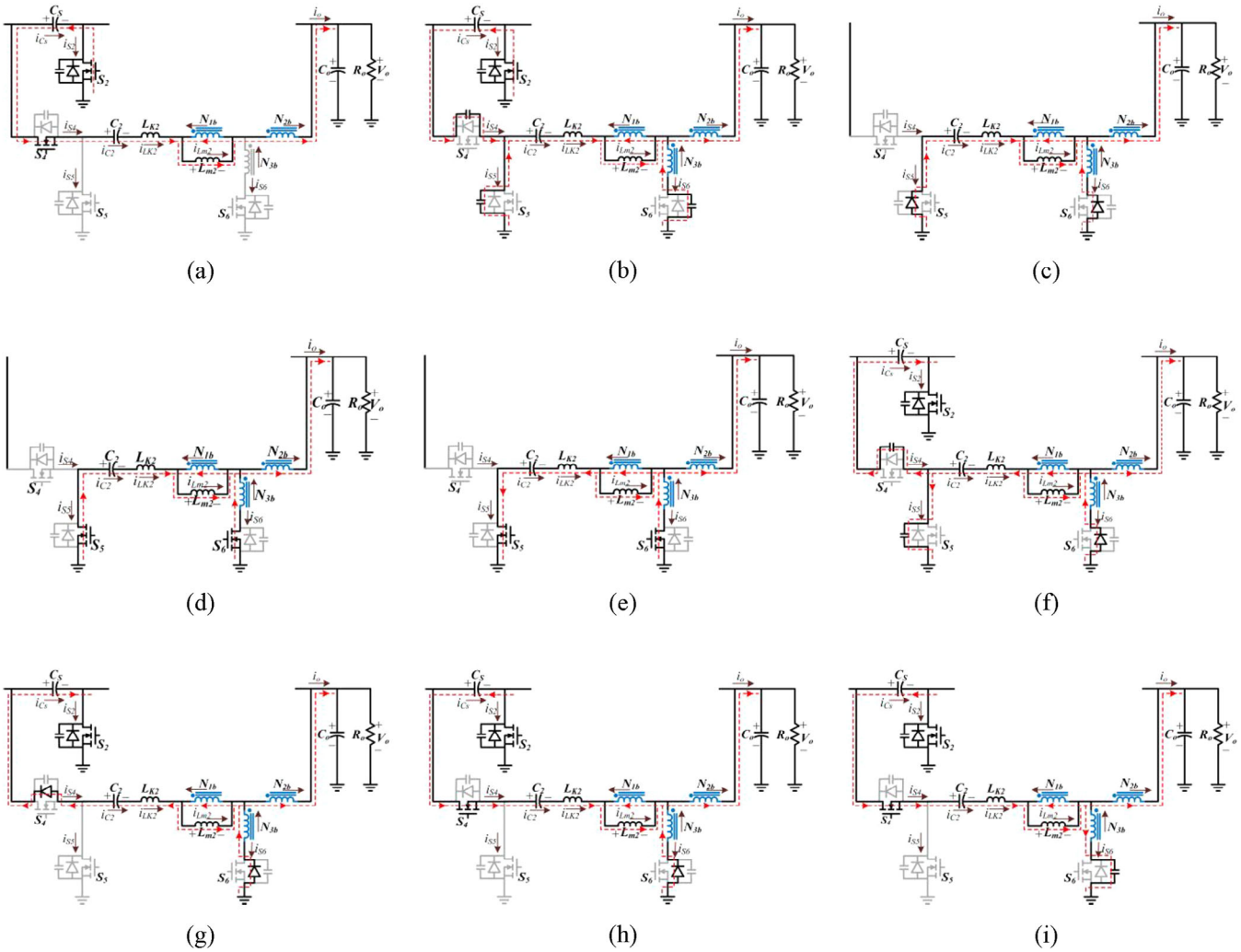

FIGURE 3 Equivalent circuits at modes: (a) 1, (b) 2, (c) 3, (d) 4, (e) 5, (f) 6, (g) 7, (h) 8 and (i) 9.

current i_{Lm2} and leakage inductor current i_{Lk2} increase linearly.

Mode 2 [t_1–t_2]: At t_1, S_4 is turned off, S_5 and S_6 are still off, as shown in Figure 3b. The parasitic capacitor C_{oss4} of S_4 begins to charge while C_{oss5} and C_{oss6} start to discharge.

Mode 3 [t_2–t_3]: As depicted in Figure 3c, when C_{oss5} and C_{oss6} completely discharge, the body diodes of S_5 and S_6 are forward-biased and conduct to provide a free-wheeling path for the current of leakage inductances. Therefore, i_{N3} increases from zero. Negative voltages drop across L_{m2} and L_{K2}, demagnetizing L_{m2} and L_{K2}. So, i_{Lm2} and i_{LK2} decrease. This mode ends by turning on S_5 and S_6 at t_3.

Mode 4 [t_3–t_4]: Due to the conduction of body diodes of S_5 and S_6 from the previous interval, they turn on under the ZVS condition. Moreover, S_4 is still off and the status of C_2, i_{Lm2} and i_{Lk2} are still the same as in the previous mode. This mode ends when i_{Lk2} reaches zero.

Mode 5 [t_4–t_5]: As illustrated in Figure 3e, at t_4, i_{Lk2} changes direction. During this mode, S_4 is still off while S_5 and S_6 conduct. Accordingly, the energy stored in C_2 transfers to the load through the coupled inductor. During this interval, L_{m2} still demagnetizes. In addition, at the end of this mode S_5 and S_6 are turned off.

Mode 6 [t_5–t_6]: At the beginning of this interval, S_5 and S_6 are turned off and S_4 is still off. During this interval, C_{oss4} discharges and C_{oss5} charges. Also, due to the continuity of current in the coupled inductor, the body diode of S_6 starts to conduct and i_{S6} decreases.

Mode 7 [t_6–t_7]: During this mode, when the parasitic capacitor C_{oss4} is fully discharged, the body diode of S_4 is forward-biased and conducts, as shown in Figure 3g. The current of L_{K2} decreases to zero. As i_{Lk2} is smaller than i_{N2b}, the body diode of S_6 still conducts and L_{m2} demagnetizes. This mode ends when i_{Lk2} crosses zero and S_4 turns on under the ZVS condition.

Mode 8 [t_7–t_8]: As depicted in Figure 3h, S_5 and S_6 are blocking, and due to the conduction of the body diode of S_4, it turns on under the ZVS condition. The capacitor C_S charges C_2. Also, a positive voltage drops across L_{K2}, which increases i_{Lk2}. In addition, similar to mode 7, i_{Lk2} is smaller than i_{N2} and the body diode of S_6 still

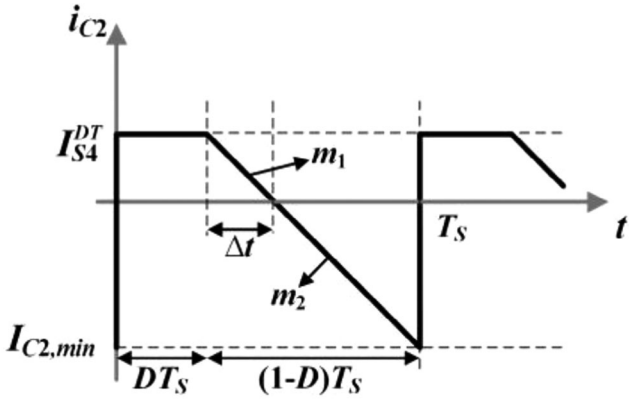

FIGURE 4 Current waveform of the capacitors C_1 and C_2.

conducts and L_{m2} demagnetizes. This mode ends when i_{S6} reaches zero at t_8.

Mode 9 [t_8–t_9]: As shown in Figure 3i, at t_8, i_{S6} becomes zero. The parasitic capacitor C_{oss6} is charged while the voltage of the magnetizing inductor L_{m2} is positive. So, the magnetizing current i_{Lm2} increases linearly. This mode ends when C_{oss6} is completely charged, initiating the converter's next switching transition.

The operation of phase A of the proposed converter is similar to phase B, except that when switch S_4 is turned on, both phases' currents flow through switch S_2, as shown in Figure 2.

3 | STEADY-STATE ANALYSIS

3.1 | Energy-transferring capacitor voltage

The steady-state analysis considers only the first, fourth and fifth modes, while other modes can be ignored because they occur at very small intervals. The turn ratios are defined as $n_{12} = N_1/N_2$ and $n_{32} = N_3/N_2$. The simplified current waveform of C_2 is shown in Figure 4. Assuming the magnetic inductance current is constant when S_4 is on, then I_{C2} is almost constant. By assuming $P_{in} = P_{out}$, average currents of S_1 and S_4 during the conduction interval are equal to:

$$I_{S1}^{DT} = I_{S4}^{DT} = \frac{V_o I_o}{V_{in} D} \tag{1}$$

Current slopes during the time interval $(1-D)T_s$, that is, the time duration of modes 4 and 5, can be calculated from Figure 4 as:

$$m_1 = \frac{0 - I_{S4}^{DT}}{\Delta t} \tag{2}$$

$$m_2 = \frac{I_{c,min} - 0}{(1-D)\,T_s - \Delta t} \tag{3}$$

During the time interval (t_2–t_6), by using KVL and considering constant voltage across leakage inductor L_{K2}, the following equations can be obtained:

$$i_{C_2} = i_{L_{K2}} = \frac{1}{L_{K2}} \int_0^t V_{L_{K2}}\, dt \tag{4}$$

$$m_1 = \frac{V_{L_{K2}}}{L_{K2}} = \frac{-V_{C2} + \frac{n_{12}+n_{32}}{1-n_{32}} V_o}{L_{K2}} \tag{5}$$

$$m_2 = \frac{V_{L_{K2}}}{L_{K2}} = \frac{\left(-V_{C2} + \frac{n_{12}+n_{32}}{1-n_{32}} V_o\right)}{L_{K2}} \tag{6}$$

From (2) and (5), the time interval Δt can be calculated as:

$$\Delta t = \frac{-L_{K2}\, I_{S4}^{DT}}{-V_{C2} + \frac{n_{12}+n_{32}}{1-n_{32}} V_o} \tag{7}$$

Also, from (3), (6) and (7) the minimum current of C_2 is:

$$\left|I_{C2,min}\right| = \frac{((1-D)\,T_s - \Delta t)\,\frac{L_{K2}\, I_{S4}^{DT}}{\Delta t}}{L_{K2}}. \tag{8}$$

From Figure 4 and by applying the ampere-second balance law to C_2, the following equation can be obtained:

$$\frac{(DT_s + DT_s + \Delta t)\, I_{S4}^{DT}}{2} = \frac{((1-D)\,T_s - \Delta t)}{2} \left|I_{C2,min}\right| \tag{9}$$

Then, by substituting (8) into (9), Δt can be calculated as:

$$\Delta t = \frac{(1-D)^2}{2}\, T_s \tag{10}$$

From (7) and (10), V_{C2} is obtained as:

$$V_{C2} = \frac{n_{12} + n_{32}}{1 - n_{32}}\, V_o + \frac{2L_{K2}\, I_{S4}^{DT}}{(1-D)^2 T_s} \tag{11}$$

and because of the similarity of phases:

$$V_{C1} = V_{C2} \tag{12}$$

3.2 | DC voltage ratio

According to Figure 3a, S_4 conducts during DT_S. The series capacitor buck converter operates at a steady state with an average voltage on C_S half the input. For this time interval, the following equation can be obtained:

$$V_{L_{m2}}\Big|_{DT_s} = \left(\frac{V_{in}}{2} - V_{C2} - V_{Lk_2}\Big|_{DT_s} - V_o\right) \frac{n_{12}}{1 + n_{12}} \tag{13}$$

and for modes 4 and 5:

$$V_{Lm2}|_{(1-D)T_s} = \frac{n_{12}}{1 - n_{32}}\ (-V_o) \tag{14}$$

$$V_{Lk2}|_{(1-D)T_s} = -V_{C2} - \frac{n_{12} + n_{32}}{n_{12}}\, V_{Lm2}|_{(1-D)T_s} \tag{15}$$

therefore

$$V_{Lk2}|_{(1-D)T_s} = -V_{C2} + \frac{n_{12}+n_{32}}{1-n_{32}}V_o \tag{16}$$

By applying the volt–second balance to L_{K2} over one switching period and using (16), the following equation can be obtained:

$$V_{L_{K2}}D + (1-D)\left(-V_{C2} + \frac{n_{12}+n_{32}}{1-n_{32}}V_o\right) = 0 \tag{17}$$

which gives

$$V_{L_{K2}}\Big|_{DT_s} = \frac{(1-D)}{D}\left(V_{C2} - \frac{n_{12}+n_{32}}{1-n_{32}}V_o\right) \tag{18}$$

Substituting (18) into (13) and considering (14), the volt-second balance equation for L_{m2} results in:

$$\frac{n_{12}}{1+n_{12}}\left(\frac{V_{in}}{2} - V_{C2} - V_{L_{K2}} - V_o\right)D + (1-D)\frac{n_{12}}{1-n_{32}}(-V_o) = 0 \tag{19}$$

Finally, substituting (11) and (18) into (19) and assuming $L_{K1} = L_{K2} = L_K$, the steady-state voltage gain of the proposed converter is calculated as:

$$\frac{V_o}{V_{in}} = \frac{D(1-n_{32})}{2\left((1+n_{12}) + \alpha L_K(1-n_{32})\right)} \tag{20}$$

where

$$\alpha = \frac{2I_o}{(1-D)^2 V_{in} D T_s} \tag{21}$$

If the leakage inductance is negligible, the gain equation simplifies to:

$$\frac{V_o}{V_{in}} = \frac{D}{2} \times \frac{(1-n_{32})}{(1+n_{12})} \tag{22}$$

According to (22), by adjusting the duty cycle and the turn ratios of the coupled inductors (n_{12} and n_{32}), this converter is very flexible to buck the input voltage over a wide range. In converters based on TWCIs such as [18, 21], and [22], the turn ratios must be chosen the same to ensure the stable performance of the converter. It is possible to arbitrarily select the two turn ratios of the proposed converter, which gives it three degrees of freedom in terms of voltage gain. Besides offering more design freedom, it is also easier to implement this converter than its competitors. Figure 5 depicts voltage gain versus n_{32} for different values of n_{12} at a constant duty cycle of $D = 0.35$. It can be seen that voltage gain decreases drastically as n_{32} approaches unity. Also, by increasing n_{12} the voltage gain decreases. The voltage gain is more sensitive to n_{32} than n_{12}.

One of the prominent features of the proposed converter is the sub-unity turn ratio of n_{32}. Indeed, unlike other similar converters based on coupled inductors, the ultra-step-down voltage gain of the proposed converter can be achieved as the turn ratio approaches unity leading to a significant reduction of ohmic power losses.

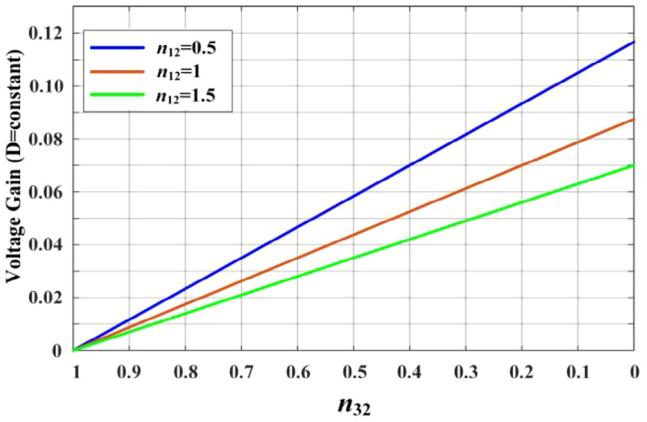

FIGURE 5 Voltage gain of the proposed converter versus n_{32} for different values of n_{12} at a constant duty cycle ($D = 0.35$).

3.3 | Automatic current balancing

The proposed converter offers automatic current balancing between the two phases, which is demonstrated here. First, the ampere-second balance law is applied to the series capacitor C_S. It charges and discharges during the conduction of S_1 and S_4, respectively. For the charge operation ($D_1 T_S$), the following equations can be obtained:

$$\begin{cases} i_{Cs}|_{D_1T_s} = i_{N2a} \\ i_{Lm1} = i_{N1a} + i_{Cs} \\ i_{N1a} = \frac{1}{n_{12}}i_{N2a} - \frac{n_{32}}{n_{12}}i_{N3a} \end{cases} \tag{23}$$

Also, during this time interval, i_{N3a} is zero, so:

$$i_{C_S}\Big|_{D_1T_s} = \frac{n_{12}}{1+n_{12}}i_{Lm1} \tag{24}$$

In the same way, during the discharge interval ($D_2 T_S$):

$$\begin{cases} i_{Cs}|_{D_2T_s} = -i_{N2b} \\ i_{Lm2} = i_{N1b} - i_{Cs} \\ i_{N1b} = \frac{1}{n_{12}}i_{N2b} - \frac{n_{32}}{n_{12}}i_{N3b} \end{cases} \tag{25}$$

Similarly, i_{N3b} is zero, so:

$$i_{C_S}\Big|_{D_2T_s} = \frac{-n_{12}}{1+n_{12}}i_{Lm2} \tag{26}$$

The ampere-second balance equation then gives:

$$\frac{n_{12}}{1+n_{12}}i_{Lm1}(D_1T_S) + \frac{-n_{12}}{1+n_{12}}i_{Lm2}(D_2T_S) = 0 \tag{27}$$

since $D_1 = D_2 = D$, therefore:

$$i_{Lm1} = i_{Lm2} \tag{28}$$

The proposed converter balances the currents automatically.

3.4 | Voltage and current stress

The voltage stresses on switches are:

$$\begin{cases} V_{ds1} = V_{ds2} = V_{ds5} = \frac{V_{in}}{2} \\ V_{ds4} = V_{in}\,,\ \frac{V_{in}}{2} \\ V_{ds3} = V_{ds6} = \frac{1-n_{32}}{1+n_{12}}\ \frac{V_{in}}{2} \end{cases} \tag{29}$$

The maximum voltage stress across the switch S_4 can be obtained by applying the KVL principle at modes 4 and 5. When the main switch of the first phase is on, the voltage across S_4 is the input voltage, but when S_1 is off, the voltage stress on S_4 is equal to V_{Cs}, which is half the input voltage.

As Equation (29) represents, for less-than-unity turn ratios the voltage stress on the synchronously rectified (SR) switches is less than one-twelfth of the input voltage, allowing the converter to use lower voltage components.

By assuming that $P_{in} = P_{out}$, the peak currents are calculated as:

$$\begin{cases} \mathrm{I}_{\mathrm{S1}}^{\max} = \mathrm{I}_{\mathrm{S4}}^{\max} = \frac{\mathrm{I_o}(1-\mathrm{n_{32}})}{2(1+\mathrm{n_{12}})} \\ \left|\mathrm{I}_{\mathrm{S2}}^{\max}\right| = \mathrm{I}_{\mathrm{S5}}^{\max} = \frac{((1-\mathrm{D})\mathrm{T_s}-\Delta\mathrm{t})\frac{\mathrm{L_K}\ \mathrm{I}_{\mathrm{S4}}^{\mathrm{DT}}}{\Delta\mathrm{t}}}{\mathrm{L_K}} \\ \mathrm{I}_{\mathrm{S3}}^{\max} = \mathrm{I}_{\mathrm{S6}}^{\max} = \frac{\mathrm{I_o}}{1-\mathrm{D}} \end{cases} \tag{30}$$

3.5 | ZVS condition

In the proposed converter, switch pairs S_2, S_3 and S_5, S_6 are synchronous rectifier switches for freewheeling operation. This behaviour is like the low-side switch of the conventional SR buck converter, which turns on under ZVS conditions. For other switches, ZVS condition is constrained by the following factors:

1. Leakage inductors must have enough energy to charge and discharge the output capacitors of switches;
2. Adequate blanking or dead time must be inserted between gate signals to allow the charge and discharge of the output capacitors.

3.6 | Derivation of small-signal model

Due to its six switching components, the proposed converter presents a challenge for analysing its dynamic characteristics using linear control theory. To overcome this, a small-signal model is obtained using the circuit averaging technique, which involves averaging currents and voltages of the switching devices over a switching period [23] and [24].

In the following study, the leakage inductances are ignored for simplicity. The average voltage of switches can be found by following a similar approach to (29), as:

$$\begin{cases} V_{ds1} = \frac{V_{in}}{2}\ (1-D) \\ V_{ds2} = V_{ds5} = \frac{V_{in}}{2}\ D \\ V_{ds4} = \frac{V_{in}}{2} \\ V_{ds3} = V_{ds6} = \frac{(1-n_{32})}{2(1+n_{12})}\ V_{in}D \end{cases} \tag{31}$$

By considering the values with $\sim$ as small perturbations around the steady-state operation point, the large signal equations of the voltages can be obtained as:

$$\begin{cases} v_{ds1} = V_{ds1} + \tilde{v}_{ds1} = \frac{V_{in}+\tilde{v}_{in}}{2}\ \left(1-\left(D+\tilde{d}\right)\right) \\ v_{ds2} = V_{ds2} + \tilde{v}_{ds2} = \frac{V_{in}+\tilde{v}_{in}}{2}\ \left(D+\tilde{d}\right) \\ v_{ds3} = V_{ds3} + \tilde{v}_{ds3} = K\left(V_{in}+\tilde{v}_{in}\right)\times\left(D+\tilde{d}\right) \\ v_{ds4} = V_{ds4} + \tilde{v}_{ds4} = \frac{V_{in}+\tilde{v}_{in}}{2} \\ v_{ds5} = V_{ds5} + \tilde{v}_{ds5} = \frac{V_{in}+\tilde{v}_{in}}{2}\ \left(D+\tilde{d}\right) \\ v_{ds6} = V_{ds6} + \tilde{v}_{ds6} = K\left(V_{in}+\tilde{v}_{in}\right)\times\left(D+\tilde{d}\right) \end{cases} \tag{32}$$

where

$$K = \frac{(1-n_{32})}{2\,(1+n_{12})} \tag{33}$$

Expanding (32) and neglecting the second-order terms of ac perturbation signals, the small-signal model of the switches can be found as

$$\begin{cases} \tilde{v}_{ds1} = \frac{\tilde{v}_{in}}{2} - \frac{V_{in}\tilde{d}}{2} - \frac{D\tilde{v}_{in}}{2} \\ \tilde{v}_{ds2} = \frac{V_{in}\tilde{d}}{2} + \frac{D\tilde{v}_{in}}{2} \\ \tilde{v}_{ds3} = KD\tilde{v}_{in} + KV_{in}\tilde{d} \\ \tilde{v}_{ds4} = \frac{\tilde{v}_{in}}{2} \\ \tilde{v}_{ds5} = \frac{V_{in}\tilde{d}}{2} + \frac{D\tilde{v}_{in}}{2} \\ \tilde{v}_{ds6} = KD\tilde{v}_{in} + KV_{in}\tilde{d} \end{cases} \tag{34}$$

Using (34), the small-signal model of the proposed converter can be seen in Figure 6, which has been realized by replacing the switches with voltage-controlled sources. In order to derive the control-to-output transfer function, $T_p(s)$, $\tilde{v}_{in}$ is ignored ($\tilde{v}_{in} = 0$). By applying KVL to the loop consisting of the coupled inductor winding N_3, N_2 and output capacitor C_o and KCL in the output node in the s-domain, the transfer function yields as

$$T_p\ (s)\ = \frac{\tilde{v}_o\,(s)}{\tilde{d}\,(s)} = \frac{(1-n_{32})\,V_{in}}{2\,(1+n_{12})} \times \frac{1}{\left[\frac{1}{2}\left(\frac{1-n_{32}}{n_{12}}\right)^2 L_m C_o s^2 + \frac{1}{2}\left(\frac{1-n_{32}}{n_{12}}\right)^2 \frac{L_m}{R_o}s + 1\right]} \tag{35}$$

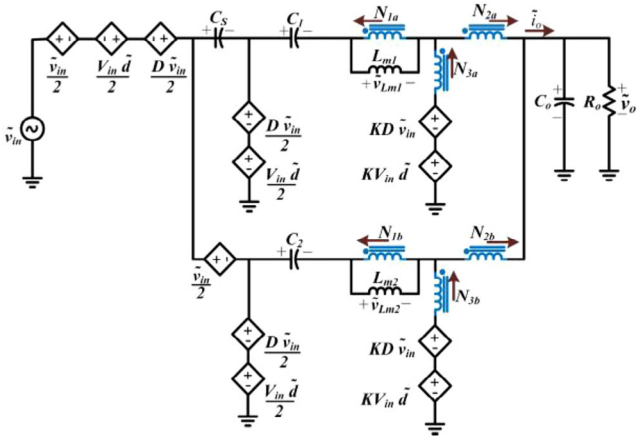

FIGURE 6 Small-signal model of the proposed converter.

In a similar way, with $\tilde{d} = 0$:

$$M_v(s) = \frac{\tilde{v}_o(s)}{\tilde{v}_{in}(s)} = \frac{(1-n_{32})D}{2(1+n_{12})} \times \frac{1}{\left[\frac{1}{2}\left(\frac{1-n_{32}}{n_{12}}\right)^2 L_m C_o s^2 + \frac{1}{2}\left(\frac{1-n_{32}}{n_{12}}\right)^2 \frac{L_m}{R_o} s + 1\right]} \tag{36}$$

From (35), $T_p(s)$ has no right half-plane zeros, so the behaviour of the proposed converter is similar to the conventional buck converter, which is a great advantage. For instance, a simple single-loop controller can be used to adjust the output. Figure 7 depicts the step response of M_v for different values of n_{12} and n_{32}. As can be seen, unlike n_{12}, n_{32} has a profound effect on the transient behaviour of the converter. By increasing n_{32}, the proposed converter responds much faster to input voltage possible fluctuations.

4 | DESIGN CONSIDERATION

For simplicity, the leakage inductances and the effect of dead time are ignored.

4.1 | Inductor design

To ensure that the converter operates in CCM condition, the following equation should be satisfied:

$$\begin{cases} 2I_{Lm1} \geq \Delta i_{Lm1} \\ 2I_{Lm2} \geq \Delta i_{Lm2} \end{cases} \tag{37}$$

From the equivalent circuit of Figure 1, the current through L_{m2} can be derived as:

$$i_{Lm2} = i_{C2} + i_{N1b} \tag{38}$$

In steady state, using the ampere-turn law and zero average current of C_2, Equation (38) can be rewritten as:

$$I_{Lm2} = I_{N1b} = \frac{1}{n_{12}} I_{N_{2b}} - \frac{n_{32}}{n_{12}} I_{N_{3b}} \tag{39}$$

Also, the output current is equally shared between the two phases. So, in a steady state,

$$I_{N_{2b}} = I_{N_{3b}} = \frac{I_o}{2} \tag{40}$$

therefore

$$I_{Lm2} = \frac{I_o}{2}\left(\frac{1-n_{32}}{n_{12}}\right) \tag{41}$$

From (14), during the time interval $[t_3–t_5]$, the current ripple of L_{m2} is:

$$\Delta i_{Lm2} = \frac{V_{L_{m2}} \Delta t}{L_{m2}} = \frac{\frac{n_{12}}{1-n_{32}} V_o (1-D) T_s}{L_{m2}} \tag{42}$$

By assuming that $L_{m1} = L_{m2} = L_m$ and substituting (41) and (42) into (37), the minimum value of the magnetizing inductance L_m is calculated as:

$$L_m \geq \left(\frac{n_{12}}{1-n_{32}}\right)^2 \frac{V_o (1-D) T_s}{I_{o,min}} \tag{43}$$

where $I_{o,min}$ is usually set at 20% of the rated load current.

4.2 | Capacitor design

In steady state, and by ignoring the leakage inductance, the average voltage of capacitors C_1 and C_2 can be obtained from (11) as:

$$V_{C1} = V_{C2} = \frac{n_{12}+n_{32}}{1-n_{32}} V_o \tag{44}$$

Thus, from Figure 4, C_1 and C_2 can be designed as:

$$C_1 = C_2 \geq \frac{\frac{I_o}{2}\frac{(1-n_{32})}{(1+n_{12})} D}{\Delta V_c f_s} \tag{45}$$

where ΔV_C is the tolerable voltage ripple of the capacitors, which is here set to 1% of their average voltage.

When switches S_1 or S_4 are on, by considering ΔV_{CS} as the voltage ripple of C_S, its capacitance is determined as:

$$C_S \geq \frac{\frac{I_o}{2}\frac{(1-n_{32})}{(1+n_{12})} D}{\Delta V_{Cs} f_s}. \tag{46}$$

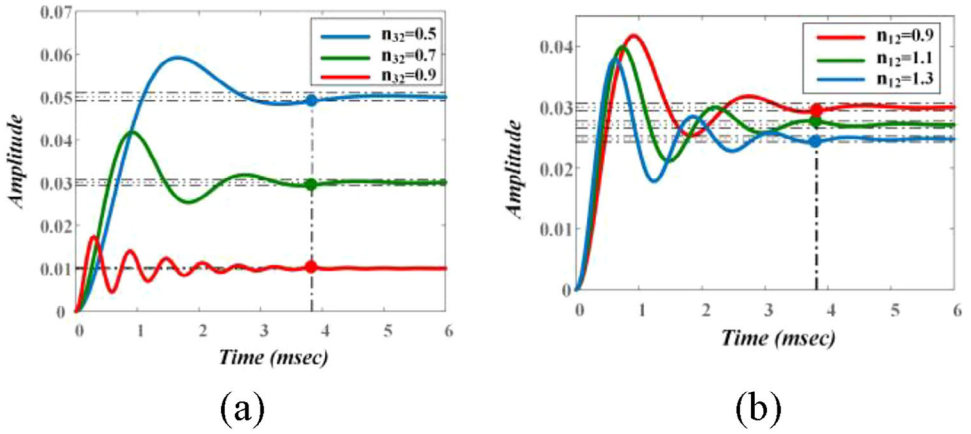

FIGURE 7 Small-signal model of the proposed converter.

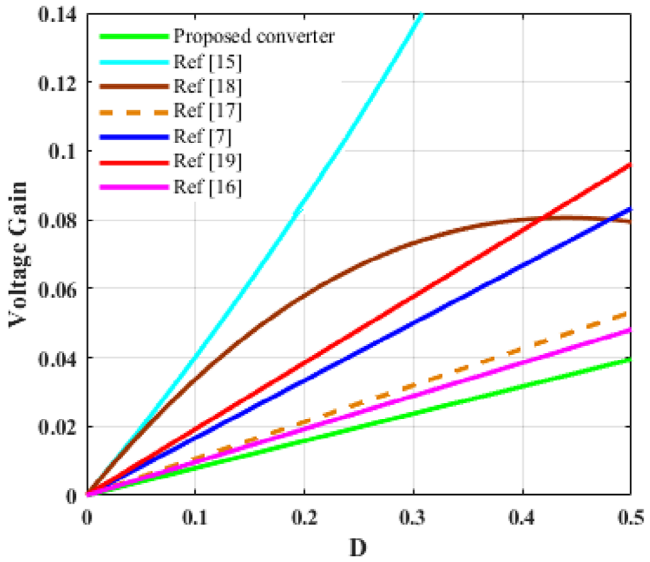

FIGURE 8 Voltage gain comparison of proposed converter and converters given in Table 1.

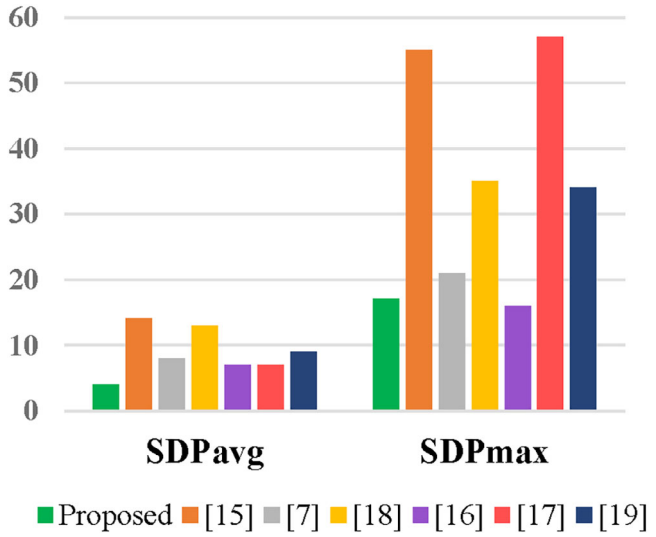

FIGURE 9 Comparison of normalized total SDP_{avg} and SDP_{max}.

5 | COMPARISON WITH OTHER CONVERTERS

A comparison of the proposed converter and other similar buck converters is shown in Table 1. It should be mentioned that for the sake of fairness, all comparisons are conducted under the same conditions: 400 V/12 V, 200 W, 50 kHz, $n_{12} = 0.9$, $n_{32} = 0.7$, $n = n_{12}+n_{32} = 1.6$, using the assumptions and approaches presented in [25] and [26]. The voltage conversion ratio of the proposed converter and counterparts is shown in Figure 8 under the same turn ratios of $n_{12} = 0.9$, $n_{32} = 0.7$ (for the proposed converter), and $n = 1.6$ (for other converters with two or three-winding CI). The proposed converter achieves a higher step-down conversion than others. For the sake of fairness, capacitors and inductors are designed with the same voltage and current ripples. The efficiencies are obtained from PSIM Thermal module simulations and the results are reported in Table 1. In these simulations, all parasitic components are considered based on the datasheets and recommendations by [27] and [28]. In addition, to evaluate the switching devices' requirements, the total peak and average switching device powers, that is, SDP_{max} and SDP_{avg} as given in (47), are being calculated and compared where N is the total number of semiconductors, V_i^{peak} is the peak voltage across i^{th} semiconductor, I_i^{peak} is its peak current and I_i^{avg} is its average current during a switching period [29].

$$\begin{cases} SDP_{pk} = \sum_{i=1}^{N} V_i^{peak} I_i^{peak} \\ SDP_{avg} = \sum_{i=1}^{N} V_i^{peak} I_i^{avg} \end{cases} \tag{47}$$

The results are normalized by the output power and given in Table 1 and plotted in Figure 9. Accordingly, except for the converter in [16], the proposed converter offers lower required ratings of the semiconductors and related losses. Although

TABLE 1 Comparison of the proposed converter with other similar converters.

	[19]	[17]	[16]	[18]	[7]	[15]	Proposed converter
Voltage gain	$\frac{D}{2(1+n)}$	$D/[D(2-D)(2n+1)+2n+2]$	$\frac{D}{4(n+1)}$	$D(1-D)/[1+n(1+D)+D(D-1)]$	$\frac{D}{6}$	$\frac{nD}{n(2-D)+1-D}$	$\frac{(1-n_{32})D}{2(1+n_{12})}$
No. of phases	2	2	4	2	2	2	2
No. of semiconductors	6	7	10	5	8	6	6
No. of capacitors	4	5	4	5	7	3	4
No. of mag. cores	2	2	6	3	2	2	2
Switches peak current (A)	3.9	20.3/3.1	1.6	5.6	2.8	8.3	1.8
Synch. rectifiers (or diodes) current (A)	19.7, 4.4	37, 50	8.3	16.6, 6.2, 0.6	16.6, 13.9	8.3	22.8, 2.9
Normalized SDP^{tot}_{max}, SDP^{tot}_{avg}	34, 9	57, 7	16, 7	35, 13	21, 8	55, 14	17, 4
Switching condition	ZVS	ZVS	ZVS	ZVS	Hard	Hard	ZVS
Efficiency	92.1%	89.8%	89.2%	92.4%	91.7%	92.2%	94.8%
Common ground	Yes	Yes	Yes	No	No	No	Yes
Voltage stress on switches	S_1 S_2 S_5	$\frac{V_{in}}{2}$	S_1 S_4 S_5	$\frac{V_{in}}{3}$	S_1 – S_4	$\frac{V_{in}}{2}$	S_1 S_3	See below[a]	S_1 – S_6	$\frac{V_{in}}{3}$	S_1 S_2	See below[e,f]	S_1 S_2 S_5	$\frac{V_{in}}{2}$
	S_4	$\frac{V_{in}}{2}, V_{in}$	S_2 S_3	$\frac{2V_{in}}{3}$	S_5 – S_6	$\frac{V_{in}}{4}$	S_2	See below[b]	S_2	$\frac{V_{in}}{6}$			S_4	$\frac{V_{in}}{2}, V_{in}$
Voltage stress on SRs/diodes	S_3 S_6	$\frac{V_{in}}{2(1+n)}$	S_6 S_7	$\frac{V_o}{D}$	D_1 – D_4	$\frac{V_{in}}{4(n+1)}$	D_1	See below[c]	D_1 D_2	$\frac{V_{in}}{6}$	D_a D_b	V_{in}	S_3 S_6	$\frac{(1-n_{32})V_{in}}{2(1+n_{12})}$
					D_2	See below[d]					D_1 D_2	See below[f]		

[a] $V_{S_1,S_3} = \frac{(n-D+1)V_{in}}{n(D+1)+D(D-1)+1}$;

[b] $V_{S_2} = \frac{(n+D)V_{in}}{n(D+1)+D(D-1)+1}$;

[c] $V_{D_1} = \frac{(1-D)V_{in}}{n(D+1)+D(D-1)+1}$;

[d] $V_{D_2} = \frac{DV_{in}}{n(D+1)+D(D-1)+1}$;

[e] $V_{S_1} = \frac{(1+n)V_{in}}{n(2-D)+1-D}$;

[f] $V_{S_2,D_1,D_2} = \frac{nV_{in}}{n(2-D)+1-D}$.

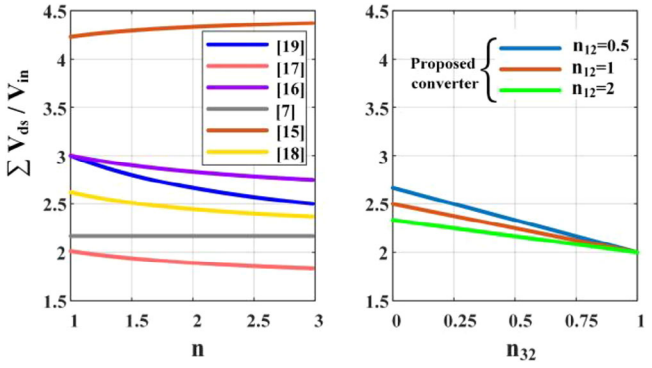

FIGURE 10 Comparison of normalized total voltage stress across the semiconductors.

the converter in [16] has a lower SDP_{max} than the proposed converter but at the cost of a significantly high number of semiconductor and magnetic components. Furthermore, the normalized total voltage stress across the semiconductors is compared in Figure 10. This comparison is conducted at a constant duty cycle of 0.38. As can be seen, when the turn ratio approaches unity, the total voltage stress of the proposed converter is lower than others, except for [17]. However, the converter in [17] utilizes more components and its SDPs are much higher than the proposed converter as shown in Figure 9.

Overall, ZVS conditions for all semiconductors, low ratings and a turns ratio close to the unity of TWCI lead to a reduction in losses and a higher efficiency.

6 | EXPERIMENTAL RESULTS

A laboratory prototype of the proposed converter was constructed with input and output voltages of 400 and 12 V, respectively. Considering the limitations of the laboratory equipment, the switching frequency is chosen as 50 kHz. According to Equation (22), there are three degrees of freedom when determining the voltage ratio. The turn ratios (n_{12} and n_{32}) of the TWCIs were chosen to satisfy the conditions outlined in Table 1, thereby setting the duty cycle to 0.38. The prototype's parameters are detailed in Table 2, and the test rig is illustrated in Figure 11.

Figure 12 presents the turn-on transients of S_1–S_6. The drain-source voltage of each switch reaches zero just before its gate-source voltage rises, achieving ZVS. The voltage stresses are consistent with (29). Notably, the voltage stress across SR switches is 32 V, permitting low-voltage rating MOSFETs with minimum resistance. Figure 13a displays the measured input and output voltage waveforms, with the input voltage measured 400 V and the output voltage 11.7 V, closely matching the calculated voltage conversion ratio. Figure 13b is the voltage waveforms of C_1, C_2, C_S and the source, verifying that the capacitors' voltages remain constant during converter operation at 68 V, 68 V and 200 V, as already calculated from (11). Figure 14a depicts the current waveforms of energy-transferring capacitors C_1 and C_2, with maximum and minimum currents of

TABLE 2 Parameters of prototype setup value.

Parameter	Values
Input voltage (V_{in})	400 V
Output voltage (V_{out})	12 V
Rated power (P_{out})	200 W
Duty cycle	0.38
Capacitors C_1, C_2	22 μF
Capacitor C_S	47 μF
Capacitor C_o	330 μF × 2
Magnetizing inductances L_m	360 μH
Turns ratios (N_1:N_2:N_3 → n_{12}:1:n_{32})	EE42/21/20 Ferrite (19:21:15 → 0.9:1:0.7)
Leakage inductances L_K	7.4 μH
Switches S_1, S_2, S_5	IRFP4767
Switch S_4	STW26NM50
Switches S_3, S_6	IRFB7440

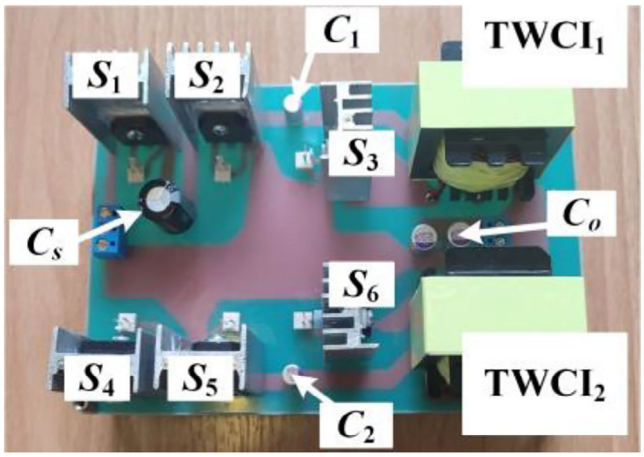

FIGURE 11 Experimental setup.

approximately 1.4 A and −2.4 A, respectively, in agreement with the waveforms of Figure 2 and values of (1) and (8). Figure 14b shows that the average value of the magnetizing current for the two phases is around 2.7 A, in close agreement with the theoretical value of 2.78 A derived from Equation (41). It should be noted that the magnetizing current, as observed in experimental tests, is determined by the relationship between this current and the number of turns of the windings and their currents ($0.9I_{Lm} = 0.7I_{N3} + I_{N2} + 0.9I_{N1}$). To measure this current, the windings are wound around the current probe clamp with a number of turns based on this relationship. Consequently, the measured current is 9 times its real value. Additionally, as shown in Figure 14, the currents of the two phases are interleaved and automatically balanced, minimizing the output current ripple. Based on the similarity between the converter in [19] and the proposed converter, a comparison of their efficiencies is presented in Figure 15. As can be seen, the maximum efficiency of the implemented prototype is 95% and its full-load efficiency is 94.8%, well above the competitor. However, the

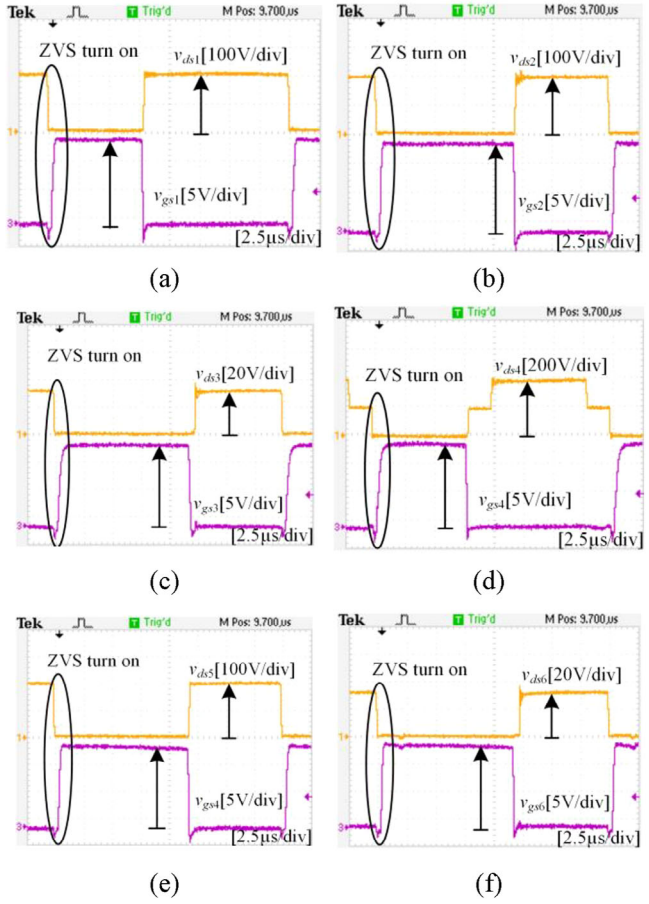

FIGURE 12 Experimental results: Drain-source and gate-source voltages of switches (a) S_1, (b) S_2, (c) S_3, (d) S_4, (e) S_5 and (f) S_6.

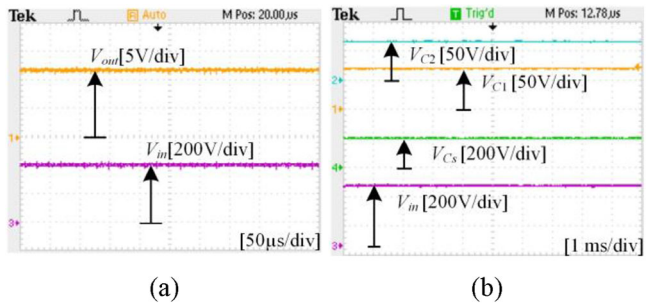

FIGURE 13 Experimental results: (a) Input and output voltages, and (b) capacitors' and input voltages.

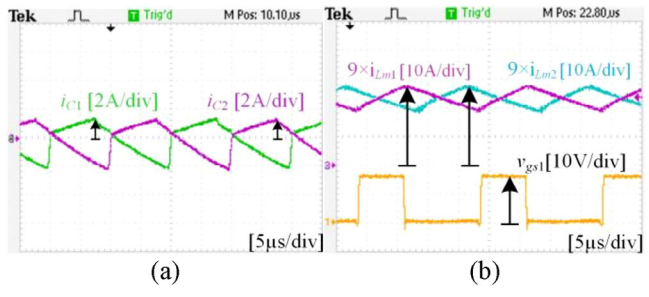

FIGURE 14 Experimental results: (a) Currents of capacitors C_1, C_2 and (b) currents of inductors L_{m1}, L_{m2} and gate-source voltage of S_1.

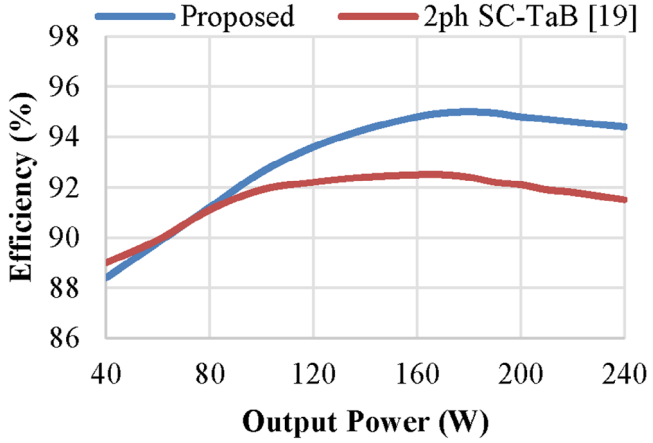

FIGURE 15 Measured efficiencies.

power loss associated with the third winding hinders the efficiency improvement at light load compared to [19].

7 | CONCLUSION

An ultra-high step-down non-isolated DC-DC converter has been developed using series capacitors and coupled-inductor techniques. Instead of increasing the turn ratios of coupled inductors to achieve a high step-down conversion ratio, the proposed converter employs ratios close to unity. In addition to providing ultra-high voltage gain, extended duty cycles and low magnetizing currents, the proposed converter also minimizes ohmic losses associated with increased turn ratios. All of these benefits, combined with very low SDP and ZVS for all switches, lead to exceptional efficiency. In addition, the turns ratios of the coupled inductors are not required to be identical, which gives three degrees of freedom to the voltage gain design. Lastly, experimental results obtained from a 400–12 V/200 W laboratory setup confirm the aforementioned properties.

AUTHOR CONTRIBUTIONS

Wahid Eskandary: Conceptualization; data curation; formal analysis; investigation; methodology; software; validation; visualization; writing—original draft; writing—review and editing. **Mohammad Monfared**: Conceptualization; data curation; formal analysis; investigation; methodology; project administration; resources; software; supervision; validation; visualization; writing—original draft; writing—review and editing. **Ali Nikbahar**: Formal analysis; investigation; validation; visualization; writing—review and editing. **Ahmad Mahdave**: Investigation; methodology; validation; visualization; writing—original draft.

CONFLICT OF INTEREST STATEMENT

The authors declare no conflicts of interest.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author, upon reasonable request.

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