Triple-Mode Flying Inductor Common-Ground PV Inverter with Reactive Power Capability and Low Semiconductor Component Count

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***Abstract*—This paper proposes the flying inductor based common ground single-phase PV inverter which can support reactive power to the ac grid. The proposed buck-boost transformerless PV inverter eliminates the leakage current and is suitable for use in on-grid applications which require active and reactive power support. The proposed converter also features a low number of semiconductor devices, no ac type capacitor, acceptable quality of the grid side current even during non-unity power factor operations, reducing switching loss by adopting time-sharing technique, and high efficiency. The converter uses a dead-beat controller in the control loop which has a smooth, accurate and fast response. Experimental results for a 500 W, 100 Vdc and 180 Vdc to 110 Vrms, prototype is provided in a closed-loop system in the presence of the proposed dead-beat controller. The results from the prototype validate the theoretical analysis and the applicability of the proposed structure. The converter exhibits the capability for stepping up the dc to ac power conversion and demonstrates a peak efficiency of 97.2% and 96.8% from 180 Vdc and 100 Vdc, respectively.**

***Index Terms*—Common ground inverter, flying inductor converter, reactive power capability, transformerless PV inverter.**

I. Introduction

COMMON-ground transformerless photovoltaic (PV) inverters are fast becoming the dominant solution for distributed energy resources (DERs) due to their many advantages, including reduced electromagnetic interference (EMI) noise, elimination of leakage current, and higher efficiency.

In addition to reducing the EMI noise and leakage current, other requirements for the grid connected PV inverters include: a) the ability to provide reactive power to the ac grid as requested by IEEE 1547-2018 [1], b) a low active component count, and c) buck-boost capability.

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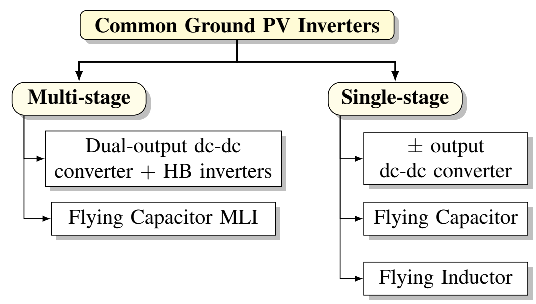

Fig. 1. Classification of common ground inverters.

Different types of common ground inverters have been reported in the literature, and based on their configuration, as shown in Fig. 1 they can be classified into:

1) Single stage inverters which can be further classified as dc-dc converters with positive and negative voltage outputs, flying capacitor (FC) or flying inductor (FI) inverter configurations.
2) Multi stage inverters which can be further classified as the integration of a dual-output dc-dc converter and a half bridge (HB) inverter and flying capacitor multilevel inverter (MLI) configurations.

In the case of the dual-output dc-dc converter in series with HB inverter, a dc-dc converter with a midpoint at the output dc side is typically adopted as a pre-front stage for different types of HB inverter. The converter in [2] employs two buck-boost dc-dc converters to regulate the dc bus voltage with positive, zero and negative voltages and a conventional HB inverter generates sinusoidal output voltage. The converters in [3], [4], [5] and [6] have used the input and the output of the conventional buck-boost dc-dc converter as the pre-front stage of the conventional HB, T-type, dual-buck and buck inverter, respectively. Among all the converters in [2], [3], [4], [5], [6], only [4] can generate reactive power, which is usually referred to as reactive power capability (RPC) for the ac grid. As regards buck-boost capability, the converter in [2] achieves this by using two buck-boost dc-dc converters and the converter in [7] adopts one boost and one buck-boost converter in the input stage which gives stepping up operation with no RPC.

Dc-dc converters with positive and negative voltage gain ratio can also be used as an inverter such as the topologies suggested in [8]–[11]. The voltage gain ratio of the converters in [8], [9] (and also in [10]) is $(1-2d)/(d-d^2)$ (and $(1-2d)/(1-d)$) and therefore the voltage gain is lower and more sensitive than that of the conventional buck-boost voltage gain ratio i.e. $d/(1-d)$. Moreover, the application of converters in [8]–[10] is limited only to off-grid PV inverters since they are incapable of meeting the volt-var settings required by IEEE 1547-2018. As a successful solution, the converter in [11] has improved the voltage gain ratio and provided RPC at the cost of using nine semiconductor devices, three capacitors and three inductors.

The FC common ground inverters have been proposed in [12]–[14] which require the input dc voltage level to be higher than the peak value of ac voltage, in other words they are step-down converters. Moreover, the voltage ripple across the grid side filter varies between zero and the dc side voltage level. Hence, the grid side filter is relatively large, and due to the larger current ripple of the FC converters, one can expect more core losses [15]. Recently, improved FC common ground inverters have been reported such as the flying capacitor MLI in [16], [17] and the integrated boost FC inverter in [18]–[20]. However, the high number of active and passive components increases the volume and adds complexity to modulation and control algorithms. Furthermore, the large capacitor demands a significant amount of charging current which could damage active components of circuit.

The flying inductor inverter is another type of common ground inverter which provides the charging and discharging circuit loop for an inductor through both positive and negative half cycles of ac grid. In other words, an inductor flies between connection to the input side and connection to the output side with the ability to connect it to the output in a positive or negative manner during the positive or negative half cycles. Consequently FI type inverters have the significant advantage that the ac side current filter can be considerably smaller. In addition they do not have the large capacitor and associated charging current requirements of the FC type converters.

With regards to the FI common ground inverters, the first such inverter was proposed in [21]. The $Karschny$-inverter is based on a current source inverter with seven semiconductor devices and is capable of stepping-up the input dc voltage. However, the inability to support the ac grid by reactive power, limits the use of the $Karschny$-inverter only to off-grid applications. Another FI inverter with five switches and three diodes has been proposed in [22] which offers the buck-boost voltage gain ratio i.e., $\pm d/(1-d)$, during either positive or negative half cycle. The structure [22] has been updated by reverse blocking insulated gate bipolar transistors (RB-IGBT) to reduce the number of semiconductor devices. However, the switching performance of the RB-IGBT is not optimized and reverse recovery current of the internal diode and turn-ON losses of the associated IGBT are greater compared to standard fast freewheel diodes [23].

The converter in [24] uses only MOSFET switches and the converter in [25] uses MOSFET and discrete diodes in the structure of [22] and offers soft switching and the triple-mode switching strategy, respectively to improve the efficiency. However again, due to the inability of the FI based converters in [22], [24]–[26] to inject or absorb reactive power, they are not suitable for connection to the ac network.

Recently, the structure of [24] was further improved by a bidirectional MOSFET switch in [27]-type-1 and so it has nine semiconductor devices. The new FI based converters have been presented as type-3 and type-4 in paper [27] which both have six semiconductor devices. All the common ground FI inverters in [27] use bidirectional MOSFET switches, they are able to support the ac grid with reactive power.

The converter described in [28] features 8 switches, 1 diode, 3 capacitors, and 2 inductors. Operating with a two-stage power processing method, it offers buck-boost capability and utilizes a five-level switched capacitor inverter that includes reactive power exchange capability. Moving on to [29], this converter is equipped with 6 switches, 2 diodes, 2 capacitors, and 1 inductor. Despite providing a voltage gain ratio of 2 through its switched capacitor design, it lacks reactive power exchange capability. Another noteworthy converter is discussed in [30], has 9 switches, 2 diodes, 3 capacitors, and 1 inductor. Offering reactive power exchange capability and a voltage gain ratio of 4, it operates as a switched capacitor 9-level inverter. In [31], an 8-switch configuration is combined with 2 diodes and 2 capacitors, featuring a switch capacitor type inverter capable of nine-level operation with reactive power capability. Furthermore, the converter detailed in [32] incorporates 8 switches, 2 diodes, 3 capacitors, and 1 inductor, providing both reactive power capability and boost capability through its switch capacitor inverter design. [33] presents a converter comprising 6 switches, 3 diodes, 3 capacitors, and 1 inductor, offering both buck-boost capability and reactive power exchange capability.

In this paper, a novel triple-mode flying inductor common-ground (TMFICG) single-stage PV inverter is proposed. Significantly, this is an FI converter with reactive power capability. In addition it has a lower semiconductor device count compared to the previously published FI common ground inverters and unlike the previous converters it does not require an ac type capacitor. Using a dc capacitor instead of ac capacitors offers several advantages, including reduced size and weight, lower cost, and enhanced reliability. dc capacitors are subjected to less voltage stress compared to ac capacitors, leading to increased longevity and improved performance. The proposed converter comprises a total of 7 semiconductor devices (6 switches and 1 diode). Despite this count, compared to the main common-ground flying inductor inverters, the proposed inverter falls into the low-number category. This suggests that the proposed converter offers a relatively reduced semiconductor device count compared to typical common-ground flying inductor inverters. To control the proposed inverter, the FI current indirect dead-beat controller (IDBC) and the grid side current direct dead-beat controller is adopted during the positive and negative power regions respectively, which achieves accurate, fast, and smooth operation under different states of operation.

The rest of this paper is organized as follows. The proposed FI common ground inverter is presented in section II. Section III is devoted to the practical considerations and design calculations for the proposed converter. A comprehen-

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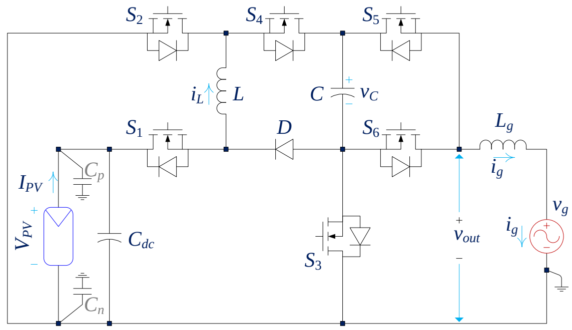

Fig. 2. Proposed triple-mode flying inductor common ground (TMFICG) PV inverter.

sive comparative study with the state-of-the-art is presented in section IV, the proposed dead-beat controller description is given in section V and the experimental verification is provided in section VI. Finally, section VII concludes the paper.

II. Proposed FI Common-Ground Inverter Operation Analysis

Figure 2 shows the proposed flying-inductor common-ground PV inverter structure. V_{PV}, v_{out} and v_g denotes the PV voltage, output voltage of inverter and the ac grid voltage, respectively. The proposed inverter consists of two inductors L and L_g, two capacitors C and C_{dc}, six switches S_1, S_2, S_3, S_4, S_5 and S_6 and one diode D. It is worth noting that the parasitic capacitor of the positive (C_p) and the negative rails (C_n) of the PV side are not actual capacitors; in fact, they are unintended capacitances inherent in the circuit design and physical configuration. These capacitances arise due to the stray capacitance between the Cell-to-frame, Cell-to-rack, and Cell-to-ground [34]. These capacitors are not necessary for the operation of the proposed PV inverter but are essentially a result of the mechanical structure of the PV modules and their installation.

The proposed PWM scheme is shown in Fig. 3. The equivalent circuit for dual operation modes (buck and boost) during the positive half cycle and single mode of buck-boost operation during the negative half cycle of the grid side ac voltage are shown in Fig. 4(a), (b), and (c), respectively. Moreover, the steady-state operation modes during the negative power region (NPR) are shown in Fig. 4(d). To support the ac grid with the reactive power, during the NPRs the proposed inverter injects negative (positive) current during the positive (negative) half cycle of the ac voltage.

Four states for operation during the positive and the two states for the negative half-cycle are defined as:

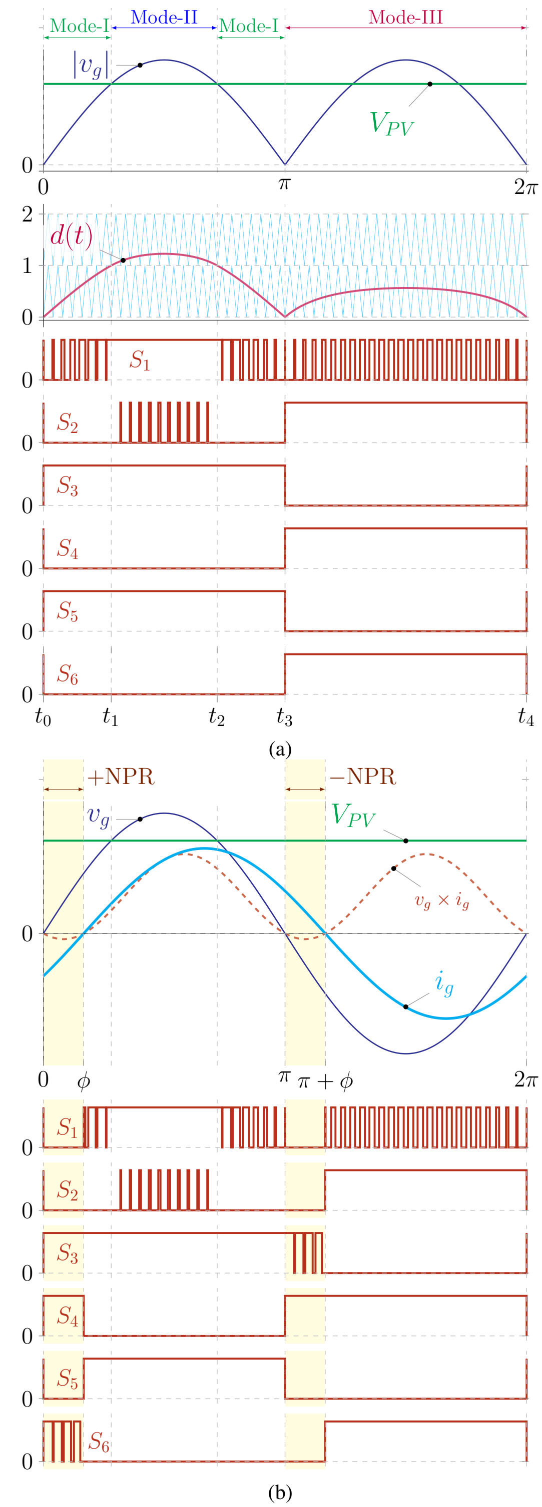

Fig. 3. Different modes of operation and PWM signals during: (a) unity and (b) non-unity power factor.

A. Positive and negative half cycles operation modes

Mode-I $[t_0 - t_1]$ and $[t_2 - t_3]$: During $0 \le t \le dT_s$ (d represents the duty cycle) or state-1 of mode-I and according to Fig. 3, when the instantaneous ac grid voltage is lower than the input dc voltage level, the switches S_3 and S_5 are turned on and S_1 is PWM controlled while S_2, S_4, and S_6 are turned off.

As shown in Fig. 4(a) left, the flying inductor L is charged from the input dc source i.e. V_{PV}. Furthermore, V_{PV} transfers the energy to v_g and the inductor filter L_g, through S_1, S_5, and the body diode of S_4. Moreover, the Proposed converter is connected to the ac system via a dc-type capacitor, denoted as C. This dc capacitor charges and discharges from the dc side through the ac side during the positive half cycle. Conversely,

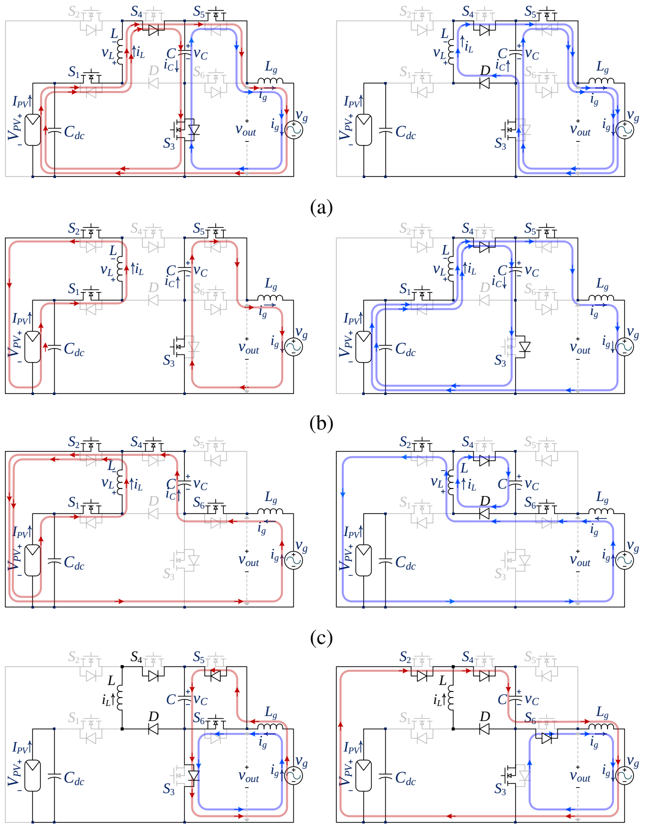

Fig. 4. Equivalent circuit of the proposed converter during the positive half cycle (a) mode-I, (b) mode-II, the negative half cycle (c) mode-III and (d) the negative power region (left: state-1 and right: state-2).

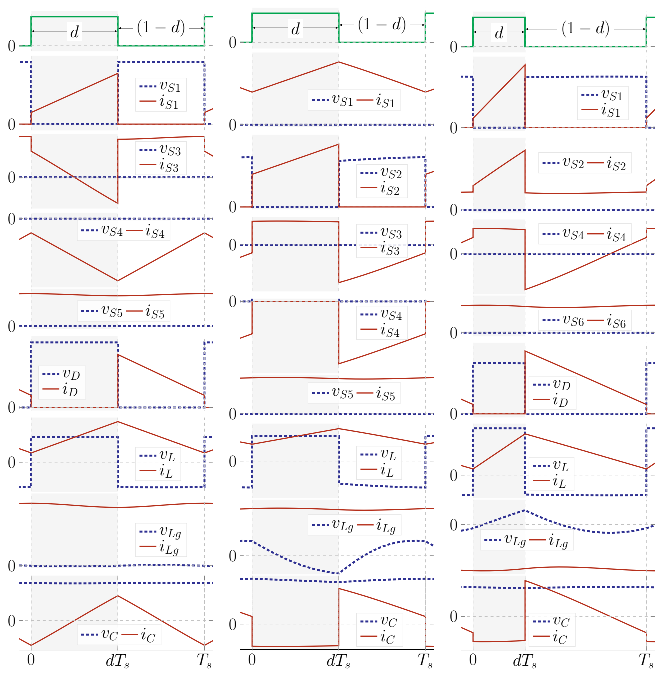

Fig. 5. Typical time-domain waveforms mode: (a) I, (b) II and (c) III.

during the negative half cycle, the converter switches the capacitor to discharge through the negative terminal of the ac grid. The capacitor C is first discharged into L_g and v_g through S_3 and S_5 and then charged from V_{PV} and L through S_1 and body diodes of S_3 and S_4. According to the typical time-domain waveforms in Fig. 5(a), the current through L increases, and the energy of L_g is increased from the input source and L. Thus, the derived voltage and current equations are:

$$\begin{cases} v_L = L\frac{di_L}{dt} = V_{PV} - v_C = V_{PV} - v_{out} \\ i_C = C\frac{dv_C}{dt} = i_L - i_g \end{cases} \tag{1}$$

During $dT_s \le t \le T_s$ or state-2 of mode-I as shown in Fig. 4(a) right, S_3 and S_5 are turned on whereas S_1, S_2, S_4, and S_6 are turned off. During this state, L releases its energy to v_g and L_g, through S_3, S_5, D and body diode of S_4. Moreover, C is discharged to the grid side through S_3 and S_5. According to the typical time-domain waveforms in Fig. 5(a), the current through L decreases, and the energy of L_g is released to the ac grid. Thus, the derived equations are:

$$\begin{cases} v_L = L\frac{di_L}{dt} = -v_C = -v_{out} \\ -i_C = -C\frac{dv_C}{dt} = i_g - i_L \end{cases} \tag{2}$$

By applying the volt-second and amp-second balances to L and C, respectively

$$d(V_{PV} - v_C) + (1-d)(-v_C) = 0 \tag{3}$$

$$d(i_L - i_g) - (1-d)(i_g - i_L) = 0 \tag{4}$$

where $v_C = v_{out}$.

From (3) and (4), the voltage conversion ratio of the proposed converter and i_L during the step-down mode-I for the positive half cycle operation can be calculated as follows

$$M_{mode-I} = \frac{v_{out}}{V_{PV}} = d \tag{5}$$

$$i_L = i_g \tag{6}$$

Mode-II $[t_1 - t_2]$: During $0 \le t \le dT_s$ or state-1 of mode-II and according to Fig. 3, when the instantaneous grid voltage is higher than the input dc voltage level, the switches S_1, S_3 and S_5 are turned on and S_2 is PWM controlled while S_4, and S_6 are turned off. In Fig. 4(b) left, L is charged by V_{PV} and C releases its energy to L_g and v_g. Thus, the current through L increases, while the energy of L_g decreases. According to the typical time-domain waveforms in Fig. 5(b) the derived equations are:

$$\begin{cases} v_L = L\frac{di_L}{dt} = V_{PV} \\ i_C = C\frac{dv_C}{dt} = i_g \end{cases} \tag{7}$$

During $dT_s \le t \le T_s$ or state-2 of mode-II, as shown in Fig. 4(b) right, S_2, S_3, S_4, S_6, and D are turned off whereas the body diode of S_3 and S_4 are conducting and the switches S_1 and S_5 are turned on. The inductor L in series with V_{PV} releases its energy into C, L_g, and the ac grid. Hence, we have:

$$\begin{cases} v_L = L\frac{di_L}{dt} = V_{PV} - v_C \\ i_C = C\frac{dv_C}{dt} = i_L - i_g \end{cases} \tag{8}$$

Now the volt-second and amp-second balances are applied to L and C.

$$d(V_{PV}) + (1-d)(V_{PV} - v_C) = 0 \tag{9}$$

$$d(i_g)+(1-d)(i_L-i_g)=0 \tag{10}$$

As a result, the voltage gain ratio and i_L are:

$$M_{mode-II}=\frac{v_{out}}{V_{PV}}=\frac{1}{1-d} \tag{11}$$

$$i_L=\frac{1}{1-d}i_g \tag{12}$$

Mode-III $[t_3-t_4]$: During $0\leq t\leq dT_s$ or state-1 of mode-III and according to Fig. 3, the switches S_2, S_4 and S_6 are turned on and S_1 is PWM controlled while S_3 and S_5 are turned off and D is not conducting. In Fig. 4(c) left, the flying inductor L is charged from V_{PV}. Moreover, L_g is charged by the released energy from C. Thus, the current through L and L_g increases. According to the typical time-domain waveforms in Fig. 5(c) the derived equations are:

$$\begin{cases} v_L=L\frac{di_L}{dt}=V_{PV} \\ i_C=C\frac{dv_C}{dt}=-i_g \end{cases} \tag{13}$$

During $dT_s\leq t\leq T_s$ or state-2 of mode-III as shown in Fig. 4(c) right, the switches S_1, S_3, S_4 and S_5 are turned off while S_2, S_6, D and the body diode of S_4 are on. In this period, L and L_g are discharged to v_g. Moreover, C is charged by the released energy from L. In this state the derived current and voltage equations are:

$$\begin{cases} v_L=L\frac{di_L}{dt}=-v_C \\ i_C=C\frac{dv_C}{dt}=i_L-i_g \end{cases} \tag{14}$$

Again from the volt-second and amp-second balances, one can obtain:

$$d(V_{PV})+(1-d)(-v_C)=0 \tag{15}$$

$$d(-i_g)+(1-d)(i_L-i_g)=0 \tag{16}$$

Therefore, the voltage conversion ratio of the proposed converter during the negative half cycle and i_L can be calculated as follows

$$M_{mode-III}=\frac{v_{out}}{V_{PV}}=\frac{-d}{1-d} \tag{17}$$

$$i_L=\frac{1}{1-d}i_g \tag{18}$$

B. NPR operation modes

During the positive half cycle of the grid voltage, Fig. 4(d) left, and when i_g is negative, as shown in Fig. 3, S_6 is PWM controlled and when it turns off, the current through L_g increases in the circuit consisting of C, and the anti-parallel diodes of S_3 and S_5. When S_6 is turned on the negative current can flow in the freewheeling circuit consisting S_6 and the body diode of S_3.

During the negative half cycle of the grid voltage, Fig. 4(d) right, and when i_g is positive, when S_3 is off, the current can increase and flow through L_g in the circuit consisting of C the anti-parallel diodes of S_2, S_4 and S_6. When S_3 is turned on the negative current decreases and flows the freewheeling circuit consisting of S_3 and body diode of S_6.

By using the switching strategy as described, the proposed FI converter can inject or absorb reactive power to the ac grid while preserving the quality of the grid current. Therefore, the proposed converter can satisfy the volt-var setting requirements of standards such as IEEE 1547-2018.

III. Design Considerations

A. Passive components design

The C_{dc} acts as a buffer for the instantaneous power difference between the ac grid and the dc side of PV. Thus, to maintain the ripple of the dc-link voltage (ΔV_{dc}) below a specific value, the required C_{dc} is:

$$C_{dc}=\frac{P_{PV}}{\omega_0 V_{PV}\Delta V_{dc}} \tag{19}$$

where P_{PV} is the average output power of the PV, ω_0 is the grid angular frequency and V_{PV} is the PV side dc voltage.

The flying inductor L performs the role as either step-down or step-up for the positive and step-down-up for the negative half cycles. For all three operation modes, L can be decided with respect to the tolerable current ripple Δi_L. The Δi_L in each operation mode can be calculated as follows.

$$\Delta i_{L,mode-I}=\frac{(V_{PV}-|v_g|)|v_g|}{V_{PV}L}T_s \tag{20}$$

$$\Delta i_{L,mode-II}=\frac{V_{PV}(|v_g|-V_{PV})}{|v_g|L}T_s \tag{21}$$

$$\Delta i_{L,mode-III}=\frac{V_{PV}|v_g|}{(V_{PV}+|v_g|)L}T_s \tag{22}$$

In above equations, T_s is the switching period. Thus, after deciding the permissible Δi_L, one can calculate L.

$$L_{mode-I}\geq\frac{|v_g|(V_{PV}-|v_g|)}{V_{PV}\Delta i_L}T_s \tag{23}$$

$$L_{mode-II}\geq\frac{V_{PV}(|v_g|-V_{PV})}{|v_g|\Delta i_L}T_s \tag{24}$$

$$L_{mode-III}\geq\frac{V_{PV}.|v_g|}{(V_{PV}+|v_g|)\Delta i_L}T_s \tag{25}$$

The inductor can therefore be chosen to be greater than the largest of these which depends on the specific application values of V_{PV} and amplitude of v_g.

Similarly, the value of grid side inductor, L_g, is chosen from the maximum allowed current ripple, Δi_g, as follows

$$L_g\geq\frac{\Delta v_C}{2\Delta i_g}T_s \tag{26}$$

Equation (27) indicates that the current ripple during the positive power region (PPR) is influenced by the difference between v_C and v_g, while during the NPR, it is primarily influenced by v_g. Therefore, during the NPR, the grid side experiences more ripple.

$$\begin{cases} \Delta i_g=\dfrac{(1-d_{mode-I,III})T_s|v_C-v_g|}{2L_g} \quad , \quad PPR \\ \Delta i_g=\dfrac{(1-d_{\pm NPR})T_s v_g}{2L_g} \quad , \quad NPR \end{cases} \tag{27}$$

To keep the output voltage ripple (Δv_C) below a certain value, the capacitor C must satisfy

$$C\geq\frac{\Delta Q_C}{\Delta v_C} \tag{28}$$

where ΔQ_C is the total capacitor charge change and can be calculated as

$$\Delta Q_{C,mode-I} = \frac{(V_{PV} - v_g)v_g}{8LV_{PV}} T_s^2 \tag{29}$$

$$\Delta Q_{C,mode-II} = I_g \frac{v_g - V_{PV}}{v_g} T_s \tag{30}$$

$$\Delta Q_{C,mode-III} = I_g \frac{v_g}{V_{PV} + v_g} T_s \tag{31}$$

With considering $P_{PV} = 500W$, $v_g = 110\sqrt{2}\sin\omega_0 t$ and $V_{PV} = 100\ V$, the value of $L = 1.0\ mH$ satisfies (23)-(25) for a current ripple below 20%.

From (26) and considering 4% as the maximum tolerable ripple of the injected current, the value of L_g is calculated as $400\ \mu H$. Replacing from (29)-(31) in (28) with the assumption that the maximum voltage ripple is 40%, and then the required capacitance of C is about $2.2\ \mu F$.

B. Semiconductors ratings

The average (over a switching cycle) ON-state current and average OFF-state voltage across the switches and the diode can be expressed as:

$$\text{Mode-I:} \begin{cases} V_{S1} = [1-d(t)]V_{PV} \\ V_{S2} = V_{S6} = V_{out} \\ V_{S3} = V_{S4} = V_{S5} = 0 \\ V_D = [d(t)]V_{PV} \end{cases}, \begin{cases} I_{S1} = [d(t)]I_L \\ I_{S3} = I_D = [1-d(t)]I_L \\ I_{S4} = I_{S5} = I_L \\ I_{S2} = I_{S6} = 0 \end{cases} \tag{32}$$

$$\text{Mode-II:} \begin{cases} V_{S2} = [1-d(t)]V_{out} \\ V_{S1} = V_{S3} = V_{S5} = 0 \\ V_{S4} = [d(t)]V_{out} \\ V_{S6} = V_{out} \\ V_D = [d(t)]V_{PV} \end{cases}, \begin{cases} I_{S1} = I_L \\ I_{S2} = [d(t)]I_L \\ I_{S3} = [d(t)]I_g + \\ [1+d(t)](I_L - I_g) \\ I_{S4} = I_{S5} = I_g \\ I_{S6} = I_D = 0 \end{cases} \tag{33}$$

$$\text{Mode-III:} \begin{cases} V_{S1} = [1-d(t)] \\ (V_{PV} - V_{out}) \\ V_{S2} = V_{S4} = V_{S6} = 0 \\ V_{S3} = V_{S5} = -V_{out} \\ V_D = [d(t)] \\ (V_{PV} - V_{out}) \end{cases}, \begin{cases} I_{S1} = [d(t)]I_L \\ I_{S2} = I_L \\ I_{S3} = I_{S5} = 0 \\ I_{S4} = [d(t)]I_g \\ I_{S6} = I_g \\ I_D = [1-d(t)]I_L \end{cases} \tag{34}$$

Therefore, the rms value of total current stress (TCS) and total voltage stress (TVS) of semiconductor devices during each mode is

$$\text{Mode-I:} \begin{cases} TVS_{rms} = [2d+1]V_{PV} \\ TCS_{rms} = \sqrt{16-7d}I_g \end{cases} \tag{35}$$

$$\text{Mode-II:} \begin{cases} TVS_{rms} = \dfrac{3-d}{1-d}V_{PV} \\ TCS_{rms} = \dfrac{\sqrt{d[4-2d]^2 + 9[1-d]}}{1-d}I_g \end{cases} \tag{36}$$

$$\text{Mode-III:} \begin{cases} TVS_{rms} = \dfrac{|2d+1|}{1-d}V_{PV} \\ TCS_{rms} = \dfrac{\sqrt{8d^3 - 23d^2 + 10d + 9}}{1-d}I_g \end{cases} \tag{37}$$

IV. Comparison of the Proposed FI Inverter to the State of Art

A comparative study of the main characteristics of the other successful common ground flying inductor PV inverters and the proposed inverter are provided in Table I.

The main point of Table I is that the proposed converter has the lowest semiconductor device count without any limitation on the ability to support ac grid with reactive power. The proposed FI converter has seven semiconductor devices and adapts the triple-mode operation to reduce unnecessary switching losses. The total semiconductor device count of flying inductor inverters i.e. the proposed converter, and the converters in [21], [22], [26], [25], [27] type-I, type-III and type-IV is 7, 7, 8, 8, 8, 9, 8 and 8, respectively. Although the total semiconductor device count of converter in [21] is similar to the proposed converter, it is not able to meet the requirements of IEEE 1547-2018 in terms of reactive power provision.

As shown in Table I, while the converters in [35] possess RPC functionality and the type-IV converter can be classified as a flying inductor-based converter, their applications are limited due to their step-down voltage gain ratio.

The proposed converter has fewer elements compared to [11], however it operates with all four semiconductor devices conducting in all modes, while [11] employs varying numbers of devices in different modes. Although the THD difference is minimal, it can be attributed to the transition from buck to boost mode in the proposed converter may also contribute to the slight THD increase.

Converter [36] also offers advantages such as low number of semiconductor devices, which can help reduce costs and simplify the overall circuit design. However, it lacks the buck-boost operation of the proposed converter. Additionally, it operates in two stages of power processing, potentially impacting overall efficiency.

Converter [6], on the other hand, shares the advantage of a single-stage power conversion with the proposed converter, simplifying the design and reducing complexity. It also has a low number of semiconductor devices, contributing to cost savings. However, it lacks both the buck-boost operation and the reactive power capability. Additionally, it employs a flying capacitor inverter, which may introduce core loss.

Converter [7] offers the advantage of buck-boost operation, similar to the proposed converter, allowing for voltage regulation. It also operates in a single stage, simplifying the circuit design. However, it lacks the reactive power capability and has a high number of semiconductor devices, which can increase costs and complexity.

Converter [37] shares the advantages of buck-boost operation and reactive power capability with the proposed converter. However, it employs a flying capacitor inverter and operates in two stages, potentially impacting efficiency and introducing complexity.

Another comparison can be made between the proposed converter and its main competitors based on the normalized rms value of total voltage stress (TVS_{rms}/V_{PV}) and the normalized rms value of total current stress of semiconductor

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devices (TCS_{rms}/I_g). The comparisons are presented in Table II and shown in Figs. 6 and 7, respectively where the TVS and TCS are plotted vs. voltage gain ratio. It can be seen that depending on the voltage gain ratio, the proposed converter can be either better or worse than previous converters. At lower gains, the proposed converter outperforms the competitors. For example the proposed converter offers the lowest TVS_{rms}/V_{PV} when the gain voltage in lower than 0.5 and 1.0 during positive and negative half cycles, respectively.

Also, TCS_{rms}/I_g of the proposed converter is lower than converter in [21], [22], [26], and [27] type-III during the positive half cycle and lower than TCS of [27] type-IV at the voltage gains higher than 2.0. It can be seen that the TCS_{rms}/I_g of converters in [21], [22], [26] and converter in [25] during negative half cycle, is lower than the proposed converter although the converters in [22], [25]–[27], have one more semiconductor device and are not able to support reactive power.

It is also useful to compare the high frequency switching semiconductor device count of the proposed converter and the main competitors. As shown in Table. I, it is clear that the proposed converter has only two high frequency switching semiconductor devices during each mode which is the lowest compared to all the other FI PV inverters.

It is also worth noting that, unlike the previously published FI inverters, the proposed inverter uses only dc type capacitors in the structure which can reduce the volume and cost of the PV inverter.

Furthermore, as will be shown in section VI, the measured maximum efficiency of the proposed converter is 97.2%, the leakage current is eliminated and it provides RPC. In summary the proposed converter presents a good balance between the component count, number of high frequency switching components, semiconductor device ratings, common ground between PV side and the output terminals and efficiency which makes it a practical solution for PV power converter units.

The advantages and disadvantages of the proposed converter, in comparison with the primary common-ground inverters, are outlined in Table III. Specifically, converters referenced in [21], [22], [24]–[26], [37] lack the capability for reactive power exchange with the AC grid. Additionally, converters cited in [35] lack both buck and boost capabilities. Moreover, converters referenced in [11], [22], [24]–[27], [37] utilize a greater number of semiconductor devices compared to the proposed converter.

V. Control System Design

The control system is based on a deadbeat controller which includes the control of the grid side current during both positive and negative power regions. It is assumed that the reference value of grid side current amplitude and phase i.e. I_g^* and ϕ^* is calculated by a maximum power point tracking (MPPT) loop and the volt-var setting of IEEE-1547-2018, respectively, which are not described here. As shown in Fig. 8(a), from v_g and i_g the duration of the positive or negative power regions can be determined and if operation is in the NPR then NPR=1. If NPR=1 then the control diagram as shown in Fig. 8(b) applies and the duty cycle is calculated

TABLE I
Comparison among main Common Ground Inverters

Ref.	Number of Elements†	Conducting S or D @ modes and half-cycles	High Freq S or D @ modes and half-cycles	$\frac{v_{out}}{V_{PV}}$	Main test results RPC?
Proposed	6 S 1 D 2 L, 2 C	+, I: 4, 4 +, II: 4, 4 −, III: 4, 4	+, I: 2 +, II: 2 −, III: 2	$d, \frac{1}{1-d}$ $\frac{-d}{1-d}$	180, $100V_{dc}$,$110V_{ac}$ $500W$,$20kHz$ η_{max}:97.2% THD:3.1% RPC:✓
[21]	5 S 2 D 2 L, 2 C	+: 2, 4 −: 2, 3	+: 6 −: 3	$\frac{\pm d}{1-d}$	NA RPC:×
[22]	5 S 3 D 2 L, 2 C	+: 2, 4 −: 2, 3	+: 6 −: 3	$\frac{\pm d}{1-d}$	$92V_{dc}$,$100V_{ac}$ $193W$,$10kHz$ η_{max}:− THD:4.9% RPC:×
[26]	5 S 3 SD 2 L, 2 C	+: 2, 4 −: 2, 3	+: 6 −: 3	$\frac{\pm d}{1-d}$	$200V_{dc}$,$220V_{ac}$ $200W$, $20kHz$ η_{max}:< 96% THD:− RPC:×
[24]	8 S 0 D 2 L, 2 C	+: 2, 4 −: 2, 3	+: 6 −: 3	$\frac{\pm d}{1-d}$	$100V_{dc}$,$220V_{ac}$ $200W$, $10kHz$ η_{max}:95% THD:3.3% RPC:×
[25]	5 S 3 D 2 L, 2 C	+, I: 3, 4 +, II: 2, 3 −, III: 2, 3	+, I: 3 +, II: 3 −, III: 3	$d, \frac{1}{1-d}$ $\frac{-d}{1-d}$	200, $130V_{dc}$,$110V_{ac}$ $500W$, $40kHz$ η_{max}:98.81% THD:4.28% RPC:×
[11]	3 S 6 D 3 L, 3 C	+: 2, 4 −: 2, 3	+: 4 −: 4	$\frac{\pm d}{1-d}$	180, $100V_{dc}$,$110V_{ac}$ $500W$, $20kHz$ η_{max}:97.5% THD:3% RPC:✓
[27] I	9 S 0 D 2 L, 2 C	+, I: 3, 4 +, II: 3, 3 + : 3, 4 − : 3, 4	+, I: 3 +, I: 4 +: 7 −: 3	$d, \frac{1}{1-d}$ $\frac{\pm d}{1-d}$	NA RPC:✓
[27] III	8 S 0 D 2 L, 2 C	+, I: 4, 3 +, II: 4, 4 + : 4, 3 − : 3, 3	+, I: 2 +, I: 4 +: 6 −: 3	$d, \frac{1}{1-d}$ $\frac{\pm d}{1-d}$	100, $400V_{dc}$,$230V_{ac}$ $2kW$, $25kHz$ η_{max}:97.5% THD:− RPC:✓
[27] IV	8 S 0 D 2 L, 2 C	+, I: 3, 3 +, II: 3, 3 +: 3, 3 −: 3, 3	+, I: 2 +, II: 4 +: 6 −: 4	$d, \frac{1}{1-d}$ $\frac{\pm d}{1-d}$	NA RPC:✓
[35] III	2 S 0 D 2 L, 2 C	+: 1, 1 −: 1, 1	+: 2 −: 2	$\frac{1-2d}{1-d}$	$400V_{dc}$,$220V_{ac}$ $1kW$, $50kHz$ η_{max}:95.25% THD:− RPC:✓
[6]	4 S 2 D 3 L, 2 C	+: 1, 2 −: 2, 2	+: 1 −: 1	d $\frac{-d}{1-d}$	$180V_{dc}$,$110V_{ac}$ $350W$,$37kHz$ η_{max}:98.55% THD:2.53% RPC:×
[7]	5 S 3 D 3 L, 3 C	+, I: 2, 3 +, II: 2, 2 −, III: 2, 2	+, I: 3 +, II: 2 −, III: 2	$d, \frac{1}{1-d}$ $\frac{-d}{1-d}$	$192V_{dc}$,$110V_{ac}$ $450W$,$75kHz$ η_{max}:97.22% THD:1.81% RPC:×
[37]	5 S 1 D 2 L, 2 C	+: 3, 3, 2 −: 3, 3, 2	+: 3 −: 3	$\frac{d}{1-d}$ $\frac{-d}{1-d}$	$75V_{dc}$,$110V_{ac}$ $1000W$,$10kHz$ η_{max}:96% THD:2.18% RPC:×
[36]‡	4 S 0 D 2 L, 2 C	+: 3, 3 −: 3, 3	+: 4 −: 4	$\frac{d_i - d_b}{1-d_b}$	$400V_{dc}$,$240V_{ac}$ $3\ kVA$,$75kHz$ η_{max}:< 97% THD:2.1% RPC:✓

† S: switch, D: diode, SD: series body diode, L: inductor, C: capacitor.
‡ d_i: inverter stage duty-cycle in [36] and d_b: boost stage duty-cycle in [36].

TABLE II
RMS VALUE OF TOTAL VOLTAGE AND CURRENT STRESS

Ref.	TVS_{RMS}/V_{PV} ± half cycle	TCS_{RMS}/i_g ± half cycle
Proposed	$(2d+1)$, $\frac{3-d}{1-d}$, $\frac{\lvert 2d+1\rvert}{1-d}$	$\sqrt{16-7d}$, $\frac{1}{1-d}\sqrt{\begin{array}{c}d(4-2d)^2+\\9(1-d)\end{array}}$, $\frac{1}{1-d}\sqrt{\begin{array}{c}8d^3-23d^2\\+10d+9\end{array}}$
[21]	$\frac{1+d}{1-d}$, $\frac{\lvert 4d-1\rvert}{1-d}$	$\frac{1}{1-d}\sqrt{16-7d}$, $\frac{1}{1-d}\sqrt{9-5d}$
[22]	$\frac{1}{1-d}\sqrt{\begin{array}{c}d(1+\lvert 2d-1\rvert)^2+\\(1-d)(1+d)^2\end{array}}$, $\frac{1}{1-d}\sqrt{\begin{array}{c}d(1+\lvert 2d-1\rvert)^2+\\(1-d)(4d-1)^2\end{array}}$	$\frac{1}{1-d}\sqrt{16-12d}$, $\frac{1}{1-d}\sqrt{9-5d}$
[26]	$\frac{1}{1-d}\sqrt{\begin{array}{c}d(1+\lvert 2d-1\rvert)^2+\\(1-d)(1+d)^2\end{array}}$, $\frac{1}{1-d}\sqrt{\begin{array}{c}d(1+\lvert 2d-1\rvert)^2+\\(1-d)(4d-1)^2\end{array}}$	$\frac{1}{1-d}\sqrt{16-12d}$, $\frac{1}{1-d}\sqrt{9-5d}$
[25]	$\sqrt{4d+(1-d)(2d+1)^2}$, $\frac{2}{1-d}$, $\frac{1}{1-d}\sqrt{\begin{array}{c}d(1+\lvert 2d-1\rvert)^2+\\(1-d)(4d-1)^2\end{array}}$	$\sqrt{16-7d}$, $\frac{1}{1-d}\sqrt{9-5d}$, $\frac{1}{1-d}\sqrt{9-5d}$
[27] III	2, $\frac{1}{1-d}\sqrt{d(3-2d)^2+4(1-d)}$, $\frac{1}{1-d}\sqrt{\begin{array}{c}d(2-d)^2+\\(1-d)(1+\lvert 2d-1\rvert)^2\end{array}}$, $\frac{1}{1-d}\sqrt{\begin{array}{c}d(2-2d+\lvert 2d-1\rvert)^2+\\(1-d)(1+\lvert 2d-1\rvert)^2\end{array}}$	$\sqrt{9+7d}$, $\frac{4}{1-d}$, $\frac{1}{1-d}\sqrt{9+7d}$, $\frac{3}{1-d}$
[27] IV	2, $\frac{1}{1-d}\sqrt{d(3-2d)^2+4(1-d)}$, $\frac{1}{1-d}\sqrt{\begin{array}{c}d(2-d)^2+\\(1-d)(1+\lvert 2d-1\rvert)^2\end{array}}$, $\frac{1}{1-d}\sqrt{\begin{array}{c}d(2-2d+\lvert 2d-1\rvert)^2+\\(1-d)(1+\lvert 2d-1\rvert)^2\end{array}}$	3, $\frac{3}{1-d}$, $\frac{3}{1-d}$, $\frac{3}{1-d}$

TABLE III
PROS AND CONS OF MAIN COMMON GROUNDED INVERTERS

Ref.	Pros (✓) and Cons (×)
Proposed	✓ Buck-boost operation ✓ Reactive power capability ✓ Flying inductor inverter ✓ Single-stage power converter
[21]	✓ Buck-boost operation × No reactive power capability ✓ Flying inductor inverter ✓ Single-stage power converter
[22], [26], [24], [25]	✓ Buck-boost operation × No reactive power capability ✓ Flying inductor inverter ✓ Single-stage power converter × High number of semiconductor devices
[35] type-4	× Buck-boost operation ✓ Reactive power capability ✓ Flying inductor inverter ✓ Single-stage power converter
[35] type-1,2,3	× Buck-boost operation ✓ Reactive power capability × Flying capacitor inverter ✓ Single-stage power converter
[11]	✓ Buck-boost operation ✓ Reactive power capability ✓ ± output dc-dc converter ✓ Single-stage power converter × High number of semiconductor devices
[27]	✓ Buck-boost operation ✓ Reactive power capability ✓ Flying inductor inverter ✓ Single-stage power converter × High number of semiconductor devices
[37]	✓ Buck-boost operation × Reactive power capability ✓ Flying inductor inverter ✓ Single-stage power converter

using equations (64) and (65) depending on whether the grid v_g voltage is positive or negative, respectively.

When NPR≠1 and $v_g \geq 0$ then the converter will operate in either mode-I or mode-II depending on whether the instantaneous value of grid voltage is lower or higher than V_{PV}. The optimal duty cycle of mode-I or mode-II can be calculated using equation (61) and (62) respectively. Similarly, when NPR≠1 and $v_g < 0$, the optimal duty cycle for mode-III operation will be calculated according to equation (63). The overall diagram of the proposed control system during the positive power region is shown in Fig. 8(c).

After determining $d(t)$ for all three modes and NPR, the PWM module generates the gate signals for the switches.

In the inner current control loop, a simple fast and effective digital dead-beat current control system is adopted to calculate the duty cycles for all modes [38]–[41].

During the positive power mode, the controller regulates the ac side current indirectly by controlling the current though the flying inductor L. The reference for the flying inductor current is established with equation (66) and the phase information provided by the PLL. The outputs of equation (66) becomes a reference for the inner current control loop. The optimal duty cycle, for the FI converter can therefore be determined from the measured V_{PV} and v_{out} voltage, and the measured and reference current through the flying inductor L. During the NPR the controller directly regulates the current through the output filter inductor L_g.

In the outer loop, the grid or reference voltage is fed to the PLL to determine the phase angle of the ac voltage i.e. ω. By using I_g^* and $\sin(\omega t+\phi^*)$, the reference value of instantaneous ac current can be obtained. The relationships necessary for calculating the duty cycles in the various modes are described in the following. During mode-I and in the positive half cycle, when S_1 is ON, the voltage across the flying inductor L can be determined as

$$v_L = L\frac{di_L}{dt} = V_{PV} - v_{out} \tag{38}$$

Therefore, the slope of L current during S_1 ON-state in mode-I ($\delta_{I,ON}$) is

$$\delta_{I,ON} = \frac{di_L(t)}{dt} = \frac{V_{PV} - v_{out}}{L} \tag{39}$$

When S_1 is OFF and D is conducting, the inductor voltage

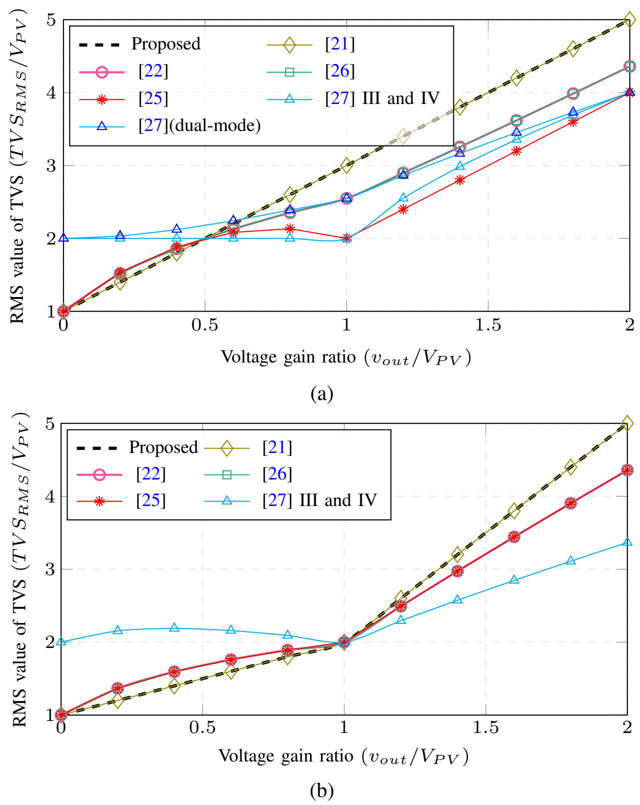

Fig. 6. RMS value of TVS during: (a) Positive and (b) Negative half-cycles.

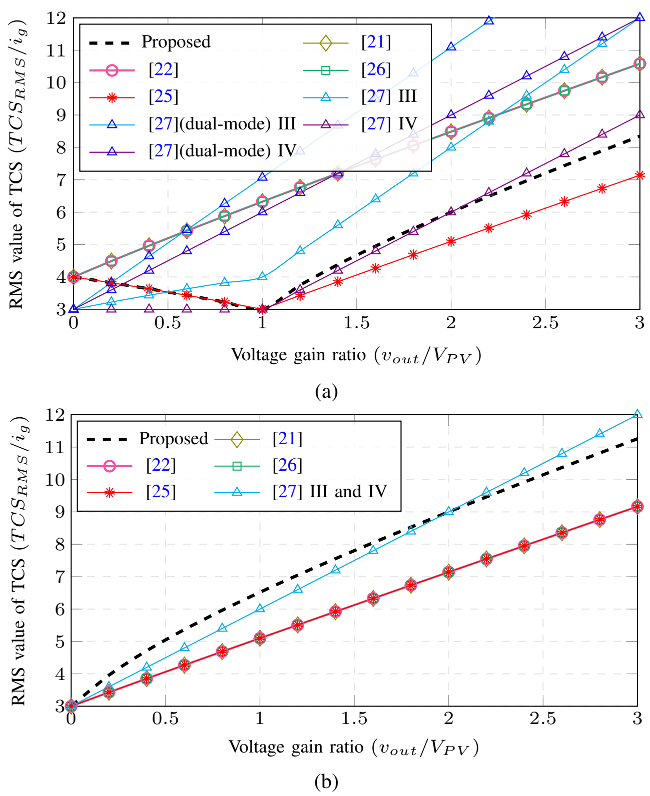

Fig. 7. RMS value of TCS during: (a) Positive and (b) Negative half-cycles.

is

$$v_L = L\frac{di_L}{dt} = -v_{out} \tag{40}$$

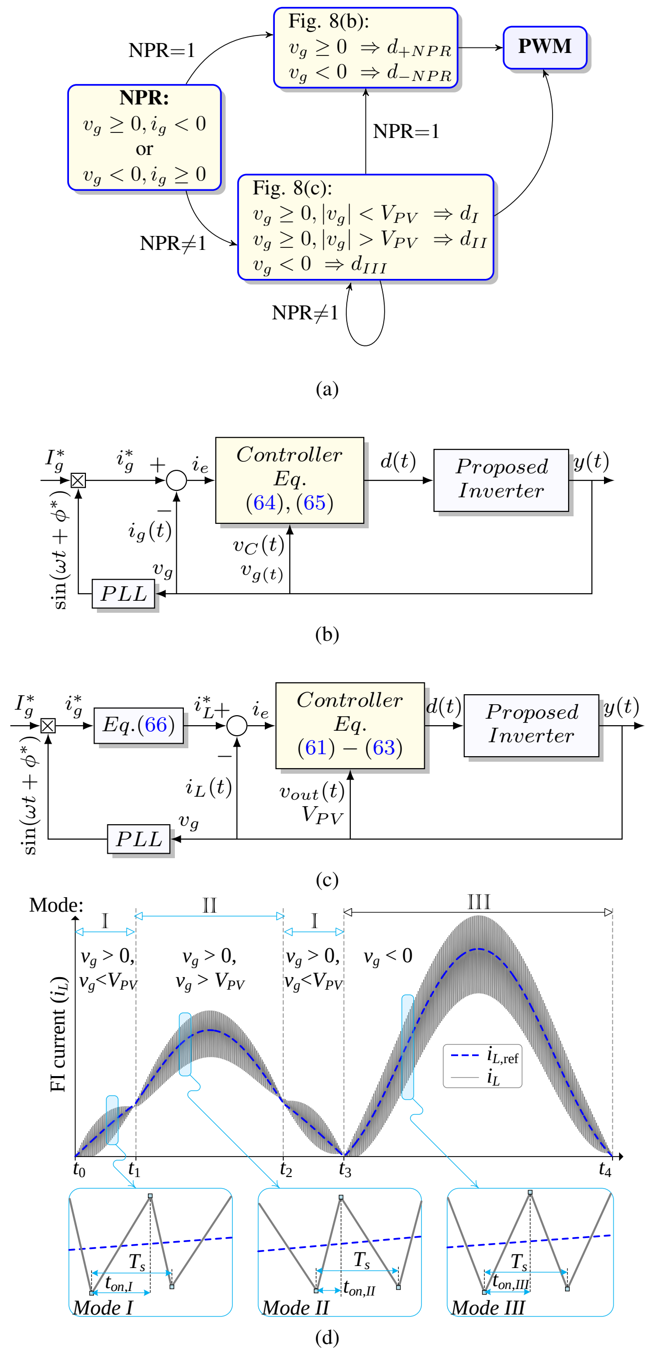

Fig. 8. (a) Proposed control system diagram, (b) control system during negative and (c) positive power region, (d) variation of the flying inductor current $i_L(t)$.

and slope of i_L when S_1 is OFF ($\delta_{I,OFF}$) can be expressed as

$$\delta_{I,OFF} = \frac{di_L(t)}{dt} = \frac{-v_{out}}{L} \tag{41}$$

Similarly, during mode-II in the positive half cycle, when the switch S_2 is ON, the voltage across L can be expressed as

$$v_L = L\frac{di_L}{dt} = V_{PV} \tag{42}$$

and when S_2 is OFF, the inductor voltage is

$$v_L = L\frac{di_L}{dt} = V_{PV} - v_{out} \tag{43}$$

The slope of the L current during S_2 ON-state ($\delta_{II,ON}$) and OFF-state ($\delta_{II,OFF}$) can be expressed as

$$\delta_{II,ON} = \frac{di_L(t)}{dt} = \frac{V_{PV}}{L} \tag{44}$$

$$\delta_{II,OFF} = \frac{di_L(t)}{dt} = \frac{V_{PV} - v_{out}}{L} \tag{45}$$

During mode-III in the negative half cycle, when the switch S_1 is ON, the voltage across L can be expressed as

$$v_L = L\frac{di_L}{dt} = V_{PV} \tag{46}$$

and when S_1 is OFF, the inductor voltage is

$$v_L = L\frac{di_L}{dt} = v_{out} \tag{47}$$

The slope of the L current during S_1 ON-state ($\delta_{III,ON}$) and OFF-state ($\delta_{III,OFF}$) can be expressed as

$$\delta_{III,ON} = \frac{di_L(t)}{dt} = \frac{V_{PV}}{L} \tag{48}$$

$$\delta_{III,OFF} = \frac{di_L(t)}{dt} = \frac{v_{out}}{L} \tag{49}$$

In the NPR and during the time that the ac grid voltage is positive, the voltage across L_g and the current slope of L_g during S_6 ON-state ($\delta_{+NPR,ON}$) and OFF-state ($\delta_{+NPR,OFF}$) can be expressed as

$$v_{Lg} = L_g\frac{di_{Lg}}{dt} = -v_g \tag{50}$$

$$\delta_{+NPR,ON} = \frac{di_{Lg}(t)}{dt} = \frac{-v_g}{L_g} \tag{51}$$

$$v_{Lg} = L_g\frac{di_{Lg}}{dt} = v_C - v_g \tag{52}$$

$$\delta_{+NPR,OFF} = \frac{di_{Lg}(t)}{dt} = \frac{v_C - v_g}{L_g} \tag{53}$$

Similarly, in the negative power region and during the negative half-cycle of ac grid voltage, the voltage across L_g and the current slope of L_g during S_3 ON-state ($\delta_{-NPR,ON}$) and OFF-state ($\delta_{-NPR,OFF}$) can be expressed as

$$v_{Lg} = L_g\frac{di_{Lg}}{dt} = -v_g \tag{54}$$

$$\delta_{-NPR,ON} = \frac{di_{Lg}(t)}{dt} = \frac{-v_g}{L_g} \tag{55}$$

$$v_{Lg} = L_g\frac{di_{Lg}}{dt} = -v_C - v_g \tag{56}$$

$$\delta_{-NPR,OFF} = \frac{di_{Lg}(t)}{dt} = \frac{-v_C - v_g}{L_g} \tag{57}$$

As shown in Fig. 8(d), and based on predictive control theory, the flying inductor current i_L at the next sampling time ($i_L[k+1]$) can be calculated from its current value ($i_L[k]$), using the ON-state and OFF-state slopes of mode-j ($j \in$ mode-I, II, III), i.e.,

$$i_L[k+1] = i_L[k] + \delta_{j,ON}t_{ON} + \delta_{j,OFF}(1 - t_{ON}) \tag{58}$$

where t_{ON} is the S_1 or S_2 ON-state dwell time.

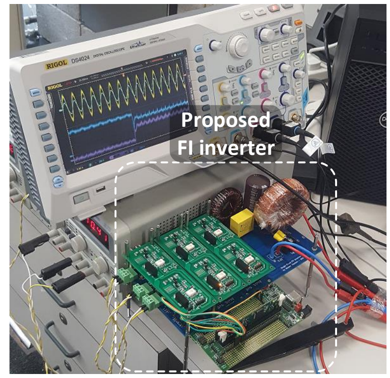

Fig. 9. Experimental prototype of the proposed TMCGFI inverter.

The controller is intended to eliminate the error i_e between the reference FI current (i_L^*) and $i_L[k+1]$ [42]–[45], which translates to

$$\begin{gathered} i_e = i_L^* - i_L[k+1] = 0 \Rightarrow \\ i_L^* - i_L[k] - \delta_{j,ON}[d_j(t)]T_s - \delta_{j,OFF}[1 - d_j(t)]T_s = 0 \end{gathered} \tag{59}$$

Then, t_{ON} and consequently, the optimal duty cycle can be obtained as

$$d_j(t) = \frac{(i_L^* - i_L[k]) - \delta_{j,OFF}T_s}{(\delta_{j,ON} - \delta_{j,OFF})T_s} \tag{60}$$

$$d_{mode-I}(t) = \frac{L(i_L^* - i_L[k]) + v_{out}T_s}{V_{PV}T_s} \tag{61}$$

$$d_{mode-II}(t) = \frac{L(i_L^* - i_L[k]) - (V_{PV} - v_{out})T_s}{v_{out}T_s} \tag{62}$$

$$d_{mode-III}(t) = \frac{L(i_L^* - i_L[k]) - v_{out}T_s}{(V_{PV} - v_{out})T_s} \tag{63}$$

Similarly, in the negative power region we have

$$d_{+NPR}(t) = \frac{L_g(i_g^* - i_g[k]) - (v_C - v_g)T_s}{-v_C T_s} \tag{64}$$

$$d_{-NPR}(t) = \frac{L_g(i_g^* - i_g[k]) + (v_C + v_g)T_s}{v_C T_s} \tag{65}$$

Note that the average current through the inductor L in each mode is equal to the average current injected into the grid since the average current of C is zero in the steady state. Therefore, one can readily conclude that

$$i_L^* = \begin{cases} |i_g^*| & Mode-I \\ |i_g^*|\dfrac{|v_g|}{V_{PV}} & Mode-II \\ |i_g^*|\dfrac{V_{PV} + |v_g|}{V_{PV}} & Mode-III \end{cases} \tag{66}$$

where i_g^* is the reference grid current.

VI. Experimental Verification

To confirm the proper operation of the proposed common ground triple-mode FI PV inverter, a laboratory hardware prototype shown in Fig. 9 has been made. The specifications of the proposed converter and component parameters are presented in Table IV.

TABLE IV
EXPERIMENTAL TEST CONDITIONS AND PARAMETERS

Parameters	Values
Rated power (P_{out}):	500 [W]
Switching frequency (f_s):	20 [kHz]
Grid side voltage (v_g):	110 [V] and 50 [Hz]
PV side voltage (V_{PV}):	100 [V] and 180 [V]
Inductors L and L_g:	1.0 [mH] and 0.4 [mH]
DC Capacitors C and C_{dc}:	2.2 [μF] and 1000 [μF]
MOSFET switches:	IPW60R017C7
Diode:	STTH30L06C
Microcontroller:	Piccolo TMS320F28035

Figure 10(a) illustrates the steady-state performance under unity power factor mode and with output power references of 500 W and 0 Var. It can be seen that the PV side voltage is 100 V and the grid current is 4.54 A. Figures 10(b) and (c) show the steady state operation under 0.8 leading and lagging power factor, respectively (or 400 W and ±300 Var). It is evident from Fig. 10 that the proposed TMCGFI inverter injects highly sinusoidal ac current with total harmonic distortion (THD)≤5% even during the non-unity power factor operation and considering that the ac grid voltage is also slightly distorted.

The transient performance of the proposed FI converter and dead-beat control system from unity (500W and 0Var) to non-unity power factors (400W and ±300Var) has been investigated experimentally and the results are shown in Fig. 11. A fast and smooth transient response, from unity power factor to 0.8 lagging is confirmed in Fig. 11(a), and from unity power factor to 0.8 leading is shown in Fig. 11(b).

The transient response to a step change in the reference ac grid side power is presented in Fig. 12. Clearly a fast-dynamic current performance is achieved and this verifies that the indirect dead-beat controller, as already expected, offers a high dynamic performance in response to any changes.

With a closer look at the ac side current waveform, one can detect a very smooth mode transition from the negative to positive half-cycle or from mode-III to mode-I operation as shown in Fig. 15(a). Figure 15(b) shows the zoomed-in view of the grid side current and flying inductor current following a transition from mode-I to mode-II. This ensures that the THD of the proposed converter current remains lower than 5% and in fact the THD of injected grid side current is 3.1%. The measured grid side current harmonic spectrum under rated output power level is shown in Fig. 13. Clearly, the grid current harmonic components are well below the IEEE 1547 limit.

Based on the approach used in [11], [26], the measured leakage current waveform through the parasitic capacitors C_p and C_n of the PV side are shown in Fig. 14. As we expect, the leakage current of the proposed common ground inverter is negligible (7 mA).

The voltage waveforms of capacitor C and the flying inductor L have been depicted in Fig. 16. As already expected, the voltage across C is unipolar. Therefore, in this part of the circuit instead of an ac type, a dc type capacitor can be used and hence, the physical volume and the cost of the proposed converter is further improved.

TABLE V
EXPERIMENTAL TEST RESULTS

Test conditions:	THD:	$\Delta i_{g,max}$:	TVS:	TCS:
Unity PF, V_{PV}=100V	3.4%	0.33A	569.78V	34.41A
Unity PF, V_{PV}=180V	3.1%	0.33A	947.12V	28.17A
0.8 leading PF, V_{PV}=100V	4.62%	0.8A	582.02V	32.32A
0.8 leading PF, V_{PV}=180V	4.38%	0.8A	695.72V	27.95A
0.8 lagging PF, V_{PV}=100V	4.55%	0.7A	598.89V	32.79A
0.8 lagging PF, V_{PV}=180V	4.43%	0.7A	717.63V	27.66A

Figure 17 illustrates the PV side current under both unity and non-unity power factors.

The transient response to a step change in the grid voltage, transitioning from 110V to 220V, under a constant current mode of 9.09A, is depicted in Fig. 18. It is evident from the figure that the proposed converter demonstrates the capability to operate effectively under higher power levels, specifically at 1kW and 2kW. Furthermore, by adjusting the PV side voltage from 84.6V to 100.3V. Fig. 19 demonstrates the capability of the proposed inverter to function effectively with a real PV voltage profile.

Measured peak efficiencies of 96.8% and 97.2% are achieved for the proposed converter when V_{PV} = 100 V and 180 V, respectively and these peak efficiencies occur at 500 W loading which can be seen from Fig. 20. The CEC (California Energy Commission) and EU (European Union) measured efficiency of the proposed converter is 96.26% and 95.78%, respectively. The power loss breakdown of the proposed converter at the peak efficiency is presented in Fig. 21. As observed, the major portion of the power loss is attributed to the conduction loss of switches, indicating its significance in the overall power loss distribution.

A summary of the experimental results is presented in Table V. Under unity power factor conditions, the Total Harmonic Distortion (THD) of i_g is measured at 3.4% and 3.1% for PV voltages of 100V and 180V, respectively. For leading power factor conditions, the THD of the current with PV voltages of 100V and 180V is illustrated, measuring at 4.62% and 4.38%, respectively. Similarly, under lagging power factor conditions, with PV voltages of 100V and 180V, the THD values are recorded at 4.55% and 4.43%, respectively. Furthermore, Table V provides information on the maximum ripple of the grid current ($\Delta i_{g,max}$) during unity, leading, and lagging power factor conditions, measured at 0.33A, 0.8A, and 0.7A, respectively. The Table V shows the TVS and TCS ratings of the semiconductor devices used in the proposed converter. The maximum TVS and TCS ratings are recorded as 947.12V and 34.41A, respectively.

VII. CONCLUSION

In this paper, the flying inductor based common ground PV inverter with the capability of supporting reactive power provision to the ac grid is presented. This converter also has the benefits of using a low number of semiconductor devices with no ac type capacitor. The proposed converter does not require an AC capacitor and has a relatively small

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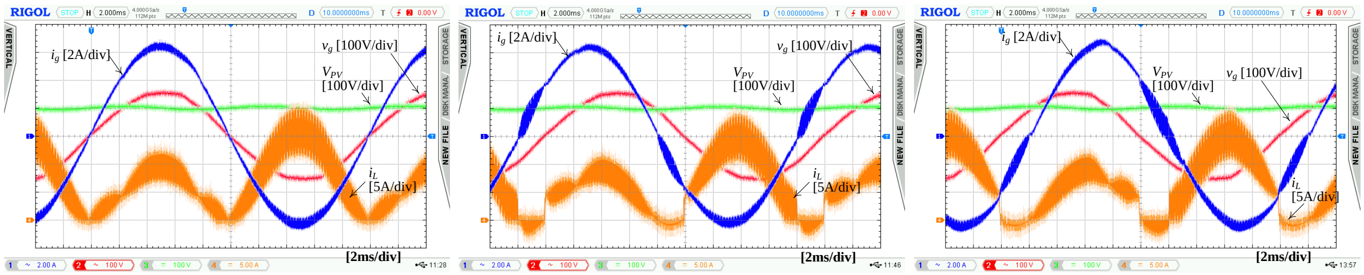
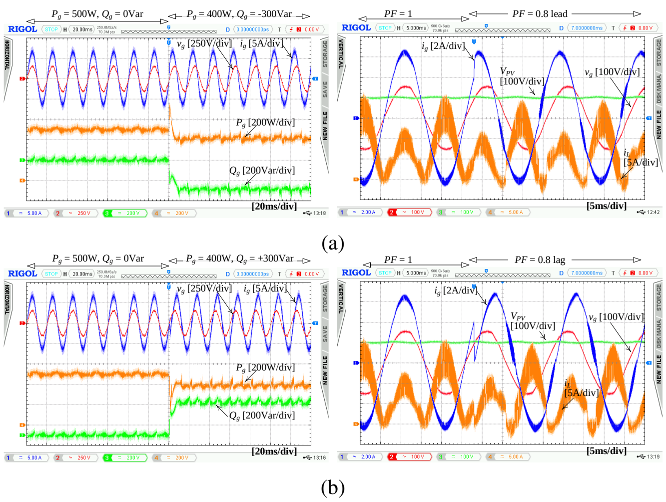


(a) (b) (c)

Fig. 10. Waveforms of V_{PV}, v_g, i_g and i_L for (a) $P_{out} = 500$ W and $Q_{out} = 0$ Var ($PF = 1$), (b) $P_{out} = 400$ W and $Q_{out} = 300$ Var ($PF = 0.8$ leading) and (c) $P_{out} = 400$ W, $Q_{out} = 300$ Var ($PF = 0.8$ lagging).



(a)

(b)

Fig. 11. Transient waveforms from unity to (a) 0.8 leading and (b) 0.8 lagging power factors.

grid filter inductor, resulting in a relatively small volume. Switching losses are reduced by adopting the triple mode time sharing technique. The proposed converter has utilized the combination of both indirect and direct dead-beat current controllers during positive and negative power region, respectively which ensures accurate and fast control of the grid side current. Active and reactive power regulation and different transient and steady state responses have been successfully demonstrated using the developed prototype. The prototype converter has a maximum efficiency of 97.2% and 96.8% at V_{dc} = 180 V and 100 V, V_{rms} = 110 V, P_{out} = 500 W, and f_s = 20 kHz. The measured waveforms from the prototype have validated the theoretical analysis and confirmed the superior operation of the proposed converter.

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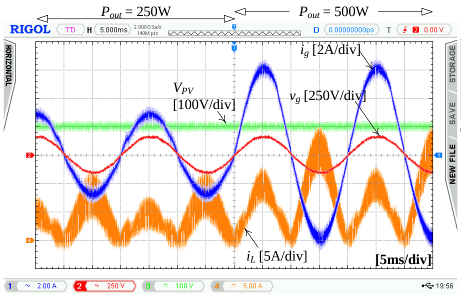


Fig. 12. Transient waveforms in response to power jump from 250 to 500W grid side power.

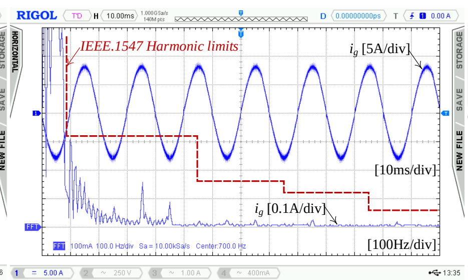


Fig. 13. Harmonic spectrum of the grid side current at the rated power.

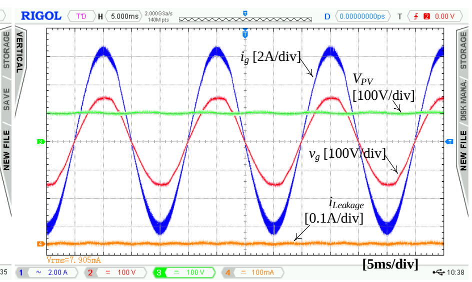
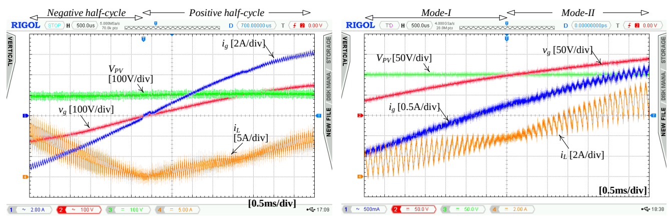


Fig. 14. The leakage current waveform.



(a) (b)

Fig. 15. Zoomed-in view of transient from (a) negative (mode-III) to positive (mode-I) half cycle and (b) from mode-I to mode-II.

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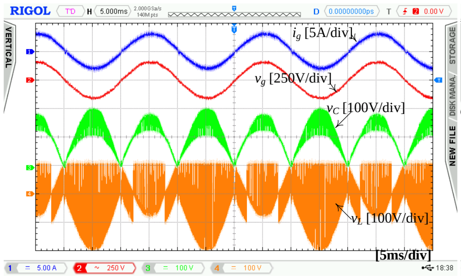

Fig. 16. The voltage waveforms of C and L.

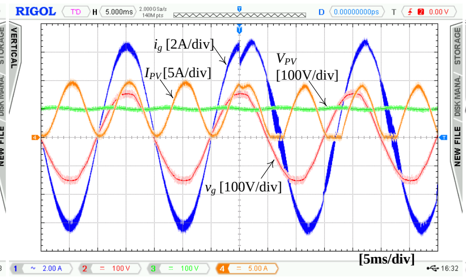

Fig. 17. The measured PV side current (I_{PV}) of the proposed converter.

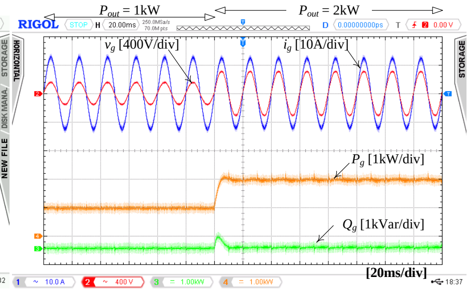

Fig. 18. Waveforms i_g, v_g, P_g, and Q_g for grid side power ranging from 1kW to 2kW.

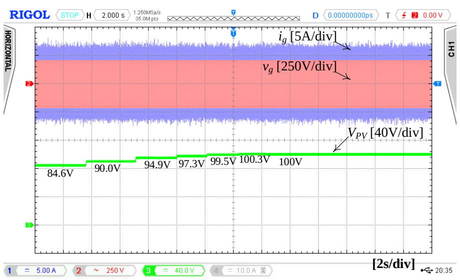

Fig. 19. Waveforms a real PV voltage, grid voltage and injected current.

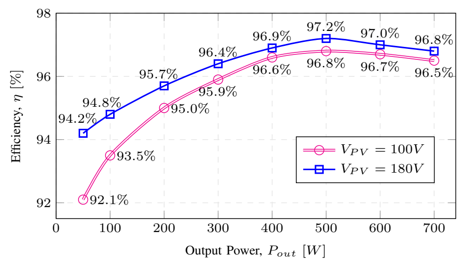

Fig. 20. Proposed FI converter efficiency curve versus output power levels.

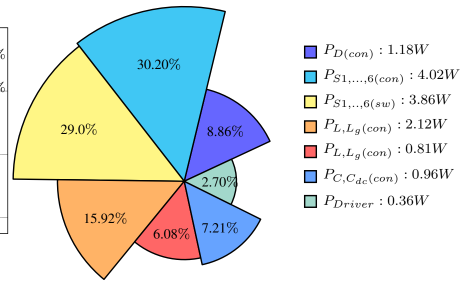

Fig. 21. Power loss break down of the proposed converter at η_{max}.

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