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Impact of In-Situ Cd Saturation MOCVD Grown CdTe Solar Cells on As Doping and V_{OC}

Ochai Oklobia, Steve Jones, Giray Kartopu, Dingyuan Lu, Wes Miller, Rajni Mallick, Xiaoping Li, Gang Xiong, Vladislav Kornienko, Ali Abbas, Martin Bliss, John Michael Walls, and Stuart J. C. Irvine

***Abstract*—In-situ Cd-saturated growth of polycrystalline CdTe:As thin film was performed by metal organic chemical vapour deposition at a low temperature of 350 °C, to investigate the impact on As doping and device V_{OC}. Device characterization showed conversion efficiency of ∼14%, and V_{OC} of 772 mV, which is an improvement to the baseline device with CdTe:As absorber layer grown at 390 °C under non-saturated conditions. When the low temperature Cd-saturated growth was combined with chlorine heat treatment at a higher temperature of 440 °C (in contrast with the standard 420 °C) for 10 min, device efficiency improved to ∼17% with a high V_{OC} of 877 mV. As a result, ∼100 mV boost in V_{OC} from baseline is demonstrated with Cd-saturated CdTe:As device. Micro-photoluminescence and time-resolved photoluminescence measurements performed on these Cd-saturated CdTe:As devices confirmed that minority carrier lifetime significantly improved.**

***Index Terms*—As doping, Cd-saturated, CdTe, metal organic chemical vapour deposition (MOCVD), open circuit voltage, solar cells, thin films.**

I. Introduction

CADMIUM telluride solar cells are the leading thin film photovoltaic (PV) production technology with small area record efficiency of ∼22.1% and module performance of 19% [1], making it very cost competitive with monocrystalline Si PV technology [2]. Even with such impressive progress in performance over a short period of time compared with Si PV technology, cell efficiencies are still well below the theoretical maximum of ∼30% [3]. Much of this deficit is because of the relatively poor V_{OC}. Recent improvements in the efficiencies of polycrystalline CdTe thin film solar cells have been attributed to a graded absorber layer using Se incorporation [4], [5], yielding improved long wavelength photocurrent collection with device short circuit current density (J_{SC}) values approaching the theoretical maximum [6], [7]. The open circuit (V_{OC}) deficit on the other hand, remains a challenge to overcome, and has been receiving much attention [8], [9]. In polycrystalline (px) CdTe thin film solar cells (TFSC), V_{OC} remains below 900 mV, at 25 °C [8]. Overcoming absorber doping concentration limits and minimizing recombination defects are necessary for further V_{OC} improvement [8], [9]. According to device modeling studies [10], acceptor densities $>10^{16}$ cm^{-3}, without compromising minority carrier lifetime, can result in V_{OC}s exceeding 1 V and enhance device efficiency to 25% [11]. With p-type doping concentration in Cu-doped CdTe absorber layers limited to less than $\sim10^{15}$ cm^{-3} [12]–[14] combined with stability issues, group V (As or P) doping has become a dominant and promising alternative route to increased hole density, accessing doping levels as high as 10^{16}–10^{17} cm^{-3} in px CdTe [7], [9], [15]. Incorporation of group V dopant atoms such as As or P into the CdTe lattice requires Te site availability (V_{Te}) for As_{Te} (or P_{Te}) substitutional doping under Cd-rich conditions [14], [16]. McCandless et al. [8] reported in-situ p-type (As) doping of px CdTe by vapour transport deposition (VTD), with acceptor concentration exceeding 10^{15} cm^{-3}, but minority carrier lifetime was limited to below 2 ns. Recent laboratory studies [15] demonstrated hole density as high as $\sim3 \times 10^{16}$ cm^{-3} with in-situ As doped px CdTe under Cd-rich growth conditions by metal organic chemical vapour deposition (MOCVD), but lifetimes were also limited to 1–2 ns. The impact of Cd-rich stoichiometry on minority carrier lifetimes was studied by Ma and co-workers [16]. Improvement in minority carrier lifetimes and hence device performance was shown with CdTe layers grown at a low temperature (484 °C), which is thermodynamically favorable for Cd-rich stoichiometry and energetically favors anion-site dopants. Depositing high quality px CdTe thin films is therefore crucial for efficient group V doping and consequently enhancing device efficiency.

In this work, in-situ Cd-saturated growth of px thin film CdTe:As absorbers was performed by MOCVD at a low temperature of 350 °C, to investigate the impact on As doping and device V_{OC}. MOCVD is particularly advantageous for controlled

Manuscript received 31 May 2022; revised 7 July 2022; accepted 19 July 2022. This work was supported in part by the Engineering and Physical Sciences Research Council, U.K. under Grant EP/W000555/1, in part by the European Regional Development Fund, in part by the Welsh European Funding Office for the 2nd Solar Photovoltaic Academic Research Consortium (SPARC II), and in part by First Solar, Inc. *(Corresponding author: Ochai Oklobia.)*

Ochai Oklobia, Steve Jones, and Stuart J. C. Irvine are with the Centre for Solar Energy Research, Faculty of Science and Engineering, Swansea University, SA2 8PP Swansea, U.K. (e-mail: ochai.oklobia@swansea.ac.uk; stephen.jones@swansea.ac.uk; s.j.c.irvine@swansea.ac.uk).

Giray Kartopu is with the Department of Mathematics, Physics and Electrical Engineering, Northumbria University, NE1 8ST Newcastle upon Tyne, U.K. (e-mail: giray.kartopu@northumbria.ac.uk).

Dingyuan Lu, Wes Miller, Rajni Mallick, Xiaoping Li, and Gang Xiong are with First Solar, Inc., Santa Clara, CA 95050 USA (e-mail: dingyuan.lu@firstsolar.com; david.miller@firstsolar.com; rajni.mallick@firstsolar.com; xiaoping.li@firstsolar.com; gxiong@firstsolar.com).

Vladislav Kornienko, Ali Abbas, Martin Bliss, and John Michael Walls are with the Centre for Renewable Energy Systems Technology, Loughborough University, LE11 3TU Loughborough, U.K. (e-mail: v.kornienko@lboro.ac.uk; a.abbas@lboro.ac.uk; m.bliss@lboro.ac.uk; j.m.walls@lboro.ac.uk).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JPHOTOV.2022.3195086.

Digital Object Identifier 10.1109/JPHOTOV.2022.3195086

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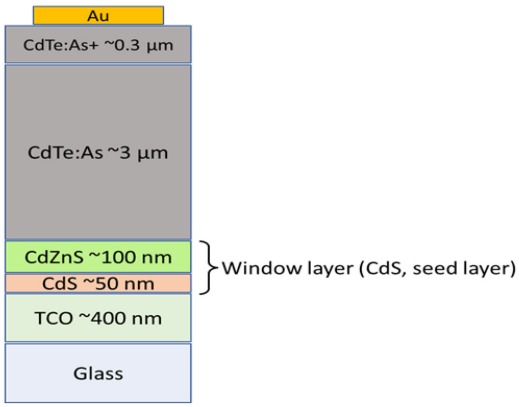

Fig. 1. Schematic of the MOCVD superstrate CdTe:As device structure.

compositional alloying and incorporation of dopants during (in-situ) thin film deposition [17] and is ideal in contrast with postdeposition (ex-situ) approaches, the latter resulting in inhomogeneous dopant distribution within the film [14]. The high quality px CdTe:As absorber layers deposited under thermodynamically saturated Cd conditions, combined with high temperature (440 °C) chlorine heat treatment (CHT) gained further enhancement in device efficiency, compared with the MOCVD grown baseline device fabricated under non-saturated conditions and subjected to lower CHT temperature (i.e., 420 °C). With this approach, a significant improvement was measured in the minority carrier lifetimes, increasing from below 1 to ∼3 ns. By optimizing the II/VI precursor partial pressure ratio during film deposition, ∼17% device efficiency was achieved with a ∼100 mV boost in V_{OC}.

II. Experimental

To establish Cd super-saturation over a substrate surface, an in-situ laser (633 nm) reflectometry set up [18] was used to monitor and detect Cd deposition as a function of temperature and concentration of the organometallic precursor for Cd, i.e., dimethylcadmium (DMCd). The method relied on a reduction in reflectivity from the glass substrate as Cd droplets condensed onto the surface when supersaturation was achieved. A fixed concentration of DMCd was introduced into the MOCVD reactor, using a H_2 carrier gas, at varying substrate temperatures in the range of 300 °C–360 °C (in steps of 5 °C). A similar scan was also performed for fixed substrate temperature and varying DMCd concentration. Dwell time for precursor flow was 5 min.

CdTe:As-based TFSC were fabricated in the superstrate configuration, according to the schematic in Fig. 1, using a horizontal MOCVD system, at atmospheric pressure, on transparent conducting oxide coated glass, supplied by First Solar, Inc. ∼50 nm CdS seed layer deposited at 315 °C was followed by ∼100 nm CdZnS deposited at 360 °C, using DMCd, diethylzinc, and ditertiarybutylsulphide organometallic precursors for Cd, Zn, and S with H_2 carrier gas. Upon device completion following the $CdCl_2$ treatment, these layers merge to yield a 150 nm thick n-type emitter layer with a graded CdZnS composition. This was followed by depositing a CdTe:As absorber under Cd-saturated conditions at a low temperature of 350 °C using an initial DMCd/diisopropyltelluride (DIPTe) partial pressure ratio of 3, with DMCd partial pressure of 0.236 Torr, at the Cd-rich phase boundary. DMCd, DIPTe, and tris-dimethylaminoarsine were used as the organometallic precursors for Cd, Te, and As, respectively, with H_2 carrier gas. The As concentration was increased to over 1×10^{19} cm^{-3} in the last 0.3 μm of the absorber deposition, herein referred to as the back contact layer, which helps to maintain low series resistance with the back contact metal. A CHT was performed on the completed device stack, without taking it out of the reactor. This involved deposition of ∼1 μm of $CdCl_2$ at 200 °C on the device structure and subsequent annealing at 420 °C for 10 min under a H_2 ambient. Tertiarybutylchloride was used as the organometallic precursor for Cl along with DMCd for Cd. Upon cooling down, the device structure was taken out of the MOCVD reactor, rinsed with deionized water to dissolve the excess $CdCl_2$, dried with N_2 gas and annealed at a low temperature (170 °C) for 90 min in air ambient [19]. Gold (Au) contact pads of approximately 0.5×0.5 cm^2 were thermally evaporated on the treated CdTe:As surface, to complete the solar cell.

AM 1.5 current density–voltage (J–V) measurements obtained with a Keithley 2400 source meter were performed using an Abet Technologies, Ltd., solar Sun 2000 solar simulator (Class A) with the light power density calibrated using a GaAs reference cell (ReRa Solutions). The capacitance–voltage (C–V) characteristics were measured in the dark using a Solartron Impedance Analyzer, with –4 to +2.0 V voltage sweep at 300 Hz with 20 mV amplitude applied. C–V derived acceptor concentration (N_A) was read from the value at the flat bottom part, i.e., trough, of the Mott–Schottky plot. External quantum efficiency (EQE) measurements were performed on a Bentham PV300 spectrometer, with system response calibrated with a certified c-Si reference detector.

Room temperature micro-photoluminescence (PL) measurements were performed with a Renishaw InVia confocal Raman microscope in backscattering configuration using a 532 nm green laser operated at a maximum power of 30 mW with a 50x objective (numerical aperture = 0.50, beam diameter ≈ 1 μm).

Secondary-ion mass spectroscopy (SIMS) of As was carried out using a Cameca IMS-4f instrument with Cs+ ion source operating at 10 keV energy and 20 nA current (LSA Ltd).

Sample cross sections for scanning transmission electron microscopy (STEM) were prepared using a gallium focused ion beam (FIB) with a dual beam FEI Nova 600 Nanolab. A standard in situ lift out method was used to prepare cross-sectional samples through the coating into the glass substrate. A platinum over-layer was deposited to define the surface and homogenize the final thinning of the samples down to ∼100 nm. Transmission electron microscopy (TEM) was undertaken using a Tecnai F20 operating at 200 kV to investigate the detailed microstructures of the cell cross sections. The system was equipped with an Oxford instruments X-max N80 TLE SDD EDX detector and this was used in STEM mode to collect elemental distribution maps. Details of the procedures followed are available elsewhere [20]. A Helios G4 Xe PFIB was used to carry out 3-D electron back scatter diffraction (EBSD) analysis. Samples were tilted

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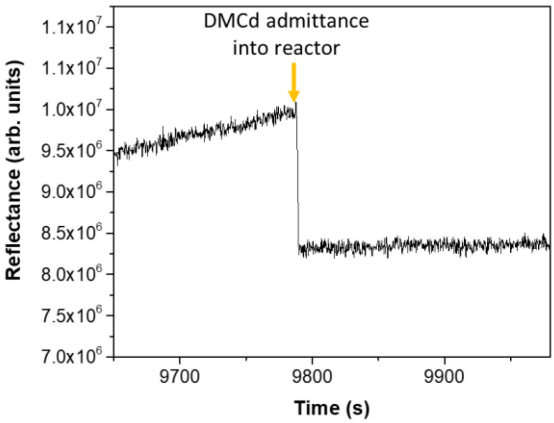

Fig. 2. Example of the change in normal incidence, in-situ, reflectivity because of condensation of Cd onto glass surface from the pyrolysis of DMCd at 360 °C substrate temperature.

to 54° for ion milling before performing EBSD scanning at 70° angle of orientation (mounted on a 36° pre-tilt holder). To protect the film during milling, a 3 μm layer of Pt layer was deposited at the cross-section edge. The ion milling current was set to 60 nA. EBSD scan was carried out at 10 kV and 6.4 nA with 85 nm step size.

Time-resolved photoluminescence (TRPL) was carried out by an in-house built system which included a PicoQuant PDL 800-B laser system. The excitation source is a 640 nm wavelength pulsed picosecond laser. For TRPL the laser intensity was "3.4" on an arbitrary unit scale with a pulse frequency of 2.5 MHz. The photomultiplier tube (PMT) used for TRPL measurement has a 230–920 nm range. The PL was analyzed between wavelengths 600–1000 nm , but was first measured with a laser intensity "4" and pulse frequency of 40 MHz. A Hamamatsu InGaAs photodiode (G10899-01K) with a wavelength range of 500–1700 nm, was used to measure the PL spectrum.

III. Results and Discussion

A. Determination of Cd Supersaturation Using MOCVD

An example of how the reflectivity changed when the DMCd is introduced to the MOCVD reactor at 360 °C and partial pressure of 0.368 Torr is given in Fig. 2. Under these conditions the pyrolysis of the DMCd was sufficient to yield an overpressure of Cd causing a reduction in reflectivity because of the condensation of Cd. The pyrolysis of DMCd will start around 300 °C (yielding very low pressure of Cd) and will be close to 100% at 350 °C yielding a Cd partial pressure close to the inlet DMCd partial pressure.

Starting at 300 °C, where no change of reflectance was observed, the temperature was increased in 5 °C increments, each time admitting a flow of DMCd and observing the change in reflectance. Fig. 3(a) shows a plot of ΔR/R, where R is the reflectance and ΔR is with respect to the previous data point in the graph, for a range of temperatures from 300 to 360 °C. The onset of a reflectance change occurred at 310 °C, indicating that for this pressure of DMCd the yield of Cd was sufficient to initiate Cd condensation. The increase in ΔR/R for higher temperatures indicates that the Cd overpressure continues to be

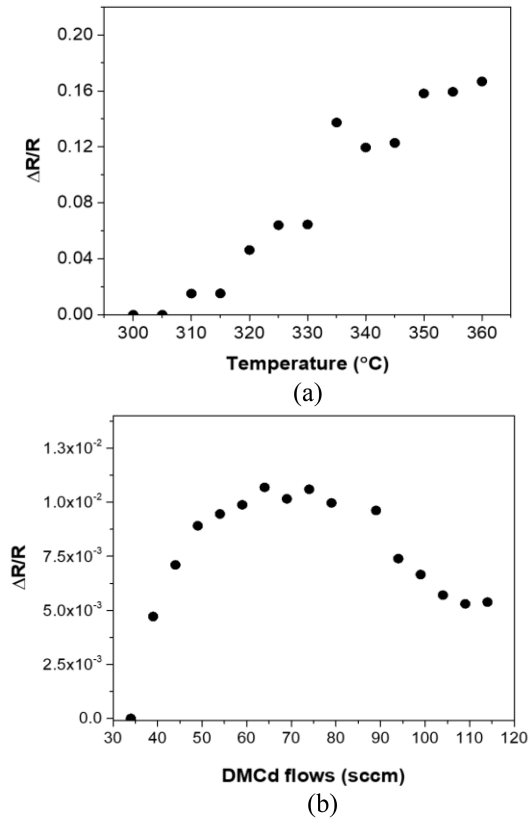

Fig. 3. (a) ΔR/R versus substrate temperature for a fixed DMCd partial pressure of 0.368 Torr. (b) ΔR/R versus DMCd flow for a fixed substrate temperature of 350 °C.

saturated until it plateaus above 350 °C where an equilibrium is established with the Cd saturated vapour pressure.

A further experiment was conducted at a fixed temperature of 350 °C where the DMCd pyrolysis appears to be efficient to determine the minimum DMCd flow needed for supersaturation. Any excess over this minimum flow will give Cd supersaturation but some margin will be needed in the CdTe deposition to allow for depletion of the precursor along the reactor tube. The plot of ΔR/R with DMCd flow is shown in Fig. 3(b). It can be seen that at the lowest flow there is no Cd condensation but increases rapidly at 30 sccm up to a maximum around 64 sccm. The reason for a decrease in ΔR/R for higher flows was coalescence of the Cd droplets forming an increasingly reflective surface. This was confirmed after removal of the substrate which showed a continuous Cd film. Following this experiment, it was possible to confidently fix the growth conditions for Cd saturation at 350 °C and a flow of DMCd of 64 sccm (corresponding to a partial pressure of 0.236 Torr). Provided the DMCd/DIPTe ratio remains above 2 these conditions will ensure that even for severe depletion of DIPTe along the reactor tube the DMCd will remain saturated.

B. Cd-Saturated Growth of CdTe:As TFSCs

Fig. 4(a) compares the current J–V curve of a baseline device with solar cells fabricated under Cd-saturated conditions. Similar II/VI precursor partial pressure ratio of 3 was used during the deposition of CdTe:As absorber in both baseline (non-saturated

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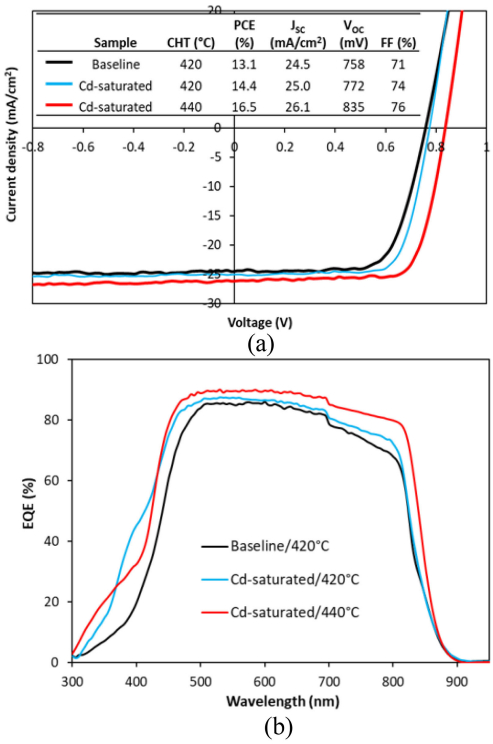

Fig. 4. (a) J–V curves of baseline device compared with Cd-saturated devices with absorber deposited at 350 °C. Inset: PV parameters of respective solar cells. (b) EQE spectra of corresponding devices.

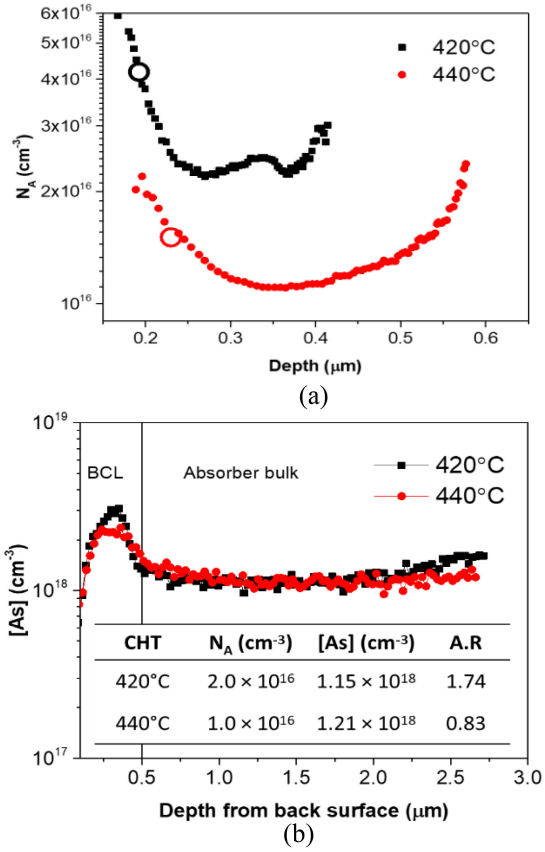

Fig. 5. (a) Acceptor concentration (N_A) versus depth profiles (zero-bias point for each curve is represented with an open circle for reference). (b) As SIMS depth profiles of Cd-saturated CdTe:As device with 420 °C and 440 °C CHT, for 10 min (inset showing calculated A.R.).

at 390 °C) and Cd-saturated devices (350 °C) discussed in this section. The device performance [PV parameters shown in the inset of Fig. 4(a)] improves in Cd-saturated device with similar CHT (420 °C) as performed on baseline devices. Power conversion efficiency (PCE) increases from baseline values of ∼13% to 14.4%. This is mainly because of improvements in both V_{OC} (758 to 772 mV) and FF (71 to 76%). J_{SC} nevertheless did not change significantly. Following CHT at a higher temperature of 440 °C for 10 min, V_{OC} in Cd-saturated devices increased to as high as 835 mV. When a similar high temperature CHT was applied to the baseline device, the performance improved only slightly, with efficiency similar to that of Cd-saturated device with CHT at 420 °C (results not shown here). This V_{OC} gain in Cd-saturated device with high temperature CHT, together with some small improvements in J_{SC} and FF significantly contributed to increasing PCE to 16.5%. The small gain in J_{SC} is consistent with the improvement in photocurrent generation especially in the long wavelength of the EQE spectra [Fig. 4(b)]. Interestingly, the activation ratio (A.R.), determined by comparing the N_A to dopant concentration measured by SIMS, was significantly increased in Cd-saturated devices (420 °C CHT). The A.R. increased from below 1% for baseline device to as high as 1.74%. This is consistent with an improved CdTe:As absorber quality, which lends strength to the merit of CdTe:As absorber growth under Cd-saturated conditions. The increased A.R. may also be because of a reduction in the concentration of compensating defects in the px CdTe:As film [21].

CHT at 440 °C for a longer time was also investigated for the Cd-saturated device. Extending anneal time from 10 to 30 min resulted in poor device performance, where all PV parameters degraded, suggesting "over-treatment" [22]. Although the longer anneal was detrimental to Cd-saturated devices, the PV performance was however still comparable to that of baseline devices. SIMS analysis was also carried out to probe the impact of Cd-saturated growth on As incorporation and doping efficiency. Relatively similar bulk As concentration levels were measured in both Cd-saturated devices that received the two different CHT anneals (420 °C and 440 °C), in the order of 1–1.2 × 10^{18} cm^{-3} [Fig. 5(b)]. Such As incorporation levels are consistent with previously reported CdTe:As absorber layers [8], [15]. However, the N_A reduced from ∼2 × 10^{16} cm^{-3} to ∼1 × 10^{16} cm^{-3} as the CHT annealing temperature was increased from 420 °C to 440 °C [Fig. 5(a)]. Despite improvement in V_{OC}, the higher temperature-induced drop in N_A consequently resulted in a lower dopant A.R. of 0.83. It is not clear at this stage what could be the reason for the reduced doping efficiency observed at more aggressive CHT.

Cross-sectional STEM images of Cd-saturated based devices with 420 °C and 440 °C CHT anneal temperatures are shown in Fig. 6. With 420 °C CHT, small grains are still present especially near the front interface and a significant density of stacking faults is evident [Fig. 6(a)]. Increasing the CHT temperature to 440 °C results in grain enlargement and reduction in stacking faults [Fig. 6(b)]. Comparing the elemental line profiles (particularly Zn and Cd) at the CdZnS/CdTe:As (emitter/absorber)

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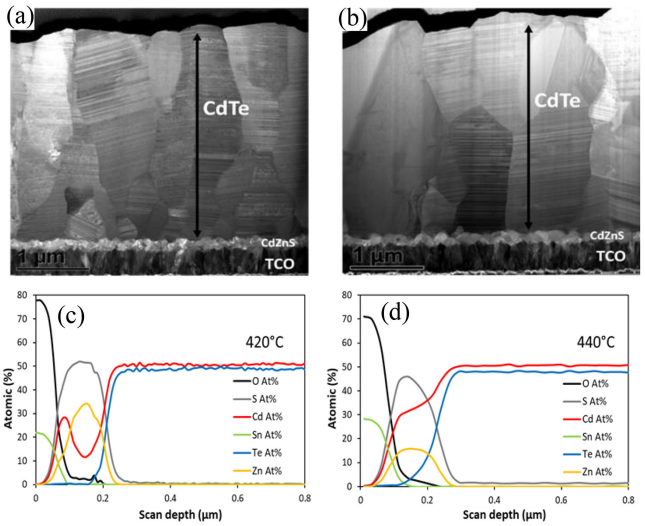

Fig. 6. Cross-sectional STEM images of Cd-saturated CdTe:As device with (a) 420 °C and (b) 440 °C CHT for 10 min, respectively, and corresponding EDS elemental line profiles (c) and (d).

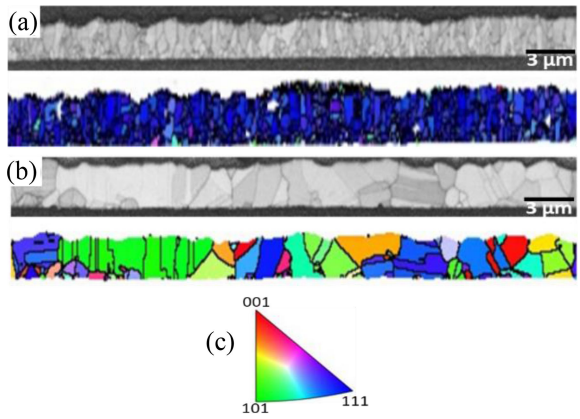

Fig. 7. EBSD of Cd-saturated devices which received (a) 420 °C and (b) 440 °C CHT for 10 min (top image and bottom images are band contrast image and the inverse pole figure, IPF maps), and (c) IPF reference triangle showing colors referring to orientation parallel to growth direction.

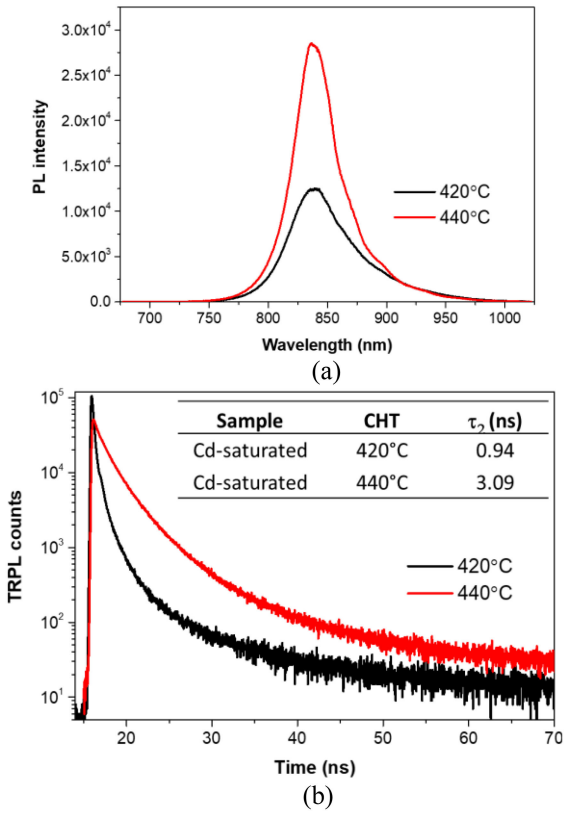

Fig. 8. (a) PL spectra and (b) TRPL decays of Cd-saturated devices which received different CHTs at 420 °C compared with 440 °C (inset: deduced τ_2 lifetimes from biexponential fits to TRPL decay curves).

interface [Fig. 6(c) and (d)], it is noted that the degree of atomic interdiffusion is more significant following the higher CHT annealing temperature (440 °C). This indicates that the extent of interdiffusion at the emitter/absorber interface plays a significant role in device performance following the CHT step. The improved grain structure and structural quality, especially near the emitter/absorber interface, combined with reduction in front interface states because of enhanced interdiffusion are clearly beneficial for device performance improvement, particularly V_{OC}, at the elevated CHT temperature when combined with Cd-saturated growth. Different CHT conditions appear to lead to varying degrees of intermixing between CdS and CdZnS layers and on the "Zn leaching" effect [24]. This can lead to changes in the composition of the emitter layer interfacing the absorber and hence possibly the emitter/absorber band alignment. This in turn would have an impact on V_{OC}, but it is believed to be a minor factor and not the primary driver of the very high V_{OC} values obtained in this work. In a previous study [17], CdZnS emitter composition was intentionally varied from CdS toward the ZnS phase whilst keeping the CHT conditions constant; the optimum PCE was observed around $Cd_{0.3}Zn_{0.7}S$ emitter composition but the V_{OC} did not exceed 800 mV.

Cross-sectional EBSD shows that a 420 °C CHT was insufficient to produce fully recrystalized grains in the bulk material [Fig. 7(a)], whereas higher temperature CHT (440 °C) makes a dramatic change in grain growth and more randomized texture [Fig. 7(b)], from highly oriented (111) [Fig. 7(a)]. This is consistent with cross-sectional STEM data in Fig. 6(b).

Opto-electronically, the increase in room temperature PL intensity [Fig. 8(a)] measured from the emitter/absorber interface on a lifted-off device structure (lift-off performed according to the method in Perkins et al. [23]), is consistent with an improved CdTe:As absorber quality for Cd-saturated growth combined with high temperature CHT, compared with both non-saturated [15] and Cd-saturated absorber layers which were subjected to the same CHT process (420 °C). This is consistent with longer minority carrier lifetimes [25], which is confirmed from TRPL analysis as the τ_2 lifetime increased from 0.95 to 3.09 ns [Fig. 6(b) inset].

This agrees with the observation of improved long wavelength EQE for the Cd-saturated growth combined with higher CHT temperature, which consequently contributed to the J_{SC} gain [Fig. 4(a) inset].

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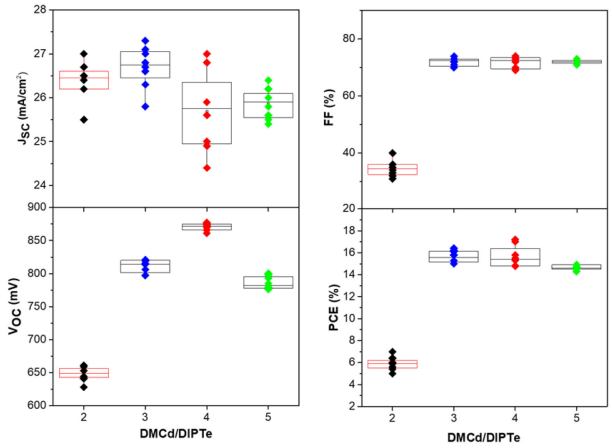

Fig. 9. Boxplots of J–V parameters for eight (~0.25 cm^2) cells of Cd-saturated CdTe:As devices as a function of DMCd/DIPTe partial pressure ratio.

TABLE I
SUMMARY OF BEST AND MEAN (8 CELLS) J–V PARAMETERS OF CD-SATURATED CDTE:AS DEVICES AS A FUNCTION OF DMCD/DIPTE PARTIAL PRESSURE RATIO

DMCd/DIPTe	PCE (%)	J_{SC} (mA/cm²)	V_{OC} (mV)	FF (%)
2	7.0 (5.9 ± 0.6)	27.0 (26.4 ± 0.4)	661 (648 ± 11)	40.0 (34.6 ± 2.8)
3	16.4 (15.6 ± 0.6)	27.3 (26.7 ± 0.5)	821 (811 ± 10)	74.0 (72.0 ± 1.5)
4	17.2 (15.7 ± 1.1)	27.1 (25.4 ± 1.0)	877 (870 ± 6)	73.0 (71.0 ± 2.5)
5	14.9 (14.7 ± 0.2)	26.4 (25.9 ± 0.4)	800 (786 ± 10)	73.0 (72.0 ± 0.8)

C. *Impact of DMCd/DIPTe Ratios on CdTe:As TFSCs*

The impact of Cd/Te precursor partial pressure ratio in the reaction mixture during CdTe:As absorber deposition, under Cd-saturated conditions, on corresponding device performance was also investigated. DMCd partial pressure was kept at 0.236 Torr and that of DIPTe was varied to yield a DMCd/DIPTe partial pressure ratio from 2 to 5. Fig. 9 shows the boxplots of device PV parameters as a function of the DMCd/DIPTe ratio. Table I is a summary of the PV parameters. With DMCd/DIPTe = 2, device performance was observed to be very poor. As DMCd/DIPTe ratio is increased to 3, device efficiency improves significantly, due to increase in all PV parameters, especially V_{OC} and FF. Device efficiency improves slightly further when DMCd/DIPTe = 4, particularly because of the boost in V_{OC}, but begins to drop above this ratio (i.e., DMCd/DIPTe = 5). The data presented in Fig. 9 indicates DMCd/DIPTe = 4, is the optimum, yielding 17.2% best cell efficiency with 877 mV best V_{OC} which is the highest value combined with good FF reported for As doped, pure CdTe (Se-free) absorber solar cells. Compared with the baseline device, a significant ~100 mV boost in V_{OC} is demonstrated with Cd-saturated devices.

Fig. 10 shows the EQE spectra and N_A versus depth plots of cells based on Cd-saturated CdTe:As absorbers with varying DMCd/DIPTe ratios. EQE data trends with the V_{OC}. The highest long wavelength response is associated with Cd-saturated device with lowest V_{OC} (i.e., DCMd/DIPTe = 2). This decreases as the DCMd/DIPTe ratio is increased to 4, after which it slightly recovers [Fig. 10(a)]. A correlation between N_A and DCMd/DIPTe ratio [Fig. 10(b)] is also noted. N_A increases as DMCd/DIPTe is increased from 2 to 4. As expected, the depletion width becomes narrow too. CdTe:As deposited in a reaction mixture rich in Cd precursor is clearly beneficial for increased device N_A which leads to increase in the V_{OC}. N_A seems to saturate at around DMCd/DIPTe ratio of 4.

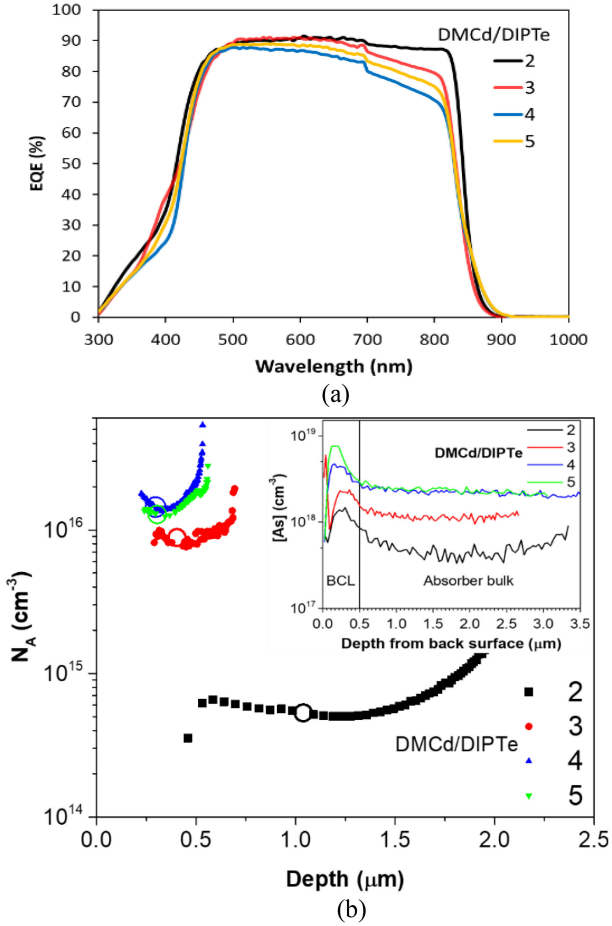

Fig. 10. (a) EQE spectra of Cd-saturated CdTe:As devices. (b) Acceptor concentration (N_A) versus depth profiles from varying DMCd/DIPTe partial pressure ratio (inset: Bulk As SIMS depth profiles versus varying DMCd/DiPTe partial pressure ratio). The zero-bias point for each curve is marked with an open circle.

Bulk As incorporation trends similarly with the ratio of DMCd/DIPTe partial pressures [see Fig. 10(b) inset], as it can be seen to saturate beyond DMCd/DIPTe ratio of 4. This indicates that the bulk As incorporation can be controlled by the DMCd/DIPTe ratio in the reaction mixture during CdTe:As absorber growth at the substrate temperature employed in this study (350 °C) to an optimum of 2–2.5 × 10^{18} cm^{-3}, i.e., DMCd/DIPTe = 4 or 5.

Increase in the density of defects associated with As doping is suspected, resulting in higher bulk recombination, with the higher DMCd/DIPTe ratio of 5. This could be playing a role in the drop in V_{OC} (Fig. 9). Effects of self-compensation are also plausible. Further investigations outside the scope of the current work will be required for better understanding of this in more detail.

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V. Conclusion

1) Fabrication of in-situ CdTe:As devices under Cd-saturated growth conditions at the Cd-rich phase boundary displaying high efficiency has been demonstrated in this work.
2) It was possible to achieve the potential of high temperature CHT with Cd-saturated grown CdTe:As (which was not possible with baseline process).
3) Cd-saturated CdTe:As device, combined with CHT at a high temperature of 440 °C enhanced device performance by increasing PCE from baseline of ∼13% to 16.5%, because of significant V_{OC} boost.
4) Optimization of the Cd:Te precursor partial pressure ratio led to device efficiency as high as 17.2% with 877 mV V_{OC}, which is so far the best V_{OC} (when combined with good FF) reported for Se-free px CdTe:As TFSCs.
5) Cd-saturated growth for in situ As doping was shown to improve CdTe absorber quality, increasing minority carrier lifetime, and to be a promising path to much higher V_{OC}s.
6) High acceptor concentration ($>10^{16}$ cm^{-3}) is easily enabled with Cd-saturated CdTe:As, but the limiting issues with defects and self-compensation associated with As doping cannot be completely ruled out.
7) İnadequate emitter doping with respect to the higher absorber acceptor concentration may also be a limiting factor in the devices utilizing Cd-saturated growth. Much higher V_{OC}s could be achieved with further optimization. To this end, additional studies are required on varying other device parameters, characterization of electronic properties of the CdTe:As absorber and exploring novel emitters with sufficiently high doping concentrations.

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