Development and scale-up of fully printable perovskite solar modules

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Summary

Perovskite solar cells represent a new class of photovoltaic devices that, in only a decade, has already been achieved comparable performance to that of the most established photovoltaic technologies. To satisfy the demanding market requirements, however, perovskite solar cells need to have the high performances with the use of low-cost materials and cost-effective fabrication processes, during a long term in the working environment and this needs to be possible for both small scale and large-scale devices.

The fully printable carbon perovskite solar cells are based on an inorganic triple mesoscopic stack that is infiltrated by a perovskite precursors solution. This architecture seems to be the most promising to satisfy the requirements of the market, because the manufacture can simply occur with low-cost materials and well-established industrial deposition techniques, such as screen printing. Furthermore, the stability of these cells was reported to be one of the longest among perovskite solar cells, making this technology the closest to make market penetration.

This work focuses on fully printable perovskite solar cells with a special outlook at their up-scaling in series-connected modules. The fabrication of large area modules with both high performance and substrate coverage will be discussed, in a journey that starts from single cell devices, overcomes issues found in the up-scaling process, and finally reaches design optimisation. Devices of single cells with 1 cm^2 active area will be presented, as well as modules on 5 $\times$ 5 cm^2 or 10 $\times$ 10 cm^2 substrates. Finally, series-connected modules with around 200 cm^2 active area and high coverage on the substrate will be shown.

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List of abbreviations and definitions

Below are the most important abbreviations and definitions for this work:

Abbreviation	Definition and section of first appearance	
a-Si SC	amorphous silicon solar cell	1.2.1
ABX_3	generic perovskite formula	1.3.1
AC	alternating current	2.3.1
Al-tape	the conductive tape that was developed for the C-PSC and discussed in Chapter 3	3.3.2
ALD	atomic layer deposition	1.4.2
AM 0, AM 1, AM 1.5, AM 1.5G	different definitions of solar spectrum at different air mass conditions	1.2.2
aperture area	the area of the module that includes the active area and interspace between cells	1.6.3
ASTM	American society for testing and materials	1.2.2
AVA	5-aminovaleric acid $[NH_3(CH_2)_4COOH]^+$	1.3.1
AVA-MAPI	2D/3D MAPI perovskite with AVA	1.3.1
AVAI	5-aminovaleric acid iodide $[NH_3(CH_2)_4COOH]^+$ I^-	1.3.1
bLayer	compact titanium(IV) oxide	1.4
C-PSC	the triple-mesoscopic carbon perovskite solar cell	1.3.1
c-Si SC	monocrystalline or multicrystalline silicon solar cell	1
CdTe	cadmium telluride solar cell	1.2.1
CIGS	CuInGaSe solar cell	1.2.1
DC	direct current	1.2.2
DMF	N,N-dimethylformamide, solvent	1.3.2
DMSO	dimethyl sulfoxide, solvent	1.3.2
DSSC	dye sensitised solar cell	1.2.1
EDX	energy dispersive X-ray	2.3.2
E_g	band gap energy	1.2.2
EQE	external quantum efficiency	1.4.1
ETM	electron transporting material	1.2.2
FAB	formamidinium $[NH_2(CH)NH_2]^+$	1.4.1
FABI	formamidinium iodide $[NH_2(CH)NH_2]^+$ I^-	1.4.1
FTO	fluorine-doped tin(IV) oxide	1.4
GBL	γ-butyrolactone, solvent	1.3.2
H	length of the cell	5.3.1

HTM	hole transporting material	1.2.2
IV or JV curve	current (density) - voltage characteristic	1.2.2
IoT	internet of things	1.2.2
IPA	2-propanol, solvent	2.2.1
iR-drop	current·resistance drop	1.5.3
L_t	transfer line	2.3.1
LED	light emission diode	1.3.2
MA	methylammonium $[CH_3NH_3]^+$	1.3.2
MAI	methylammonium iodide $[CH_3NH_3]^+$ I^-	1.3.2
mAl_2O_3	mesoporous aluminium(III) oxide	1.3.2
MAPI	$CH_3NH_3PbI_3$ perovskite	1.3.1
MAPIC	perovskite fabricated starting from a 3:1 molar ratio CH_3NH_3I:$PbCl_2$ solution	1.3.2
$mTiO_2$	mesoporous titanium(IV) oxide	1.2.1
$mSiO_2$	mesoporous silicon(IV) oxide	1.4.2
$mZrO_2$	mesoporous zirconium(IV) oxide	1.4
M1, M2, M3, M1max, M2max	module layouts that are presented in Chapter 6	6.3.6
n-type	semiconductors that collect negative charge, hole barrier (ETM)	1.2.2
n_c	number of cells	1.6.1
NMP	N-methyl-2-pyrrolidone, solvent	1.4.1
OPV	organic photovoltaic	1.2.1
p-n or p-i-n junctions	that are formed by the junctions of a p- and a n-type materials and eventually an intrinsic semiconductor in between	1.2.2
p-type	semiconductors that collect positive charge, electron barrier (HTM)	1.2.2
Pa-M	parallel-connected module	1.6.1
PCBM	phenyl-C61-butyric acid methyl ester	1.2.1
PEDOT:PSS	poly(3,4-ethylenedioxythiophene) polystyrene sulfonate	1.2.1
PSC	perovskite solar cell	1
PV	photovoltaic	1
PVA	poly(vinyl acetate)	3.2
P1, P2, P3	pattern 1, 2, 3; the scribes that form the interconnects in the series-connected modules that are discussed in Chapter 6	6.1
P3HT	poly(3-hexylthiophene-2,5-diyl)	1.2.1
QDSSC	quantum dots solar cell	1.2.1
R_A, R_B, R_X	ionic radii of the ABX_3	1.3.1
RbM	robotic mesh deposition method	4.1
R_{El}	resistance of the electrode	5.3.1
R_q	roughness: root mean square	2.3.2
R_p	roughness: maximum peak height	2.3.2
R_{rec}	recombination resistance	4.3.4
R_{sq}	sheet resistance	2.3.1
R_t	roughness: maximum height of the profile	2.3.2

S-H, S-M, S-L, D-H, D-M, D-L	nomenclature for some devices presented in Chapter 3. "S" and "D" refer to the thickness of the ZrO_2 layer; "H", "M" and "L" refer to the concentration of the infiltrated solution	3.3.7
Se-M	series-connected module	1.6.2
SEM	scanning electron microscope	2.3.2
Si SC	silicon solar cells	1
Spiro-OMeTaD	2,2',7,7'-tetrakis[N,N-di(4-methoxyphenyl)amino]-9,9'-spirobifluorene	1
S1, S2	space 1, 2; the space between P1 and P2 and the space between P2 and P3 that are presented in Chapter 6	6.1
TAA	titanium diisopropoxide bis(acetylacetonate)	1.4.2
TFT	thin film transistor	1.3.2
TLM	transmission line measurement	2.3.1
triple mesoscopic stack	glass/FTO/bLayer/mTiO_2/mZrO_2/carbon substrate without perovskite	1.4
UNFCCC	United Nations framework convention on climate change	1.1
UV, Vis, NIR, IR	ultraviolet, visible, near infra-red and infra red	1.2.2
XRD	X-ray diffraction	2.3.4

List of symbols

Symbol and units		Definition and section of first appearance	
A		ideality factor	1.5
A_r	%	coverage relatively to the aperture area or aperture ratio	1.6.3
Av-V_{oc}	V, mV	averaged voltage of single cells in module design	1.6.4
Cv	%	coverage relatively to the total area	1.6.3
FF	%	fill factor	1.2.2
E_g	eV	band gap	1.2.2
G	KΩ	shunt resistance	1.5
g-FF	%	geometric fill factor	1.6.3
I_d	A, mA	dark current	1.2.2
I_L	A, mA	photocurrent	1.2.2
I_{sc}	A or mA	short circuit current	1.2.2
J	A, mA	current density	1.5
J_{MP}	A/cm^2, mA/cm^2	current density at the P_{MP}	1.2.2
J_{sc}	A/cm^2, mA/cm^2	short circuit current density	1.2.2
J_o	A, mA $/cm^2$	saturation current density	1.5
K	$1.380649 \cdot 10^{-23}$ J/K	Boltzmann constant	1.5
Min-J_{sc}	A/cm^2, mA/cm^2	current density of a module relatively to the active area of a single cell	1.6.4
PCE	%	power conversion efficiency relatively to the active area	1.2.1
P_{in}	mW	incident power from the light source	1.2.2
P_{MP} or MPP	mW	power at the maximum point	1.2.2
q	$1.602 \cdot 10^{-19}$ C	electric charge	1.5
R_c	Ω	contact resistance	2
RH	%	relative humidity	1.3.1
R_s	Ω	series resistance	1.5
T	K	temperature	1.5
V	V, mV	applied voltage	1.5
V_{MP}	V, mV	voltage at the P_{MP}	1.2.2
V_{oc}	V or mV	open circuit voltage	1.2.2

All elements will be referred to their chemical symbol.

Contents

Chapter 1

Introduction

One of the biggest issues of the modern economic system is energy. However, solar energy is abundant and freely available on Earth. To quantify the amount of solar energy that is available, it is estimated that the earth receives the energy consumed by all humanity in the year 2012 every 1.8 h [1]. Theoretically, solar energy represents a limitless, free and inexhaustible resource which may also be harnessed through photovoltaic (PV) technology. In order to produce electricity, Si-based solar cells (Si SC) represent the most successful PV technology available on the market so far. However, thin film PV can be much more versatile than Si due to the possibility of exploiting printing as a deposition technique, allowing high control of the final device design and low-cost manufacture.

An emerging and promising class of materials that can be utilised in thin film technology is the halide perovskite. This class of semiconductors is characterised by high charge-carrier mobility and good spectrum absorption in visible light (Section 1.3). Moreover, halide compounds are solution-phase processable, enabling low-cost and large-area production. In the PV field, the organic-inorganic Pb halide perovskite solar cells (PSC) have shown astonishing performance and, in only a decade of research, the achieved efficiency is comparable to the more established technologies, such as monocrystalline and multicrystalline Si SC (c-Si SC), i.e. with a certified efficiency above 25 % (Fig 1.1). The fully-printable carbon PSC based on three porous layers (C-PSC) is a novel architecture that emerged in the literature in 2013 and represents, probably, the closest to achieve market penetration: it is fully printable, stable for more than a year under illumination and does not requires expensive materials such as Spiro-OMeTaD and noble metal contacts (Section 1.4).

This chapter wants to go over the basic concepts of solar cells with a special focus on the key points that will be utilised in the discussion of the next chapters.

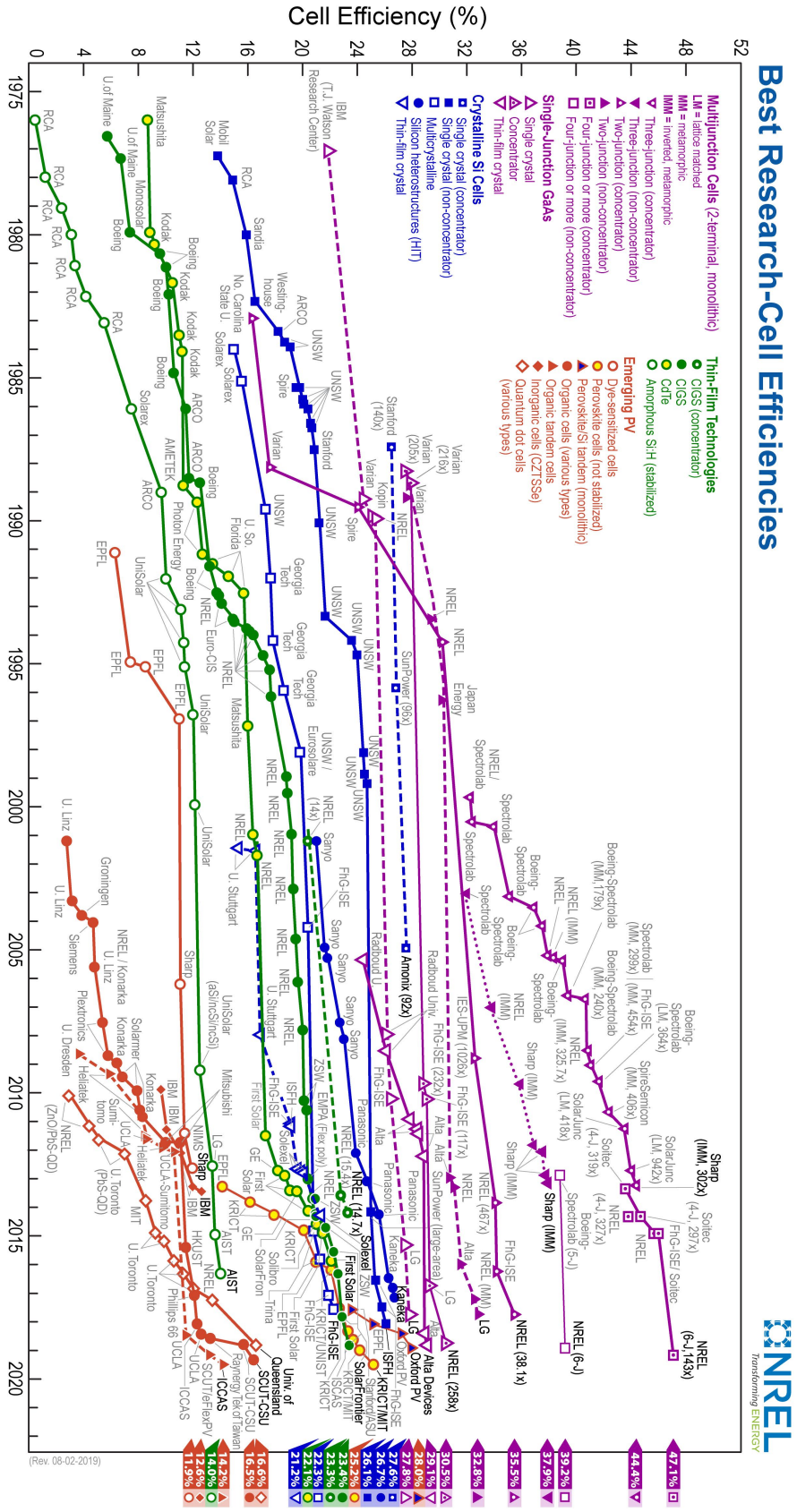


Figure 1.1: Certified PCE of best research solar cells worldwide for various PV technologies from 1976 to 2019. From www.nrel.gov [2].

The energy demand issue and a brief overview of solar cell history, to introduce the event of PSC, will open the chapter. A general explanation of the solar cell working principles will be given. A deeper explanation of the PSC and C-PSC will be presented; the large area modules and screen printing will be introduced at the end of the chapter.

1.1 The energy challenge

The development of renewable energy sources is becoming urgent after the realization of the negative effects that burning fossil fuels have on the environment. Climate change and global warming are becoming, in particular, the most urgent issues that modern society must tackle nowadays. The 2015 United Nations framework convention on climate change (UNFCCC) agreement aims to limit global warming to below 1.5 °C above pre-industrial levels. Different reports have been prepared to compare different scenarios and predict the effect of our life style and energy policy in accordance to the UNFCCC [3; 4] showing the importance of producing energy from low greenhouse gas emission energy sources, for example PV.

The use of renewable sources would be the largest contributor to mitigation over 2015–2050 and would increase their impact in all sectors, i.e. industry, transport and building sectors (Fig 1.2). They are used in final energy demand either directly (solar thermal, geothermal, heat pumps, etc.) or through energy carriers, such as electricity and liquid biofuels production (from wind, solar, hydro and biomass). In the industrial sector, renewable would come to represent nearly half (45%) of energy sources in 2050, principally thanks to an increased participation of renewable electricity. The transport sector exhibited the lowest share in renewable in 2015 among all sectors (3%) and would remain so despite a high growth in renewables penetration (36% in 2050). The share of transport fuel from renewable energy sources in 2050 would be dominated by biomass (liquid biofuels), followed by renewable electricity. The buildings sector accounts and will still account for the largest renewable share (33% in 2015, 65% in 2050). This would occur especially for the larger consumption of electricity produced by renewable sources.

This data shows that the demand for renewable energy in the market, including PV, is increasing due to the need of a sustainable economy. Furthermore, PV and other renewable electricity sources are expected to give an important contribution to building, transport and industry sectors in order to achieve the global warming mitigation goals.

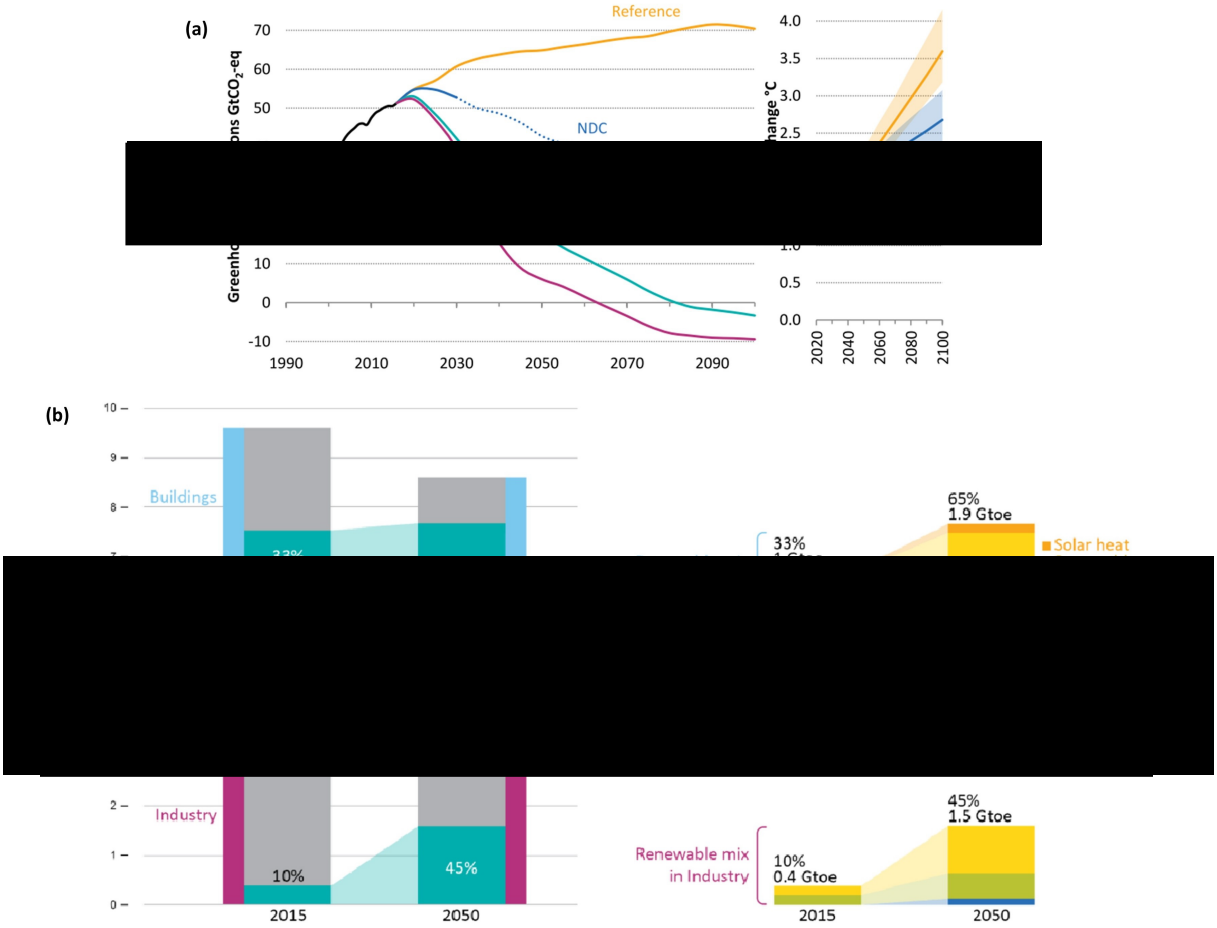


Figure 1.2: (a) Global greenhouse gas emissions and global average temperature change for different global warming scenarios. Reference refers to a scenario where no political act is taken place. (b) Share of renewables by sector in the 2 °C scenario with comparison between 2015 and 2050. On the right the renewable energy share (direct renewables and energy carriers) per sector between 2015 and 2050. Gtoe = giga tonnes of oil equivalent; Gt-CO_2-eq = giga tonnes of CO_2 equivalent. From reference [4]

1.2 Basic concepts of solar cells

1.2.1 Brief history

The history of solar cells started in 1839, when Edmund Bequerel observed that, under illumination, solutions containing a metal halide salt produced a current between two platinum electrodes immersed in the electrolyte [5]. This effect, or photoelectric effect, was explained later by Albert Einstein in 1905. The first "modern" PV device was a Si SC with 6 % power conversion efficiency (PCE) in 1954. In spite of the early discovery, PV technology has been subjected to intense scientific interest only since the 1970s, with the oil crisis [5]. Although the produc-

tion of c-Si SC became cheaper in the last few years, the Si wafer has always been considered a major cost of PV modules [6]. Thin film technology is convenient in terms of low-cost production, minimisation of material consumption and versatile applications such as controlling the pattern, feasibility for semi-transparent devices and deposition on multiple substrates including flexible and textile. Some important commercially available thin film PV are CdTe, CIGS (with CuInGaSe as absorber material) and amorphous Si SC (a-Si SC). Other emerging technologies are organic or polymer PV (OPV) and dye sensitised solar cell (DSSC), which are the closest relatives of PSC.

OPV is an interesting class of PV that has been studied for decades. The importance of OPV is not only the low-cost and the flexible devices that have been widely reported in the literature, but also the recent achievement in PCE, more than 16.5 % (Fig 1.1). OPV is based on a planar architecture with donor and acceptor materials, polymers or small organic molecules [7; 8; 9]. The research in the field of OPV was, in some terms, of great support for the PSC because many materials that had been developed for OPV were then utilised for PSC. Some outstanding examples are poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS), Poly(3-hexylthiophene-2,5-diyl) (P3HT) and Phenyl-C61-butyric acid methyl ester (PCBM) [10; 11; 12; 13; 14].

Thin film technology can be based on compact thin layers (planar architectures) or mesoporous thin layers. The advantage of using mesoporous thin layers is the increase of the surface area and the maximisation of the light absorption. This is the case of DSSC, developed for the first time by Michael Grätzel and Brian O'Regan in 1991 [15]. A photoanode, based on a transparent conductor as substrate and mesoporous TiO_2 ($mTiO_2$), is infiltrated by a dye and then placed in contact with an electrolyte. The cathode is in electrical contact with the electrolyte. The DSSC represents also the starting technology for the PSC. The PSC, which was proposed for the first time by Tsutomu Miyasaka and co-workers in 2009 [16], was initially prepared in a typical DSSC architecture with perovskite as a dye.

The quantum dot sensitised solar cell (QDSSC), is another emerging class of PV technology analogous to DSSC. Starting from a similar architecture based on $mTiO_2$, the absorber material is in nanoparticles. The nanoparticles are small enough to exhibit quantum properties (quantum dots). The quantum dots can exhibit different properties compared to classical nanoparticles, including multiple charge generation per single incident photon [17]. Several materials were utilised to make QDSSC [18; 19], including perovskite quantum dots [20].

PSC has already achieved above 25 % in PCE, close to the efficiency of best research single c-Si SC (26.1 %) and slightly higher than multi c-Si SC (22.3 %) (Fig 1.1). Intensive research has been invested in this technology, which can be based on the mesoporous architecture, similarly to the DSSC, or planar, similarly to OPV and CIGS. PSC will be discussed in more detail in Section 1.3.2.

1.2.2 Working principle

The working principle of a solar cell is simple: first, absorb the energy of a photon to generate a positive and a negative charge carriers; then, collect them with a cathode and an anode respectively. In order to generate charge in solid state matter, electrons need to be promoted to energy levels where they are free to move. This promotion generates also voids, or holes, in the original position of the respective electrons. The electron-hole pair can be described as a quantum-mechanical particle called "exciton", which is bonded together by Coulomb interactions. The electron tends to recombine with the hole via a decay process that can result in the emission of radiative or non-radiative energy. This phenomenon of absorption of the light and recombination of the generated exciton is the most common mechanism for colour generation in most objects around us [21]. However, when the exciton is split into the two negative and positive components, energetic charge carriers can be collected and generate electrical energy. This occurs when the hole is filled with a low energetic electron, whereas the electron that transport energy is collected by the anode. The process results in positive and negative poles for a DC (direct current) generation.

The splitting of the exciton is possible by exploiting the electronic properties of semiconductors, especially band gap (E_g). To understand in more depth how solar cells work, basic concepts of E_g, semiconductors, diodes, and the mechanism of electron-hole pair recombination, should be introduced. However, more inherently to the discussion of this work, only some key aspects of the role of semiconductors in PV and the figure of merits to define the performance of solar cell will be presented.

Semiconductors in solar cells

The minimum energy required to achieve the absorption of light is that the photon has energy equal or higher to the E_g of the material. Small E_g results in large absorption in the solar spectrum region, which includes ultraviolet (UV), visible (Vis) and infrared (IR, NIR for near IR). If the E_g is extremely low or even

zero (e.g. metals and semimetals), electrons are promoted through a continuum of energy levels. However, they decay back down to the ground state through a series of intermediate levels [22]. Therefore, metals and semi-metals can absorb all the solar spectrum, but the recombination occurs so quickly that no charge can be collected. If the E_g is large (e.g. semiconductors and insulators) the lifetime of the generated excitons is increased. In insulators, for examples, electron-hole pairs can form stable excitons, that eventually can form complexes, such as biexcitons [23]. However, the absorption in the light spectrum is reduced and, in case of insulators there is no or very little absorption in the solar spectrum. A compromise between small and large E_g is necessary, and is found in semiconductors. Examples of E_g values for some semiconductors utilised in PV are 0.67 eV for Ge, 1.1 eV for Si and 1.5 eV for GaAs.

Charge collection is possible when different semiconductors are interfaced to create a specific energy alignment and force the current to move only in one direction. This can occur thanks to p-n or p-i-n junctions. The p-n junction is an electrical contact between p-type (that transport positive charge) and n-type (that transport negative charge) materials. Materials that are p-type and n-type are also called respectively hole or electron transporting materials (HTM, ETM). The p-i-n junction involves also an intrinsic material in between the p- and n-type materials. Diodes are devices formed by a p-n or p-i-n junction. Metals, semimetals, and insulators cannot be used for the light absorption or for the diode, although they can still play a role in devices, e.g. for electrical contacts (metals and semimetals) or for specific design or architecture (insulators).

Solar cells are, therefore, diodes that can generate current under illumination (photocurrent, I_L) due to the promotion of electrons to the conduction band when photons are absorbed. The light absorption in a diode and the relative behaviour during a current-voltage scan (IV or JV curve) is shown in Fig 1.3. When a voltage $V \leq 0$ is applied, no current is measured in the dark due to the energy alignment of the p-n junction but, under illumination, I_L is generated. At short circuit conditions, i.e. $V = 0$, no dark current (I_d) is generated, thus, the measured current in such a condition is I_L. The I_L at $V = 0$ is called short circuit current (I_{sc}) or current density (J_{sc}). J_{sc} is expected to be proportional to the light absorption, thus, when E_g is small J_{sc} should be high. For example, Si SC can present values of $J_{sc} > 35$ mA/cm^2 ($E_g = 1.1$ eV) whereas perovskites with $E_g \sim 1.6$ eV cannot exceed 25 mA/cm^2.

When $V > 0$, I_d can be measured and, under illumination, is opposite to the I_L. A special case is when the current is equal to 0 under illumination because

I_d = -I_L. This is the open circuit condition and it is possible to define V = V_{oc} (Fig 1.3). The V_{oc} is expected to be high when E_g is large. Similarly to the previous comparison, Si SC can exhibit $V_{oc} \sim 600$ mV, whereas PSC can have $V_{oc} > 1$ V in optimal devices. V_{oc}, furthermore, becomes smaller at lower light intensity and it should be 0 in dark condition.

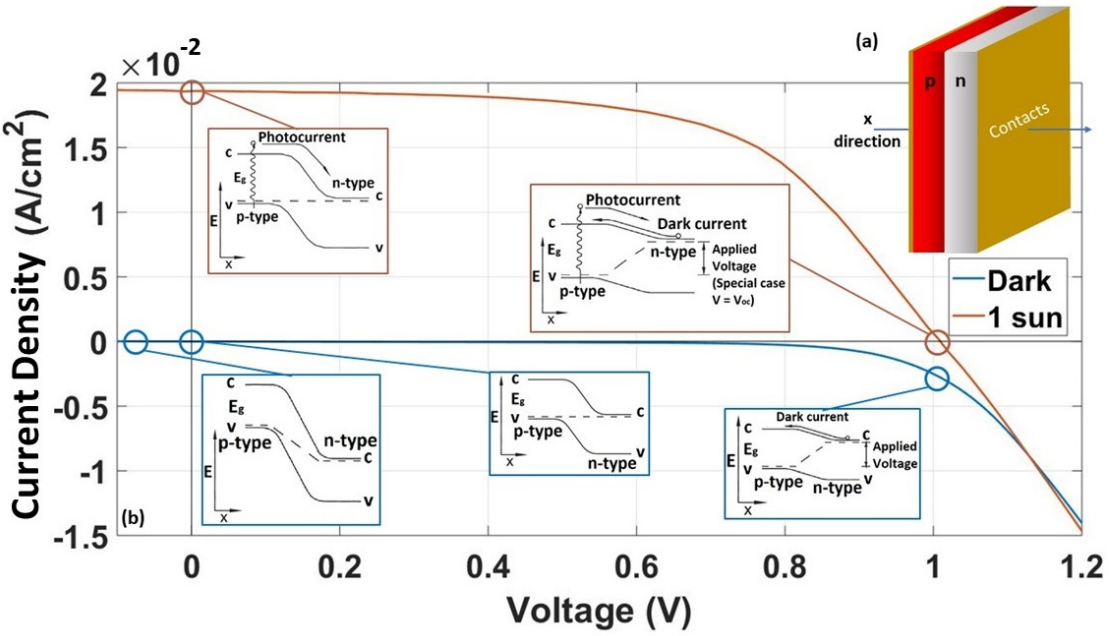


Figure 1.3: The p-n junction behaviour at different applied voltage. (a) Schematic of a p-n junction connected by two conductors and definition of the x-direction. (b) Experimental current-voltage characteristic in the dark and under illumination of a PV device. When V $\leq$ 0, no current is measured in the dark. Under illumination, the photocurrent is generated. The measured photocurrent in short circuit condition (V = 0) is called short circuit current, I_{sc}, or current density, J_{sc}. When V > 0, dark current can be measured and, under illumination, is opposite to the photocurrent. Special case when the current is equal to 0 under illumination. This is the open circuit condition at which voltage, V = V_{oc}, the dark current is equal and opposite to the photocurrent.

Figure of merits

The main parameter to define the performance of solar cells is the PCE, which is the ratio between the maximum generated power of the device and the incident power of the light source (P_{in}). The maximum power can be measured with a tracker that determines the point of maximum generated current at the maximum extraction voltage, so it is called maximum power point (MPP) or power at the maximum point (P_{MP}). With a P_{MP} tracker, it is possible to detect this point

and define the PCE, according to Eq 1.1.

$$PCE = \frac{P_{MP}}{P_{in}} \tag{1.1}$$

Where the light source is calibrated at a known P_{in}. However, it is also possible to measure the IV curve to find the P_{MP}, including also other useful PV parameters.

The J_{sc} and V_{oc} were identified in the JV curve in Fig 1.3. The P_{MP} is characterised by a voltage and a current at maximum power (V_{MP}, J_{MP}). The product between the V_{MP} and J_{MP} define a square inside the JV curve. Ideally, the JV curve should as squared as the product of V_{MP} and J_{MP} or, in other words, the product of V_{MP} and J_{MP} should be equal to the product of V_{oc} and J_{sc}. The ratio of the two products is called fill factor (FF, Eq 1.2).

$$FF = \frac{V_{MP} \cdot J_{MP}}{V_{oc} \cdot J_{sc}} = \frac{P_{MP}}{V_{oc} \cdot J_{sc}} \tag{1.2}$$

The FF, J_{sc}, and V_{oc} can be used to measure the PCE from a JV curve (Eq 1.3).

$$PCE = \frac{P_{MP}}{P_{in}} = \frac{FF \cdot V_{oc} \cdot J_{sc}}{P_{in}} \tag{1.3}$$

P_{in} depends on the light source and can influence the PCE, especially due to the characteristic absorption of the spectrum of light. The next section will give the definition of few important light spectra.

Spectrum of the light

The definition of the spectrum of light is crucial to define the performance of a PV device at different light conditions. The most important light source is undeniably the sun, thus, the definition of the solar spectrum is crucial. The solar spectrum can be closely described with the black body equation considering a temperature of 5760 K: ranging from the UV to the IR region and having the greatest irradiance at wavelength between 300 and 800 nm.

The power density at the Earth's atmosphere is nearly 1.4 KW/m^2. The light is then absorbed and scattered by the atmosphere, so that the power is further decreased at the Earth's surface [22]. The effect of the atmosphere becomes more or less important according to the altitude and the height above sea level. Moreover, the solar spectrum varies with the seasons, weather condition, and the time of day. This variation of the solar spectrum makes the standardisation not straightforward. The American society for testing and materials (ASTM) has developed

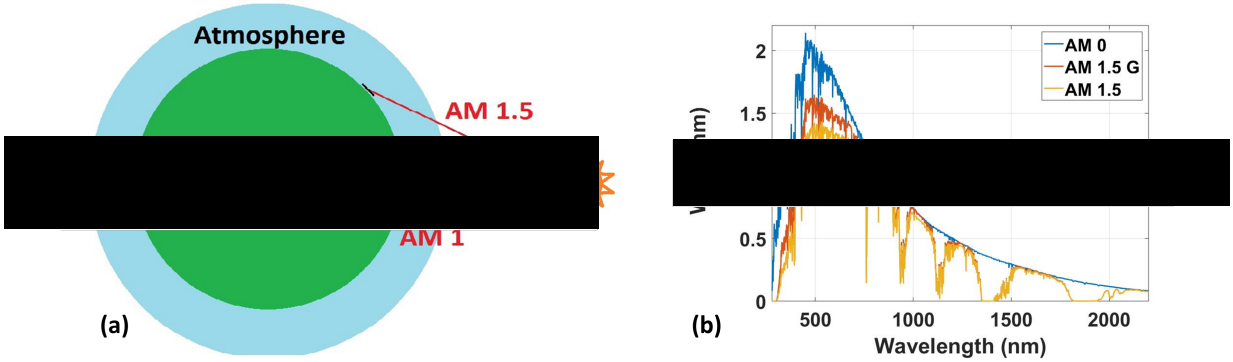


Figure 1.4: Definition of AM 0, AM 1, and AM 1.5. (a) Definition of the solar spectrum at different points relative to the Earth. (b) Standard solar spectra, downloaded from [24].

different standards to define the solar spectrum in a conventional way. According to the mass of air that the light will meet, it is possible to define the air mass (AM) 0, 1, and 1.5 (Fig 1.4a). The AM 0 is the solar spectrum at the atmosphere surface, AM 1 at the sea level and perpendicular point. The AM 1.5 is the light spectrum at the sea level and a tilted point of 37 °, so a thicker atmosphere layer is considered. Normally, AM 1.5 is intended as direct light but AM 1.5 G, or global, accounts also the effects of diffusion (Fig 1.4b). The AM 1.5 G is commonly used for the characterisation of PV devices and 100 mW/cm^2 is the defined density of power at 1 sun.

Another important definition is the light source for indoor applications. A huge number of items can work together through an internet connection in indoor. These items are called "internet of things" (IoT) [25]. The IoT can be sensors, LED, or any device that is applied in a specific environment, i.e. in a house or car. These items need to be powered, typically by a battery that can be recharged by PV devices. Since the IoT works mostly in indoor environment, an interest to test solar cells in such conditions has been raised. Semiconductors with small E_g, e.g. Si, can absorb light until the red or even a small portion of the NIR region, which can be found in the solar spectrum. Because modern LED and fluorescent lamps do not contain the NIR component, interesting applications can be found for semiconductors with large E_g, e.g. perovskite ($E_g \simeq 1.5$ eV [26]).

Some modules that were fabricated in this work were measured with fluorescent lamps by Tsoi and co-workers [27; 28] and the emission spectrum is shown in Fig 1.5. However, these results will not be presented here because the core of this work is based on the characterisation under 1 sun AM 1.5 G.

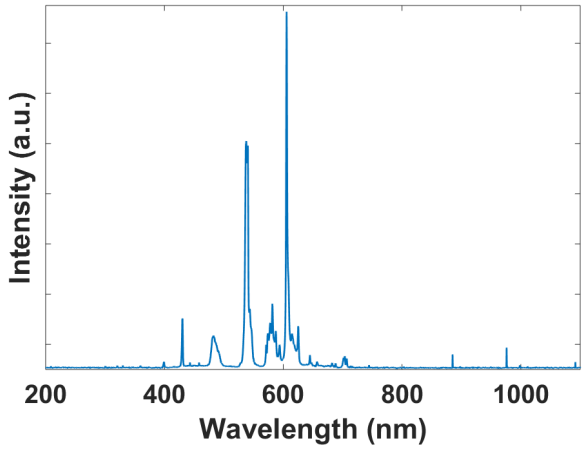


Figure 1.5: Light spectrum of a fluorescent lamp.

1.3 Perovskite

PSCs have been in the centre of an intense research effort, due to the unexpected steep increase in performance that has been achieved in the last ten years. This has made the name "perovskite" very well-known in the PV field. However, the crystal structure and the relative halide-based compounds have been studied for decades. One of the oldest publications related to halide perovskite is probably dated to 1973, with a study of $CsPbX_3$ and $CsSnX_3$ [29]. It is unlikely that anyone could predict at that time the multiple applications of such a class of compounds, from LED (light emission diode), TFT (thin film transistors), and of course PV.

The perovskite crystal structure is particularly flexible compared to others. Several different elements and organic ions can be hosted by the perovskite structure with no or little phase segregation. The flexibility in the chemical composition of perovskite crystal structure is beneficial in terms of ease in the process and tunability of the material properties.

1.3.1 Chemistry, crystallography and properties

Perovskite is a crystal structure of the homonym mineral based on $CaTiO_3$. The general perovskite formula is ABX_3 with A and X ions forming a face centred cube (fcc) structure. The close packed layers parallel to {111} planes have the formula AX_3 (Fig 1.6a) [30]. The cation B is placed in $\frac{1}{4}$ of the octahedral interstices. If the crystal structure is not distorted, the space group will be $Pm\bar{3}m$ [31]. An alternative way to describe the perovskite structure is given by edge-sharing B-centred X_6 octahedral. The latter representation shows clearly that the perovskite structure can be distorted with relative ease (Fig 1.6b). The degree of distortion

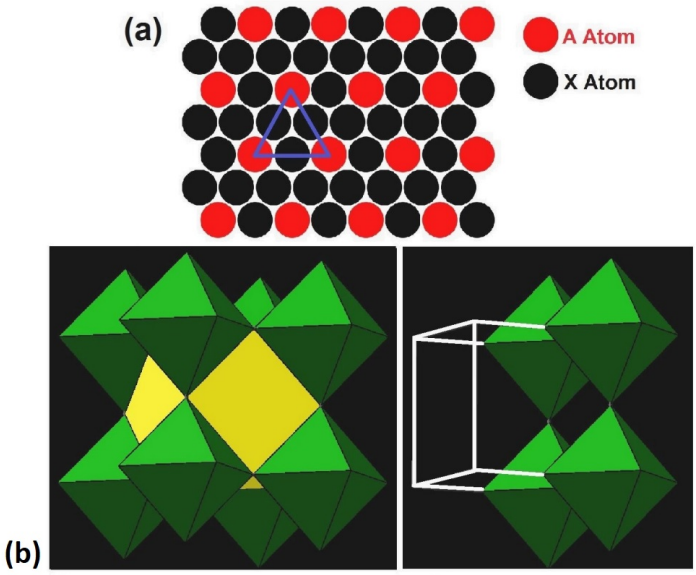


Figure 1.6: Perovskite crystal structure. (a) The AX_3 structure that is parallel layer to the {111} planes. (b) Undistorted perovskite structure (space group $Pm\bar{3}m$) in polyhedra representation. B atoms are in the centre and X at the corners of octahedral, A is cuboctahedrally coordinated. The position of the cubic unit cell is also shown.

(t) for perovskite structures can be calculated as:

$$t = \frac{R_A + R_X}{\sqrt{2}(R_B + R_X)} \tag{1.4}$$

where R_A, R_B, or R_X are the ionic radii of the respective elements in ABX_3 perovskite. The value "t" is between 0.8 and 1 in case of the perovskite structure [32], explaining why the perovskite structure is quite flexible to host different kind of elements. The elements can fit into the structure at different symmetries with a strong influence on the optical and electronic properties. Some outstanding examples of materials with perovskite structure are $BaTiO_3$ and $YBa_2Cu_3O_{7-x}$. The former shows ferroelectric properties due to the displacement of Ti and loss of the centrosymmetry. The latter perovskite is defective and it is a high-temperature superconductor [30]. In case of $CH_3NH_3PbI_3$, in this thesis known as MAPI, the crystal system is tetragonal (space group I4/mcm) at room temperature [31]. $CH_3NH_3^+$ belongs to a non-centrosymmetric group, thus it does not agree with the octahedral symmetry for the A cation required for the of the $Pm\bar{3}m$ and I4/mcm space groups. This means that the organic cation must be orientationally disordered [31].

While it is relatively straightforward to assign ionic radii for elemental inorganic ions, non-spherically symmetric organic cations and charged complexes pose a

Table 1.1: Ionic radii of some important cations and anions related to the organic-inorganic Pb halide perovskite. From reference [32].

Cation (A)		Effective ionic radius R_A (pm)
Ammonium	$[NH4]^+$	146
Hydroxylammonium	$[H_3NOH]^+$	216
Methylammonium	$[CH_3NH_3]^+$	217
Azetidinium	$[(CH_2)_3NH_2]^+$	250
Formamidinium	$[NH_2(CH)NH_2]^+$	253
Cation (B)		R_B
Lead	Pb^{II}	119
Anion (X)		R_X
Fluoride	F^-	129
Chloride	Cl^-	181
Bromide	Br^-	196
Iodide	I^-	220

greater challenge. With the assumption of the molecule being free to rotate around its centre of mass, it becomes possible to assign effective radii for organic cations. Tab 1.1 shows some of the possible ions that can be incorporated in the organic-inorganic Pb-based halide perovskite.

One of the most remarkable properties of the halide perovskites is their solubility. Halide-based compounds are soluble in different solvents, whereas oxides are not. The synthesis and the deposition of thin film perovskite, therefore, requires only the mixing of the precursors and the deposition can occur by solution-processed methods. This means that no hydrothermal, high temperature or vacuum processes are in principle needed, reducing the complexity of film fabrication.

One of the most critical downsides of the halide perovskites is the stability, which strongly limits their application. The degradation process is caused by a synergy of different factors, e.g. O_2, moisture, UV light, the solution process (solvents, solutes, additives), and temperature. Considering the special case of MAPI films, perovskite tends to hydrolyse in the presence of moisture due to the well-known high sensitivity to water, leading to the formation of $CH_3NH_{2(g)}$ and PbI_2 [33]. The presence of O_2 affects the stability of MAPI due to the formation of superoxide ($O_2^{\bullet\,-}$). The process requires the presence of photo-generated electrons in the conduction band (under illumination) [34]. Even if a MAPI film is encapsulated in a moisture-free environment, still the presence of O_2 and light will cause the generation of H_2O as by-product of the degradation process [34].

The combined effect of O_2 and light is much faster than the degradation in moisture [35] and it can be hindered with an enhanced charge extraction that removes the carrier efficiently, e.g. in presence of mTiO_2 [36] in spite of the well-known photo-degradation processes that TiO_2 can trigger under UV light [37].

Moisture and the combined effect of O_2 and light can be the cause of important degradation processes in MAPI films, but when the three factors are all present in the film, the degradation process can be much faster [38]. Films in presence of only O_2 and light degrades more slowly than films placed in the same condition and 25 % relative humidity (RH). The effect if more striking when the film is in 85 % RH. However, the degradation appears much slower when O_2 is removed, i.e. in presence of only moisture and light. Overall, the removal of both moisture and O_2 is beneficial in the stability of the film [38].

Defects in the crystal structure can facilitate the diffusion of O_2, making the film more unstable [39]. Moreover, the defects are highly energetic crystallographic sites where perovskite can start degrading [40; 41; 42]. The presence of Br^- in substitution of I^- can improve the stability of the crystal structure because the shorter Pb-Br bond is thermodynamically more stable than Pb-I [43]. The presence of Br^-, furthermore, makes the crystal structure cubic, i.e. undistorted, which helps the stability also at relative high temperature [44].

The crystallographic defects can be reduced by passivation with organic molecules [45] or even breaking the 3D crystal structure in 2D [32]. The 2D perovskite, which dimensionality refers to the corner-sharing BX_6, is much more flexible in terms of cation insertion than the 3D perovskite. As the perovskite structure is cut into slices, the size restrictions, as outlined by the tolerance factor for the 3D structures, are gradually lifted [46]. A special case is with the 5-aminovaleric acid ($NH_2(CH_2)_4COOH$, AVA) that is typically added to MAPI (AVA-MAPI) in C-PSC, forming a 2D/3D crystal structure (Section 1.4). The insertion of a large organic molecule can change the properties of the material. The electronic properties, such as the E_g, can be tuned from a 3D to a 2D perovskite [47]. Another important property than can be changed with the insertion of organic molecules is the surface energy. It is possible, in fact, to make the perovskite hydrophobic in order to improve the moisture resistivity with the insertion of relative large organic cations, i.e. tetrabutylammonium ($[N(C_4H_9)_4]^+$), butylammonium ($[NH_3C_4H_9]^+$, and octylammonium ($[NH_3C_8H_{17}]^+$), in the perovskite crystal structure [48; 49]. AVA-MAPI raised a great interest in PSC technology for the higher stability that was observed over MAPI [50; 51] as also reported in Section 3.3.3. The stability of MAPI when AVA is inserted into the crystal structure can be also attributed to the

passivation of the surface defects resulting in a superior resistance to superoxide induced degradation [52].

1.3.2 Perovskite for solar cell applications

Organic-inorganic perovskites were considered promising for flexible electronics for quite a long time. A good example is the conference proceeding of Mitzi and co-worker in 2001 [53], where organic-inorganic perovskites are presented as a good opportunity for TFTs and LEDs. This is a result of the outstanding charge mobility of this semiconductor, that can be processed by solution phase deposition. In the PV field, perovskite represents a breakthrough. The first application of PSC as alternative dye for a DSSC architecture in 2009 [16] was based on a rigid glass substrate with a $mTiO_2$ layer where a dye, or perovskite in this case, can infiltrate. Then, a liquid electrolyte was placed in contact with the active layers, as per typical DSSC architecture, resulting in a reported PCE of 3.81 %.

Perovskite is unstable in water, therefore a further improvement was done by using a solid state architecture, i.e. using Spiro-OMeTAD (2,2',7,7'-Tetrakis[N,N-di(4-methoxyphenyl)amino]-9,9'-spirobifluorene) as hole collector [54]. The performance of PSC with MAPI jumped to 9.7 % in 2012, that was in only 3 years of research. Another important milestone was achieved when an insulator material, mAl_2O_3, was used in substitution of $mTiO_2$, resulting in an enhancement in PCE, above 10 % [55]. The importance of this result, however, goes beyond the mere improvement in PCE. In a traditional DSSC, $mTiO_2$ plays the key role in the charge extraction from the dye and avoids the rapid charge recombination that would occur otherwise. However, mAl_2O_3 is an insulating material and the charge is forced to move through the perovskite. This experiment has confirmed the outstanding carrier lifetime for MAPI and the efficient charge extraction. The result has opened new prospects for PSC, from the physical and manufacture points of view: MAPI represents a unique semiconductor with an extraordinary charge mobility and charge lifetime [56; 57]; perovskite allows a great flexibility in the device architecture because the presence of the mesoporous layer is not strictly necessary for the charge transfer.

The next key experiment in the PSC evolution was the deposition of MAPI as a compact layer without using mesoporous layers. This planar device, fabricated by evaporation process in the first instance by Snaith and co-workers in 2013 [58], resulted in a new record, up to 15.4 % PCE. PSC can, therefore, assume either a mesoporous (like DSSC) or a planar (like CIGS or OPV) architecture.

PSC can assume also an inverted structure. The architecture with ETM on the

transparent conductive substrate and HTM on the top of the cell has been widely adopted with TiO_2 as n-type on the bottom cells. However, perovskite can be prepared also in an inverted architecture with a HTM on the substrate side. The most applied are PEDOT:PSS or NiO, both HTM, with PCBM as n-type material on the top of the device [59; 60].

Perovskite can be processed in a single step or in a 2-step approach. In a single step approach, all the precursors of perovskite are dissolved in the same solvent to make a solution that can be deposited on the substrate. The single step deposition represents a low-cost and facile route towards high-performance PSCs. The perovskite absorber is deposited starting from a solution of both PbX_2 and CH_3NH_3X (X: I, Cl, Br) in a polar solvent, such as N,N-dimethylformamide (DMF) [61], dimethyl sulfoxide (DMSO) [62], or γ-Butyrolactone (GBL) [63] or mixed solvents [64]. Although the film deposition is very easy, the control over the crystallization process can be difficult due to several factors that affect the film formation. Among the several approaches to improve the crystallisation control and reliability, it is important to state the anti-solvent method. Designed for spin coating deposition, a non-polar solvent is spun on the just deposited perovskite film to extract the remaining solvent and improve the perovskite crystallinity. The first anti-solvent reported dripping chlorobenzene onto a spinning MAPI film from a DMF solution, resulting in planar cells with PCE of over 13 % [65]. Other solvents were also reported, allowing the manufacture of perovskite thin films even in high humidity environments [66]. The 2-step deposition was originally introduced for the deposition of PbI_2 via spin coating followed by a second step, i.e. the immersion in a solution of methylammonium iodide (CH_3NH_3I, MAI) [67] as $PbI_2 + CH_3NH_3^+ + I^- \longrightarrow CH_3NH_3PbI_3$. PbI_2 films converted instantaneously into $CH_3NH_3PbI_3$, enabling much better control over the film morphology and higher reproducibility than with standard single step deposition. However, 2-step deposition introduces an additional step, making the process more complex and slower.

Another outstanding characteristic of PSC is the ambipolarity [68; 69], that is, when the harvest material can also play the role of either HTM [70] or ETM [71]. This property can be exploited to reduce the complexity of the device fabrication by removing a layer, as also observed in C-PSC (Section 1.4).

The chemical composition of perovskite can be very flexible, as already pointed out in Section 1.3.1. The exchange of the cation in the "A" site, until now occupied

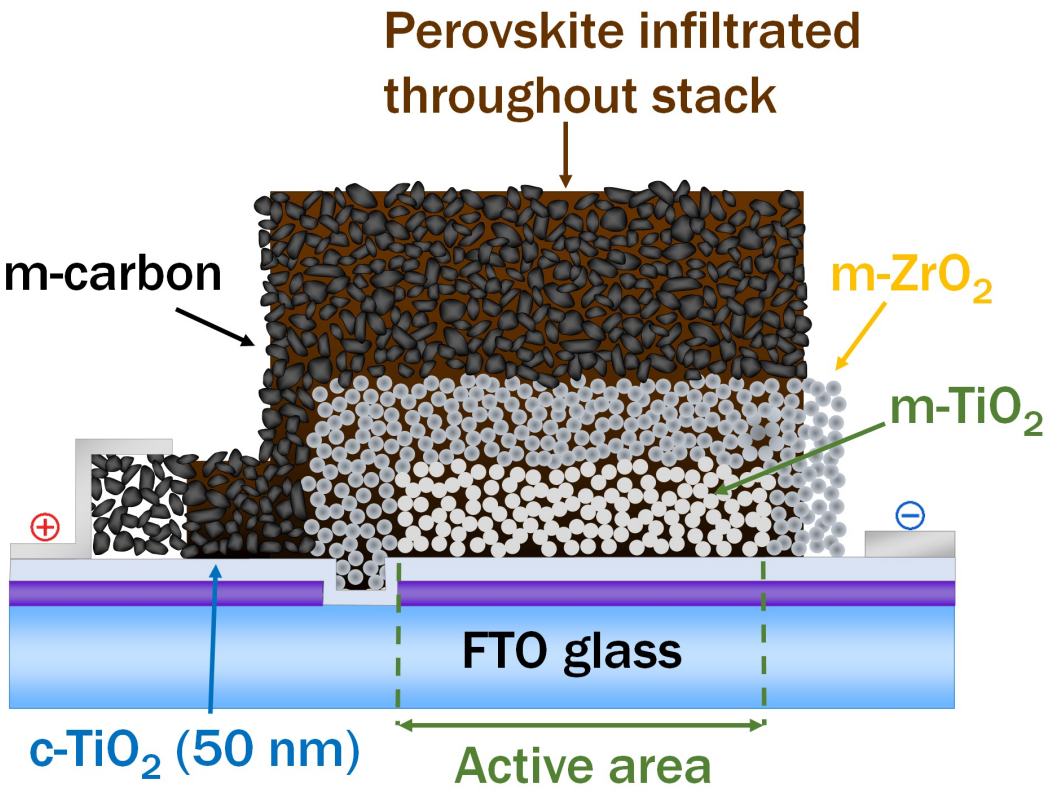
by $CH_3NH_3^+$, can result in improved performance and/or stability. The variation with formamidinium ($HC(NH_2)_2^+$) in a mixed MAPI composition [72], and the triple-cation composition, i.e. Cs^+, $HC(NH_2)_2^+$ and $CH_3NH_3^+$ [73] are prominent examples of mixed cation perovskites. Fully inorganic perovskites have been studied, especially for the attraction to improve the long-term stability of the material. The only inorganic cation that can fit in the A site for a 3D Pb-based perovskite, is Cs^+. Examples of Cs perovskites are $CsPbI_3$ [74] and $CsPbBr_3$ [75; 76].

The halides can be substituted resulting in an easy and effective way to tune the E_g [77; 78; 79]. The 3:1 molar ratio CH_3NH_3I:$PbCl_2$ perovskite (MAPIC) is an important example of harvesting material [80]. However, MAPIC was reported to result in a MAPI composition with an improved crystal formation because Cl^-, which is much smaller than I^-, allows a rapid crystal formation of $CH_3NH_3PbCl_3$ but $CH_3NH_3PbI_3$ gradually forms due to the higher thermodynamical stability, with the exclusion of $CH_3NH_3Cl_{(g)}$ [81].

Pb-free perovskite alternatives have been investigated. The issue of the use of Pb is related to its toxicity, which is made worse by its solubility in water [82; 83; 84; 85]. The perovskite crystal structure does not require Pb, and alternatives can be adopted, e.g. Sn [86; 87], Bi [88; 89], Bi-Ag [90] and others. However, the astonishing results that were achieved in the last years in PV were possible with the Pb content in the perovskite crystal structure, making the substitution of the toxic element challenging. The Pb-free perovskite for PV applications is still an open field and, so far, the optimal option to utilise PSC in a real environment is the development of encapsulation strategies to properly protect the device.

1.4 The fully printable carbon perovskite solar cells

C-PSC is a fully printable architecture based on three porous layers, or triple mesoscopic stack, with carbon as counter electrode. It was developed for both PSC and DSSC by Han and co-workers in 2013 [91; 92]. This special architecture, that can work with either a dye or perovskite, has found a larger interest for PSC applications. A schematic of the C-PSC architecture is shown in Fig 1.7. The C-PSC shows lower PCE compared to other PSC types in terms of record efficiency on lab scale cells, i.e. about 17 % [93], versus over 22 % for a $mTiO_2$/perovskite/poly(triarylamine) (PTAA)/Au [94]). However, some key aspects to enable large scale production are satisfied in C-PSC, i.e.:



[h]

Figure 1.7: Schematic cross section of the C-PSC showing the conductive glass substrate with layers of TiO_2, ZrO_2, carbon, and the infiltration of perovskite through the mesoporous layers as last step.

- low capital cost, especially because of the use of low-cost screen printing;
- the use of inexpensive materials, excluding layers of gold or Spiro-OMeTAD [92; 95; 96];
- high performance even after long term exposure (more than 1000 h) in different working environment and external stresses when AVAI is added to the perovskite solution [95; 51; 97].

The architecture is based on a three-layers stack which includes firstly a $mTiO_2$ layer ($mTiO_2$) followed by a mesoporous ZrO_2 layer ($mZrO_2$) as an insulating spacer and then, finally, a porous conductive carbon layer as top contact. To complete the device, droplets of a perovskite solution are applied to the carbon surface which then wet and infiltrate through the porous stack. Because of the high temperature process at which each layer needs to be fired to remove the binder and leave open pores to infiltrate perovskite, a rigid glass substrate must be adopted. This glass is usually coated with fluorine-doped SnO_2 (FTO) as electrode and compact TiO_2 as blocking layer (bLayer). When the charge is generated, the

electrons are injected into TiO_2, which is close to the transparent electrode (or photoanode), whereas the holes are transferred through perovskite to be injected into the top electrode (or cathode, Fig 1.8a). The stack is very thick compared to conventional architectures, in the order of μm, so only perovskite with very high charge mobility and lifetime can support the long path at which the charge must travel without significant recombination. The holes are, then, injected into the carbon layer, which is massively thicker than the other layers to achieve enough conductivity (Fig 1.8b).

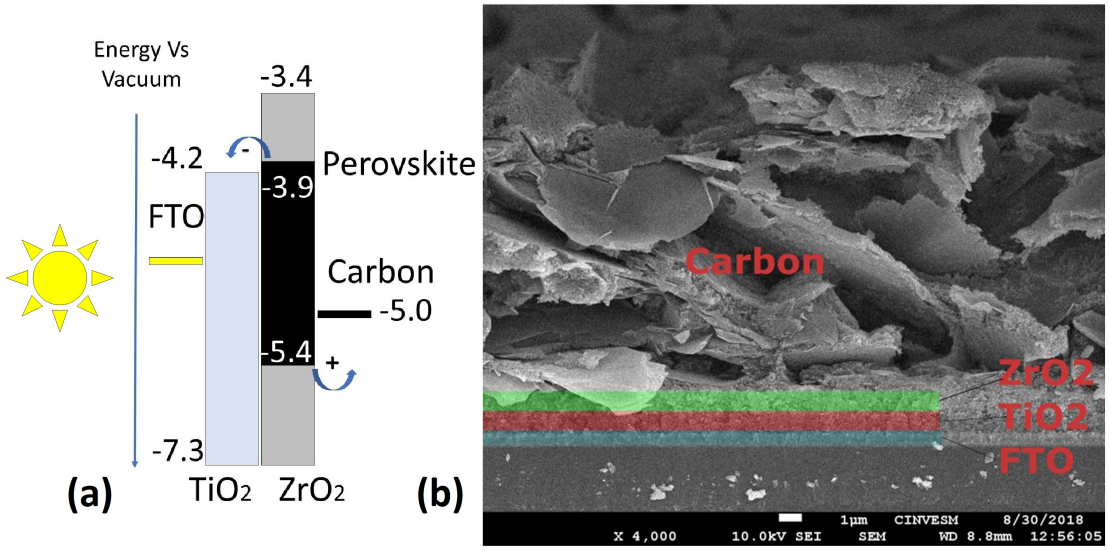


Figure 1.8: (a) Energy level and band gaps of TiO_2, ZrO_2, and carbon showing the active role of perovskite in the charge transfer through the ZrO_2 layer. Values from reference [98; 99]. (b) SEM cross section of a device with false colouring map. SEM images kindly taken by Dr. Dena Pourjafari from CINVESTAV-Mérida.

Other PSCs based on a carbon top electrode were proposed, where perovskite is deposited before carbon [100] and no insulating layer is necessary because the perovskite capping layer plays the role of spacer layer. However, the chemical composition of the binder for carbon needs to be designed in a way that does not affect the perovskite. The C-PSC, which is based on the triple mesoscopic stack, has a number of advantages compared to the other carbon devices. First, it can be printed to form a very stable inorganic stack where perovskite can be infiltrated when required. This is advantageous for an eventual industrial production, where meters of layers can be printed and stored, and the infiltration can occur only on demand. Another advantage is the relatively simple recycling process. The perovskite can be washed off when the device is exhausted, to recycle both the inorganic stack and the Pb content [101]. A disadvantage of the C-PSC is that the layers need to be fired at very high temperature in order to remove the binder and

leave porous layers. This means that a large amount of energy needs to be spent during the fabrication. However, the energy consumption, as well as the heating time, can be strongly reduced using NIR ovens [102].

The first reported PCE for the C-PSC was 6.6 % on an active area of 0.5 cm^2 and mask open area of 0.125 cm^2 [92]. Since then, the perovskite formulation and the layers of the stack were optimised to improve both stability and performance. In the following, the most important modifications in the perovskite formulation and stack, to enhance both performance and stability, are discussed.

1.4.1 Modifications in the perovskite formulation

MAPI

The first applied perovskite in C-PSC was MAPI deposited by the 1-step deposition [92] with PCE of 6.6 %. Also the 2-step deposition was adopted with PCE up to 11.9 %, obtained in 2016 [103]. The use of N-methyl-2-pyrrolidone (NMP) was reported for the manufacture of 15 % device based on the single step deposition of MAPI [104]. The DMF/DMSO mixture is also reported for highly performing MAPI C-PSCs [105]. An outstanding device with MAPI as harvesting material is fabricated with an extra interlayer of NiO between ZrO_2 and carbon to improve the hole extraction in 2015 (14.9 % [106]).

AVA-MAPI

An important aspect of the C-PSC is the stability. The addition of AVAI in the MAPI formulation in a single-step deposition can enormously improve the stability, as reported since its first appearance in 2014 [50]. The high stability of the device was further investigated under simulated sunlight with the UV component [107]. Grancini et al. have shown the long term high performance without the UV component and devices encapsulated in air [51]. The outstanding stability of the AVA-MAPI was attributed to the 2D/3D nature of the perovskite, where the 2D component protects the 3D perovskite. In fact, the presence of the 2D/3D crystal structure allows an improvement of the stability [108] due to the low defect concentration typical of the 2D perovskite, without affecting the highly efficient charge transfer [52].

The interest in the AVA-MAPI C-PSC is not only related to the application and engineering point of view, but also from the physical point of view. Since the first publication [50] the need for 3 minutes of light soaking to properly measure the

device with the AVA-MAPI was outlined. The J_{sc}, in particular, was reported to be strongly affected by the light soaking, making the external quantum efficiency (EQE) measurement difficult to relate to the current. The effect can be attributed to the exceptionally slow response time under illumination [109]. Some aspects of these phenomena will be discussed in Section 3.3.4.

Another special characteristic of AVA-MAPI C-PSC is the possibility to improve PCE and JV hysteresis with a post-annealing process in humidity condition (70 % RH) [110]. Although it is not clear whether this treatment acts as just an accelerating ageing effect on the device [28], the result gives confidence that the manufacture process can simply occur in ambient condition. Moreover, the peculiar effect of the moisture that is observed in this kind of PSC increases the scientific interest behind the chemical mechanisms that act in this architecture.

The highest performing device with AVA-MAPI, $mZrO_2$, no HTM and no special modifications on the carbon layer was reported to be around 14 - 15 % in 2018 [111; 112], although the performance seems strongly related to both the thickness and conductivity of the carbon.

Other formulations

Other perovskites that were utilised in the C-PSC include mixed cations, e.g. MA/FAB (Methylamine and Formamidinium [113; 114; 115] or triple-cation with Cs [116] and Br perovskites [117; 118]. Other additives, e.g. BF_4 [119], Phenethylamine [120], NH_4Cl [121], were also reported. The optimal performance is achieved with $Cs_{0.05}(FAB_{0.4}MA_{0.6})_{0.95}PbI_{2.8}Br_{0.2}$ triple-cation perovskite and NiO interlayer, which is reported to be around 17 % PCE in 2017 [116]. With a simplified architecture without NiO, the mixed cation with FAB and Cs was reported to achieve 15 % [122].

1.4.2 Modifications in the triple mesoporous stack

The triple mesoscopic stack plays an important role in the performance of the C-PSC. In following, the modifications that were reported for each layer will be discussed.

The effect of the carbon counter electrode

The thickness of the carbon layer affects both the infiltration and the conductivity. The conductivity of the carbon increases with the thickness, which is beneficial to the device performance, especially in terms of FF. However, thick car-

bon layers can negatively affect the performance of the devices because they can hinder the infiltration of perovskite. An optimal thickness was observed to balance conductivity and infiltration and was reported to be between 9 and 14 μm [123]

The morphology of the carbon particles plays a role in the infiltration. Large flakes of graphite can result in compact or semi-compact layers that do not allow the infiltration of the perovskite [92]. The use of carbon black can increase the porosity of the layer. Therefore, an optimised ratio of graphite and carbon black is necessary [124].

The deposition of an extra conductive layer on the top of the device after perovskite infiltration was reported with the use of graphite flakes (up to 14 % from 12.6 % PCE) [125] or carbon nanotubes in a NiO matrix (up to 12.7 % from 10.5 % PCE) [126]. The carbon layer does not act as an effective electron barrier and, to increase the hole selectivity of the top electrode, the work-function of carbon can be raised by functionalisation. An approach is to use oxygen groups, i.e. C-OH or C=O [112], approach that was reported to achieve the highest performance for C-PSC based on AVA-MAPI, up to 15.7 % from 13.6 % PCE. Similarly, also B was tried to functionalise the carbon layer with an increase from around 12.5 to 13.5 % PCE [127].

Since the first publication of the C-PSC, it was clear that all the layers, including carbon, require to be fired at high temperature to remove the binder of the ink and leave porous layers. The presence of binder in the carbon layer, in fact, affects the performance of the device, especially where there is a chemical interaction with the perovskite [102]. The effect of the heating temperature in device and, thus, the effect of the remaining binder in the device, was systematically studied and reported in 2019 [128].

The effect of the insulating layer

The spacer layer is crucial in the C-PSC architecture. The insulating oxide gives a separation between the n-type material and the top electrode avoiding recombination in the eventual TiO_2/carbon interface. This layer is not present in other architectures where the HTM, or a capping layer of perovskite, gives the necessary separation between the top electrode and the ETM [70; 71; 100].

The most widely used spacer layers are mZrO_2 and mAl_2O_3, but also mesoporous SiO_2 (mSiO_2) has been reported. It seems logical to think that the spacer layer should be thick enough to avoid any pinhole and properly separate carbon from TiO_2, but also thin enough to not hinder the charge transport. According to early reports, the spacer layer is crucial to obtain working devices, and the optimal

thickness of the spacer layer can be larger than 1 μm [129]. In particular, it is reported that with the thickness of the spacer layer, J_{sc} and V_{oc} tend to improve, whereas the FF is roughly independent. When the layer is too thick, however, the FF and V_{oc} are negatively affected whereas the J_{sc} may still improve. The optimum thickness of the spacer layer was reported to be between 1 and 1.4 μm for ZrO_2 in 2015 [129]. However, efficient devices with more than 15 % PCE can be achieved with 3 μm as reported in 2018 [111; 130]. Reference [111] and [130] do not focus on the role of the spacer layer and the reason for the exceptional thick insulating layer of such efficient devices is not discussed. However, devices with 3 or 2 μm thick ZrO_2 layer show better performance than devices with 1.2 μm ZrO_2 layer if the stack is properly infiltrated with perovskite according to reference [111]. Apparently, the infiltration of the perovskite solution is more critical when the ZrO_2 layer is thicker, but higher performance can be achieved. This aspect will be further discussed in Section 3.3.7.

Much thinner spacer layers, in the order of hundreds of nm, were obtained by spin coating as reported in a publication focusing of the role of the ZrO_2 thickness [131]. The architecture is, however, slightly different to the C-PSC because a glass/FTO/bLayer/mTiO_2/mZrO_2/perovskite/carbon architecture, where perovskite was deposited before the carbon layer, was used. In this system, perovskite can form a capping layer that play the role of the spacer between ETM and the carbon top electrode, turning the role of mZrO_2 layer to a mere scaffold where perovskite can crystallise.

Al_2O_3 is also a common spacer layer, although the AVA-MAPI perovskite was reported mostly in combination with ZrO_2. A comparison between Al_2O_3 and ZrO_2 in presence of AVA-MAPI can be found in reference [132]. Al_2O_3 was reported to achieve high performance with different perovskite formulations, e.g. MAPI [133; 126; 134; 135], MAPIBr [136], and triple-cation [116]. The combination of Al_2O_3 and triple-cation is so far the best reported for the preparation of C-PSC in terms of PCE (17 %). Another example of spacer layer is SiO_2 with either MAPI [103] or AVA-MAPI [121].

The effect of the mesoporous TiO_2 layer

The thickness of the TiO_2 layer is reported to be around 1 μm [51] or less [137; 120]. The effect of the particle size was reported to have little effect on the PCE of the devices [138]. When the particle size is around 15 nm in diameter, a low PCE (between 8 and 10 %), compared to other devices prepared with nanoparticles of

from 20 to 35 nm (all around 11 %), was reported. Also, the use of nanosheets instead of the more common nanoparticles was reported [98].

The expected role of $mTiO_2$ is to offer a very large surface where perovskite can interface with the ETM and inject the electrons. The removal of the $mTiO_2$ causes a decrease in the C-PSC device performance, unless a much thicker $mZrO_2$ is utilised [139]. In detail, $mZrO_2$ must be increased from 1.4 to 2.1 μm to substitute the 0.5 μm layer of $mTiO_2$ and achieve nearly the same performance of a standard architecture in the reported work (11.9 % PCE standard architecture, 7.8 % PCE without $mTiO_2$, and 9.7 % PCE with thicker $mZrO_2$) [139]. This result leads to think that $mTiO_2$ does play an important role in the device performance, but the key parameter is the distance between carbon top electrode and photoanode.

The effect of the blocking layer

The thickness of the bLayer plays an important role. Thin bLayers are more transparent and more conductive in the z-direction compared to thick ones. Moreover, a correlation between the thickness of the bLayer and the hysteresis for the C-PSC was reported. In particular, the hysteresis can be suppressed, or even inverted, when the bLayer is very thin, up to around 13 nm for no hysteresis or 7 nm for inverted hysteresis [140].

The bLayer is typically deposited by spray starting from a solution of titanium diisopropoxide bis(acetylacetonate) (TAA), but other deposition techniques can be adopted, including screen printing [141]. Spray pyrolysis can achieve very thin and compact layers. However, other techniques are more reliable for a very thin layer, for example Atomic Layer Deposition (ALD). An example of application of ALD on carbon-based PSC is given in reference [142], where a non triple mesoscopic C-PSC was utilised.

The addition of a hole transporting material

The C-PSC is often defined as HTM-free. However, HTM can be utilised in the architecture to improve the hole extraction. Because the C-PSC is based on layers that can be fired before the deposition of perovskite, inorganic materials must be used.

The most common and successful HTM is NiO, introduced by Wang and coworkers in 2015 by using Al_2O_3 [133] or ZrO_2 [106; 143] as insulating layer. However, most of the research activity with NiO was carried out with Al_2O_3, including the C-PSC with highest reported PCE [116]. Another strategy to deposit NiO on $mZrO_2$ is via flame assisted chemical vapour deposition (FACVD), allowing a

small improvement in PCE for C-PSC [144]. This technique allows the deposition of a very thin layer of oxide in nanoparticle form on another mesoporous layer, such as $mZrO_2$. Other strategies to improve the hole extraction in the C-PSC includes the use of NiO in the carbon ink [145], the use of the spinel Co_3O_4 [146] or the Cu-doped NiO [147].

1.5 Theoretical behaviours

The interpretation of the PV parameters can be helped with the understanding of the theoretical behaviour of the devices. In particular, the interpretation of the issues related to the parasitic resistances, i.e. the series resistance (R_s) and the shunt resistance (G), can help the improvement of the devices from small scale to large area modules. Starting from the diode equation, some basic theoretical behaviour will be shown, to facilitate further discussions in this thesis.

The general diode equation that describes the JV curve, including the effect of the parasitic resistances, is:

$$J = J_o \left[e^{\frac{q}{A \cdot K \cdot T}(V - J \cdot R_s)} - 1 \right] + \frac{V - J \cdot R_s}{G} - J_L \tag{1.5}$$

where "J_o" is the dark saturation current density, "q" the electrical charge, "A" the ideality factor, "K" the Boltzmann's constant, "T" the temperature, "V" the applied voltage and "J" is the current density output. A simplified equivalent circuit of a single cell is shown in Fig 1.9.

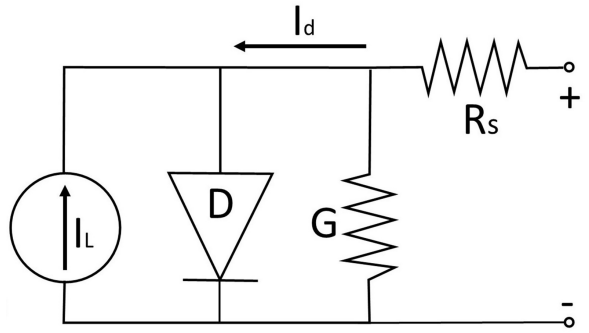


Figure 1.9: Simplified equivalent circuit of a single cell with a diode (D) and the parameters of Eq 1.5.

1.5.1 The shunt resistance

The current flows in one direction in a p-n junction. However, preferential paths can be found to bypass the diode. G is the parallel resistance that hinders

the charge to move from alternatives paths that are not the diode itself (Eq 1.5 and Fig 1.9). The effect of a poor (low) G on the JV curve is a loss in the typical flat shape of the diode curve at low applied voltage. The main effect is on the FF but, when G is particularly low, also the V_{oc} can decrease even by few hundreds mV in extreme cases (Fig 1.10a). Typical factors that can reduce G are:

1. The top and bottom electrodes are shorted. This can be caused by:
   (a) design issue;
   (b) registration issues, i.e. mismatch between layers during printing processing;
   (c) material removal issues, i.e. an incorrect removal when the electrodes are patterned.
2. Pinholes in either HTM or ETM.
   The presence of pinholes and defects in general becomes more important during the up-scaling of the device because the likelihood to have defects on the active area increases with the device size. In order to avoid the decrease of G, high homogeneous deposition over large area is crucial for successful up-scaling.

1.5.2 The series resistance

The generated power of a solar cell is also dissipated by the resistance during the charge transfer. In particular, the distance at which charge needs to flow, the resistance of the electrodes and the resistance between the layers, can have a great impact on the cell performance. All these effects can be included in R_s (Eq 1.5 and Fig 1.9). The effect of R_s on the JV curve is the loss of the typical steep decay in current from just below the V_{oc}, due to the hindered flow of current between the electrical contacts. The FF is mainly affected but also the J_{sc} can be reduced when R_s is particularly high (Fig 1.10c). The factors that can increase R_s are:

1. The conductivity of materials.
   The higher is the conductivity of the materials that are utilised in the device, the lower the resistance will be. This is reflected on:
   (a) the resistance through the layers inside the stack.
   Very thin films can minimise the resistance through the layers in z direction. However, the thickness cannot be too low, for example, to

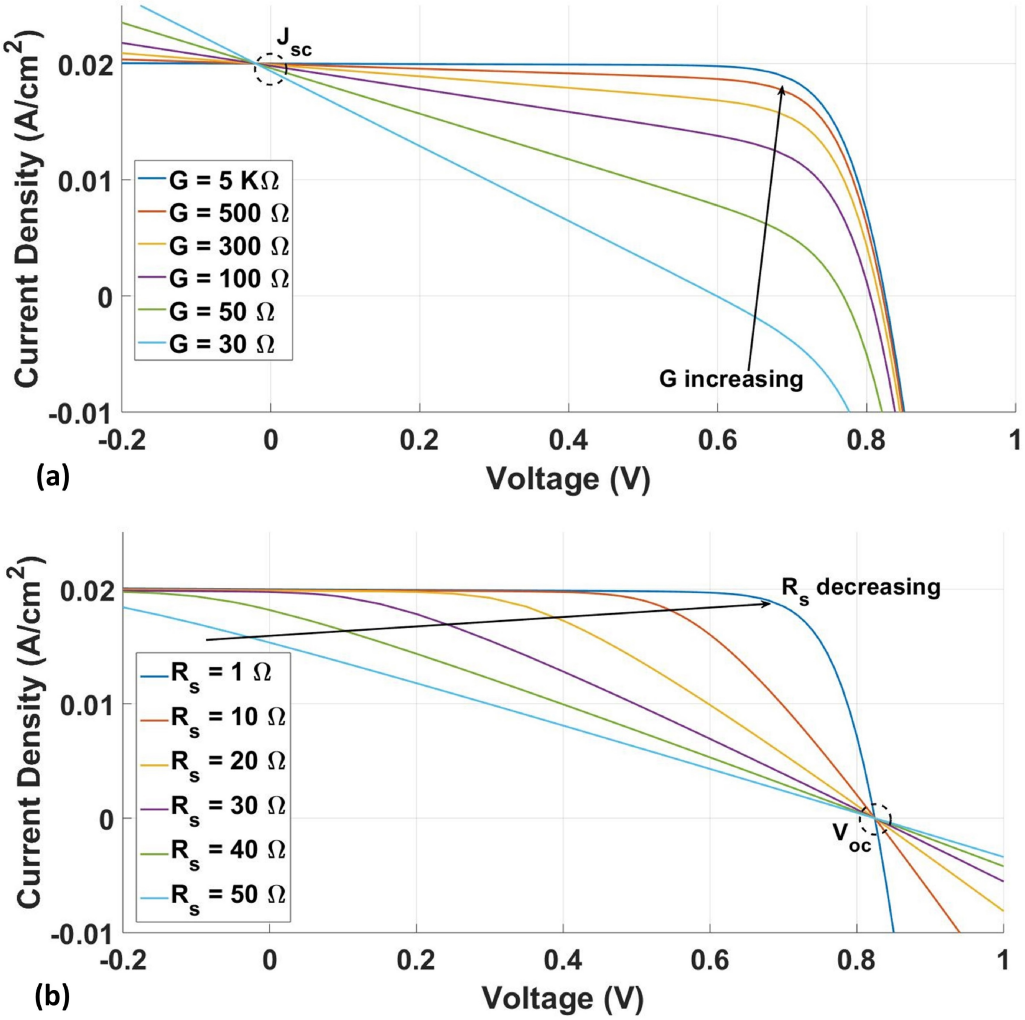


Figure 1.10: The effect of (a) G and (b) R_s on the JV curve. The set parameters, unless when specified, are $I_o = 1{\cdot}10^{-11}$ A, T = 298 K, A = 1.5, $R_s = 1\ \Omega$, G = 5 KΩ, $I_L = 20$ mA, and active area 1 cm^2. Calculation performed with Matlab.

allow a proper light absorption by the harvesting material (perovskite in this case) or minimise the likelihood to have defects and pinholes in the layer.

(b) the lateral resistance.

The electrons should be collected as close as possible to the position of the charge generation. This parameter is usually not difficult to optimise in small devices, but is crucial in large-area modules. The lateral conductivity can be easily increased with the thickness of the electrode, but this approach might have some side effects. For example, the carbon layer utilised in C-PSC can hinder the infiltration of perovskite solution when it is too thick.

(c) contact resistance.

In series connected modules, single cells are connected through a contact resistance that must be minimised.

2. The design of the device.
   Appropriate geometry is required to overcome the issues related to the lateral resistance of the layers and the contact resistance at the interconnects (R_c). This is crucial especially during the up-scaling, where the material conductivity becomes more important due to the increased distance that charge must travel.

1.5.3 The current-resistance drop

R_s causes a drop in voltage proportional to the current. In Eq 1.5, R_s multiplies J, thus, when J is small or even zero, R_s plays a negligible role or no role at all. This is also observable in Fig 1.10b at open circuit condition, i.e. J = 0, where no effect is observed on the V_{oc} at different R_s scenarios. This effect is commonly known as current-resistance drop (iR-drop) [148].

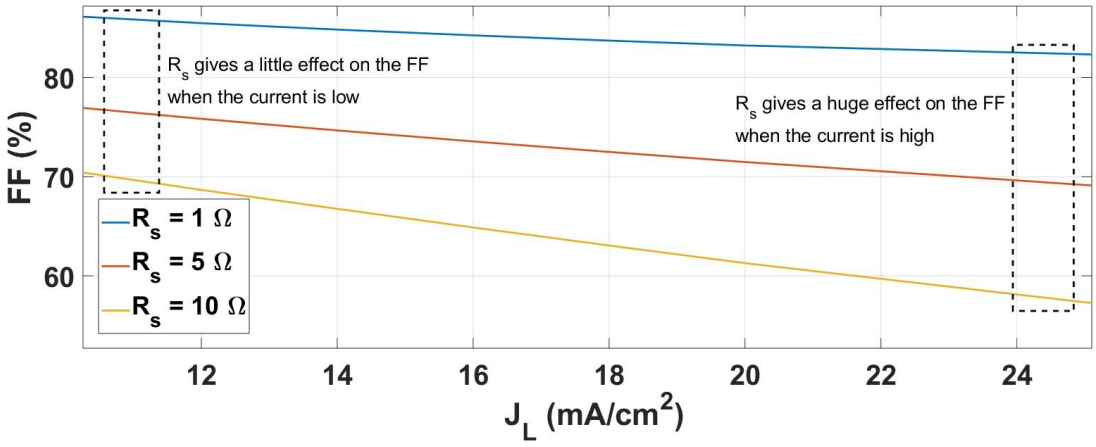


Figure 1.11: The effect of the current on the FF due to the R_s. At given R_s the effect of the current reduces the FF. The trend becomes more striking when R_s increases. Calculation according to Eq 1.5 made with Matlab.

R_s becomes more prominent when the current increases, giving an effect on the FF, as the plot in Fig 1.11 shows. Generally speaking, the FF cannot be compared between devices when the current is significantly different, especially in C-PSC where very conductive metal electrodes are not utilised.

1.6 Large scale devices

The main issues of the up-scaling of thin film devices are:

- the deposition of the layers without defects, e.g. pinholes, which can affect G, or layer thickness inhomogeneity;
- the increase in R_s due to the device size. R_s, however, can be kept low enough with optimal design and electrical connection.

The likelihood of defects in the active layers increases with larger area devices. Therefore, homogeneity and control of the film deposition becomes more important. A special method to deposit perovskite on the C-PSC over large areas is presented in Chapter 4.

The electrical connection and design are the second main issues that need to be addressed in order to scale-up solar cells. The R_s increases with the substrate size. In order to limit this effect, electrical connections need to be placed as close as possible to the area where the charge is generated. A possible approach is to use a metallic grid that can be printed on the transparent side of the device. Screen-printed Ag grids are the most common solution to the issue, especially in Si SC. Still, some areas are shadowed by the metallic grid, so a portion of the device is inactive. Conductive inks can be expensive and can chemically interact the active layers. Perovskite, for example, can react with Ag and many organics that might be present in the ink, especially in C-PSC where the conductive ink may penetrate through the porous carbon and enter into direct contact with perovskite.

When the size of the cells is limited by the conductivity of the electrodes, connection of single cells in parallel or in series are possible. In this case, the R_s is small due to the small width of the single cells. The connection can occur externally from the substrate or on the same substrate. External connections, however, might require high manufacturing work and complexity due to the wiring in the final device. Connection on the same substrate, by contrast, can be manufactured in a single pass during the layer deposition.

In order to prepare modules on the same substrate, different patterning methods can be used, i.e. printing technology, material removal, and material exclusion. Cells can be connected in parallel or in series. These designs will be discussed in the next two sections.

1.6.1 Parallel-connected modules

When cells are connected in parallel, it is possible to fabricate a device where current increases with the number of the cells (n_c, Fig 1.12a). From the electrical point of view, a parallel-connected module (Pa-M) behaves as if it was a large solar cell but the construction does not require highly conductive electrodes.

The most reported architectures for Pa-M are based on long and narrow single cells deposited on a transparent conductive substrate, such as FTO glass. The cells are then connected in parallel by either a second conductive substrate that seals the device from the top, or by busbars that are printed on the same substrate (Fig 1.12b). The former approach is widely used in DSSC with liquid electrolyte, because the double glass, which seals the active layers in between, also allows the electrolyte to be incorporated [149].

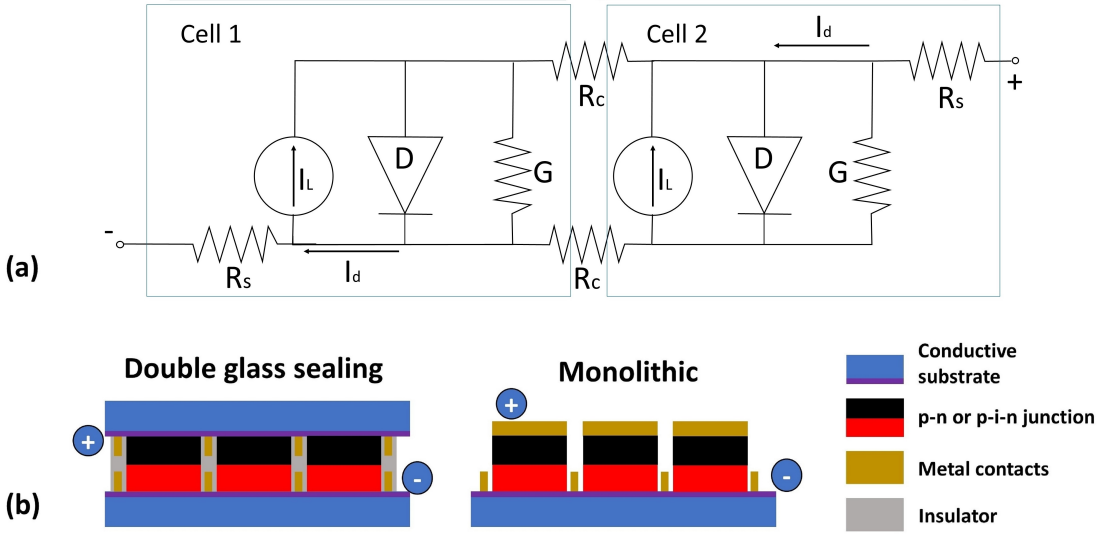


Figure 1.12: Schematic representation of Pa-M. (a) Semplified equivalent circuit of two single solar cells. (b) Two possible configurations to connect cells in parallel. Two conductive glasses can be in electrical contact with one side and the other side of the solar cells; monolithic configuration where the contact are on the same substrate.

1.6.2 Series-connected modules

When cells are connected in series, to make a series-connected module (Se-M), the voltage increases proportionally with n_c (Fig 1.13a). Conversely, current is limited by the cell with the lowest current. Therefore, the overall current density referred to the module active area is inversely proportional to the number of cells.

Each cell in Se-M transports charge along adjacent cells. The conductive bus-bar, required for local charge collection in Pa-Ms, is therefore rendered unnecessary.

This removal of the busbar makes the construction simpler and more inexpensive, which is an interesting advantage over Pa-M. The possibility to increase the voltage of the device is the special feature that differentiate Se-Ms from Pa-Ms and large solar cells. This means, that whereas either Pa-M or large solar cells can be fabricated to increase the current, depending on the conductivity of the electrodes, Se-Ms are always necessary to increase the voltage. However, it should be underlined that the combination of large cells and/or Pa-M with Se-M would allow a proper customisation of current and voltage for specific applications.

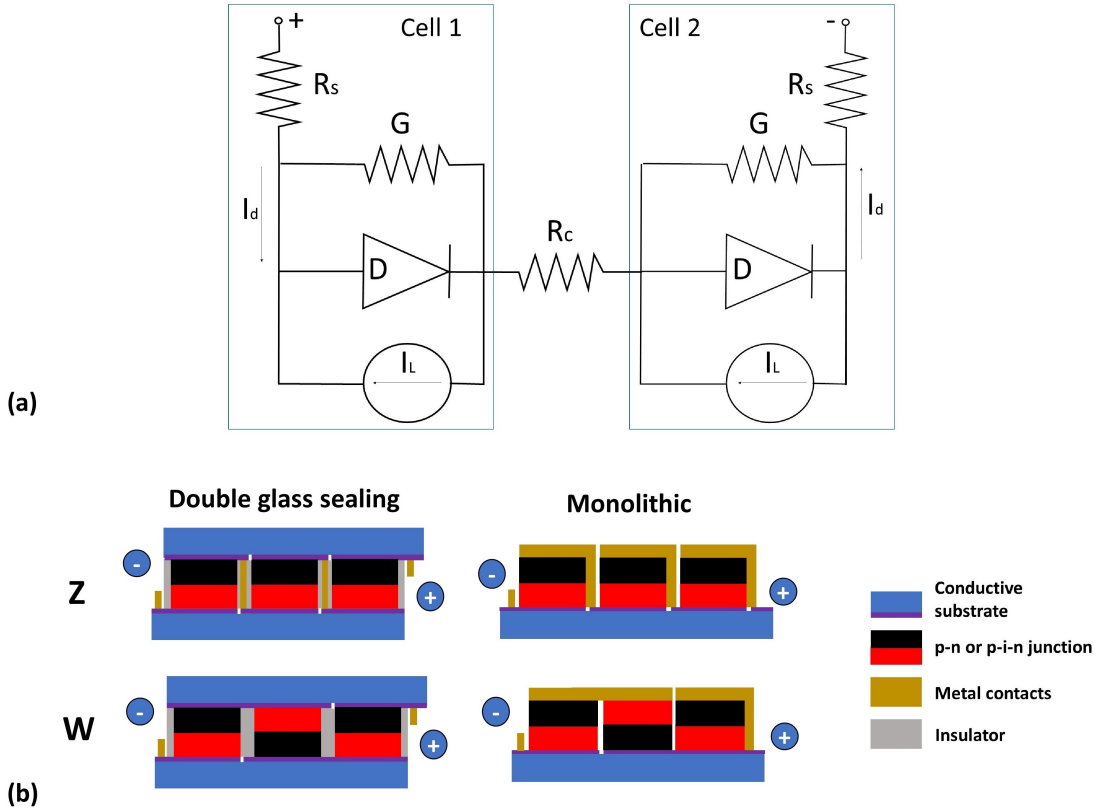


Figure 1.13: Schematic representation of Se-M. (a) Simplified equivalent circuit of two single solar cells. (b) Two possible configurations for Se-M. Z-series interconnect type of module, where the cells are all oriented in the same directions, and the W-series interconnect type module, where the cell are regularly flipped from one to another.

Se-M can be fabricated between two conductive substrates or in a monolithic design, like in the case of Pa-Ms. The two conductive substrates approach, as for Pa-Ms, is typically used for devices with liquid electrolyte, such as DSSC. Furthermore, Se-M can be designed in "Z" or "W" orientation, i.e. the same orientation or flipped orientation [150] (Fig 1.13b). The W configuration has advantages in the case of double glass sealed modules, since vertical metal connections are not required. However, changing the orientation of the cells like in the W configuration,

adds further complexity in the design because the generated current of cells at different orientation may be different, especially due to the different light absorption of the HTM and ETM. In W configuration, therefore, the design may consider different size for different cells in order to achieve a current match. Solid-state based devices are generally prepared via a monolithic architecture in Z configuration, although the W configuration is also possible.

In this work, the up-scaling effort focuses on the monolithic Se-Ms in Z configuration and "module" will refer to this, unless differently specified.

1.6.3 The geometric fill factor

The quality of a module design is not evaluated only by the PCE referred to the active area, but also by the power produced considered the total area of the device. A good design should maximise the coverage of the active area of the cells on the substrate. If the substrate was completely covered by the active area, all the available area would be active and the power maximised. The coverage (Cv) of the substrate is defined as:

$$Cv \;=\; \frac{Active\ area}{Substrate\ area} \tag{1.6}$$

The main factors that limit the coverage are:

- the inter-cell separation required for the interconnects;
- the presence of edge electrical contacts to collect the current;
- the space required for the device encapsulation.

The electrical contact and encapsulation area can be minimised by precision printing, such as screen printing or inkjet. The impact of the contacts and the encapsulation on the coverage, moreover, become less important during the scaling-up process because they occupy a smaller portion of the substrate with the increase of module size. The intrinsic limitation on the coverage is the inter-distance between cells.

In order to define the Cv in consideration only on the active area and interspace, the coverage can be referred only of the aperture area and called "aperture ratio" (A_r), defined as:

$$A_r \;=\; \frac{A_a\ n_c}{A_a\ n_c \;+\; A_d\ (n_c - 1)} \;=\; \frac{W_a\ n_c}{W_a\ n_c \;+\; W_d\ (n_c - 1)} \tag{1.7}$$

where "A_a" is the active area and "W_a" is the relative width, "A_d" is the dead area and "W_d" is the relative width (Fig 1.14). When the length of the cells is the same, either the areas or the widths can be used.

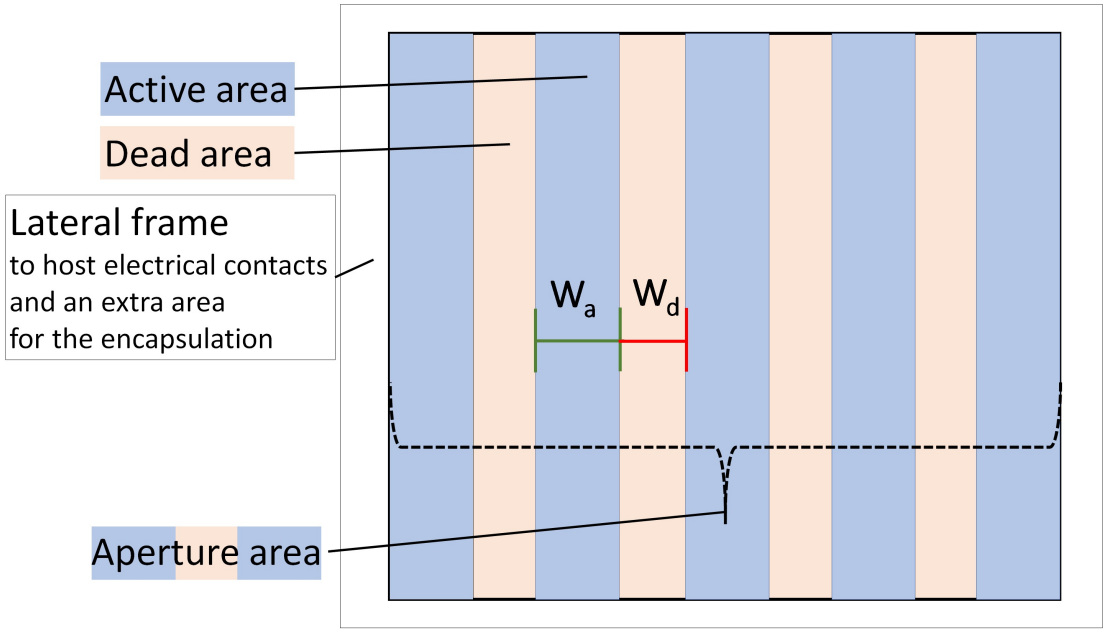


Figure 1.14: Generic scheme of a module with $n_c = 5$.

The factor "-1" arises from the fact that there are -1 interconnects compared to n_c. When n_c is small, -1 is important and the coverage is high and vice-versa. When $n_c \rightarrow \infty$, "-1" is negligible. In this case, it is possible to define a parameter that is independent from n_c and that represents the coverage of a very large scale device. This is called here geometric fill factor (g-FF), and is defined as:

$$g - FF = \frac{W_a}{(W_a + W_d)} \tag{1.8}$$

The effect of the design on Cv, A_r and g-FF will be discussed in Section 6.3.1.

1.6.4 Nomenclature for modules

Modules in series connection can present values of voltage and current that are difficult to relate to the typical values for single small devices. For example, the voltage is the sum of the voltages of the single cells in Se-M (Section 1.6.2), thus, a high V_{oc} for single cells, e.g. 1.2 V, is very low for a Se-M. Special nomenclature was therefore introduced for relating module performance to that of single devices. Furthermore, some terms are not univocal or not generally known and clear definitions are important for this work.

- PCE. As for small devices, PCE refers to the power conversion efficiency relatively to the active area.
  Some authors prefer referring to the PCE on the total area [151]. This is necessary when considering the effect of design on module performance. PCE × g-FF will be used when the impact of the geometry on the performance is presented in this work.

- The total area is the area of the entire substrate.

- The aperture area is the area that includes the active area and the interspace between single cells.

- The electrodes are the conductive layers on the top and bottom of the devices, named also cathode (carbon in case of C-PSC) and anode or photoanode (FTO in case of C-PSC).

- Electrical contacts are the two metal busbars that connect the first and the last cell in Se-Ms, to properly connect the device.

- Min-J_{sc} is the current density of the cell that limits the current of the module. It is calculated as the measured I_{sc} over the active area of a single cell or, equivalently, as the J_{sc} of the module times n_c.

- Av-V_{oc} is the averaged V_{oc} of the single cells. It is calculated as the measured V_{oc} of the module over n_c.

Min-J_{sc} and Av-V_{oc}, in particular, are important tools to compare the module properties to the expected values of single cells.

1.7 Screen printing

Screen printing is a very well-established technique that is widely used in industrial scale. It is a versatile printing technique and allows a full 2-dimensional patterning of the printed layer. There is essentially no loss of coating solution during printing. The final film can be very thick, in the orders of μm, and the ink requires high viscosity and low volatility.

The process involves a woven mesh screen that has been glued to a frame under tension (Fig 1.15). Common materials include synthetic fibre or steel mesh. The pattern is obtained by filling the screen with an emulsion that is impervious to the coating solution in the areas where no print should appear. This can be

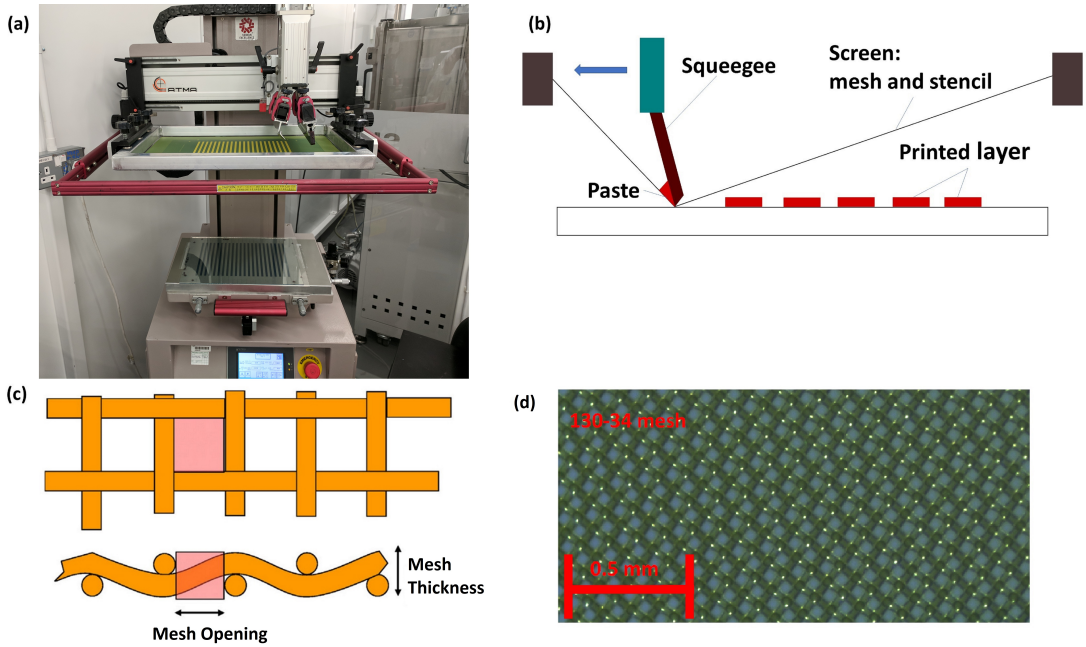


Figure 1.15: (a) Example of automatic screen printer. (b) Schematic of the technique working principle. (c) Schematic of the mesh waving. (d) optic microscope image of mesh 130/34 (Tab 1.2).

achieved with a UV-curable emulsion. The screen is exposed only in the negative photograph of the pattern. The emulsion that is not cured can be washed off from the mesh (printing area).

A squeegee, a piece of flexible material with at least one edge, is forced onto the screen to ensure the screen-substrate contact and is drawn linearly across the screen to force the ink through the printing area onto the substrate. After printing, a small amount of ink is left in the mesh. The ink, therefore, must be spread again on the screen surface. This could either be done with the same squeegee in a manual process or with a so-called flood coater in an automatic process. The flood coater is usually a blade that spreads the ink back without pressing on the screen to restart the process.

1.7.1 Some key parameters

There are several parameters that can affect the printing quality and the most crucial ones will be presented here.

Ink rheology: This is an important parameter in every printing process. In the case of screen printing, the ink must be viscous enough to avoid slumping through the mesh during printing. The rheology requirement can be different depending on the chosen mesh of the screen and the characteristic of the wanted

film. A study of the effect of the ink rheology (and solid content of the ink) on the utilised mesh is given in reference [152].

Solid content in the ink: This is clearly related to the solvent content. The influence of this parameter is important in the dried film. While it is possible to predict with relative accuracy the thickness of the wet film, the thickness of the dried film can change significantly depending on the amount of solvent present in the ink. Solid content can also affect the ink rheology.

The amount of the solvent and the relative evaporation rate can also affect the film quality. Screen printing typically allows the deposition of films in the order of μm thick. With a low solid content, it is possible to achieve much thinner films. However, the consistency of the film quality might be influenced by the evaporation of the solvent, which varies the ink rheology during the process.

Moreover, the size of eventual nano or micro particles can affect the printing. The particles and eventual agglomerations must pass through the mesh without clogging it. As an empirical rule, the particle size should be a tenth of the mesh aperture area.

Mesh characteristic: After the rheology and the solid content of the ink, the mesh characteristic is probably the most important parameter in screen printing. The diameter of the woven threads and the distance between them define the aperture area of the mesh. The aperture area of the mesh and the thread diameter define the volume of ink that can pass through the mesh and, thus, the final thickness. Since some ink remains stuck in the mesh even after printing, also other parameters, such as the squeegee pressure, gap between screen and mesh, and speed, can affect the amount of ink that is transferred on the substrate. However, the thickness is mostly dependent on the aperture area of the mesh.

The nomenclature of the mesh includes information on the thread diameter and the number of threads per cm (mesh count). Once these parameters are known, it is possible to figure out the mesh aperture, the theoretical printed volume and the largest particle that can be printed through the mesh, based on simple geometrical calculations. However, calculated values do not accurately reflect those of the real print, as factors such as residual ink on the screen are not accounted for. The mesh characteristics of some important examples of screens are reported in Tab 1.2.

Table 1.2: Example of mesh used in screen printing and relative properties. The mesh opening is the area that is unoccupied by threads over the unit area; the mesh thickness is twice the mesh diameter; the theoretical ink volume is the product between the mesh opening and the mesh thickness. The declared values are taken from MCI precision Ltd products.

		Mesh count inch	Mesh count cm	Thread diameter μm	Mesh opening %	Mesh thickness μm	Theoretical ink volume cm^3/m^2
MCI	10/260	25	**10**	**260**	54.6	498	272.0
calculated					54.8	520	284.8
MCI	48/70	123	**48**	**70**	41	113	45.1
calculated					44	140	62
MCI	61/64	156	**61**	**64**	30.1	101	30.4
calculated					37	128	48
MCI	90/48	230	**90**	**48**	24.6	78	19.2
calculated					32	96	31
MCI	130/34	330	**130**	**34**	26.9	55	14.3
calculated					31	68	21
MCI	180/27	460	**180**	**27**	15.1	43	6.5
calculated					26	54	14

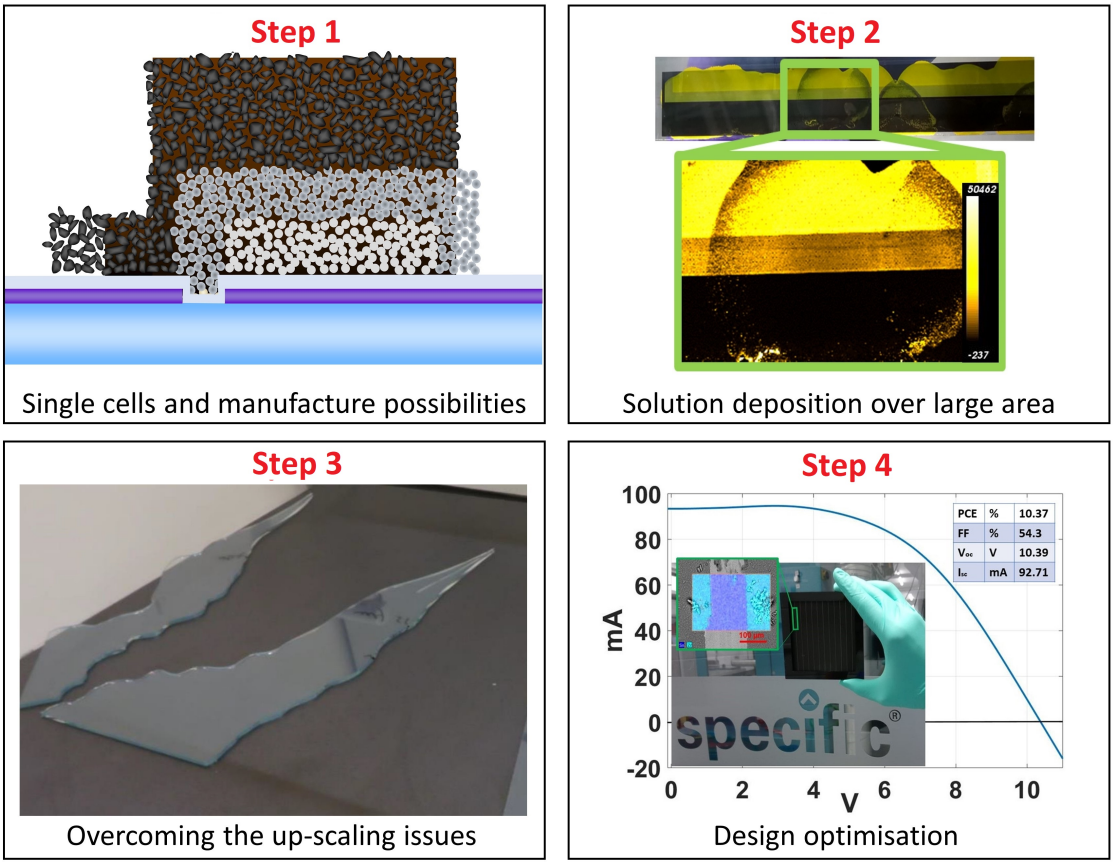
1.8 Remarks

PSC is an emerging technology with promising applications for large scale production, due to the feasibility to fabricate highly performing devices via solution-phase deposition. The C-PSC is the closest architecture to penetrate the exigent market demands, due to the use of low-cost material and a mature industrial process to print the layers, i.e. screen printing. The high stability that AVA-MAPI C-PSC can achieve is also crucial for market penetration. However, the performance of the C-PSC needs to be enhanced with an adequate manufacture procedure and a module design with high g-FF and PCE. The journey of this thesis will follow the below steps:

Step 1, shown in Chapter 3: the C-PSC will be studied as single cells to learn their characteristic, for both MAPI and AVA-MAPI C-PSCs. Furthermore, some peculiar behaviour of the AVA-MAPI C-PSC will be presented.

Step 2, shown in Chapter 4: the MAPI C-PSC will be fabricated to optimise the infiltration of the perovskite in large area stripes. This will be done in the 2-step method to have a visual observation of the infiltration of the PbI_2. A novel approach to deposit low viscosity inks, such as perovskite solutions, on porous materials, such as the triple mesoscopic stack, will be introduced.

Step 3, shown in Chapter 5: the module design will be optimised starting with



some theoretical calculations and experimental data on small modules. This will be based on the registration of the different layers to create the interconnects, as commonly reported for C-PSC. The largest modules that is so far reported in the literature (198 cm^2 active area) will be presented, and some critical issues relative to the up-scaling that were overcome will be discussed.

Step 4, shown in Chapter 6: the module design will be optimised in order to improve the g-FF. The layers will be deposited as large solid areas all over the substrate, whereas the interconnects can be created by scribing to reduce the waste of space. Modules with over 200 cm^2 of active area will be shown.

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Chapter 2

Experimental Methods

2.1 Introduction

There are several variations in the C-PSC architecture that can be found in the literature (Section 1.4). These include the chemical and morphological composition of the mesoporous stack and the formulation of the perovskite. Section 2.2 aims to describe the preparation of the consistent baselines for C-PSCs, for both MAPI and AVA-MAPI devices that will be used in this work. For the triple mesoscopic stack, FTO/bLayer/mTiO_2/mZrO_2/carbon was the layer sequence adopted in this work. Other process improvements that were tested in this work will be discussed in Chapters 3 and 4. The module preparation will be described in Chapters 5 and 6. Characterisation methods will be described in Section 2.3.

2.2 Device preparation

This section will describe the preparation of the triple mesoscopic stack by screen printing. After layer deposition, perovskite needs to be infiltrated. Here, the preparation of MAPI and AVA-MAPI will be described below.

2.2.1 Triple mesoscopic stack

Materials

- Conductive fluorine-doped tin oxide glass (FTO, XOP, TEC-7)
- Ti diisopropoxide bis(acetylacetonate) (TAA, Sigma-Aldrich, 75 % in IPA)
- Anhydrous 2-propanol (IPA, Sigma-Aldrich, 99.5 %)
- TiO_2 paste (Dyesol, 30NR-D)

- Terpineol (Sigma-Aldrich, 95 %)
- ZrO_2 paste (Solaronix, ZT/SP)
- Carbon paste (Gwent electronic materials)

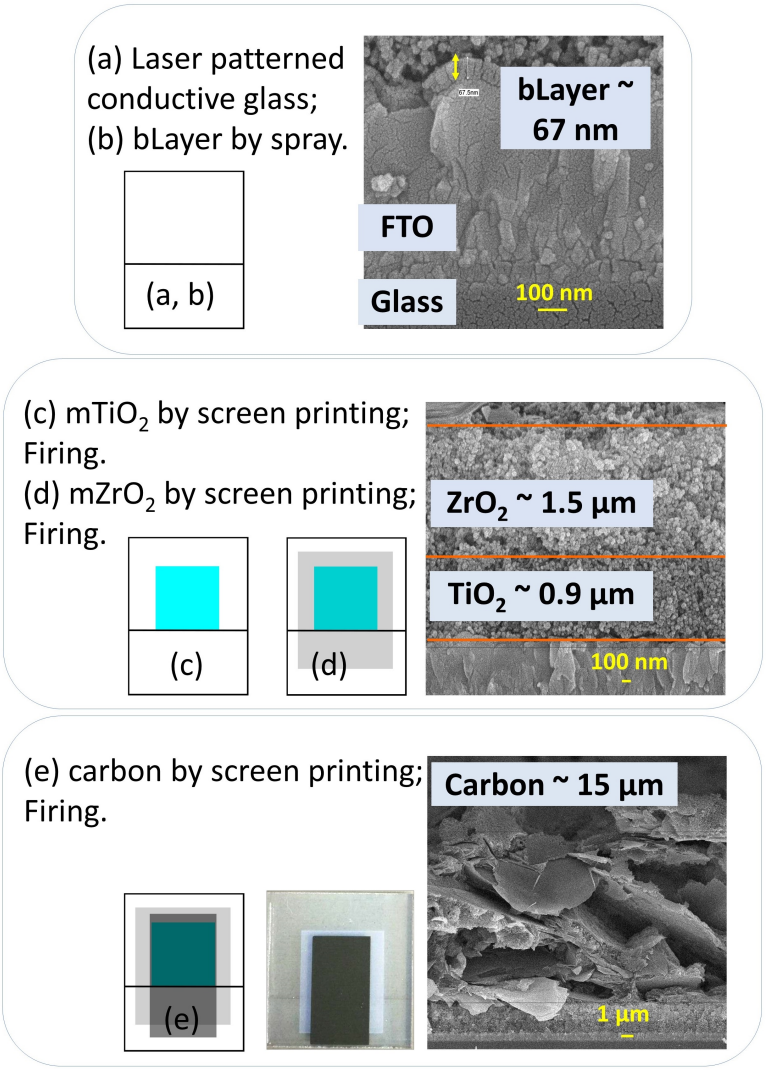

Figure 2.1: Preparation of the inorganic triple mesoscopic stack. (a, b) FTO substrate patterned by laser and subsequent deposition of the bLayer by spray. On the side, SEM image of the bLayer that conformably covers the FTO. (c, d) Deposition of $mTiO_2$ and $mZrO_2$. On the side, SEM image of the two mesoporous layers. (e) Deposition of carbon with photographic image of a fully printed substrate. On the side, SEM image of the carbon layer. SEM images kindly taken by Dr. Dena Pourjafari from CINVESTAV-Mérida.

Method

The inorganic triple mesoscopic stack was prepared on an FTO conductive glass substrate, which was initially patterned to separate the cathode from the anode.

The FTO was patterned with a Nd:YVO_4 laser, Rofin, diode end-pumped, 532 nm wavelength, at 50 kHz frequency, average output power 30 W at 200 mm/s, pulse width 10.0 μs. The patterned substrate was then cleaned with a solution of Hellmanex^{TM} III in deionised water, rinsed with acetone and IPA, and finally plasma cleaned in an O_2 atmosphere for 5 min. A compact TiO_2 layer was deposited by spray pyrolysis with a solution of 10 % TAA in IPA, 25 passes with 10 s between sprays at 300 °C. The spray coating was performed with an airbrush, 0.3 mm nozzle (Fig 2.1a and b).

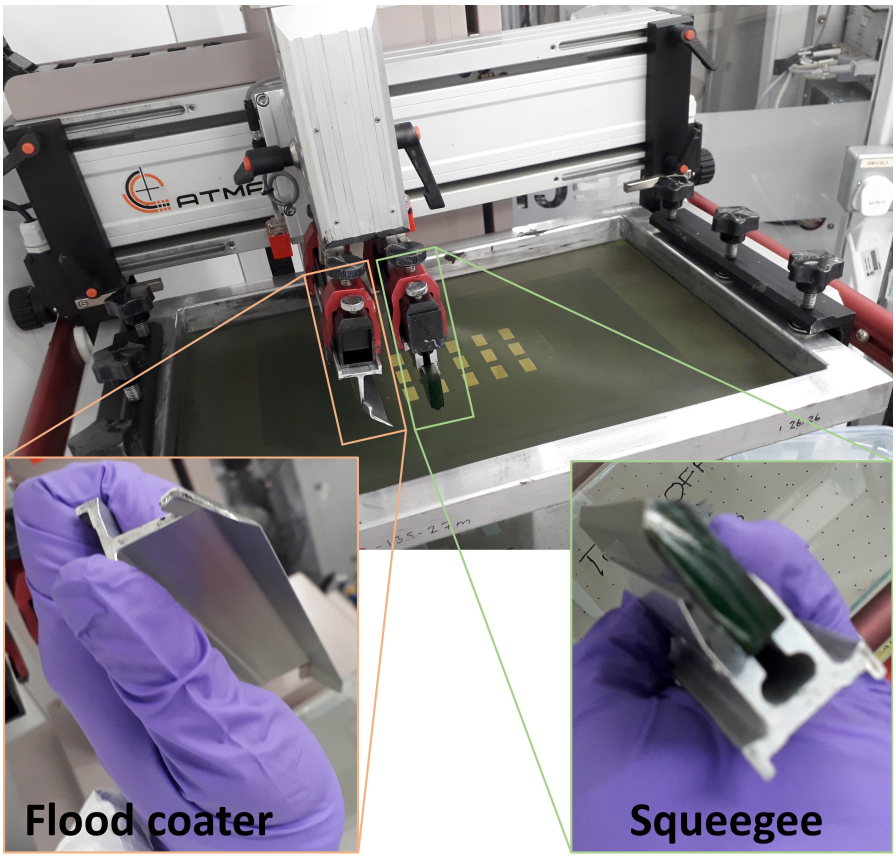

Figure 2.2: AMTA screen printer with flood coater and diamond shaped squeegee.

Mesoporous layers of TiO_2, ZrO_2 and carbon were screen printed and annealed one by one (Fig 2.1c, d, and e). The firing temperature was 550 °C for TiO_2 and 400 °C for both ZrO_2 and carbon. The paste for the TiO_2 layer was diluted in terpineol in a 1:1 ratio by weight, whereas the other pastes were used as provided. The screen printing was performed with a 45 ° diamond-shaped dark green squeegee. An ATMA electric flat screen printer AT-25PA was utilised with a diamond shaped squeegee (45 °, Fig 2.2). The mesh orientation is 45 °. The other printing parameters are summarised in Tab 2.1.

Table 2.1: Printing parameters for the three porous layers.

Layer	SCREEN		Printing mode
	Mesh characteristics	Emulsion thickness	
$mTiO_2$	130-34	9 μm	flood and then coating
$mZrO_2$	130-34	9 μm	double print
Carbon	48-70	25 μm	coating and then flood

2.2.2 MAPI Devices

For MAPI C-PSCs, the 2-step deposition was adopted with some modifications from reference [1]. In the 2-step method, PbI_2 is infiltrated first and then the substrate is dipped in a solution of MAI to convert the PbI_2 phase into perovskite.

Materials

- PbI_2 (Sigma-Aldrich, 99 %)
- Methylammonium iodide (MAI, Dyesol)
- Anhydrous N,N-dimethylformamide (DMF, Sigma-Aldrich, 99.8 %)
- Anhydrous 2-propanol (IPA, Sigma-Aldrich, 99.5 %)

Method

The preparation of MAPI C-PSC devices was based on the 2-step method. Two drops of solution 1 M (460 mg/mL) PbI_2 solution in DMF (kept at 70 °C to avoid crystallisation), were deposited on the triple mesoscopic stack (Fig 2.3a). One drop was deposited on the carbon contact area (4 μL) and another on the active area (9.6 μL) with a 1-10 μL pipette.

After the drop deposition, PbI_2 was dried at 70 °C in an oven for 30 minutes. Subsequently, the cells were dipped in a 10 mg/mL MAI solution in IPA. When the perovskite conversion was fully completed (after around 30 minutes), the cells were rinsed in IPA (Fig 2.3b).

2.2.3 AVA-MAPI Devices

For AVA-MAPI C-PSC, the use of three components, i.e. AVAI, MAI, and PbI_2, make the use of the 2-step deposition more difficult in regards to the control of the ratio between AVAI and MAI in the perovskite crystal structure. Therefore,

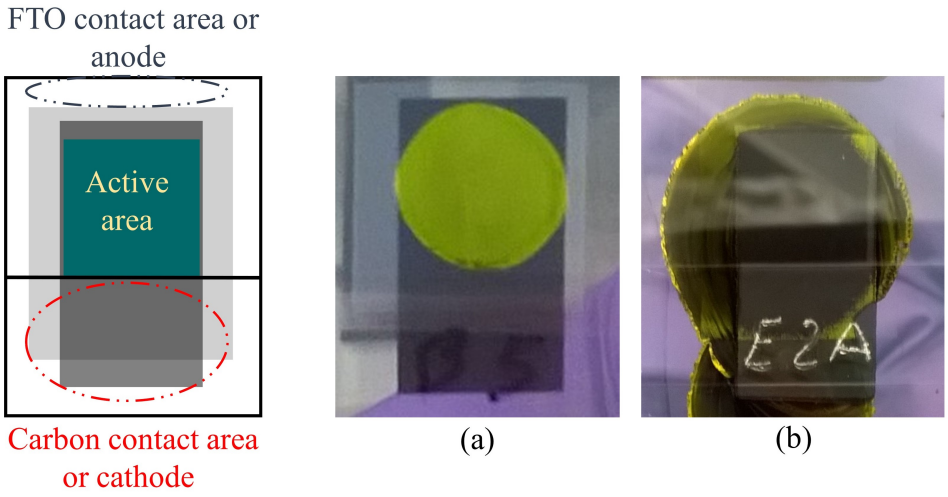

Figure 2.3: Description of the a MAPI C-PSC device. (a) Deposition of PbI_2 solution on the active area. (b) a fully prepared device after conversion of PbI_2 into MAPI.

a single step deposition was adopted, starting from the process described from reference [2].

Materials

- PbI_2 (TCI, 99.99 %)
- CH_3NH_3I (Dyesol)
- γ-butyrolactone (GBL, Sigma-Aldrich, 99.8 %)
- 5-aminovaleric acid iodide (AVAI, Dyesol)

Method

The AVA-MAPI precursors solution was prepared with 439.0 mg, 151.4 mg, and 6.7 mg of respectively PbI_2, CH_3NH_3I, and AVAI in 1 mL of GBL. A drop of solution (15 μL) was deposited on the top of the active area of the triple mesoscopic stack at room temperature (Fig 2.4).

After the drop deposition, the wet devices were kept in a closed Petri dish for 10 min at room temperature and then heated at 50 °C in an oven to reduce the evaporation rate and allow an improved perovskite crystallisation (Section 3.3.5). After 60 minutes, the Petri dish was opened, and the devices were left in the oven for another hour to complete the drying step. For the use of the Petri dish, see Section 3.3.3. The devices were then placed in a humidity oven at 70 % RH and 25 °C for 24 hours. The presence of moisture was observed to improve the device

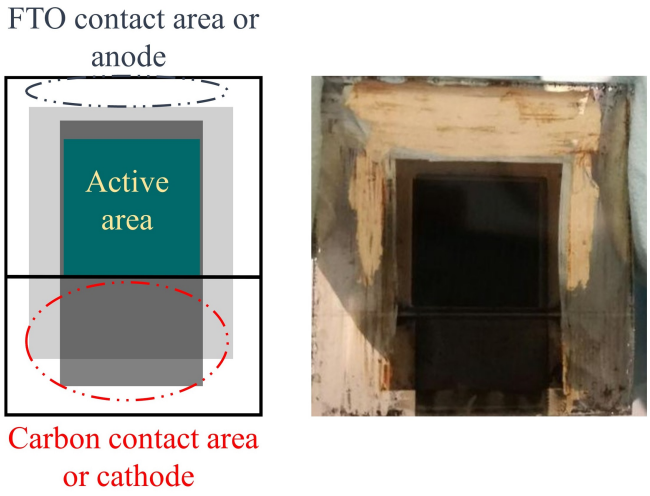

Figure 2.4: Description of the AVA-MAPI C-PSC device. Next to it a fully prepared device.

performance in a post-annealing process because it might increase the ion mobility in the perovskite and, thus, allow a better reorganisation of the crystals [3; 4].

2.3 Characterization methods

2.3.1 Electrical characterisation

Current-Voltage measurement. The JV measurement was carried out using a Keithley 2400 source meter. For measurements in 1 sun, a Newport Oriel solar simulator (class AAA) was used. The calibration was with a KG5 filtered silicon reference cell. The scanning rate was:
- for MAPI C-PSC (Section 2.2.2) 34 mV/s between -0.2 V and 1.1 V in dark and under illumination, forward and reverse directions. The active area was defined through an aperture mask with an area of 3 × 3 mm, in line with previous reports [5; 6]. This will be adopted in Chapter 4.
- for AVA-MAPI C-PSC (Section 2.2.3) 200 mV/s between -0.2 V and 1.1 V in dark and under illumination, in forward and reverse directions after 3 min light soaking. The need of light soaking was reported since the first publication [2] and it is due to the slow response of this perovskite formulation [7]. The active area was defined through an aperture mask with an area of 7 × 7 mm.
- for modules 200 mV/s between -0.2 V and 1 × n_c V, i.e. 5 V for 5 cells or 6 V for 6 cells, in forward and reverse directions. The higher voltage was necessary to measure the V_{oc} of series connected modules. The active area was defined by the width and length of the single cells times the n_c (number of cells).

For large modules from 10 × 10 cm^2 active area and above (Chapter 5 and 6) a large area solar simulator was used, i.e. a sulphur plasma lamp (Plasma International GmbH) calibrated at 1 sun against a KG5 filtered silicon reference cell (Newport Oriel 91150-KG5). The modules were scanned in reverse and forward directions between -0.2 V and n_c × 1 V at 330 mV/s, after 3 min of light soaking.

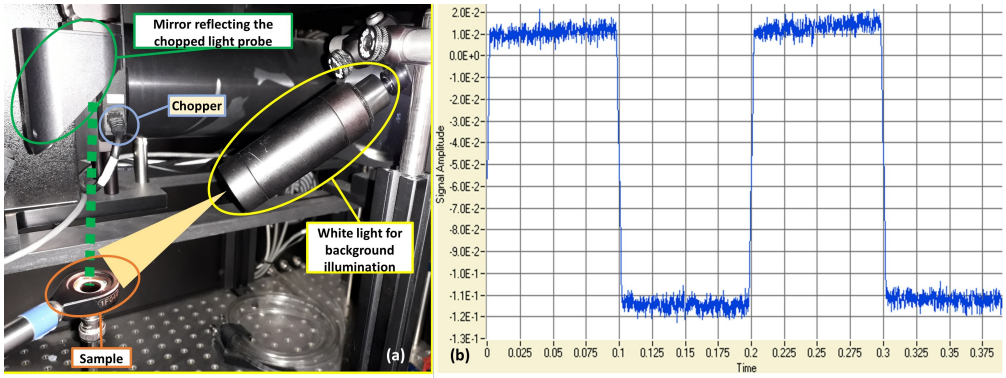

Figure 2.5: EQE measurement in AC mode. (a) The internal measurement set-up. The probing light is modulated at different wavelengths and chopped at a given frequency. The sample underneath the chopped probing light is electrically connected with a transimpedance amplifier. The voltage output of the amplifier feeds a lock-in amplifier to sample the signal at the same frequency as the chopper reference signal. The white background light illuminates the sample when required. (b) Typical measured signal at a given wavelength in AC mode.

In terms of statistics, each parameter was studied with a minimum number of 3 and a maximum of 5 substrates, where a substrate represents a single 1 cm^2 pixel. The exact number of substrates is reported in the caption of the figure that shows the results of each experiment.

External quantum efficiency. The EQE was carried out using a QE X10 system (PV Measurements) in the wavelength range between 300 and 850 nm. The light beam was always smaller than the active area. Measurements in direct current (DC) mode (Chapters 3 and 4) or in alternating current (AC) (Chapters 3) were either performed MAPI and AVA-MAPI C-PSCs.

In DC mode, a probing light illuminates the active area in a dark box. The wavelength of the light is changed by a monochromator, and the generated current of the device is measured in short circuit condition. In AC, the same probing light is chopped at a given frequency. The sample is either kept in dark or under a white light to give a background illumination (Fig 2.5a). The difference between the background current and the peak current defines the signal at the given wavelength (Fig 2.5b).

Electrochemical impedance spectroscopy. The EIS shown in (Chapter 4) was carried out using a Gamry potentiostat (Model: Reference 600). The measurements were performed on unmasked devices from 1 MHz to 0.1 Hz under illumination from LED at 530 nm at 1 equivalent sun or in the dark. Light intensity was modulated using neutral density filters.

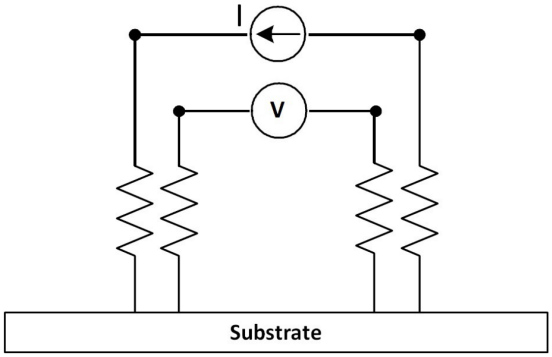

Figure 2.6: Schematics of the 4-probe measurement. The R_{sq} is proportional to the drop in voltage that is measured by the inner pins over the current applied by the external pins.

Four-probe measurement. For the measurement of R_{sq} (sheet resistance) and R_c (contact resistance), a home-made probe and a Keithley 2400 source meter were used.

For the R_{sq}, a probe with four equidistant pins in line was placed in electrical contact with a film on an insulating substrate. Due to the soft nature of the porous layers, large pins with round ends were utilised in order to avoid contact with the insulating substrate. The current passes through the external pins, whereas the two internal pins measure the drop in voltage (Fig 2.6). The dimension of the film is much larger than the dimension of the probe. The so-measured resistance was then multiplied by $\frac{ln(2)}{\pi}$ [8].

For the R_c, the transmission line measurement (TLM) was used. The samples were prepared as per the design in Fig 2.7. The current passed through the extremes of the substrate, while two probes were measuring the drop in voltage between two lines at a fixed distance. The plot of the resistance over the distance gives a straight, whose intercept with the y-axis is twice the R_c. The intercept with the x-axis is twice the transfer length (L_t) [9]. For the experiment in Chapter 6, lines of conductive material at nominal distance of 5, 10, 20, 30, and 40 mm were deposited onto FTO. Carbon was deposited by screen printing whereas silver paint was brushed through a plastic mask with a defined pattern. The carbon contacts were also tested at different P2 sizes.

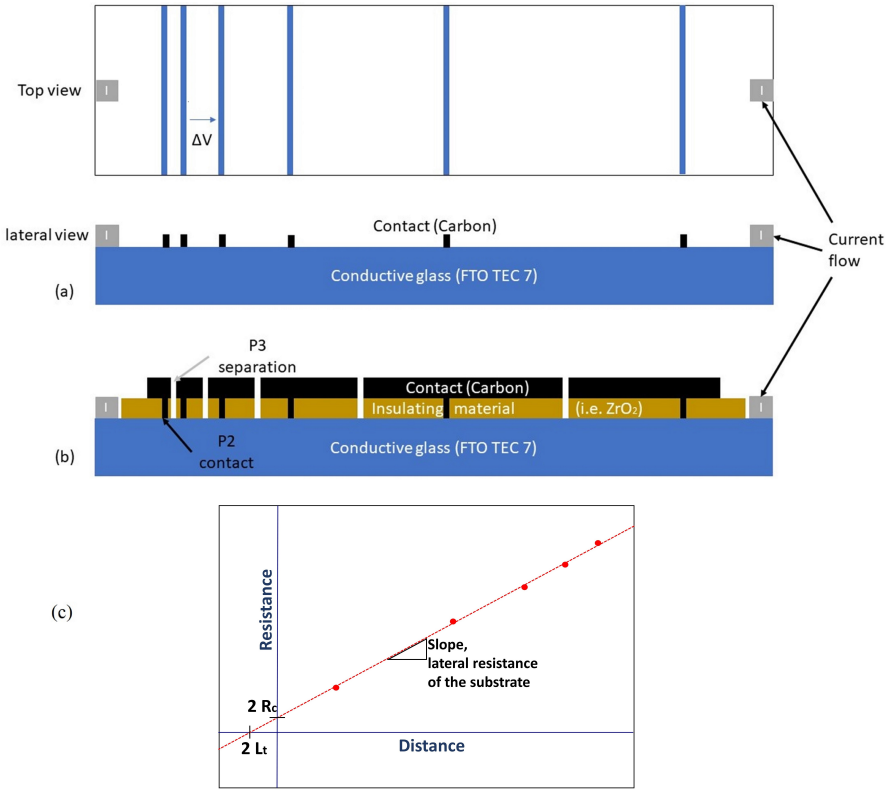

Figure 2.7: TLM configuration with the 4-probe measurement for the R_c measurement. A constant current 'I' is applied from the two sides of the substrate and the drop in voltage is measured between two lines. Line distances are 5, 10, 20, 30, and 40 mm. (a) The standard measurement layout. (b) The configuration that simulates the carbon modules in Chapter 6, with P2 contacts and P3 scribes to disconnect the carbon layer. (c) Expected plot from a TLM and extrapolation of R_c and L_t.

2.3.2 Morphological studies

Scanning electron microscopy. The SEM and the energy dispersive X-ray spectroscopy (EDX) were performed using the below instruments:

The high resolution top view and cross section images in Chapters 5 and 6 were performed using a JEOL-JSM-7800F field emission SEM (5 kV acceleration voltage, a working distance of 10 mm, and a magnification of x25000). EDX mapping was used to determine the element distribution using 20 kV acceleration voltage. The low resolution top view images on the scribe areas in Chapter 6 were performed with a Hitachi tabletop microscope TM3030 with EDX Quantax70.

Profilometer. A Veeco Dektak 150 was used to measure the profile (thickness and roughness) of surfaces with a probe of radius 12.5 μm (Chapter 3). The thickness of the layers is defined as the vertical distance between two points, the

substrate and the layer itself. The roughness can be defined as R_q (the root mean square), R_p (the maximum peak height), and R_t (the maximum height of the profile).

2.3.3 Spectroscopic studies

UV-Vis spectrophotometry. A Pelkin Elmer UV/Vis/NIR spectrometer Lambda 750 was used for the measurement of the optical properties of the samples (Chapter 3). Samples could be measured in transmission with a 100 mm InGaAs integrating sphere detector.

Raman. Raman measurements were performed with a Renishaw Invia Raman system in backscattering configuration (Chapters 3, 4, 5, and 6). A laser excitation of 532 nm and a 50 × long objective were used. Raman maps were obtained by measuring several points of the sample with an X-Y scanning stage. The signal intensity was determined using the maximal intensity of spectra in the Raman shift in the range of the observed peak over the baseline. The measurements were carried out through the glass side.

2.3.4 Other studies

X-ray diffraction. XRD measurements were carried out using a Bruker diffractometer with Bragg–Brentano geometry. Cu k_α radiation was applied as X-ray source (Chapters 3 and 4). Scans in 2 Θ were collected using a step size of 0.01 °. XRD samplings were obtained by measuring the peak heights of diffractograms collected every mm by using an X–Y scanning stage, from 12.2 ° and 14.5 °, step size of 0.04 °, and a collimator of 1 mm.

Dynamic Contact angle. Contact angle measurements were obtained using an IR Nikon camera and analysed using FTA-32 software (Chapter 4).

Viscosity test. The results shown in Chapter 4 were obtained with a Bohlin rheometer and a distance between plates of 70 μm.

Stability studies The stability tests shown in Chapters 3 and 4 were performed under continuous irradiation from white light-emitting diodes (LEDs) (1 or 0.5 equivalent sun) in ambient condition (18–22 °C, around 50 % relative humidity). Complete JV curves in reverse and forward scan were recorded at every fixed time.

The stability tests shown in Chapter 5 refer to modules that were stored in the dark, at different values of relative humidity [4]. While testing the shelf life of C-PSC modules, a more sophisticated system became available: a class AAA solar simulator with Sulfur plasma lamp (Solaronix, Solixon A-20), calibrated at 1 sun, was used for all JV measurements from 550 h after fabrication. The continuous illumination occurred in ambient condition with no control over humidity and temperature and no UV filter. Complete JV curves in reverse and forward scan were recorded at every fixed time [4].

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Chapter 3

Single cell devices

3.1 Introduction

The overarching theme of this thesis is the design and development of large area perovskite modules. In order to achieve successful up-scaling, single cells need to be characterised and optimised because the performance of the large area module depends on both the design and the performance of small scale devices. It is important to know the expected behaviour of the single cells to have a better idea of the effect of the design on the device architecture.

This chapter will deal with developments in the fabrication of lab scale 1 cm^2 C-PSC as a tool for understanding the challenges of the up-scaling. This chapter is divided into multiple subsections dedicated to different aspects of the C-PSC. These are outlined as follow:

- physical characterisation of the printed layers;
- development of a consistent baseline process for reproducible device fabrication;
- addition of AVAI to improve stability;
- characterisation of the optoelectronic properties of the devices;
- processing conditions;
- comparison of deposition methods for the bLayer;
- role of the mZrO_2 layer in the architecture.

3.2 Experimental

The most utilised methods to prepare devices and the characterisation methods were described in Chapter 2. Below are listed the experimental methods for some specific experiments that will be described in this chapter.

Metal electrodes

The metallic tape, or Al tape, that will be discussed in Section 3.3.2 to study the effect of the conductivity of the carbon layer for MAPI C-PSC, was fabricated as described below:

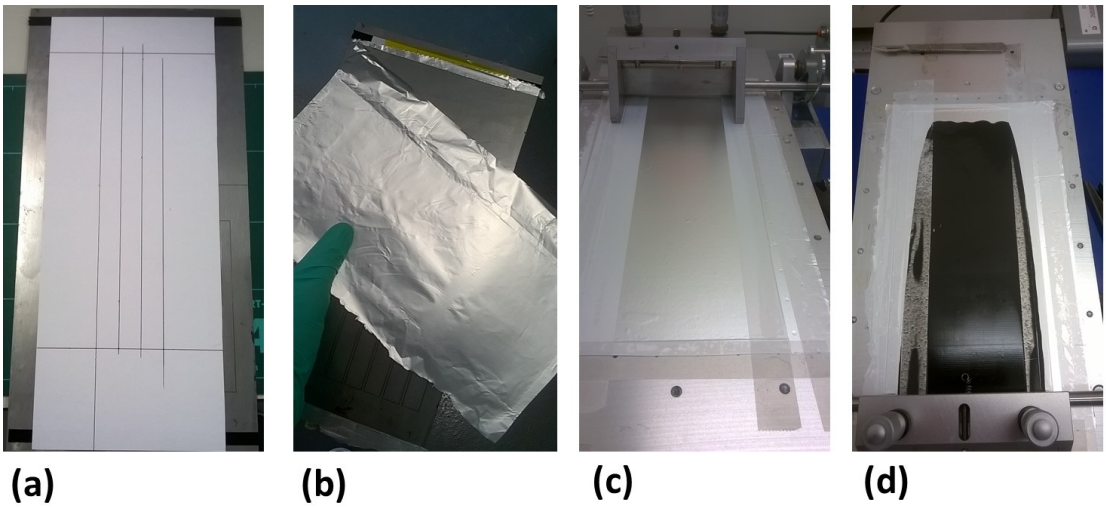


Figure 3.1: Preparation of the Al tape. (a) Take a sheet of paper and apply a double-side tape on the top and bottom parts. (b) Stick the Al-foil on the sheet to have a flexible Al foil that is back-supported by the paper. This gives better mechanical strength to the Al foil. (c) Place the Al foil supported by the paper on a vacuum bed of the doctor blade. The paper sheet allows the suction of the Al foil on the bed to achieve perfect smoothness. (d) Application of doctor blade deposition. The Al foil can be cut at the desired size allowing separation from the paper.

- Ink preparation: 3.50 g of poly(vinyl acetate), average molecular weight 100,000 (PVA, Sigma-Aldrich), were completely dissolved in 17.5 mL of ethyl acetate (99.8 %, Sigma-Aldrich). After complete dissolution, a mixture of conductive carbon black (Super P, Imerys) and graphite (1-2 μm, Sigma Aldrich) in powder were mixed together with a composition of 1.5:4.5 wt. The powder was slowly added in the PVA solution while stirring. Further 10 mL of ethyl acetate were added to improve the rheology. The mixture was kept stirring for several hours until complete homogeneity.

- Ink deposition on Al-foil: the deposition occurred by doctor blading. Due to the difficulty of handling the thin Al foil without bending it, a paper sheet was stuck on the back of the Al foil on the top and on the bottom with with a double sided tape to give higher robustness to the substrate and, in the meantime, allow the suction of the Al on a vacuum bed during doctor blading (Fig 3.1a, b and c). The paper was stuck on only on the top and bottom because the Al could be separated from the paper by simple cut after the deposition of the ink. Doctor blading occurred with a gap of around 30 μm, measured with a single layer of TESA tape (Fig 3.1d). The solvent was then let evaporate from the conductive carbon glue layer at 50 °C for a few minutes.

- Application on C-PSC: the Al-tape was placed in the designed position, with the carbon side in contact with the device. After being accurately registered with the C-PSC, the tape was stuck down by using a T-shirt press at 85 °C for 40 s.

Special methods to deposit compact TiO_2

The spray deposition that is adopted to deposit bLayer in this work was compared with alternative methods, i.e. ALD (atomic layer deposition) and screen printing (Section 3.3.6). These alternative methods are described below:

- The deposition of compact TiO_2 layer for the bLayer by Atomic Layer Deposition (ALD) was done with a Savannah S200 (Ultratech/Cambridge, Nanotech). The Ti precursor was tetrakis(dimethylamido)titanium (TDMAT), heated to 75 °C. The O precursor was H_2O, kept at room temperature. The substrate, after cleaning, was treated with O_3. The O_3 was produced using an ozone generator from high purity O_2, which was delivered at 5 psig and 0.5 L/min. High purity N_2 was used as carrier and purging gas with a flow rate of 90 sccm. The reactor temperature was kept at 150 °C. For one cycle TDMAT pulse time/purge time is 0.1 and 5 s; for one cycle H_2O time/purge time is 0.015 and 5 s. The thickness of the final layer is 12 nm for 277 deposition cycles.

- The deposition of compact TiO_2 layer for the bLayer by screen printing occurred with the commercial paste Ti-Nanoxide BL/SP (Solaronix). A screen of 130-34 was used with subsequent drying steps at 125 °C, 250 °C and 375 °C (10 minutes for each step) and final firing at 550 °C for 30 minutes.

3.3 Results and discussion

3.3.1 Characterisation of the triple mesoscopic stack

The triple mesoscopic stack plays a key role in the device performance of C-PSC. Its reproducibility is crucial for the establishment of a baseline as well as the ability to characterise each layer for a proper assessment. Based on the method described in Section 2.2.1, layers of $mTiO_2$, $mZrO_2$ and carbon were screen printed and characterised by profilometer, UV-Vis, Raman and XRD.

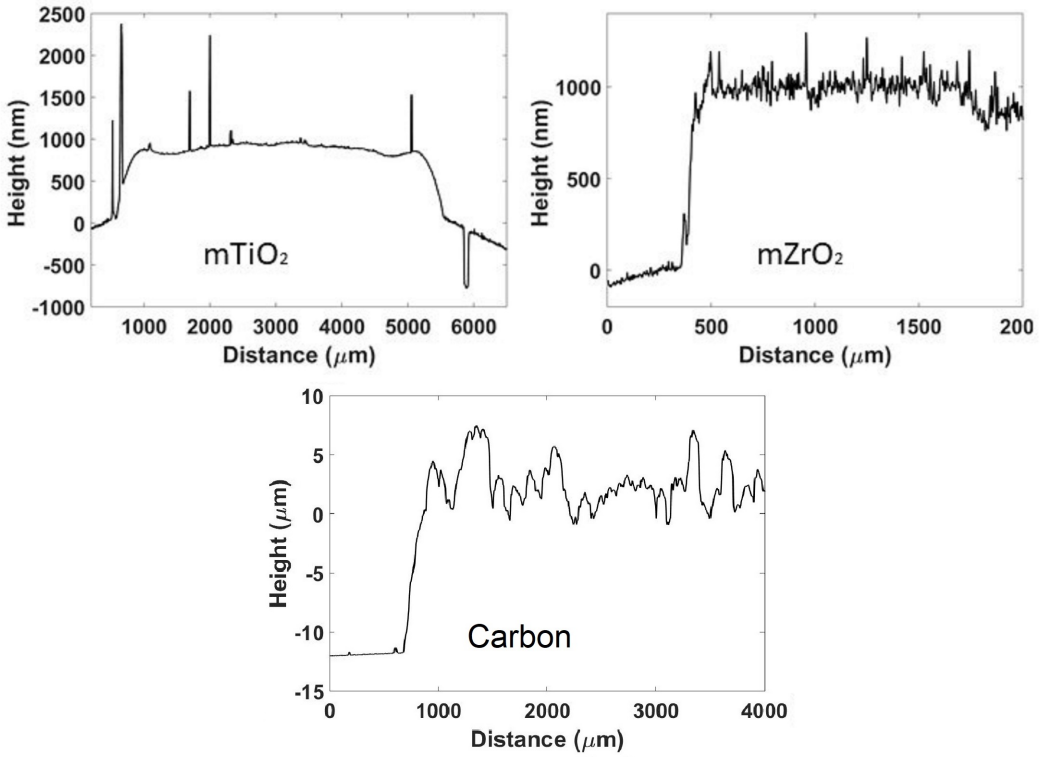


Figure 3.2: Profilometer data of layers of $mTiO_2$, $mZrO_2$ and carbon on glass/FTO substrate. For the $mTiO_2$ layer, it is possible to observe the laser scribe on the FTO layer. For the carbon layer, the scale is in μm.

The thickness of the layers is crucial for the C-PSC performance. Thick layers of TiO_2 and ZrO_2 allow proper light absorption by the perovskite but increase the path at which the charge needs to be transferred to be injected into the carbon. The thickness of the carbon controls the lateral conductivity of the top electrode and affects the infiltration of the perovskite solution into the stack. A proper assessment of the layer thickness is necessary for the establishment of the baseline. Working devices could be achieved with the reported values of layer thickness, i.e. less than 1 μm for $mTiO_2$, more than 1 μm for $mZrO_2$ and more than 10 μm for carbon [1; 2]. The layers were screen printed on FTO conductive glass to

check the thickness after printing (Section 2.2.1). Profilometer data revealed the successful achievement in terms of thickness of the layers and measured the relative roughness after the heat treatment (Fig 3.2, Tab 3.1). The profile on a 5 mm wide $mTiO_2$ layer (Fig 3.2) shows the bending of the glass after the heat treatment. Such bending makes the definition of base-line more complex, because the glass substrate does not follow a flat line. The thickness measurement was taken at two points close to each other, i.e. at the edge of the layer, to make the bending effect negligible. However, a typical edge effect for $mTiO_2$ is observable in Fig 3.2, which is around 10 % higher than the middle point. This hill, that is observable for $mTiO_2$, is probably caused during the settling of the low viscosity ink before drying. The thickness values reported here refer to the edge. The roughness measurement was taken on the top of the layer. The laser scribe next to the $mTiO_2$ layer, which is applied to separate the cathode from the anode on the monolithic configuration, shows the accuracy limit of the registration method. The registration is based on the eye observation of the screen on the substrate and the limitation is around 500 μm.

	Thickness μm	R_q nm	R_p nm	R_t nm	**Averaged Thickness**
$mTiO_2$	0.960	25	74	132	
	0.880	19	35	94	
	1.018	25	46	113	
	0.993	13	33	72	
	0.936	25	52	106	
	0.891	9	23	51	**0.946**
$mZrO_2$	2.078	68	208	326	
	1.791	96	248	429	
	1.812	153	621	869	
	1.689	75	227	392	
	1.783	158	568	805	
	1.780	144	371	570	**1.822**
Carbon	16.02	1,076	2,186	5,089	
	16.52	1,419	4,119	6,896	
	15.11	1,977	6,716	10,443	
	14.55	1,325	2,874	5.619	
	15.21	1,983	5,009	8.585	
	15.77	1,741	3,947	7.667	**15.53**

Table 3.1: Profilometer data of layers prepared with the method described in Section 2.2.1) on FTO. Six different samples were measured in terms of thickness and roughness, i.e. R_q, R_p and R_t (Section 2.3.2)

.

The roughness of $mZrO_2$ is much higher than that of $mTiO_2$, and carbon's is

even higher. This is due to the higher viscosity of the pastes, which makes it more difficult to smooth the layer before drying. Carbon, moreover, is a mixture of large graphite flakes and carbon black, and this increases the roughness of the layer.

In terms of conductivity, the carbon layer was measured with the 4-probe measurement to obtain the R_{sq} (sheet resistance). For around 15 μm, $R_{sq} = 14.5\ \Omega_{sq}$.

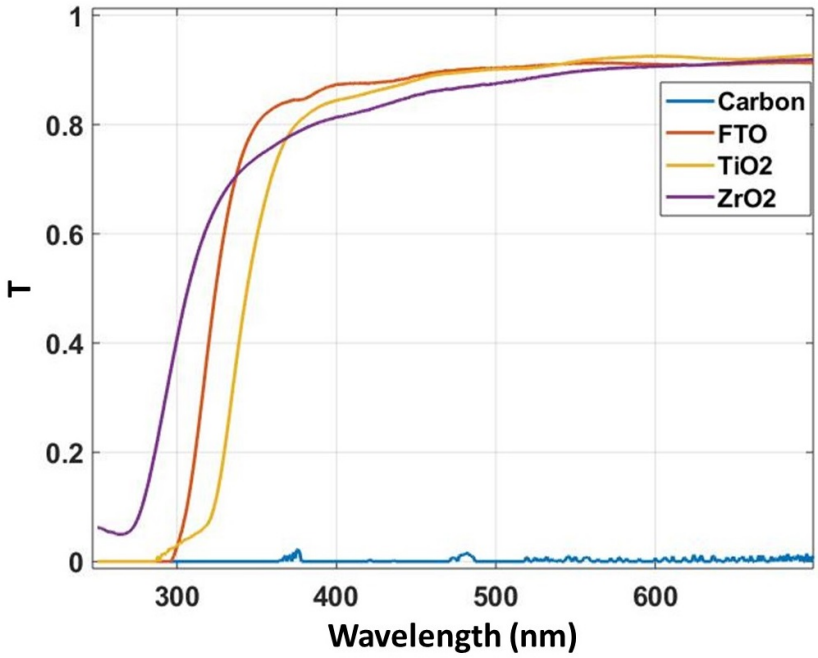


Figure 3.3: UV-Vis data in trasmission of layers of FTO, $mTiO_2$, $mZrO_2$ and carbon.

The optical properties of the layers affect the absorption of the light by the perovskite. A proper assessment of the layers requires a proper characterisation of the absorption in the UV-Vis region (Fig 3.3). Carbon, as a black material, does not transmit light. Layers of FTO, $mZrO_2$ and $mTiO_2$ are transparent until around 300-350 nm. $mZrO_2$ is opaquer than FTO and $mTiO_2$, showing a larger absorption due to the higher thickness of the layer, but a fall in transmittance is observed at lower wavelength due to the higher E_g of the insulating layer.

When analysing a device by XRD, the peak identification is crucial. Databases can be of great support for the peak identification and indexing but thin film can present variations from the bulk materials. This is because thin films present texturing effects where some crystallographic directions are privileged in the lateral direction, and some peaks can be damped or even disappear. Moreover, thin films might cover the signal of the underneath layers when they are very thick, so it is important to know which peaks can be expected to be visualised for the further investigations that will be done in this work. The XRD characterisation aimed to observe the expected peaks of layers in pile as they are fabricated in the device

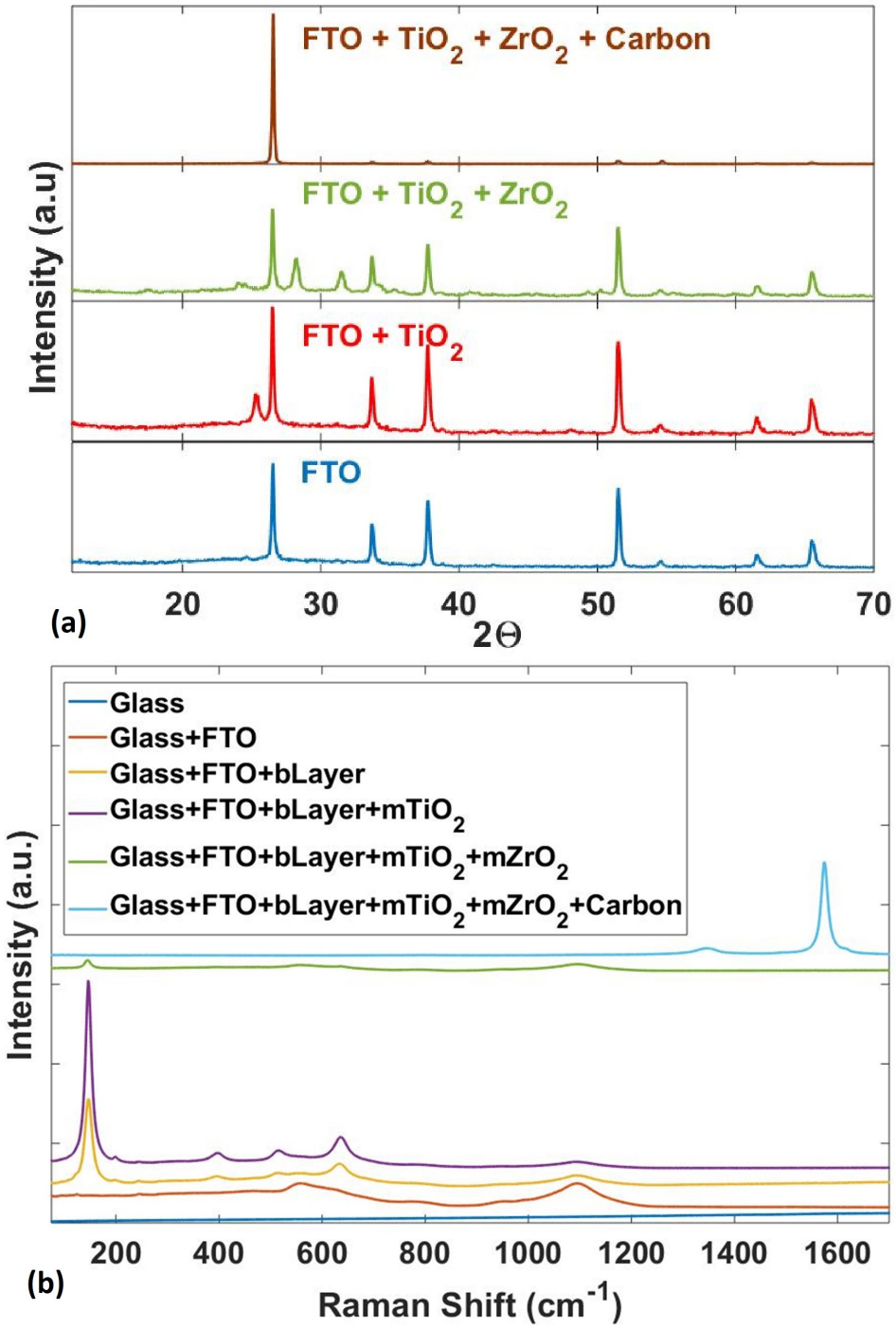


Figure 3.4: (a) XRD and (b) Raman data of layers of FTO, $mTiO_2$, $mZrO_2$ and carbon deposited in sequence on the same substrate.

architecture (Fig 3.4a). The peaks of FTO can be observed also when around 1 μm mTiO_2 is deposited. When a further 1 μm mZrO_2 is added on the top, the peaks of FTO and also mTiO_2 are damped. The peak at 28 ° is the overlap of the diffraction of the FTO and ZrO_2 phases. Carbon is more than 10 μm thick and nearly completely shadow the other phases underneath. The strong peak is due to the graphite phase.

As for the XRD, the identification of the Raman signals is crucial. Raman can be used to characterise the layers either from the top of the substrate or through the glass. Here the characterisation is done from the top of the substrate because the aim was to observe the Raman response of each layer while they are deposited in succession (Fig 3.4b). Both bLayer and mTiO_2 can be easily observed and the very thin bLayer presents a comparable signal to that of the mTiO_2. The mZrO_2 layer seems not to present any Raman signal. Carbon presents two peaks between 1350 and 1650 cm^{-1}, named D and G bands [3; 4; 5], that can be utilised to determine the presence of sp^3-reach or sp^2-reach carbon compound. The carbon ink used in this work, which is made also with graphite, presents a very intense G band. Since the very thick carbon layer hides all signals from the underneath layers, the observation of perovskite close to the photoanode will be done through the glass (Chapter 4 and 5), whereas the characterisation can be done from the top of the substrate when the fixtures observable from this side are investigated (Chapter 6).

3.3.2 MAPI perovskite baseline

The development of the C-PSC technology requires a baseline in order to prepare the devices consistently. These devices should present a relatively high performance to be able to better rely on the results. A baseline of MAPI C-PSC was prepared. The first procedure followed the method reported in Section 2.2.2 but with a single drop of PbI_2 on the active area. The first non-optimised devices shown a PCE of around 6 % with an obviously low FF due to the low conductivity of the carbon layer. A possible improvement to enhance the performance of the C-PSC is to apply metallic contacts on the top electrode. In this way it is possible to reduce the R_s of the device.

A possible approach to deposit metal on the device is by evaporation. However, one of the advantages of the C-PSC architecture is the low cost of the materials and the deposition processes. This principle is not compatible with the use of expensive evaporated Ag or Au. Starting from the idea of laminated electrodes [6; 7], the literature was examined in search of laminated electrodes potentially compat-

ible with carbon architecture. The article in reference [8] presents an example of free-standing carbon electrode for flexible carbon-based devices. A formulation of carbon black, graphite flakes and PVA glue was reported to be mixed in the low-boiling point ethyl-acetate solvent. A Teflon substrate was used in reference [8] to obtain a free-standing carbon layer, whereas Al foil was preferred here. This is because the idea was to use the carbon formulation as a conductive glue for the lamination of the foil.

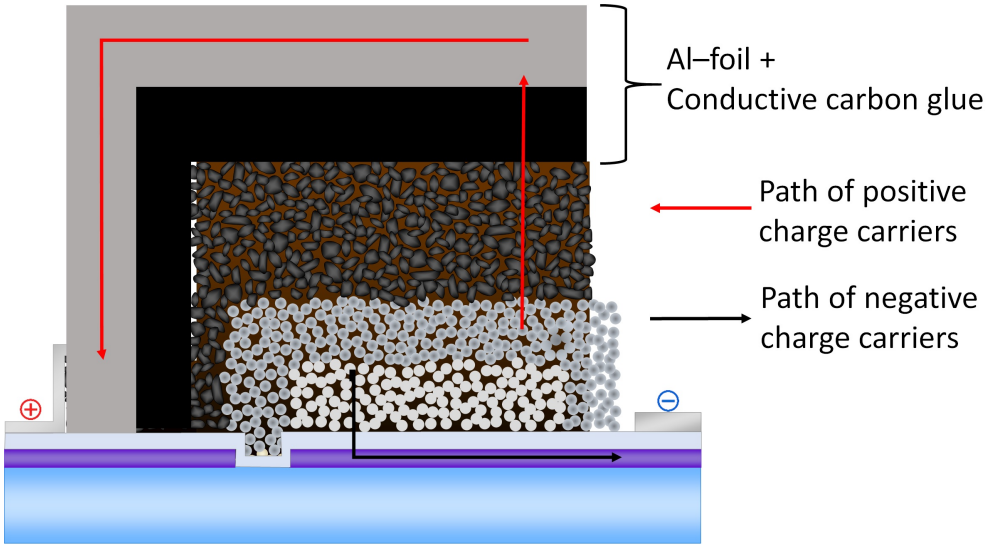
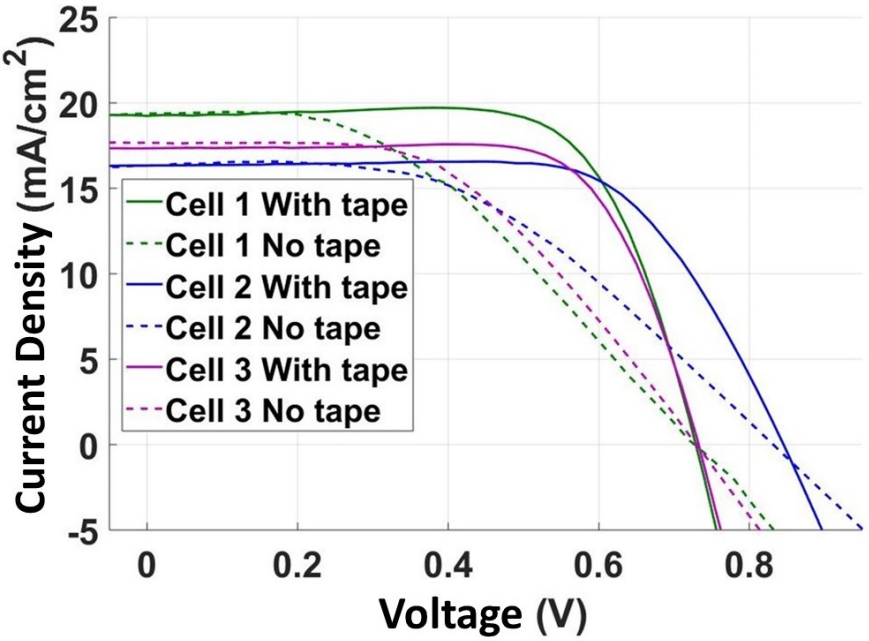


Figure 3.5: Schematic representation of a C-PSC with Al-tape on the top.

The Al-foil, widely utilised in the food industry, has the advantage to be both very conductive and inexpensive. The idea is, therefore, to fabricate metal tapes (Al-tape) with a conductive glue that allows firstly sufficient conductivity in z-direction for charge collection through the glue and secondly high lateral conductivity through the metal foil. When the metal foil is stuck on the top of the C-PSC, the purpose of the carbon layer and the carbon glue is to ensure enough conductivity in z-direction to inject the charge in the metal foil (Fig 3.5). The tape is applied after the deposition of the perovskite into the stack, but no chemical interaction between the glue and the perovskite is expected to be observed due to the lack of solvent in the glue. The Al-tape is stuck by pressure and heat. The deposition of the glue on the Al-foil was carried out via low-cost doctor blade (Section 3.2).

The FF improves from around 50 % to 70 % with the application of the Al tape, pushing the PCE from 6 - 6.5 % to 9 - 10 % (Fig 3.6). This is a sign that conductivity is an issue that can be fully overcome with the Al-tape.

The use of conductive metal electrodes on the top of the device improves the charge collection and benefits to large area design. This is because the limitation of the cell width in module design is not the 15 Ω_{sq} carbon layer, but only the



	Cell 1		Cell 2		Cell 3	
	from	to	from	to	from	to
PCE (%)	6.10	9.94	6.43	9.29	6.45	9.07
FF (%)	43.32	**70.88**	47.3	**67.25**	50.05	**71.39**
J_{sc} (mA/cm^2)	19.37	19.24	16.33	16.34	17.67	17.34
V_{oc} (mV)	727	729	832	846	730	733

Figure 3.6: MAPI C-PSC with and without Al-tape on the top carbon layer. Above, the JV curves of three devices. Below, the table with the PV parameters before and after Al-tape lamination.

7 Ω_{sq} FTO layer (Section 5.3.1). The module design would benefit on this, since the most resistive electrode is the 7 Ω_{sq} FTO layer and not the 15 Ω_{sq} carbon and relative larger cells can be fabricated. Larger cells also lead to better coverage of the substrate with photoactive materials, as discussed in Section 1.6.3 and again in Section 6.3.1. However, the application of an external tape by lamination may increase fabrication complexities, as it adds further fabrication steps. Moreover, the laminated tape could de-laminate with time, reducing the long-term performance due to the resulting loss in contact. For these reasons, it was decided to find an alternative approach to resolve the conductivity issue of the carbon top electrode.

The MAPI C-PSCs fabricated without any Al-tape and by single drop deposition presented very fragile carbon layers, due to the absence of any binder in

the porous film. This binder-free carbon layer was so fragile due to poor cohesion between the flakes of graphite, with consequent reduction in toughness and, here more importantly, conductivity. This could be one of the reasons of the high R_s in C-PSC. A complete infiltration of perovskite via a double drop of PbI_2 on the active area and on the contact area can improve the robustness of the electrode and enhance the conductivity. Devices prepared with a double drop present a baseline of around 10 % PCE, 60 % FF, 21 mA/cm^2 J_{sc} and 0.8 V V_{oc} (Fig 3.7a and b). An EQE in DC mode was run on the best performing device, showing an integrated current comparable with the J_{sc} (Fig 3.7c).

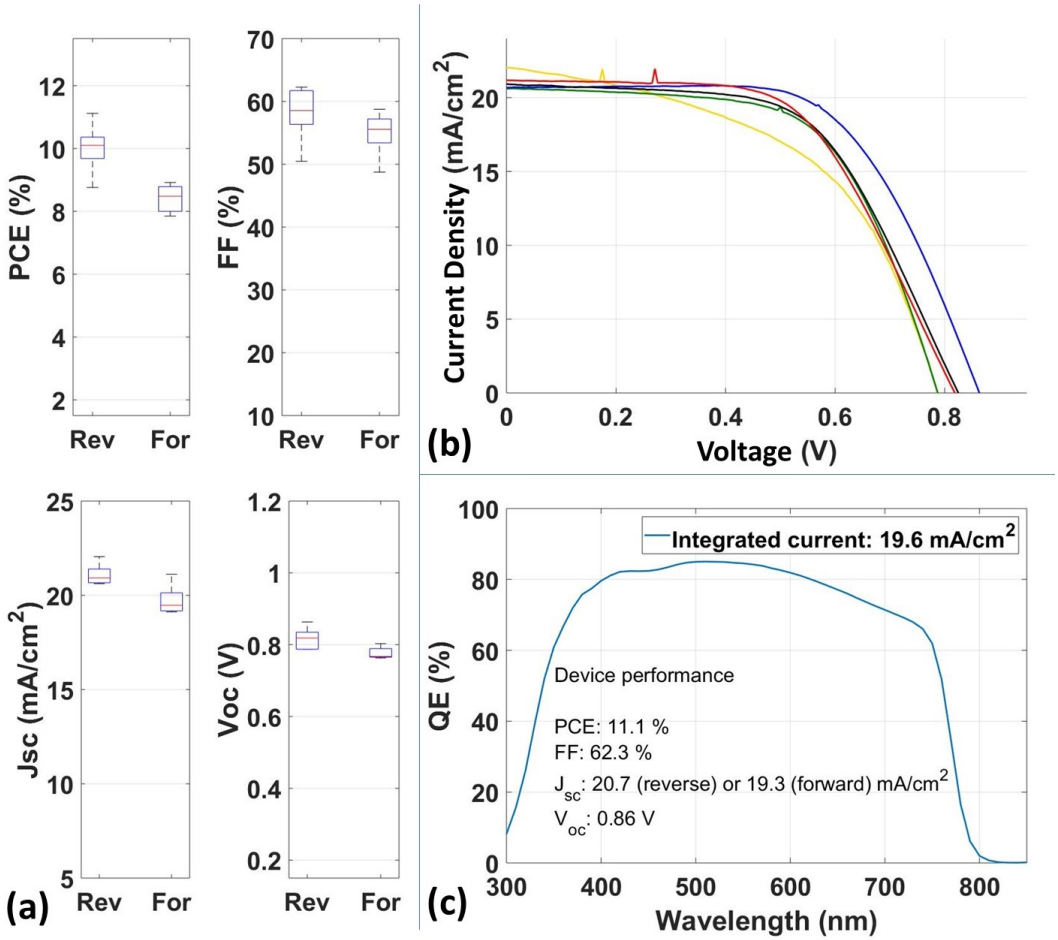


Figure 3.7: Baseline MAPI C-PSC. (a) standard deviation of the PV parameters. (b) JV curves of the devices. (c) EQE of the best performining device. Statistic 5 substrates.

The two drops of perovskite improved both FF and J_{sc}, compared to the single drop method. The effect on the FF can be attributed to the better robustness of the carbon layer. The effect on the J_{sc} could be explained with the presence of a higher amount of perovskite and a better infiltration into the stack. Devices prepared with Al-tape presented a better FF, but the double drop method allows

better robustness. In spite of the advantages in terms of conductivity and large area design that the Al-tape could offer, the double drop was adopted for the establishment of the baseline.

A baseline of around 10 % PCE is achieved with MAPI C-PSC. The method allows a simple infiltration of PbI_2 in the stack, before the conversion into perovskite by dipping in a solution MAI as per the 2-step method. This approach will be beneficial for the study in Chapter 4.

3.3.3 AVA-MAPI perovskite baseline

A crucial characteristic of the C-PSC is the high stability, which was reported to be more than a year under continuous illumination [9; 10]. The long-term stability, however, was observed for the AVA-MAPI in the C-PSC, as discussed in Section 1.4.1. For this reason, most of this work will focus on the AVA-MAPI C-PSC. This section will show the baseline for AVA-MAPI C-PSC and a comparison in terms of performance and stability with MAPI C-PSC.

The first baseline of AVA-MAPI C-PSC was prepared with a similar method to the one presented in Section 2.2.3, with the difference of the perovskite annealing step, which was done without the Petri dish. The use of the Petri dish as a closed environment where the cells are heated can slow down the evaporation of the solvent and give longer time to perovskite to crystallise in the mesoporous layers (Section 3.3.5). The method without Petri dish will be utilised for large modules, i.e. the A4 modules (Chapter 5, Section 6.3.8 and 6.3.9), whereas small modules will be prepared with Petri dish (Section 6.3.6 and 6.3.7).

A new baseline for AVA-MAPI C-PSC was established with around 10 % PCE, comparable with MAPI C-PSC (Fig 3.8). Also J_{sc}, V_{oc} and FF are similar to the MAPI C-PSC baseline. Apparently, there is no major difference between the two kinds of perovskite. The operator that fabricated the devices, however, could note the extreme differences between the formulations. First of all AVA-MAPI C-PSC shows a very slow response, with the need to apply 3 minutes light soaking before measurement (Section 2.3.1). This will be discussed in Section 3.3.4. Secondly AVA-MAPI C-PSC is extremely resistant to moisture as it can be seen when the devices are stored at 70 % RH for 24 h as post-annealing treatment (Section 2.2.3). This effect, which was used to enhance the performance of the devices, gives confidence during the fabrication of the device in ambient.

The JV curves of AVA-MAPI C-PSC, furthermore, show a peculiar behaviour: the dark current slope at high voltage is much steeper in MAPI C-PSC than in AVA-MAPI C-PSC. The AVA-MAPI device seems very resistive in dark, showing

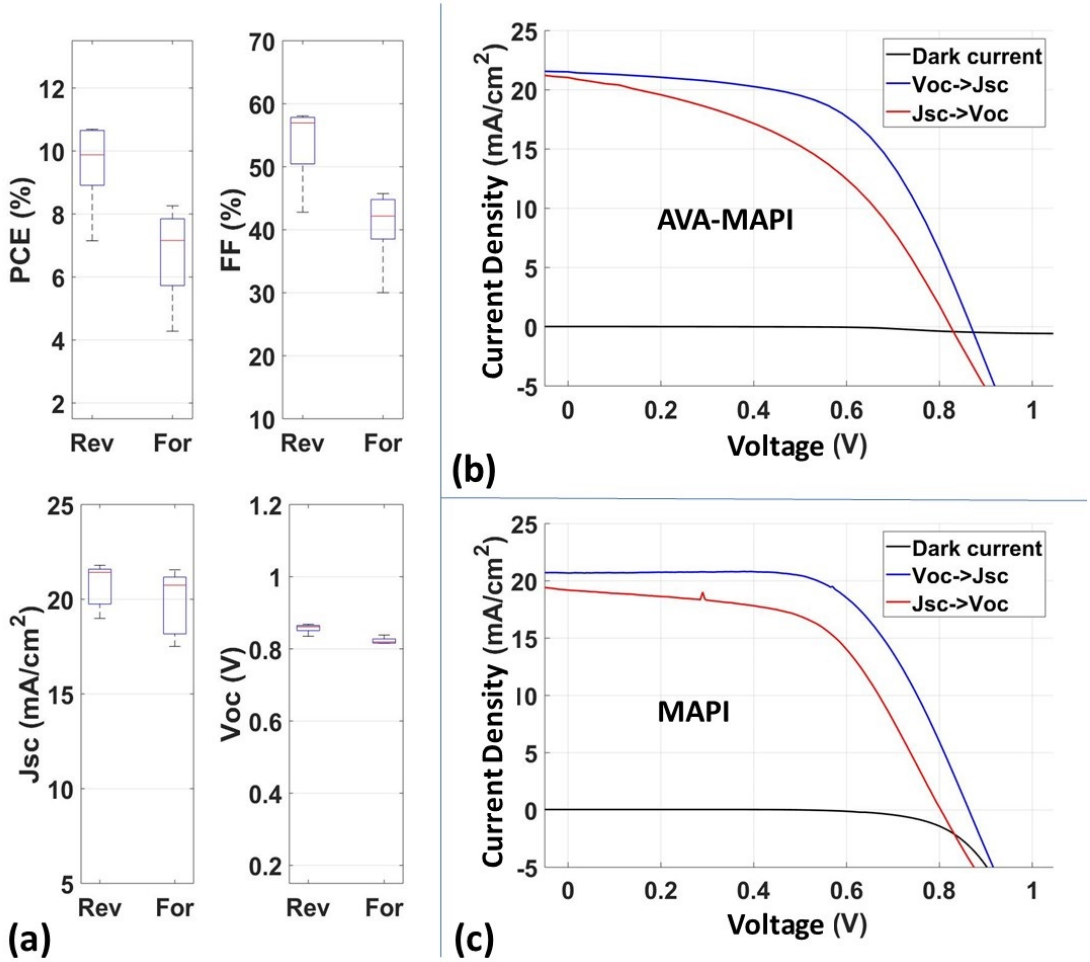


Figure 3.8: Baseline for AVA-MAPI C-PSC. (a) Standard deviation of the PV parameters. (b) JV curve of representative AVA-MAPI C-PSC. (c) JV curve of representative MAPI C-PSC. Statistic 5 substrates.

a nearly flat curve but under illumination the slope of the curve is roughly as steep as that of the MAPI C-PSC. Probably the conductivity of AVA-MAPI is strongly affected by illumination, when the promoted charge carrier density is increased. However, further investigation would be needed to understand this effect.

AVA-MAPI is much more stable than MAPI. The stability under 1 sun continuous illumination was tested on two representative devices for AVA-MAPI and MAPI (Fig 3.9). The PCE of each device drops below 80 % from the original performance after respectively around 250 h and 10 h, showing the superior stability of the 2D/3D perovskite. It should be pointed out that the stability of the AVA-MAPI C-PSC is not as high as reported in reference [10]. The reason might be due to the different experimental conditions. In reference [10] the devices were sealed and an UV filter was applied, making the two tests not comparable.

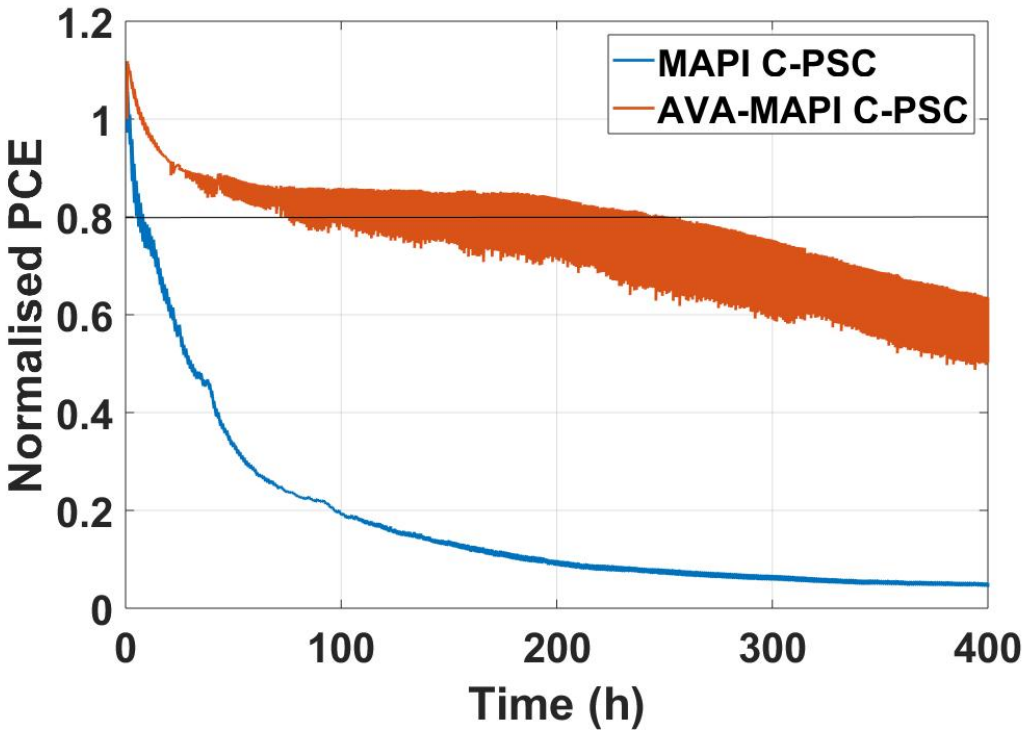


Figure 3.9: (a) Stability test comparing AVA-MAPI and MAPI C-PSC under 1 sun continuous illumination. Measurement conditions: in air, no control over humidity and temperature, no UV filter, no encapsulation. The upper profile of each curve shows the performance in reverse scan, whereas the lower profile the performance in forward scan.

3.3.4 The slow response of AVA-MAPI perovskite

The AVA-MAPI C-PSC shows an extraordinary slow response that affects the measurement. For example, a 3 minute light soaking is necessary to properly collect a JV curve for this kind of devices (Section 1.4.1). This effect might not be an issue for devices that should work continuously under illumination, but it can cause some difficulties for the characterisation. The EQE, for example, is the main technique to determine the device response at different wavelengths, and calculate the J_{sc} at given light source and intensity. This measurement, however, is strongly affected by the slow response of the AVA-MAPI C-PSC. Since the first publication of AVA-MAPI C-PSC, the integrated current of a device calculated from an EQE measurement was observed to be significantly different to the J_{sc} of a device measured after 3 minutes light soaking [9]. In other words, the EQE underestimates the optimal J_{sc} of the devices, due to the lack of proper light soaking, which is not supplied by the light probe of the EQE equipment. This phenomenon was observed also in devices prepared in this work (Fig 3.10a).

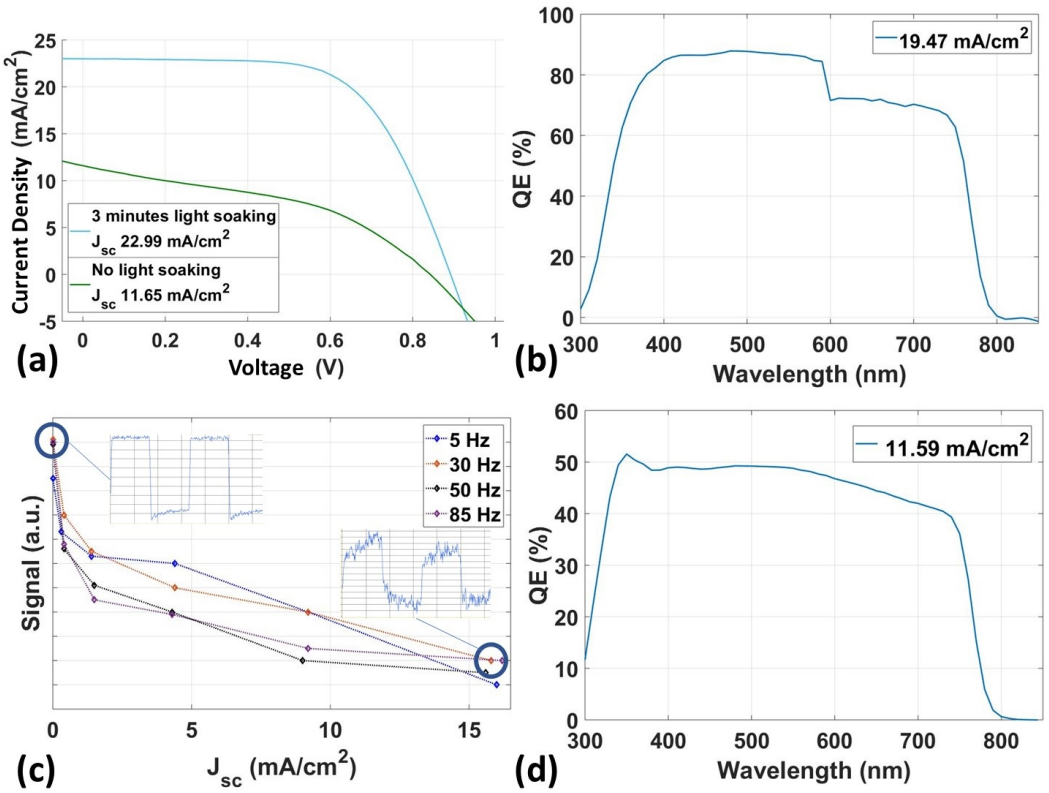


Figure 3.10: (a) JV curve of an AVA-MAPI C-PSC measured with and without light soaking. (b) EQE measurement in DC mode with integrated current of 19.47 mA/cm^2. (c) EQE signal of a device probed with a green light in AC mode at different chopped frequency. On the y-axis, the responce of the device relatively to the background current; on the x-axis, the background current due to the continuous illumination from the white light (measurement set-up in Section 2.3.1). In the inset, example of response when the white light is off ($J_{sc} = 0$) and at high illumination ($J_{sc} \sim 16$ mA/cm^2). (d) EQE measurement in AC mode with low background illumination ($J_{sc} = 0.17$ mA/cm^2) and integrated current of 11.59 mA/cm^2.

Furthermore, the slow response of the device can increase the difficulty of the EQE measurement. For example, when an AVA-MAPI C-PSC is measured with a QE X10 system (Section 2.3.1) in DC mode, a profile like the one in Fig 3.10b is systematically observed. The step observed at around 600 nm corresponds to a change of settings in the instrument. At that wavelength, the device is not probed by any light for a few seconds and the response of the device is affected.

Furthermore, the integrated current of the EQE measured in DC mode, 19.47 mA/cm^2 in this instance, is much higher than the J_{sc} measured without light soaking (11.65 mA/cm^2) and lower than the J_{sc} measured after light soaking (22.9 mA/cm^2). The light soaking effect results in a quick increase of current in the first few seconds of measurement and a continuous slow increase of current

until it reaches a plateau after a few minutes. This was observed for AVA-MAPI C-PSC at different wavelength [11]. The monochromatic light beam of the EQE creates a sort of light soaking effect, so that this measurement cannot be correlated to the JV curve started from dark conditions. However, the intensity of the light probe is much lower compared to the 1 sun illumination, giving a lower light soaking effect to the cell. We can therefore see that the EQE in DC mode is not suitable to measure AVA-MAPI C-PSC, and the results cannot be correlated to the JV characterisation.

A viable approach to overcome the instrumental issue and the effect of the light soaking could be the measurement in AC mode. In AC mode the device can be continuously illuminated by a white light, while the probing light is chopped at a given frequency. The different signal measured when the device is probed at a certain frequency is the signal that can be used to construct the EQE (Section 2.3.1). The continuous illumination can avoid the dark step at around 600 nm and can, in principle, allow a measurement at any illumination conditions. The chopping of the probing light, however, allows the measurement at a very short period, relatively to the chopping frequency. The frequency of the chopper can influence the EQE when devices, such as PSC, have a slow response [12]. If enough time to stabilise the current is needed to properly simulate the light soaking effect, a chopping period of a few minutes is necessary. Such a long period requires a chopping frequency in the order of mHz. For frequencies between 5 and 85 Hz, which is a reasonable range for the available equipment, the soaking time is very short, in this case between 0.2 and 0.0117 s. However, the C-PSC has an extraordinary slow response so no light effect is observed in this small period of time (Fig 3.10c). Therefore, any possible frequency that can be set with the available instrument would only apply a short period (< 1 s) that has no effect on the slowly responsive AVA-MAPI C-PSC. Moreover, the chopping frequency seems not to give an obvious difference in the measurement in terms of signal/noise ratio, so any possible frequency that can be applied with the available equipment could be used for the measurement. Here it was adopted 30 Hz.

Furthermore, the background light gives a huge effect on the signal/noise ratio, and the signal is very noisy when the intensity is too high. The only way to measure the AVA-MAPI C-PSC devices with a clear signal is at low background light intensity. Therefore, it was decided to run the EQE experiment at very low background light.

The measurement in AC mode is strongly correlated to the measurement without light soaking, and the integrated current and J_{sc} of the relative JV curve are

very similar, i.e. 11.59 and 11.65 mA/cm^2 (Fig 3.10d). The correlation between the two measurements can be done if the JV curve without light soaking effect is taken into account. The profile shows an unexpected shape, with a peak at low wavelength. Probably the response time of the device is different at different wavelengths, making the correlation between EQE profile and property of the device difficult. In other words, the light soaking effect can be different at different wavelengths, perhaps due to different absorption phenomena or light penetration.

In conclusion, the measurement of the EQE, which is vital for a proper characterisation of the PV performance, is not straightforward for AVA-MAPI C-PSC. This is due to the slow response of the device, and only the J_{sc} obtained without light soaking can be correlated to the EQE signal. Equipment that can measure the EQE with chopping frequency in the order of mHz could be used for a proper correlation between JV after light soaking and integrated current. The result without light soaking, however, confirms the proper calibration of the solar simulator during the JV curve and the accuracy of the measurement.

3.3.5 Effect of the perovskite annealing

The baseline was established with a performance of around 10 % PCE for the AVA-MAPI C-PSC (Section 3.3.3). However, higher PCE is desirable, especially in terms of up-scaling. This is because the PCE of large area modules is not expected to be higher than that of small devices, but rather it could be lower due to the larger nature of the device (Section 1.6). Because a requirement for the modules was to achieve at least 10 % PCE on 10 × 10 cm^2 modules, a strategy to increase single cell performance was necessary. A possible approach to optimise the device performance is to investigate the annealing of perovskite.

Compared to other perovskite formulations, AVA-MAPI in C-PSC is treated very differently:

- Annealing temperature. Typical perovskite formulations are annealed at relatively high temperature, around 100 °C or more, e.g. up to 150 °C in reference [13] and 100 °C in reference [14; 15]. High temperature seems to be beneficial for the perovskite crystal formation. The AVA-MAPI C-PSC, by contrast, is reported to be fabricated with an annealing temperature of only 50 °C, which is an extraordinarily low temperature for PSC.

- Evaporation rate. The evaporation of the solvent seems very important for the crystallisation of MAPI. The antisolvent method that extract instantaneously the remaining solvent in a spin coating approach, for example, allow a

faster crystallisation of the harvesting material and have been demonstrated a key step for the fabrication of PSC (Section 1.3.2). Also the spin coating method itself, typically adopted to prepare highly efficient devices, has been described as a successful technique, due to the high evaporation rate that the perovskite solvent experiences during the spinning [16; 17]. The AVA-MAPI in C-PSC, by contrast, requires the use of a high boiling point solvent, i.e. GBL, that does not evaporate fast.

The fact that AVA-MAPI in C-PSC requires low temperature and high boiling point solvents is, probably, because the 2D/3D perovskite needs a relative long time to properly organise the crystal structure before the solvent is completely evaporated. The annealing temperature, therefore, must influence the perovskite crystallisation and device performance, alongside with the evaporation rate. If the devices are enclosed in a small environment, the container should saturate with the vapours of the solvent and reduce the evaporation rate. This can be achieved by enclosing the devices in a Petri dish during the annealing step. This section will show the effect of two annealing temperatures on devices that are placed in an oven with or without a Petri dish.

The use of low temperature might be due to the intrinsic physical-chemical properties of the perovskite precursors. MAPI can be annealed at much higher temperature [18]. The only component that differs from the other perovskite formulations is AVAI. According to the material safety data sheet (MSDS), no decomposition temperature is recorded, but the lowest temperature that causes physical-chemical changes in the compound is the melting point, i.e. 95 °C. This temperature should not affect AVAI in solution phase for the formation of the perovskite crystal structure, but to test a safe annealing temperature higher than the standard 50 °C, 70 °C was chosen to make a first investigation.

The results are shown in Fig 3.11. The JV curves show the benefit of using a 50 °C temperature over 70 °C, especially in synergy with the Petri dish (Fig 3.11a). A higher temperature is not expected, therefore, to further improve the device performance. The striking fall in performance when the devices are annealed at 70 °C, both with the use of a Petri dish and without, is unexpected. The different evaporation rate, faster at 70 °C than at 50 °C, should not play a significant role if it is considered that even with the slower evaporation rate inside a Petri dish, the device performance falls below 5 %. Also, possible degradation phenomena can hardly occur during the process because all the chemicals in use are stable at 70 °C. A different crystal formation compared to that of a typical annealing at 50 °C could cause the poor PCE at 70 °C. The AVAI might anchor differently on

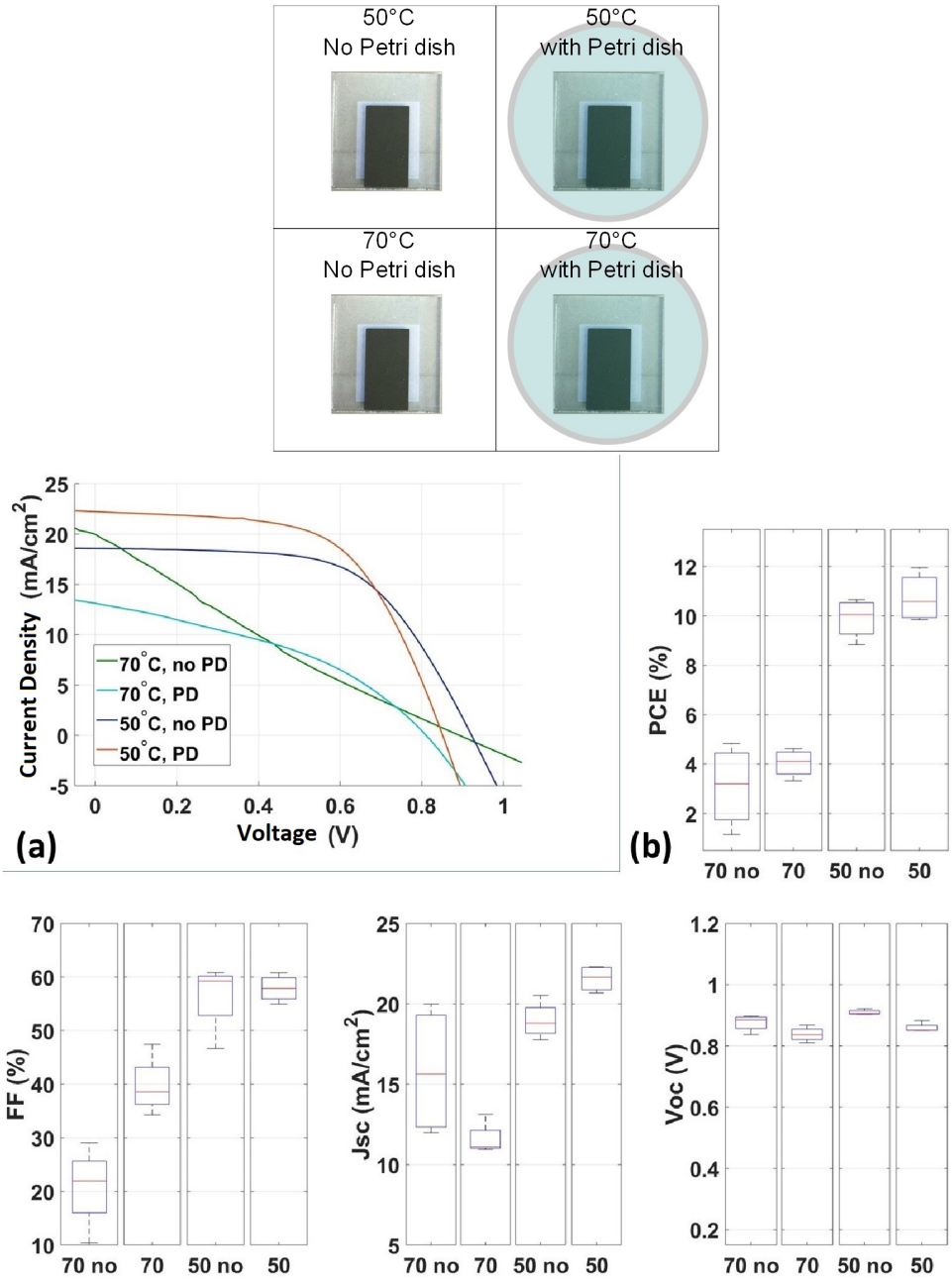


Figure 3.11: PV performance of devices where perovskite was annealed in different conditions of temperature and environment, i.e. in oven inside of a Petri dish or not, at 50 °C or 70 °C. (a) Representative JV curves of different AVA-MAPI C-PSC. The annealing of the perovskite occurred at respectively 70 °C without Petri dish, 70 °C with Petri dish, 50 °C without Petri dish and 50 °C with Petri dish. (b) Standard deviation of the different groups of cells. Statistic 4 substrates.

the scaffold oxide giving a different template effect on the 3D perovskite phase, especially at the TiO_2/ZrO_2 interface [19].

The use of the Petri dish improves the device performance at 50 °C, from an average PCE of 10 % to 11 %. Probably, the slower evaporation gives time for perovskite crystals to better reorganise themselves in the triple mesoscopic stack. It should be noted that the slow annealing that is required in C-PSC is a special peculiarity of this architecture. For planar or thin mesoporous-based PSC, the evaporation of the solvent is required to be as fast as possible. This is typically achieved by spin coating [20] or by air blade-assisted deposition methods [17].

The use of the Petri dish, however, is not scalable due to the limited dimensions of the container. It will be utilised only for small devices, both single cells and small scale modules. Large scale devices could not be treated in Petri dish due to their size.

3.3.6 Deposition methods for the compact TiO_2

The fully printable C-PSC is manufactured on a substrate of glass/FTO/bLayer. On top of the glass, therefore, there are two layers that are not printed, i.e. FTO and bLayer. Conductive glass with FTO on top is a commercially available product, whereas the bLayer is deposited in laboratory, typically by spray deposition. Commercially available substrates with an ETM as bLayer on the top were recently reported for highly performing PSC [21] but the possibility of also printing the bLayer is a fascinating prospective for the fully printable C-PSC. This section wants to show the effect of the deposition method of the bLayer for the C-PSC. The standard spray deposition is compared to screen printing, to investigate the possibility of printing the compact TiO_2 layer. Moreover, the effect of the film quality of the bLayer on the C-PSC performance will be investigated by comparing high-quality ALD deposition to the standard spray deposition.

ALD is a chemical deposition method that requires vacuum and allows the deposition of very thin and compact layers. Applications in carbon-based PSC can be found in reference [22], but so far it has never been tried in the triple mesoscopic stack. This technique is the most promising to obtain high quality and very thin TiO_2 layers, when compared to screen printing and spray deposition. Its disadvantages are related to the manufacture. A large number of cycles are required, making the process relatively slow for a large area production. Moreover, a vacuum chamber is necessary, which allowed a homogeneous deposition only on small substrates up to 10 × 10 cm^2, when considering the equipment that was adopted in this work.

Screen printing is a low-cost technique and suitable for large area production. Moreover, this technique allows patterning of the layer without the need of material removal or application of masks during the process. From the production point of view, screen printing is the simpler and faster method than to ALD and spray. However, it is suitable only for thick layer deposition, in the order of μm, and the final layer is typically rougher compared to layers deposited by ALD or spray. In order to achieve very thin layers by screen printing, the ink needs to contain a large organic content, so it can be fired to leave a very thin TiO_2 layer.

Spray deposition, which is the standard method to deposit bLayer, is low-cost, suitable for large area production and able to achieve very thin films. The thickness of the final layers achieved by spray can be higher compared to ALD, but much thinner compared to screen printing. Its disadvantage when compared to screen printing is the lack of a patterning of the layer, unless a mask is applied. Spray deposition is a well-known and largely used technique to deposit compact TiO_2 and allows a reasonable high-quality film deposition with a relatively simple deposition process.

The preparation of AVA-MAPI C-PSC on substrates with bLayer obtained with the different methods was carried out and is shown in Fig 3.12. The ALD was demonstrated to be the best method to deposit bLayer, whereas the screen printing method does not seem suitable for such an application (Fig 3.12a). The screen-printed bLayer was underperforming compared to the other bLayers and this can be observed in all PV parameters, i.e. FF, J_{sc} and V_{oc}. The low FF and V_{oc} could be explained by the low hole barrier effect of this bLayer, due to the presence of pinholes. The dark current gave a good indication of the proper diode behaviour of the devices. A flat curve can be observed at low voltage only for devices prepared by ALD and spray, but not by screen printing (Fig 3.12b). Considering that the only difference between the groups of devices is the bLayer, it is clear that the deposition of the thin compact layer via screen printing does not offer a proper method for this step of the manufacture. The screen-printed layer shrinks enormously from thicknesses of μm to nm values. It is likely, therefore, that the large organic content that is present in the ink formulation might leave pinholes when removed from the layer. This could explain the poor hole barrier that is observed in the dark current. Screen-printable bLayer for C-PSC was found to be already reported but with a subsequent dipping step in a solution of $TiCl_4$ [23]. The dipping in a TiO_2 precursor might block the pinholes making the bLayer a proper hole barrier. This solution to the issue of the pinholes, however,

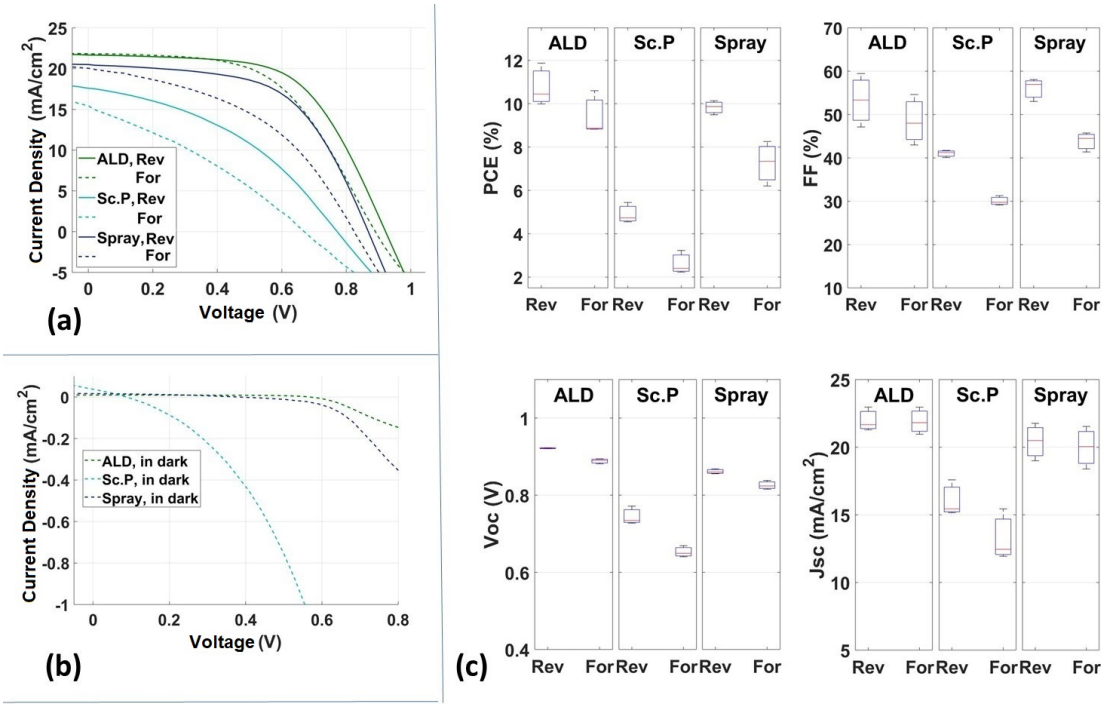


Figure 3.12: JV curves of AVA-MAPI C-PSC, which bLayers where prepared with different methods: ALD, screen printing (Sc.P) and spray deposition. (a) Under 1 sun illumination. (b) In the dark. (c) Standard deviation of the different groups of cells. Statistic 3 substrates per parameters. The thickness of the layers is around 16, 70 and 60 nm for respectively ALD, Sc.P and spray. Deposition of bLayer by ALD and relative thickness measurement by ellipsometry was kindly made by Dr. Amrita Yasin.

results in a deposition of TiO_2 all over the substrate, making the pattern of the screen-printed layer inefficient.

The bLayer plays an important role in the C-PSC, and high-quality films are crucial for device performance. ALD seems to be the best technique for achieving high-quality films, as it can be observed in Fig 3.12b, where the dark current of devices prepared via ALD is flatter compared to that of devices prepared either via spray or screen printing. The devices deposited with ALD are around 11 %, which is higher than the devices prepared by spray. The main improvement is in the V_{oc} and in the J_{sc} (Fig 3.12c). Considering the better dark current observed for ALD over spray deposition, the improved V_{oc} can be related to the better hole barrier that is offered by the bLayer prepared via ALD. the hysteresis of the devices should also be noted. The use of ALD seems to improve the hysteresis if compared to the use of spray (averaged PCE, ALD: 10.8 % in reverse and 9.4 % in forward, hysteresis 0.87; spray: 9.3 % in reverse and 7.3 % in forward, hysteresis 0.78). This could be related to the thickness of the bLayer, which can have a huge effect on the hysteresis of AVA-MAPI C-PSC [24].

In conclusion, according to these results, the bLayer cannot be printed for high performing devices. This is likely due to the challenge of achieving very thin films with a technique that typically deposits thick layers. ALD gives optimal results, very likely due to the very thin layer achievable with this technique. The technique presents a disadvantage in terms of up-scaling due to the small vacuum chamber of the available equipment, but it was useful to prove that the C-PSC requires high-quality and thin bLayer for the fabrication of high performing devices. Spray coating is a technique that allows the manufacture of devices with satisfactory performance and can be used for small and large scale devices.

3.3.7 The role of the ZrO_2 layer

The spacer layer in the C-PSC plays the role of separator between the cathode and the ETM, carbon and TiO_2 in this case. The positive charge must travel through perovskite in the spacer layer, here mZrO_2, along a path that can be longer or shorter according to the thickness of the mZrO_2 layer. Because the length of the path affects the R_s and the likelihood of recombination, it seems convenient to try to decrease the thickness of the spacer layer as much as possible. However, there is a limit to how much the spacer layer thickness can be reduced (Section 1.4.2).

The reason for this section arose from two considerations:

- The highest performing C-PSC reported in recent time present very thick spacer layers. For example, the work in reference [25] (2018), aimed to reduce the thickness of the spacer layer. The article proposed a composite of ZrO_2 and Al_2O_3 to achieve slightly more than 1 μm, which was already the thickness adopted by many authors [26; 27]. This layer was considered thin because it was compared to a much thicker layer of around 3 μm, which resulted in devices with around 15 % PCE, much higher than previous reports and higher than the devices that were presented in this chapter. The high performance seems related to the thickness of the spacer layer, because if ZrO_2 is compared, 3 μm spacer layer is reported to be more effective than 1.2 μm. It is reported, furthermore, that the thick spacer layer (3 μm) requires a larger amount of perovskite solution compared to the thin layer (1.2 μm), probably to obtain a proper pore filling [25]. The use of thick ZrO_2 layer for efficient devices is reported also in reference [28] (2018).

- The second consideration came from the collaboration for the work in reference [29], i.e. on the electro-optics of C-PSC, where the light penetration

in the red region was learnt to be extraordinary deep, going even to the carbon layer. A complete absorption of the light would occur for thicker stack according to these results.

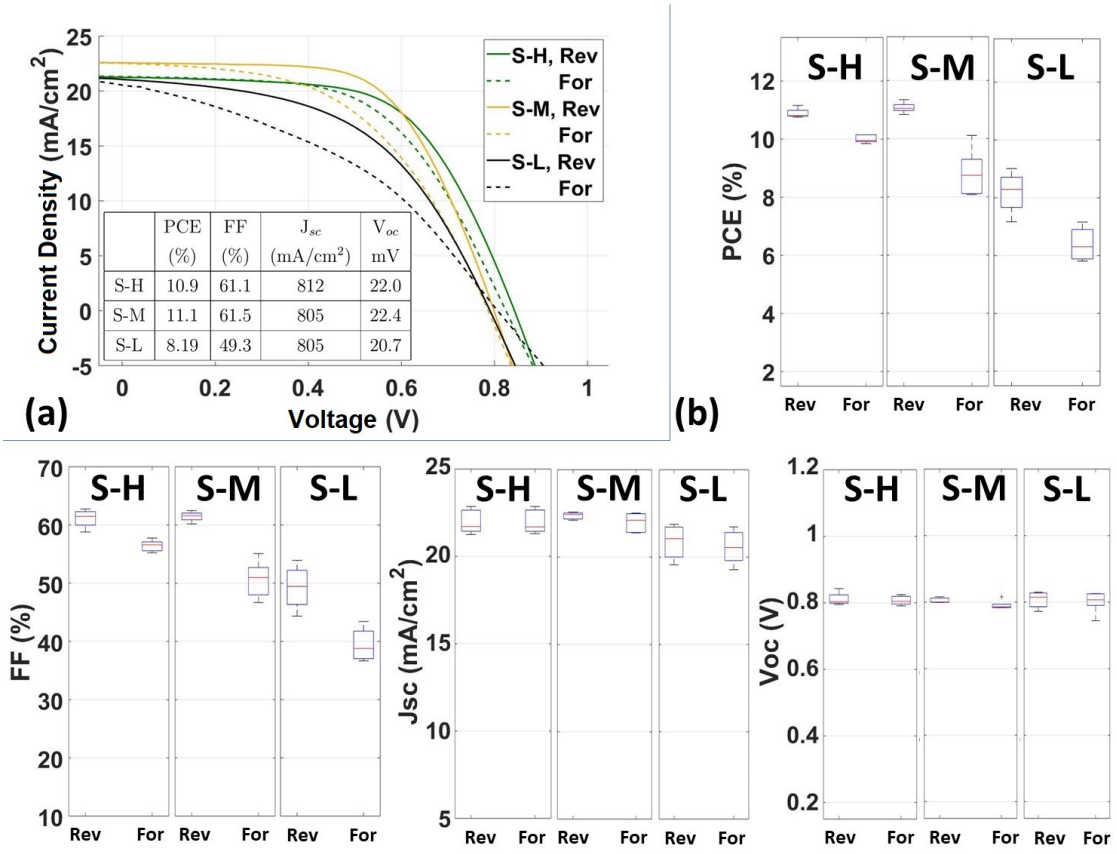
The outcome of the work in reference [29] in combination with the reported values of ZrO_2 thickness for highly efficient C-PSC [25; 28], raised the question about the real optimum for the spacer layer thickness.

The effect of the ZrO_2 with varying thickness was investigated. Moreover, the effect of the perovskite solution concentration as a way to change the amount of precursors in the stack was also studied. The thickness of the $mZrO_2$ was varied with the number of deposited layers: one single $mZrO_2$ layer (Single = S) for the baseline and double layers of $mZrO_2$ (Double = D) for thicker spacer architecture. The amount of perovskite was varied with the concentration of the solution. Solutions of 1 M (baseline), 1.2 M and 0.7 M were prepared, by conserving the same molar ratio between PbI_2, MAI and AVAI.

For devices with single $mZrO_2$ layer, the influence of the solution concentration was not strong (Fig 3.13). With high concentration and medium concentration of perovskite solution (S-H and S-M), the resulting performance was comparable, whereas with low concentration of perovskite solution (S-L), the devices were under performing, with PCE from around 11 to 8 %. The hysteresis for each group was comparable with the previous set of devices, as shown in Fig 3.8 and 3.12. The gap in PCE from S-H/S-M and S-L devices was mostly due to the FF, but also the J_{sc}, whereas the V_{oc} was basically identical for the three sets of devices. When the FF and the J_{sc} were affected, it was possible that the lower performance is because of eventual higher R_s is the device (Section 1.5). It could be that the positive charge was transferred into the carbon by following a tortuous path through the perovskite that did not fully infiltrate the stack. This tortuous path increased the charge transport length and, thus, also the R_s.

For devices with double $mZrO_2$ layer, the effect of the solution concentration was very striking when the concentration was low (D-L). Devices with high and medium concentration (D-H and D-M) showed much higher performance compared to D-L, from around 4.5 to 12.5 %. Moreover, D-L showed around a half of the PCE of S-L.

S-L devices exhibited higher PCE than D-L, but lower PCE compared to S-H and S-M. This trend from S-H/S-M, S-L and then D-L is a confirmation of the need for proper infiltration in the triple mesoscopic stack. Low concentration perovskite solution, probably, does not allow a full infiltration in the stack due

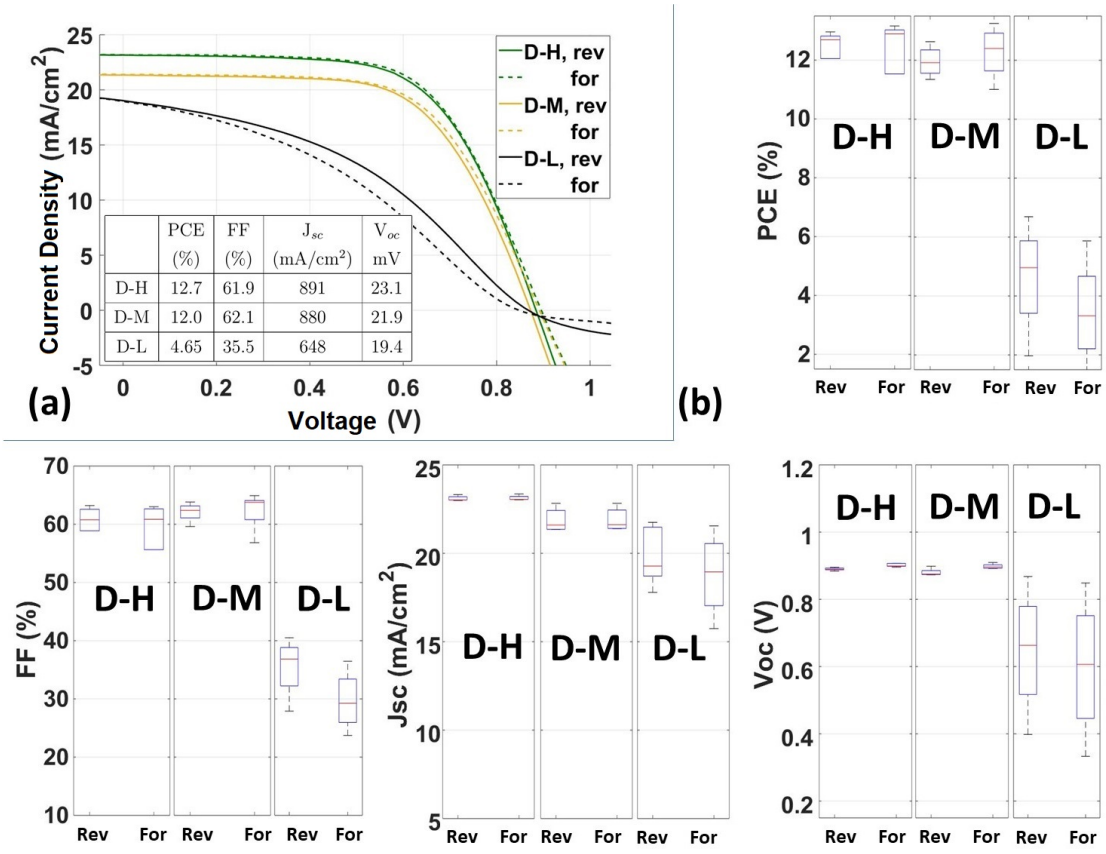


	PCE (%)	FF (%)	J_{sc} (mA/cm^2)	V_{oc} mV
S-H	10.9	61.1	812	22.0
S-M	11.1	61.5	805	22.4
S-L	8.19	49.3	805	20.7

Figure 3.13: JV characteristics AVA-MAPI C-PSC prepared with a single layer of $mZrO_2$ and different concentrations of perovskite solution, i.e. 1.2 M (S-H), 1 M (S-M) and 0.7 M (S-L). (a) JV curves of representative devices. In the inset, averaged values of PV parameters for 5 devices for each group. (b) Standard deviation of the different group of cells. Statistic 5 substrates.

to the lower amount of material that is deposited per same volume. This is already observable with a single $mZrO_2$ layer, but the effect in much more striking when a thicker stack with double ZrO_2 layer is utilised, i.e. when much more volume needs to be occupied. This poor filling of the stack from low concentrated solutions can hinder the charge extraction through perovskite, especially for the holes that need to reach the cathode at few μm from the transparent electrode. This mechanism explains the lower FF and J_{sc} than the ones from the analogous devices with higher concentration of perovskite solutions. The lower V_{oc} can be explained, however, if it is considered that charge transfer is so hindered by the poor pore filling that some charge recombines before it can be collected by the electrodes. The J_{sc} is lower compared to the other devices but still satisfactorily high, i.e. more than 19 % for most of the devices. This is a sign that the poor pore filling does not affect the absorption of the light, which is required for high J_{sc}.

D-H and D-M show lower hysteresis compared to S-H and S-M. The hysteresis



	PCE (%)	FF (%)	J_{sc} (mA/cm²)	V_{oc} mV
D-H	12.7	61.9	891	23.1
D-M	12.0	62.1	880	21.9
D-L	4.65	35.5	648	19.4

Figure 3.14: JV characteristics AVA-MAPI C-PSC prepared with a double layer of $mZrO_2$ and different concentrations of perovskite solution, i.e. 1.2 M (D-H), 1 M (D-M) and 0.7 M (D-L). (a) JV curves of representative devices. In the inset, averaged values of PV parameters for 5 devices for each group. (b) Standard deviation of the different group of cells. Statistic 5 substrates.

can also be inverted in some devices, where the forward scan shows higher output power than the reverse one. C-PSC tend to show high hysteresis. The thick nature of this architecture might cause capacitance effects in the device, which could explain difference in PCE between the two scans (hysteresis). However, the possibility to reduce the hysteresis, or even invert it, has already been demonstrated with very thin bLayers [24]. The effect of the spacer layer on the hysteresis has not been discussed in the literature yet, although this topic would deserve more investigation to understand the mechanism occurring in the device.

Devices with thicker ZrO_2 can achieve much higher PCE compared to analogous devices with thin ZrO_2. If the cases of S-L and D-L are not taken into account, an increase in PCE is observed with thicker ZrO_2 layers. This improvement in performance, from around 11 to 12.5 %, was not expected before reference [25; 28] and the cause of this phenomenon has not been investigated yet. The improvement from single to double layer is mostly in V_{oc}, from just above 800 to nearly 900 mV. Also, the J_{sc} and FF are slightly enhanced but without a clear improvement. This

is also due to the already high values that are achieved with a single layer of ZrO_2. The J_{sc} is already close to the physical limit for PSC, whereas FF, higher than 60 %, seems difficult to achieve without the aid of metallic electrodes (Section 3.3.2).

A possible explanation of the higher V_{oc} is the lower recombination that occurs in the devices. Carbon is not an electron barrier and eventual negative charge carriers that reach such a layer could be collected causing recombination with the holes. Electrons are mostly injected into TiO_2 and it is unlikely that they can be transferred through perovskite with holes to be injected into carbon. Probably, electron-hole pairs are generated very deeply in the stack, due to the deep penetration of the light with long wavelength. These photons could reach areas close to the ZrO_2/carbon interface and generate charge that is subsequently collected by the non-selective carbon. When the thickness of the spacer layer is increased, the carbon layer is pushed further, and no light, or very little amount of light, can penetrate as far as the ZrO_2/carbon interface. In this way, the generated charge can be selectively collected to avoid possible recombination at the depth of the ZrO_2 layer.

Further investigation is necessary to explain the phenomena that occur in the C-PSC architecture, but the effect of the thickness on the mesoporous layers is here proven to be much more important than expected. Due to the timeline of the research process, the baseline for AVA-MAPI C-PSC in this work is based on the single layer mZrO_2, in spite of the higher performance that was achieved with the double layer.

3.4 Conclusion

Single cell devices were successfully prepared with performance above 10 % (top devices around 13 %). This was done to understand the behaviour of the C-PSC before the up-scaling into module design. The inorganic stack was characterised, so as to properly assess the device manufacture. The MAPI C-PSC was established with the 2-step method, which will be adopted for the infiltration study in Chapter 4.

The AVA-MAPI C-PSC, which will be the main device that will be investigated in this work (Chapters 5 and 6), was established with the following outcomes:

- A performance of around 10 % was initially achieved for the baseline.
- Higher performance can be achieved by:

  - controlling the solvent evaporation rate during the perovskite solution drying step;
  - enhancing the quality of the bLayer, for example by using ALD for the deposition of the compact TiO_2;
  - controlling the thickness of the spacer layer.

- From the physical point of view, it was discussed:
  - the slow response of the AVA-MAPI in the C-PSC and the peculiar effect during EQE measurement;
  - the effect of thick ZrO_2 layers on the device performance, especially in terms of V_{oc}, which brings into consideration the effect due to recombination phenomena at the ZrO_2/carbon interface.

The cells were prepared with the drop method, which works very well for small scale devices. For large area devices, a considtent method to deposit quickly and homogeneously the perovskite precursors solution is necessary. Chapter 4 will focus on the deposition method to achieve higher homogeneity over large scale. This will be done with an automatized method, a necessary step for the up-scaling of C-PSCs.

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Chapter 4

Overcoming manual infiltration

Single cell devices based on the triple mesoscopic stack has been investigated to understand the performance of C-PSC. Because of the high expectation for this architecture to be the possible frontrunner for early industrialisation, automatised methods to prepare the device in short time and consistently are necessary. Whereas the screen printing for the inorganic layers is well established industrial method, the drop infiltration that is typically adopted for C-PSC is inhomogeneous, prone to human error and, thus, ineffective for large areas.

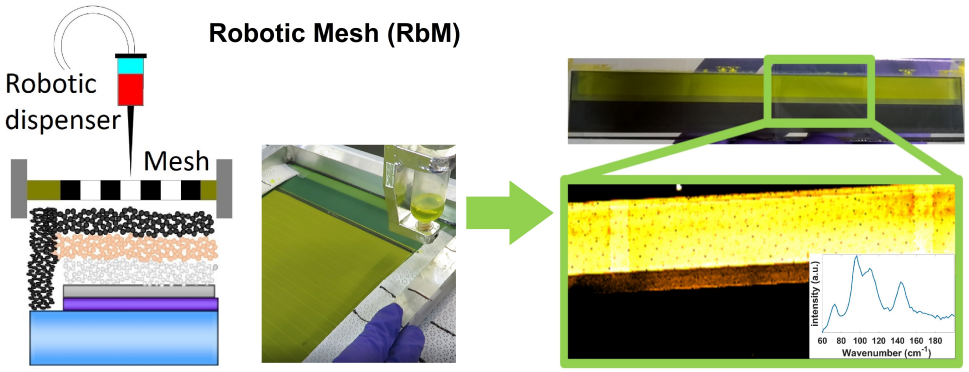

Figure 4.1: General schematic of the Robotic Mesh method.

In this chapter, an automatized method to deposit perovskite homogeneously and quickly over a large area of the triple mesoscopic stack is investigated. A robotic dispenser can be used to continuously deliver a fixed amount of perovskite solution over large area devices. When the solution of perovskite, which is in a polar solvent, comes in contact with the hydrophobic carbon layer, it reorganises itself and infiltrates inhomogeneously through the triple mesoscopic stack. A fine mesh between the needle of the dispenser and the device aids the spreading of the solution, allowing homogeneous infiltration (Fig 4.1). After preliminary tests to prove its effectiveness, this method was successfully used to prepare perovskite

solar cells with performance comparable to the cells which were made with the standard drop deposition.

4.1 Introduction

The C-PSC is based on a triple mososcopic stack which includes firstly $mTiO_2$, followed by $mZrO_2$ as an insulating spacer and then finally a conductive carbon as top contact [1]. To complete the device, droplets of a perovskite solution are applied to the carbon surface which then wet and infiltrate through the mesoporous stack [2]. Perovskite precursor solutions are typically manually applied using a pipette to the carbon surface of a C-PSC. The deposition can occur with either the 1-step [1; 2] or the 2-step [3; 4] approach. Inkjet printing was also reported for the deposition of perovskite solutions into the C-PSC [5].

Small devices (up to 1 cm^2) can be easily prepared using the drop deposition method, but large area devices require high uniformity in order to minimise the presence of pinholes and defects (Section 1.6). Achieving high uniformity over a large area using manual application is problematic due to the lack of control during the deposition. Inkjet printing allows controlled and uniform depositions, but the droplets of solution are deposited one-by-one and this requires a large number of nozzles to print over a large area in a reasonable time scale [6]. Other printing techniques, such as flexographic and screen printing, require inks with polymer-based binders to tune the rheological properties of the solution. Polymeric binders, however, may affect the electrical properties of the final layer and would need to be removed by heating the stack above 400°C, which is too high for perovskite films [6; 7]. Flexographic printing can be used to print inks with low viscosity, but gives poor homogeneity when printing solid areas such as those required for solar cells. This poor homogeneity is caused by surface instabilities in the ink between the flexographic plate cylinder and the substrate [7].

In this work, a novel deposition method is presented, which involves the use of a robotic dispenser and a mesh to deposit binder-free inks over large area, such as perovskite solutions, quickly and homogeneously (Fig 4.2). In this Robotic Mesh (RbM) deposition technique, the automated dispenser applies a controlled volume of solution onto the mesh. Upon contact with the mesh, the solution is forced to spread homogeneously onto the carbon surface. The principle of the technique can be compared to inkjet printing, where the liquid is delivered as many little drops, but in the RbM deposition all the necessary precursor solution is deposited simultaneously, reducing considerably the deposition and subsequent infiltration

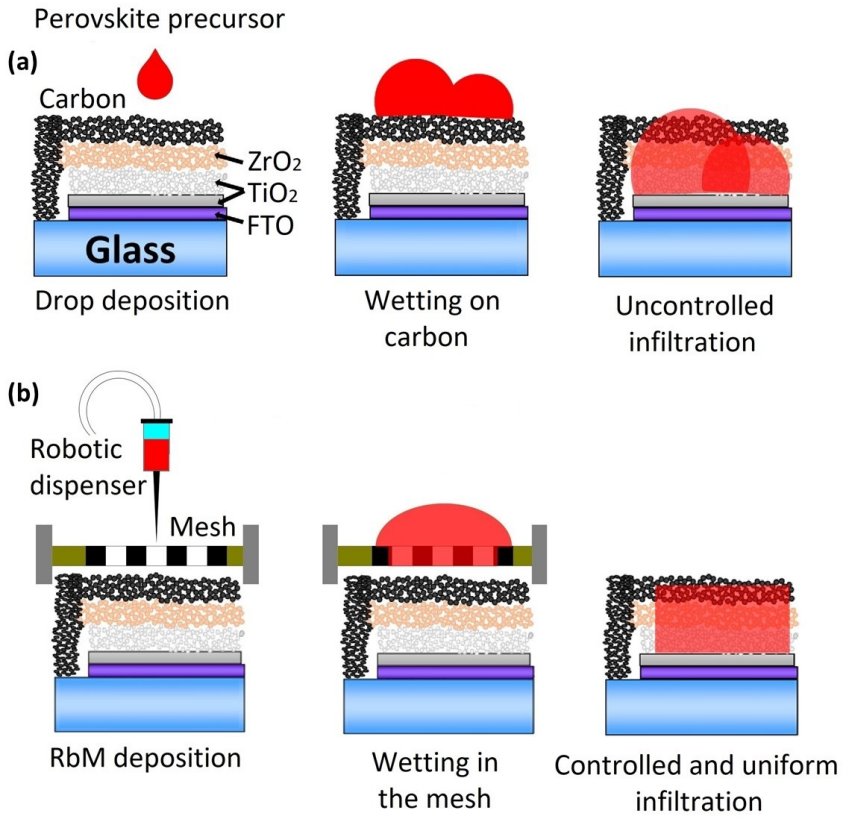

Figure 4.2: Schematic representation of deposition methods for perovskite precursor solutions on C-PSCs. (a) drop method (b) robotic mesh method (RbM).

time. RbM does not use a flow coater or a squeegee to apply a mechanical force, like in screen printing. Instead, the ink is spread on the fine mesh and transferred by gravity to the porous layer. The mesh for RbM deposition is not required to be elastic, as for screen printing.

A 2-step deposition method (Section 2.2.2) was adopted in this study. The use of PbI_2, which is bright yellow, allows a visual monitoring of its infiltration through the mesoporous layers. The homogeneity of the deposition was determined by XRD sampling and Raman mapping. Raman allows a clear visualisation and the mapping of the PbI_2 phase. XRD can detect both MAPI and PbI_2 phases and can be used to make a sampling of the two phases on the infiltrated surface.

This mechanised infiltration method has the potential to automate the final stages of device fabrication. As a consequence, every step of the device production is mechanised, including the substrate preparation, the sequential layering by screen printing, infiltration using the RbM and a final dip process are all mechanised. This has significant potential for unlocking high volume continuous manufacture.

4.2 Experimental

The main steps for the device preparation are reported in Section 2.2.1 and 2.2.2. Below, specific steps for the use of the RbM method are described.

The robotic dispenser consists of a syringe that is pressurised with compressed N_2 gas and mounted on an X-Y-Z rail (Fisnar, F5200N.1). For 1 cm^2 devices prepared via RbM, the static robot dispensed 13.6 μL of solution directly onto the mesh with a deposition time for each cell of 0.2 s. The deposition takes around 8 s for a set of 15 cells. For deposition over a large area, the needle of the dispenser, made of stainless-steel with a 0.16 mm inner diameter, continuously delivered the perovskite precursors solution to the mesh (180/27 mesh size) surface as it progressed across the sample in a single line at 12 m/min. After deposition, the liquid takes around 5 s for a complete infiltration. Therefore, the deposition of a 10 cm^2 sample lasts around 5.5 s (Fig 4.3).

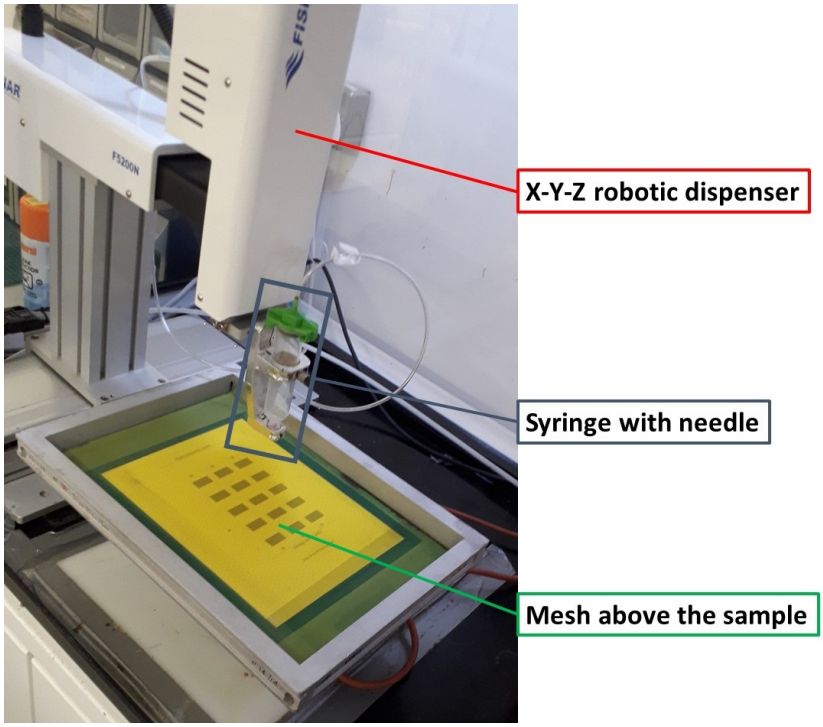

Figure 4.3: Set-up for the RbM method and the relative components.

Following application, the PbI_2 solution spreads on the mesh area and then infiltrates into the mesoporous stack. The mesh size controls the spread of the liquid. When the entire deposited solution is infiltrated, the mesh can be removed. A less concentrated (0.76 M, 350 mg/mL instead of the standard 460 mg/mL) PbI_2 solution was used to avoid crystallisation in the needle during the RbM deposition. Printing is continuous until the end of the batch. After each batch, the screen is

cleaned and reused. The subsequent steps for the device preparation with the 2-step method, including the PbI_2 heating and subsequent conversion into perovskite, followed the standard method that is shown in Section 2.2.2.

The control devices, or drop cells here, were prepared as reported in Section 2.2.1 and perform according to the baseline shown in Section 3.3.2. Characterisation was carried out as described in Section 2.3.

4.3 Results and discussion

4.3.1 Preliminary study of the drop method

To understand the issues of the drop method, this was investigated first. Based on the 2-step deposition method, PbI_2 solution drops were deposited over a large area strip of $mTiO_2/mZrO_2$/Carbon layers (10×1 cm^2). When applied as a single

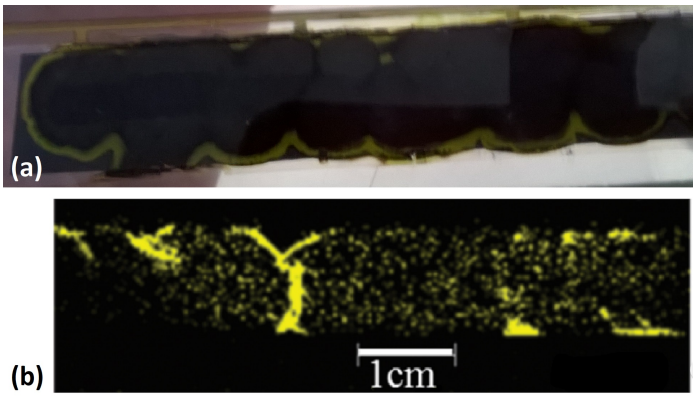

Figure 4.4: Drop deposition on the triple mesoscopic stack in stripe shape. (a) photograph of an infiltrated sample with consequent conversion of the PbI_2 into MAPI. (b) Raman chemical map of an equivalent sample.

drop, the PbI_2 solution infiltrates into the mesoscopic layers with a characteristic coffee stain pattern [8], where a high amount of PbI_2 can accumulate at the edge of the ring. Similarly, when multiple drops are deposited the PbI_2 does not distribute homogeneously over the layer and the rings are still visible (Fig 4.4a). In the edge area, the PbI_2 crystals may saturate and block the pores, preventing conversion to MAPI during the MAI precursor immersion in the 2-step deposition. The result is the formation of black perovskite with yellow rings of unconverted PbI_2. Raman can clearly discriminate the presence of PbI_2 in a thin film. A chemical map allows the visualisation of the PbI_2 phase [9] (Fig 4.4b). This unconverted area is not active in light absorption and photocurrent generation.

4.3.2 Deposition by robotic dispenser

In order to overcome the issue of the inhomogeneous drop deposition, a simple dispensing system was adopted (Section 4.2). Initially, a continuous line of liquid was applied across a 1x10 cm^2 sample area. This approach led to a reorganisation of the liquid on top of the carbon layer, which produced a dot-like pattern of material, similar to the one of the single drop method [10] (Fig 4.5a). This uncontrolled infiltration led to an infiltration equivalent to the one obtained when using the drop method.

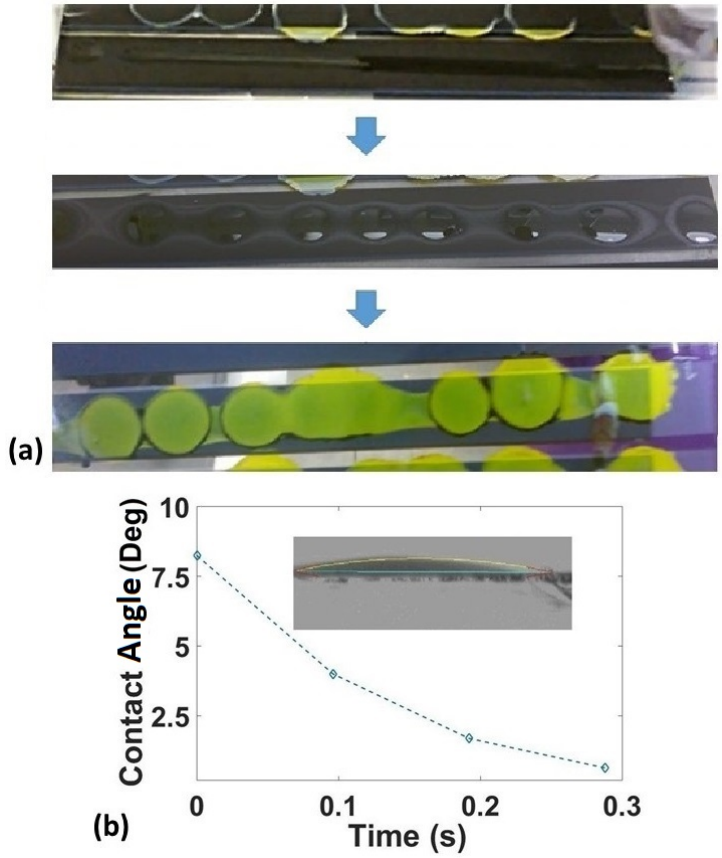

Figure 4.5: (a) Deposition of PbI_2 solution over a mesoporous stack, in sequence: a PbI_2 solution is deposited as continuous line over a carbon stripe; the liquid reorganises into drops; the characteristic dot-like pattern is shown from the back side through the glass. (b) Change in contact angle of a PbI_2 in DMF solution on a mesoporous carbon layer over time. Inset, the droplet on carbon at time 0.

Carbon is hydrophobic [11]. However, the contact angle measurement of a PbI_2 solution in DMF on carbon shows that the liquid is absorbed into the carbon in only 0.3 s, with an initial angle of only 8° (Fig 4.5b). This suggests that the surface energy of mesoporous carbon is high enough to rapidly absorb the solution and facilitate infiltration into the remaining layers. The reorganisation of the liquid observed in Fig 4.5 occurs because of the surface stabilisation of the polar solvent

on the hydrophobic layer when the absorption is too slow. This is the case when a large amount of solution needs to be accommodated into the porous stack in one go.

4.3.3 Infiltration by robotic mesh deposition

The RbM method utilises a robotic dispenser and a mesh. The robotic dispenser allows a quick and continuous supply of solution which spreads upon contact with the mesh (Fig 4.2). The homogeneity of the PbI_2 phase into the triple mesoscopic stack is much higher compared to the drop method. After conversion into MAPI, a yellow ring remains unconverted when using the drop method (Fig 4.6a), whereas no PbI_2 phase is observed when the RbM is utilised (Fig 4.6b). The RbM method allows greater control on the amount of solution deposited over the mesh. This facilitates a uniform infiltration across the entire surface and therefore, due to reduced pore clogging, an improved conversion to the MAPI phase during MAI immersion, both on small and large area samples (Fig 4.6).

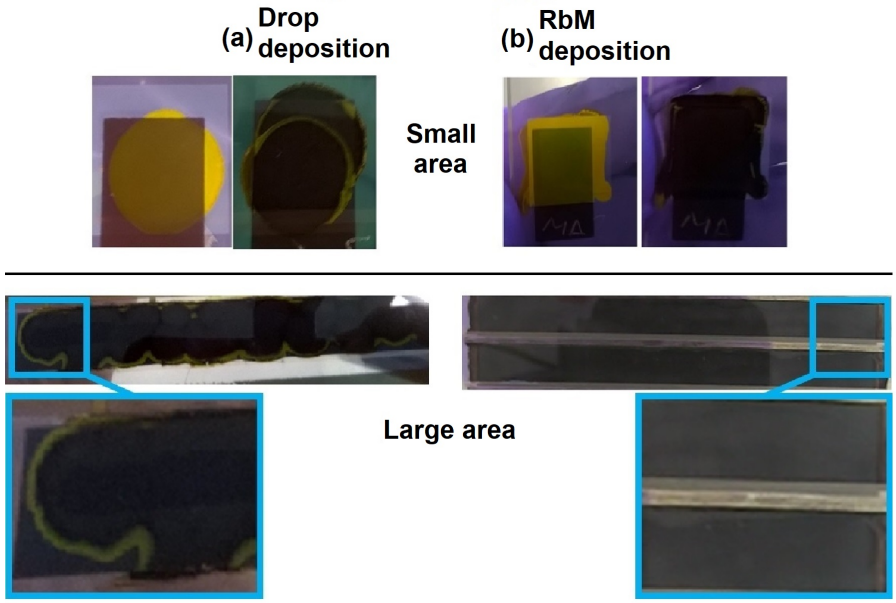

Figure 4.6: Devices prepared by (a) drop or (b) RbM deposition. On the top, small devices (1 cm^2) before and after conversion of PbI_2; at the bottom, long stripes (10 cm^2) after conversion with a blow-up of a selected area.

To demonstrate the higher control of the solution deposition over manual application, long devices (1 × 10 cm^2) were trialled. To confirm the composition and distribution of the PbI_2 phase, Raman spectroscopy was used to obtain a chemical map before the conversion into the MAPI phase (Fig 4.7). The PbI_2 signals in Raman, at around 100 nm Raman shift, are very intense and easy to detect, especially at 96 cm^{-1} [10; 12].

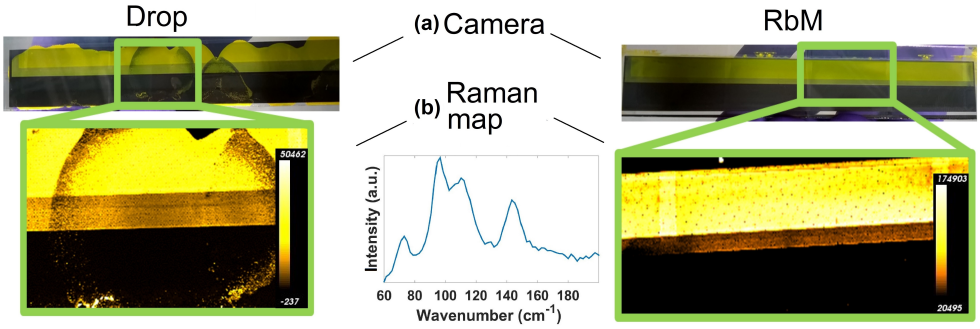

Figure 4.7: Comparison of 10 cm samples prepared by drop and RbM deposition prior to conversion into MAPI. (a) Visual appearance of samples obtained using a camera. (b) Raman map obtained at around 96 cm^{-1}. A measured PbI_2 Raman signal is also shown. The peaks at 73, 96, and 110 cm^{-1} belong to PbI_2, the peak at 144 cm^{-1} to TiO_2.

The peak at 144 cm^{-1} can be assigned to the anatase phase of TiO_2 (Section 3.3.1) and is visible because the measurements were performed through the conductive glass side. The Raman maps clearly show an increased homogeneity using the RbM method compared to the drop deposited samples. The sensitivity of the Raman system allows the visualisation of tiny dots in squared symmetry, corresponding to the knots of the mesh in RbM samples. The PbI_2 has homogeneously infiltrated into the stack, thus all the phase is expected to convert into MAPI after dipping in the MAI solution. XRD measurements were performed on

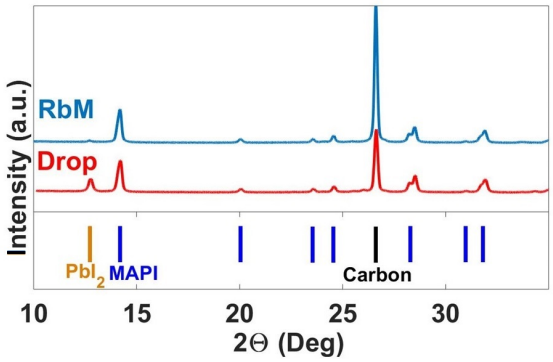

Figure 4.8: XRD of drop and RbM cells without the use of a collimator.

drop and RbM samples to detect the converted MAPI phase and any residue of the PbI_2 phase. The results show a clear tetragonal structure (space group I4/mcm) for both perovskite films, with the characteristic splitting of the peaks at around 28 ° and 31 ° [13].

The 14.2 ° peak can be used to monitor the MAPI phase, whereas the 12.7 ° peak refers to the PbI_2 phase [13; 14]. A more intense PbI_2 peak can be observed in drop samples compared to RbM (Fig 4.8). This is because the X-ray beam soaks a large area of the substrate and also detects the yellow PbI_2 phase that

does not convert due to the coffee stain effect. When a collimator is applied and a sharp X-ray beam reaches the substrate, it is possible to detect the amount of PbI_2 phase at the different regions of the substrates. This was tested on the same samples after dipping in MAI solution (Fig 4.9).

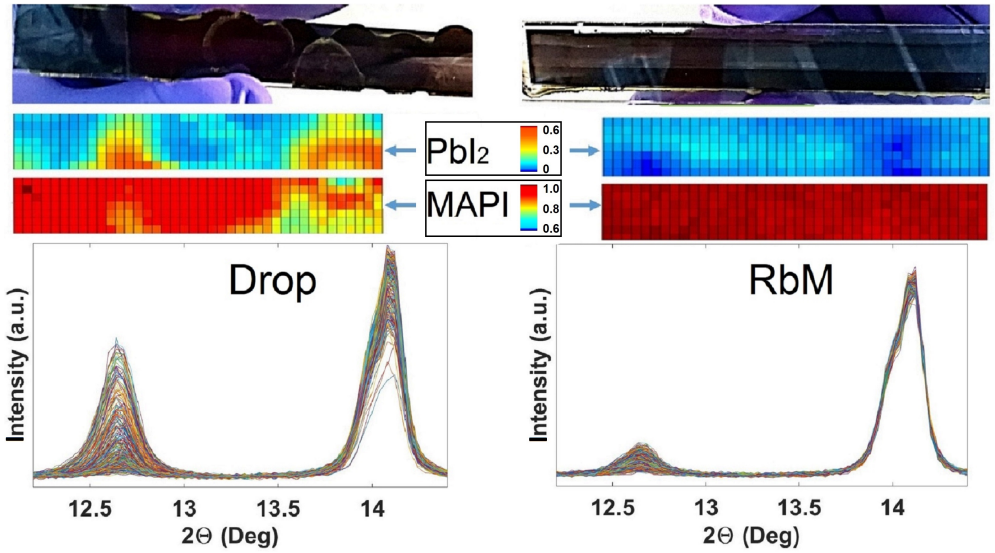

Figure 4.9: An XRD false colour map of 1 × 10 cm samples prepared by drop and RbM following conversion to MAPI. The relative intensities of the peaks at 12.7 ° and 14.2 ° were used to map the PbI_2 and MAPI phases respectively. Each square of the false colour map is 1 mm^2 of the sample area. A colour scale for each phase is shown. The diffractograms of each point are shown for drop and RbM samples.

XRD sampling shows the higher uniformity in RbM samples and the lower amount of PbI_2 phase compared to the sample prepared with the drop method. Due to the higher homogeneity of the RbM deposition, all the PbI_2 phase is converted into MAPI.

4.3.4 Robotic mesh: application on solar cells

Small devices (1 cm^2) were fabricated using the RbM method and compared to conventional devices obtained using the drop deposition method. The cells were masked reducing the illuminated portion to the dark, central, active area during JV test, so that the non-active yellow rings seen using the drop method would not affect the measurement. As per the description in the experimental Section 4.2, a lower concentration of PbI_2 was used for the RbM method to avoid clogging in the needle. This because the conventional 1 M solution is not stable at room temperature and there is no heating system in the robotic dispenser. Fig 4.10 shows the statistical performance of both drop and RbM cells, with average data shown in Table 4.1.

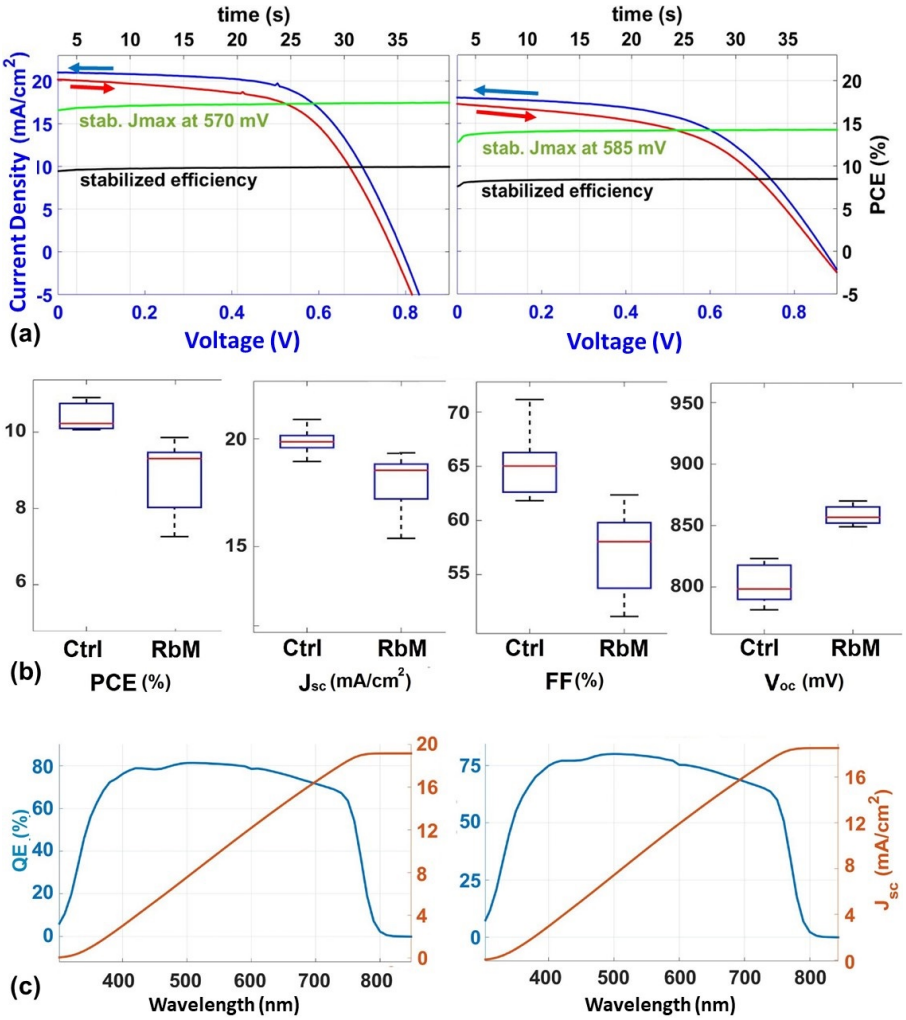

Figure 4.10: Solar cell performace of devices prepared by drop or RbM methods. (a) JV characteristic and relative stabilised current for representative devices. (b) Statistical representation of the PV parameters. (c) EQE and integrated current for representative devices.

Table 4.1: Averaged performance of drop and RbM cells. Statistic 5 substrates.

Cell type	Cell PCE (%)	Jsc (mA/cm^2)	FF(%)	Voc (mV)
drop, average	10.4	19.9	65.1	802
RbM, average	8.7	17.7	57.4	852

The data show that on average the mechanised RbM underperforms the manual drop method across all parameters associated with device measurement other than V_{oc}. This is likely due to the different PbI_2 concentration used in the two methods, which affects the PbI_2 crystallisation and thus the cell performance. Optimal performance is usually obtained from saturated (1.0 - 1.2 M) PbI_2 solutions [15], which dissolves at 70°C and then re-crystallise at room temperature. Since the temperature of the solution could not be controlled during the RbM deposition, a lower concentration of PbI_2 solution was used to avoid crystallisation in the needle of the dispenser. The drop cells were prepared using a saturated solution to enhance crystal formation. Further adjustments are ongoing to make the RbM system compatible with more concentrated PbI_2 inks. The need for an optimisation of the RbM method is also confirmed by the larger standard deviation of cell performance compared to drop cells. Important parameters to optimise are the dispensing pressure, the amount of liquid to deposit and the needle temperature during deposition. The temperature of the needle, in particular, can allow the deposition of concentrated solutions, the change in viscosity of the liquid and the modification of the evaporation rate of the solvent. The viscosity, density and surface tension of the low concentration ink at room temperature are respectively 1.79 mPa·s, 1.25 g/mL, and 30.3 nN/m.

Representative JV curves of devices and associated EQE for both methods are shown in Fig 4.10; best devices deliver comparable performance, and hysteresis and exhibit PCE values of 10.9% and 9.8% for drop and RbM cells, respectively. The method is, therefore, suitable for a quick deposition of perovskite in the C-PSC in a single passage.

The cells were further characterised by EIS. Nyquist plots obtained from the two types of cell are shown in Fig 4.11a. The spectra were fitted using a simple, R(RC), equivalent circuit to extract the resistance values of the high frequency process.

The impedance response of both cells exhibits a large high frequency arc, which varies strongly with light intensity. An additional feature is observed in the impedance spectra at lower frequencies, although it differs between the two

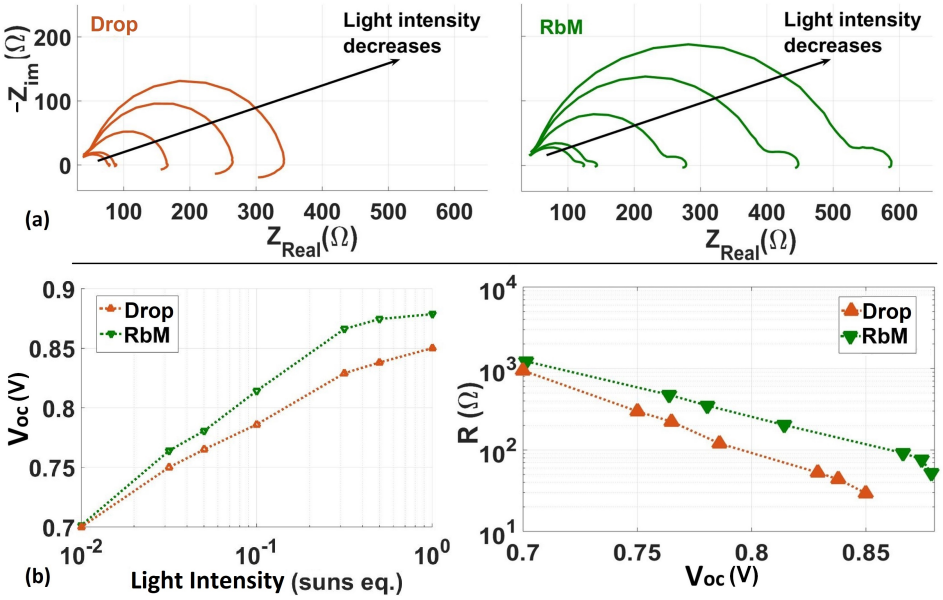

Figure 4.11: (a) EIS Nyquist plot at different light intensity of a representative cell per each deposition method. (b, left) Intensity dependence of the V_{oc}; (b, right) recombination resistance dependence of the applied voltage, V_{oc}.

devices. The response observed in the RbM cells is typical of many perovskite devices, in which the resistance increases at low frequency [16; 17]. Low-frequency features in the impedance response of perovskite solar cells have been ascribed to the impact of mobile ions in the perovskite layer on interfacial recombination [17]. In the drop cells, a negative loop is observed. The origins of this feature are not completely understood, although many hypotheses describe this as indicative of a process detrimental to performance. Yan and co-workers attributed the negative impedance loop to degradation of the perovskite [18]. A degradation product of MAPI is PbI_2 [19], which is present in the drop cells due to the incomplete conversion. This feature has also been attributed to poor charge injection, exacerbated by the presence of multiple interface layers [20]. It could be that the uncontrolled deposition of PbI_2 in the drop cells leads to inhomogeneous filling and an additional interface with the PbI_2 phase. Therefore, inferior contact at the interface between perovskite and TiO_2 may occur in the drop devices. The presence of unconverted PbI_2 may also act as a barrier to charge injection.

The resistance values obtained from the high frequency arcs scale linearly with V_{oc}, as seen in Fig 4.11b. This feature has previously been attributed to the recombination resistance (R_{rec}) in perovskite devices [21]. R_{rec} is inversely proportional to the recombination current: therefore a higher R_{rec} leads to a higher V_{oc}. The improvement in V_{oc} for the RbM cells, in comparison with the drop cells, is therefore a consequence of the higher R_{rec}. This may be explained by considering that

RbM allows a more uniform PbI_2 infiltration and, thus, better pore filling.

When analysing developments to existing cell manufacturing processes, it is vital to ensure that apparently good performance at 1 sun intensity is also consistent at lower light levels. As observed in Fig 4.11b, the V_{oc} of RbM cells is higher than the drop cells, over the range from 0.01 to 1 sun equivalent light intensity. The diode ideality factor, which gives an indication of the recombination processes occurring within a device, can be extracted from the slope of the V_{oc} - light intensity plots [21]. Both types of cell give ideality factors between 1 and 2, indicating that the recombination is mainly trap-assisted [22].

Stability tests in air and ambient conditions, under continuous illumination from white LEDs at 0.5 and 1 equivalent sun were performed on both drop and RbM non-encapsulated cells (Fig 4.12). The degradation is severe under 1 equivalent sun, as expected for MAPI C-PSCs [11]. However, at 0.5 equivalent sun the devices are stable for over 160 h.

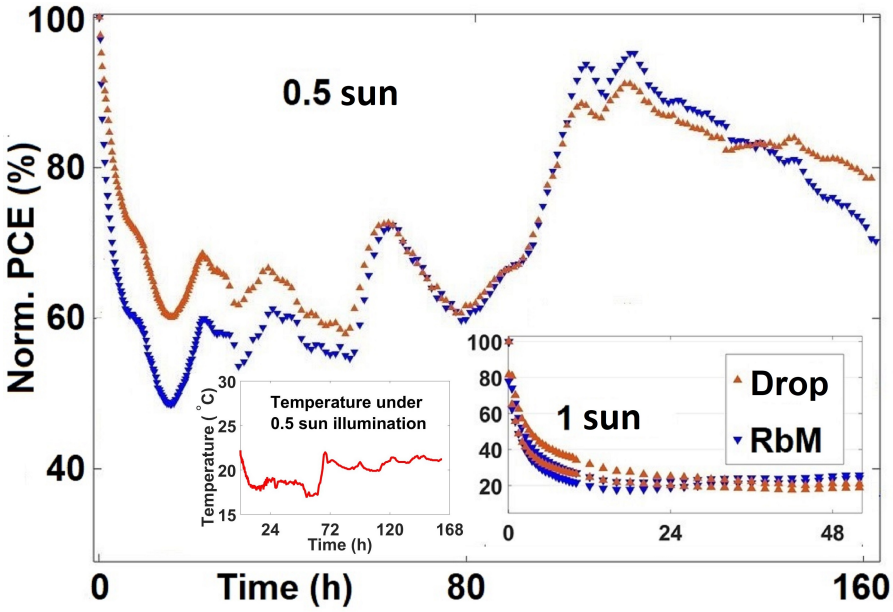

Figure 4.12: Normalised PCE of both drop and RbM cells over time during continuous illumination from white LED, at 0.5 and 1 equivalent sun; temperature profile under 0.5 sun during the test. At 0.5 sun, the drop in PCE is not as severe as under 1 sun and a nearly complete recovery is observed after few days. The PCE profile under 0.5 sun follows the temperature profile.

Interestingly, at 0.5 equivalent sun, the performance decreases dramatically in the first few hours, but an unexpected recovery occurs after a day of continuous exposure. Even a complete recovery is observed after a few days of testing. The decrease and recover of PCE is similar in both types of infiltration methods. This result confirms that RbM deposition does not affect the C-PSC devices in terms

of performance and stability. Having halved the light-induced stress, the observed fluctuations can likely be ascribed to environmental parameters, such as temperature or humidity. The fluctuations of temperature, which were recorded with a thermocouple, follow the PCE profile over time. The relative humidity, which could not be measured with our set-up, is also a function of the temperature and is expected to follow a similar trend when the humidity of the room is constant. The results call for further investigation on the thermal and humidity stability of these devices.

4.4 Conclusion

A new mechanised method to deposit solutions over a large area has been presented. This method was tested on the fully printable C-PSCs, and shows improved infiltration uniformity and control compared to the more common drop deposition method, leading to a PCE as high as 9.8% on a 1 cm^2 device. JV, EQE, EIS, and stability measurements show that the RbM method achieves similar performance to the drop cells. A chemical map of PbI_2 film in the triple mesoscopic stack was measured by Raman spectroscopy and, together with XRD sampling, confirmed the superior homogeneity that can be achieved with the RbM. Some important parameters that control the deposition are the dispensing pressure, the amount of liquid to deposit, the mesh size, and the temperature of the needle.

Using the RbM method, large area deposition can be achieved now. The up-scaling of the device is now viable through a simple, quick, and highly controlled deposition method. In Chapter 5 a provisional attempt to scale-up C-PSC will be shown. The impact of the design on the PCE will be investigated and the issues related to the up-scaling of the C-PSC will be tackled.

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Chapter 5

Module design and development

So far, this thesis has demonstrated that high performance AVA-MAPI C-PSC with superior stability compared to MAPI can be successfully fabricated in a single cell design. Moreover, the issues related to the manual infiltration can be overcome by using the RbM deposition. This opens up an opportunity for the design and development of large scale devices.

Conventional solar modules can be prepared in small (up to 10 × 10 cm^2) or large area substrates (more than 10 × 10 cm^2). Small area modules can be connected externally either in parallel or in series, to make large panels, as commonly done for Si SC. With large area modules, by contrast, the interconnects are integrated on the same substrate while the device is being fabricated. This second approach reduces the complexity of the process and the need for external connections. Ideally, a solar panel could be simply printed without any external connection.

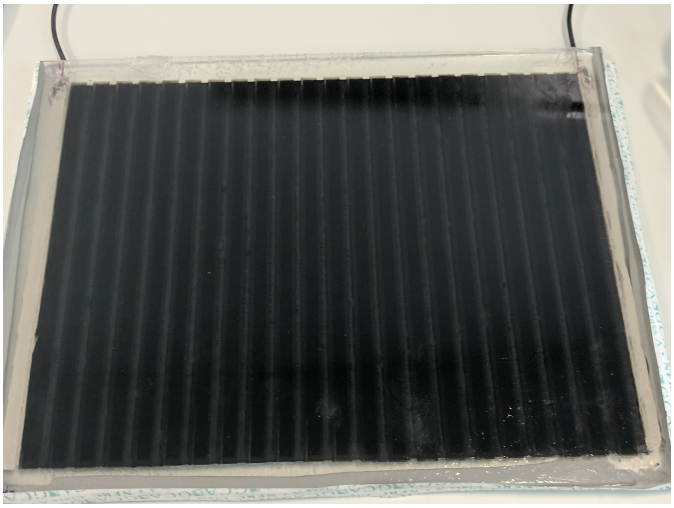


Figure 5.1: Module with 198 cm^2 active area.

In this chapter, small-area and large-area modules, with unprecedented 198 cm^2 active area, will be presented. For large area modules, PCE of more than 6 % was measured under 1 sun illumination (Fig 5.1). The issues related to the up-scaling of C-PSC on large substrates will be discussed.

5.1 Introduction

The C-PSC is fabricated using a screen printing method, which presents a simple method for patterning and registering layers. In this method, layers of $mTiO_2$, $mZrO_2$ and carbon can be printed in stripes and registered one over the other. The proper registration of the layers allows the creation of interconnects, with the purpose of allowing the overlap of the top electrode in one cell with the bottom in the subsequent cell in series on the same substrate (Fig 5.2).

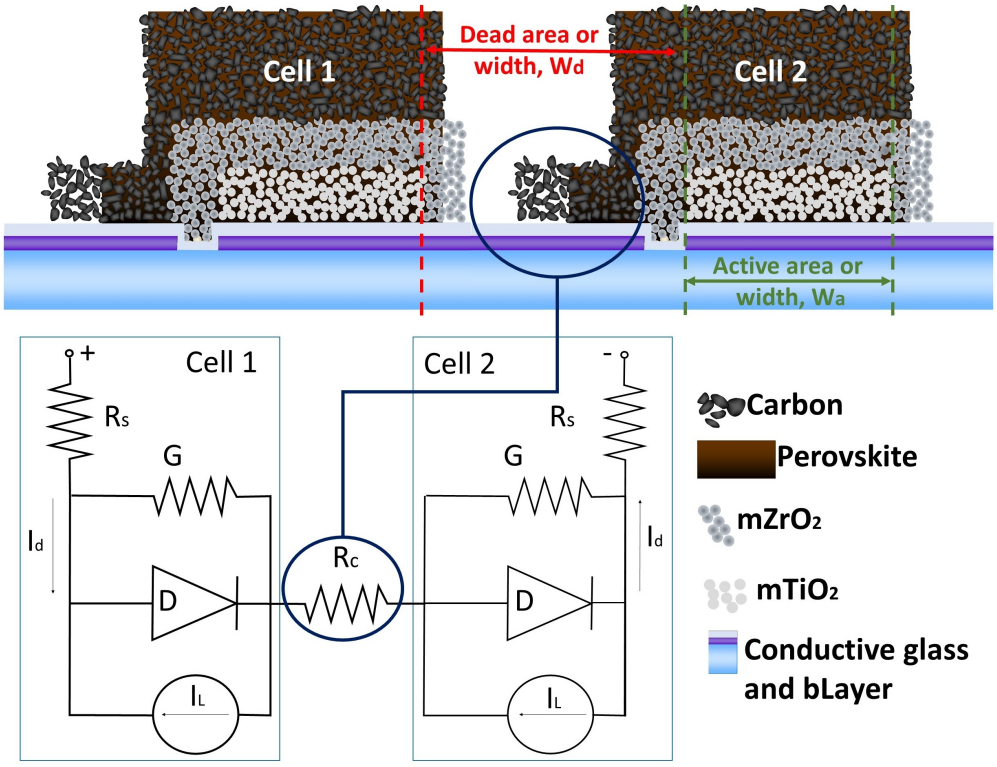


Figure 5.2: Schematic representation of a two-cell module prepared with the registration method. The active width (W_a) and the dead width (W_d) are shown. A simplified equivalent circuit of the two-cell module is shown with the contact resistance (R_c) at the FTO/carbon interface between the cells.

This approach was reported for C-PSC modules with around 10 - 11 % PCE on 10 × 10 cm^2 substrates, with different coverage, i.e. active areas ranging from 47.6 [1; 2] to 70 cm^2 [3]. If it is considered that modules with comparable active areas but evaporated metal contacts were reported to yield respectively 12.6 %

PCE on 50.6 cm^2 (with $mTiO_2$, spiro-OMeTAD, and Au) [4], 8.7 % PCE on 60 cm^2 (with PEDOT:PSS, PCBM and Au) [5] and 4.3 % PCE on 100 cm^2 (with $mTiO_2$, spiro-OMeTAD and Au) [6], the results that have been achieved with the C-PSC are remarkable. Higher performance has been reported for modules with smaller active area, e.g. 16 % PCE over 16.29 cm^2 [7].

The issues for up-scaling the C-PSC are different than the ones faced when using other architectures.

- First, the lower conductivity of porous carbon compared to compact metal contacts can increase the R_c between the cells in contact. This will require a relatively large space to ensure sufficient contact area, which, consequently, will affect the g-FF (geometric fill factor, Section 1.6.3).

- Second, the deposition of layers that require high temperature treatment can cause thermal instability of the rigid glass substrate over large area. This issue can be critical when an open hot plate is utilised, instead of a closed oven or furnace, where the temperature is homogeneous across the environment. This is the case for the spraying of the bLayer, where an open hot plate is required to allow the deposition of the TiO_2 precursor onto the substrate. At temperatures as high as 300 °C, as per the standard procedure required for the bLayer, the substrate may bend, or even crack in the worst scenario. Bending of the substrate can affect the printing of successive layers, by causing a variation in gap height across the screen and substrate, leading to inhomogeneity in the film thickness (Section 1.7). Any change in the layer thickness across the substrate can affect the performance of individual cells constituting the module. Therefore, a lower processing temperature is needed for depositing the bLayer, to avoid deformation or even cracking of the glass.

In this chapter, the module design and manufacture were developed in accordance with the characteristics of the C-PSC. A mathematical approach was used to estimate the optimal W_a. The effect of the contact area was studied on real modules, which were prepared with different FTO/carbon contacts. The effect of the spraying temperature on the bLayer was studied, showing a correlation between temperature and crystallinity regardless of the common final annealing temperature of 550 °C. The low temperature deposition of the bLayer was tested on single cells. Finally, it was demonstrated that 198 cm^2 active area modules can be manufactured by screen printing, via registration of the overlapping layers. An unexpected performance improvement of unencapsulated modules within storage,

likely related to the effect of humidity, over time is also shown. This led to a remarkable 6.6 % PCE two months after fabrication.

5.2 Experimental

The fabrication method to prepare the modules follows the method reported in Section 2.2.3 for the AVA-MAPI C-PSC. The expected performance on single cells is shown in Section 3.3.3.

In order to make the method compatible to a large area device, the use of the Petri dish during the annealing step was omitted. For the large area 198 cm^2 modules:

- In case of the patterned bLayer, prior to its spraying, the substrates were completely covered with Kapton tape at the interconnection areas. The tape was then removed afterwards. The patterning was tested to observe the influence of the carbon layer directly contacting the FTO without compact TiO_2 in between.
- The bLayer was deposited on a hot plate at 180 °C, instead of 300 °C as per the baseline. 25 passes were performed, waiting 40 s between sprays, and not 10 s as per the baseline.
- After screen printing, each layer was dried on a hot plate and then annealed in a muffle furnace, which offers a closed environment with homogeneous heat all over the substrate.

The RbM method was used to infiltrate the perovskite solution in all the modules for the AVA-MAPI perovskite in 1-step deposition (Chapter 4). The characterisation was carried out with the equipment described in Section 2.3.

5.3 Results and discussion

5.3.1 Optimal active area width

The optimal W_a is a compromise between conductivity of the electrodes and g-FF. The resistance of the electrodes and the g-FF depend on both W_a and W_d. A simple approach to obtain a qualitative prediction about the optimal W_a is to use the diode equation (Eq 1.5), adding a factor that models the geometry of the module. A possible equation can be found in reference [8], i.e.

$$R_{El} = R_{sq} \cdot \frac{W_a + W_d}{H} \tag{5.1}$$

where R_{El} is the resistance of the electrode, R_{sq} is the sheet resistance of the most resistive electrode, and H is the cell length (Fig 5.3).

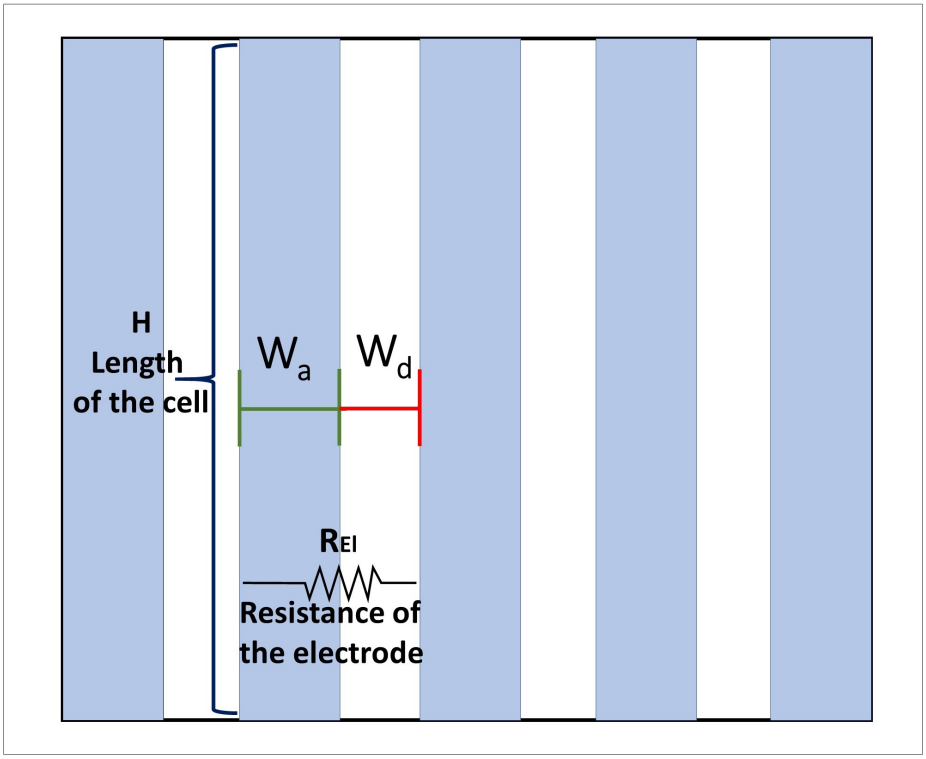


Figure 5.3: Schematic representation of a generic module with 5 cells, whose width is W_a and the distance, or dead width, is W_d. The length of the cells is H and the resistance of path distance $W_a + W_d$ is R_{El}.

Eq 5.1 gives only an approximation of the effect of the geometry on the resistance, because the charge generation occurs all over the active area and an integral would be more accurate in this instance. Moreover, only the most resistive electrode is taken into account. However, the error can be considered acceptable, as the model was reported to be approximately valid for short charge transfer distance of few mm [8].

In C-PSC, carbon is more resistive that FTO. The FTO that is utilised in this work is TEC 7, with a R_{sq} of around 7 Ω_{sq} (Section 2.2.1), whereas carbon is 14.5 Ω_{sq} for a thickness of 15 μm (Section 3.3.1). If R_{El} is used in substitution of R_s in the diode equation Eq 1.5, different geometrical scenarios can be modelled (Eq 5.2, Fig 5.4).

$$J = J_o \left[e^{\frac{q}{AKT}(V - J \cdot (R_i + R_{El}))} - 1 \right] + \frac{V - J(R_i + R_{El})}{G} - J_L \qquad (5.2)$$

where q, K, T, V, J, G, A, J_o, and J_L are the constants and parameters of the

diode equation Eq 1.5. An internal resistance R_i is included in Eq 5.2, to account for the conduction that is not related to the geometry, for example the charge transfer through the layer or the contacts between cells.

The PCE of a single cell in a module is theoretically the same as that of the entire module. For series connected modules, the V_{oc} increases with n_c, but J_{sc} is inversely proportional to n_c because I_{sc} is constant. Therefore, the PCE should not be affected by n_c and the PCE of the single cell is representative of the entire device (Eq 5.3).

$$\begin{aligned} PCE_{singC} &= \frac{FF \cdot V_{oc} \cdot J_{sc}}{P_{in}} \\ PCE_{mod} &= \frac{FF}{P_{in}} \cdot \frac{J_{sc}}{n_c} \cdot V_{oc} \cdot n_c = PCE_{singC} \end{aligned} \tag{5.3}$$

where PCE_{singC} is the PCE of a single cell, and PCE_{mod} is the PCE of the module.

In experimental devices, the PCE of the module might be different to that of a single cell because, for example, the current of the module is limited by the current of the poorest single cell (Section 1.6.2) or the contact between cells is not optimised. However, it is possible to consider $PCE_{singC} \simeq PCE_{mod}$ to obtain theoretical profiles that can be used to understand the effect of the geometry on the module performance and g-FF.

Fig 5.4 shows the effect of W_a on the module performance at different scenarios according to Eq 5.2. An increase in W_a negatively affects the PCE of the cell due to an increase of R_{El}. The straight line in Fig 5.4a shows the effect of W_a on the PCE due to the increase of R_{El} (Eq 5.2). If the g-FF is not taken into account, W_a should be as small as possible in order to minimise R_s. However, the power generation of the module (green curve) goes to zero when W_a is much smaller than W_d, because, relatively to the aperture area, the active area is only a small portion. When W_a decreases, the g-FF is also reduced. In other words, W_a increases the overall gain in PCE $\times$ g-FF until the loss due to R_{El} plays a predominant role.

When the plot of PCE $\times$ g-FF over W_a is normalised to the ideal case of $W_a \rightarrow 0$, a graphical representation of the losses due to R_s and g-FF is obtained (Fig 5.4a). For example, when the optimal W_a is considered, i.e. 5.9 mm, it is simply observed that the loss due to R_{El} and the g-FF are 12.5 % and 12.7 % respectively. The normalised plot as in Fig 5.4a is to be used for an immediate evaluation of the contribution of the losses to the module design.

W_d also plays an important role in the design. In order to consider different

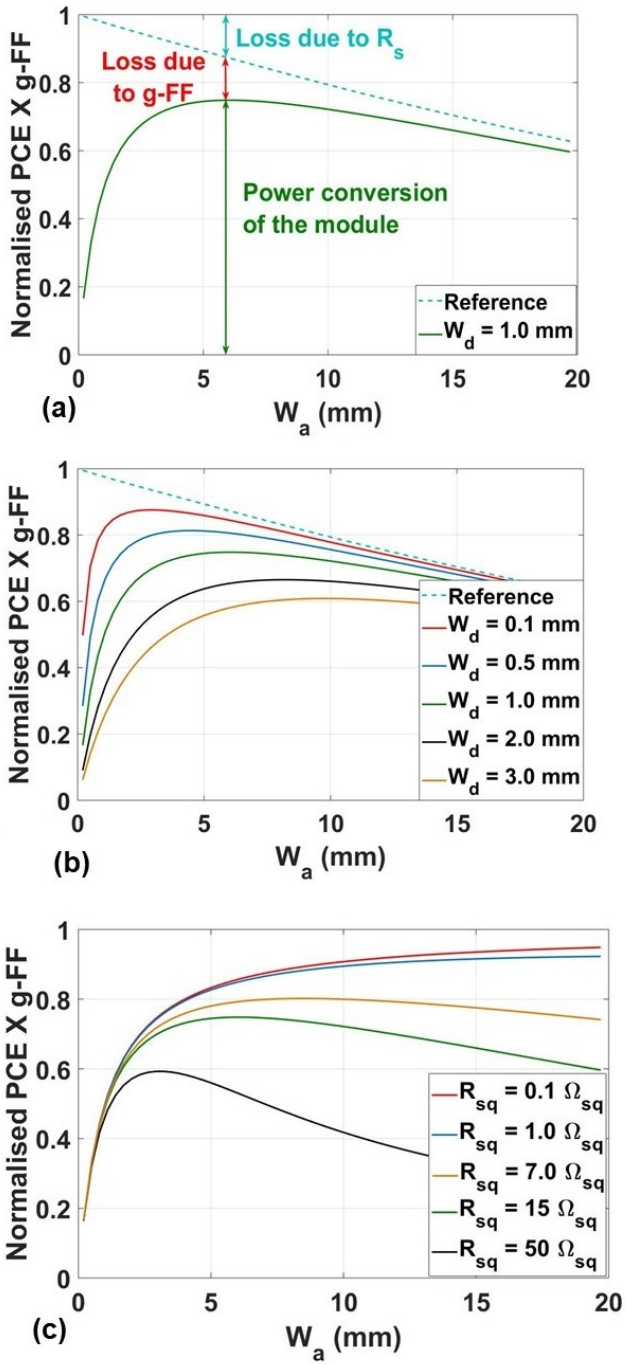


Figure 5.4: Predicted behaviour of a single cell connected in series in module design, with active stripe width W_a, distance to the next cell of W_d. Diode parameters from a device of around 12 % PCE with W_a = 1 mm and H = 20 mm are: $J_o = 10^{-10}$ mA/cm^2, J_L = 20 mA/cm^2, A = 1.5, R_{sq} = 15 Ω, R_i =5 Ω and G = 2000 Ω. The normalisation is from the PCE of the device for a theoretical W_a = 0 mm. (a) Graphic representation of the losses in a large area module. The reference shows the PCE of a single cell affected by a resistance due to the distance of W_a and W_d = 0. (b) The effect of W_d when R_{sq} = 15 Ω_{sq}. (c) The effect of R_{sq} when W_d is 1 mm. The green curve represents always the same scenario, i.e. W_d = 1 mm and R_{sq} = 15 Ω. Calculation performed with Matlab.

scenarios, the effect of W_d when it ranges between 0.1 and 3.0 mm was investigated (Fig 5.4b). When W_d increases, the optimal W_a increases as well, but generally the performance of the module is strongly affected. For example:

When $W_d = 0.1$ mm, the optimum W_a is nearly 3 mm.
For $W_d = 0.1$ mm and $W_a = 3$ mm, the g-FF is 96.8 %. The device shows a PCE × g-FF of around 0.9 from the normalised PCE of the original small single cell.

When $W_d = 0.5$ mm, the optimal W_a is about 4.5 mm.
For $W_d = 0.5$ mm and $W_a = 4.5$ mm, the g-FF is 90.0 %. The device shows a PCE × g-FF of around 0.8 from the normalised PCE of the original small single cell.

When $W_d = 3.0$ mm, the optimal W_a is about 10 mm.
For $W_d = 3.0$ mm and $W_a = 10$ mm, the g-FF is 76.9 %. The device shows a PCE × g-FF of around 0.6 from the normalised PCE of the original small single cell.

It is clear, now, that W_d negatively affects both PCE and g-FF, whereas high W_a negatively affects only the PCE but improves the g-FF. When the g-FF is not compromised too much by large W_d, a narrow W_a can be applied to achieve both high PCE and g-FF. Alternatively, for large W_d, a large W_a must be accepted in order to minimise the loss in PCE due to the lack of coverage of the substrate with active area. This result shows the importance of the minimisation of W_d on the module design. However, W_d may need to be relatively large due to:

- The limit of the accuracy that the interconnection method can achieve. Larger W_d can be more forgiving in case of misalignment.
- The size of the interconnects. W_d hosts the interconnects that ensure the proper contact between electrodes of adjacent cells. The R_c between the electrodes must be as low as possible and the size of the interconnects may need to be relatively large to ensure enough space for an adequate contact area.

It should be noted that the gain in power conversion when W_a is large can be tiny even in the case of a large W_d. When $W_d = 3$ mm, for example, the yellow curve is approximately a flat line with a negligible gain in power conversion between the optimal W_a (∼10 mm) and the narrower $W_a = 5$ mm. Increasing

of the g-FF by widening the W_a is not a winning strategy for electrodes with $R_{sq} \sim 15\ \Omega_{sq}$.

The R_{sq} affects the optimum W_a and g-FF of a device (Fig 5.4c). When R_{sq} is negligible, the device can be expected to be as large as possible without suffering too much from parasitic resistances. In this case, a single cell can theoretically be scaled-up infinitely to achieve large single cells without interconnects, i.e. 100 % g-FF. Interconnects for series-connected modules can be still be included for high voltage applications. When R_{sq} is not negligible, for example 0.1 or 1 Ω, the optimal W_a is larger than the calculated range in Fig 5.4c, i.e. above 20 mm. With higher R_{sq} the optimal W_a is in the order of mm. It is important to observe that the need to make stripe-shaped solar cells in module design comes from the need to overcome the limitations of the R_{sq} and let the charge be transferred through the narrow width of the long cells. This limitation is more pronounced when R_{sq} is very high, i.e. 50 Ω_{sq}. In this case, the optimal W_a is very small even with $W_d = 1$ mm (Fig 5.4c) in order to enhance the charge collection.

The limitations of the model do not allow a quantitative evaluation of the design. A limitation of the model based on Eq 5.1 is the lack of an integral equation that can model charge extraction in 2D like Poisson's equation [9]. The model also does not include the effect of the R_c in the interconnects [10]. However, a qualitative observation of the different trends can be given to understand the impact of the different parameters on the design. Moreover, as stated also above, the use of a normalisation method is useful to generalise the observation for modules with different numbers of interconnections and evaluate graphically the losses due to R_s or g-FF.

In 2016, Galagan et al. [9] used COMSOL to model the effect of R_{sq} on W_a. With a more accurate model based on 2D Poisson's equation, the same trend described above is observed. The optimum W_a for a device starting from 14.76 % for 9 mm^2 active area, 0.32 mm W_d and 10 Ω_{sq} R_{sq}, is 5 mm according to the article [9]. The result is not dissimilar to the simple model based on Eq 5.1 and gives confidence that the calculation can be utilised in the range of values that were studied here. Because a variation in W_a of ± 1 mm does not significantly affect the gain in PCE × g-FF of the modules when $R_{sq} = 15\ \Omega_{sq}$, a fixed $W_a = 5$ mm for all modules was adopted in this work.

5.3.2 Optimal contact area

The generated charge carriers are transferred through the electrodes and the interconnects. The interconnects are contacts between FTO and carbon in the C-PSC architecture, and can be more or less resistive according to:

- the conductivity of the employed materials;
- the contact area.

The actual contact area between the electrodes is affected by both the morphology of the electrodes and the design, i.e.:

- the roughness of the layers;
- the presence of voids in the porous layer;
- the geometrical space that is given in the design, or geometrical contact area, defined as the rectangular area where the contact is hosted, i.e the width by the length of the interconnect.

Excluding the case of compact and smooth layers such as evaporated metals, in C-PSC modules the contact area is not equal to the geometrical one (Fig 5.5). Because this work does not focus on the optimisation of the morphology of the electrodes, the geometrical space will be referred to as contact area here.

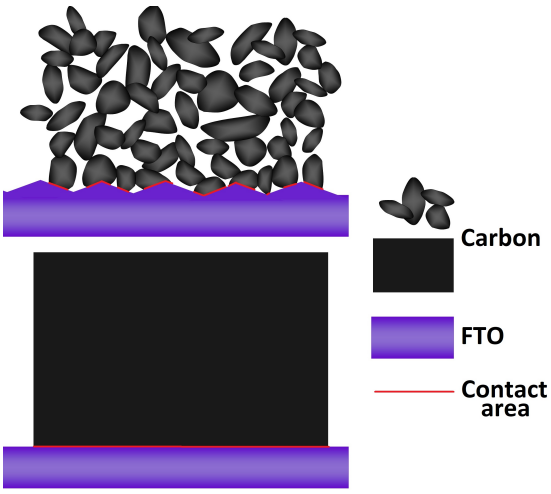


Figure 5.5: Interconnects for C-PSC modules. Above, a realistic scenario for FTO/carbon contact showing the roughness of the FTO and the porosity of the carbon layers. Below, ideal scenario with compact and smooth layers.

The optimal contact area is a compromise between the minimisation of R_c, i.e. large area, and the minimisation of R_s, i.e. small area, in order to enhance the

PCE of the module. Moreover, the optimal contact area that maximises the PCE affects the g-FF, due to the occupied space. Therefore, it is possible to define a second optimal contact area that optimises the PCE × g-FF. In this chapter, the effect of the contact area on the PCE of the modules will be investigated, whereas the optimisation of the PCE × g-FF will be investigated in Chapter 6.

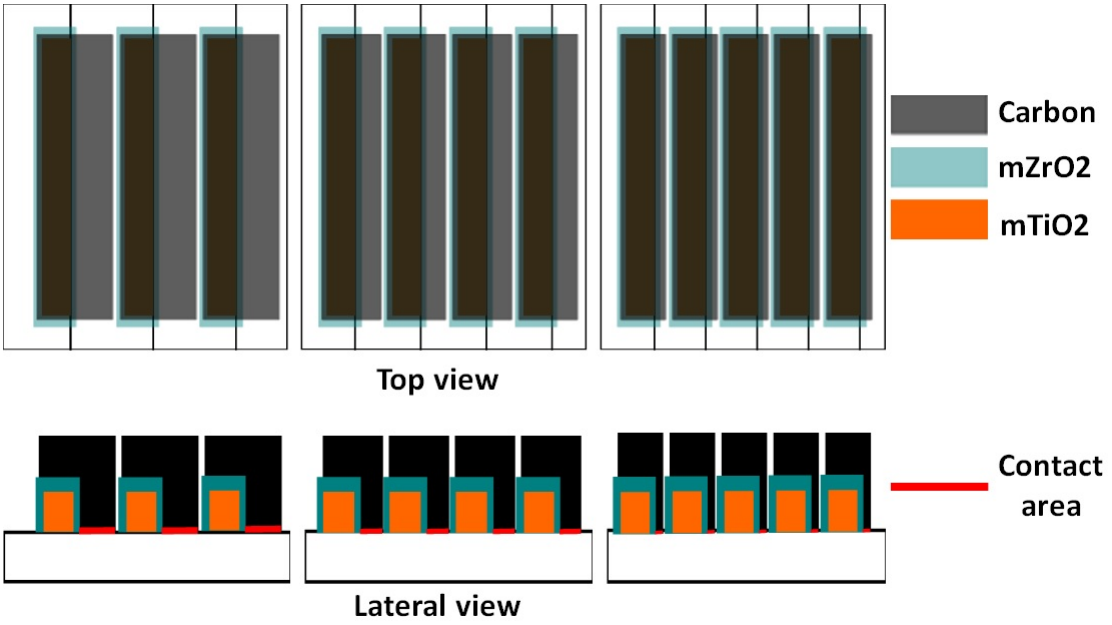


Figure 5.6: Design of three different modules with the same W_a (5 mm) but different contact area. The contact width is varied, i.e. 6.5 mm, 3.5 mm and 1 mm, and the length is constant. The number of cells changes to compare modules of the same size and same distance between the first and the last electrode. The number of cells varies from 3, 4 and 5 respectively. Above, top view; below, lateral view.

Changes in the contact area directly affect the PCE. The contact area width is typically in the range of 200 μm [11] or less [12] when metal contacts are utilised, but carbon is much less conductive than metal and its porous nature reduces the actual contact with FTO. The conductivity of the layer changes with thickness. In particular, the R_{sq} decreases with thicker layers because the lateral conductivity improves, but, by contrast, the resistance in the vertical direction becomes higher with the thickness. The vertical direction is the direction where the current flows at the interconnects. Furthermore, it should not be forgotten that the thickness negatively affects the perovskite infiltration, thus also affecting the pore filling in the stack [13]. Increasing the thickness of the already thick carbon layer to favour the lateral conductivity, therefore, is not a good strategy to reduce the R_c.

An approach to improve the R_c is the use of large contact areas. This approach, however, limits the minimisation of W_d. A compromise between the minimisation of R_c and W_d is required. In order to have an indication about the optimum contact

area, modules with different designs were prepared. Three different designs with contact area of 1 mm, 3.5 mm and even 6.5 mm were tested for mini-modules (Fig 5.6). The size of the single cell of a mini-module is 3 cm^2 ($W_a = 5$ mm). The extreme case of 6.5 mm is to ensure a scenario where the contact is so large that the increase of resistance between cells starts to play a predominant role. In order to compare devices with the same size and keep the same distance between the first and the last electrode, the n_c had to vary according to the available space. Therefore, modules with contact area of 1 mm could accommodate 5 cells, 3.5 mm 4 cells and 6.5 mm 3 cells.

The IV characteristic of the modules show that the performance of the devices depends strongly on the contact resistance (Fig 5.7). The PCE increases by around 3 times when passing from 1 to 3.5 mm contact area, in spite of the larger W_d between cells. However, the PCE decreases enormously with 6.5 cm contact area. There is likely no or very little benefit in R_c between 3.5 and 6.5 mm, whereas the increase of R_s due to the larger W_d plays a dominant role.

Min-J_{sc} and FF are optimised in the 3.5 mm design, whereas 1 and 6.5 mm designs suffer from either Min-J_{sc} and FF. When the current is high, the FF is low and vice-versa. This is a sign of poor conductivity in the device, with a large effect from the iR drop (Section 1.5.3).

The Av-V_{oc} is roughly unaffected by the design. This is a sign that the significant effect in this set of experiment is mainly due to the R_s, which includes both R_c and R_{El} (Section 1.5).

It was observed that the optimum contact area is around 3.5 mm, resulting in modules whose PCE was much higher compared to modules with 1 mm contact. This result is remarkable considering that the 3.5 mm contact requires a much higher W_d compared to 1 mm, so the effect of R_s is massively compensated by the lower R_c. A more detailed experiment was necessary in order to further define the optimal contact area, and this will be shown in Chapter 6. At this stage, it was determined that a large contact is necessary in spite of the large W_d resulting. This information was used to make the 198 cm^2 modules shown later in this chapter (Section 5.3.4).

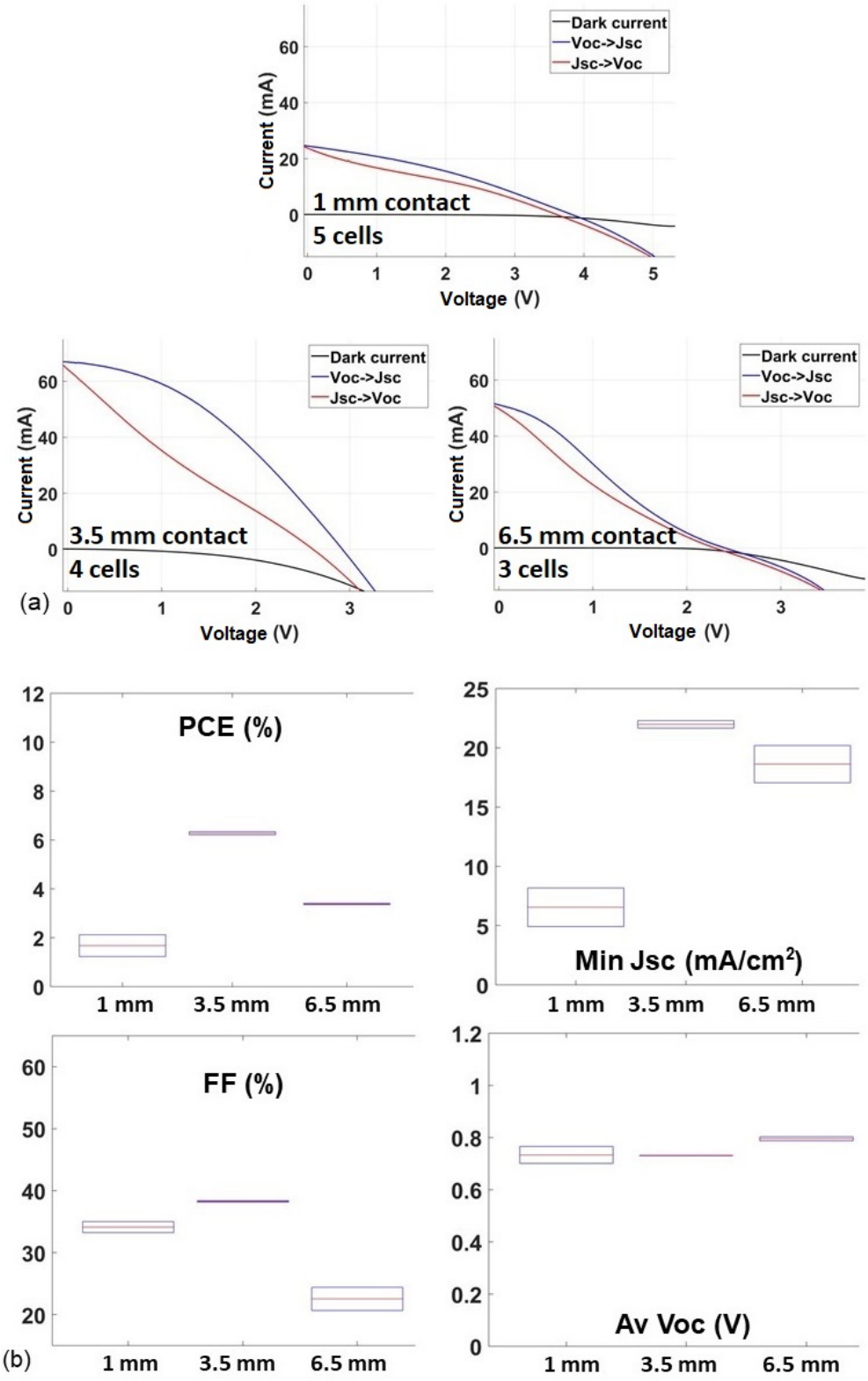


Figure 5.7: PV characteristics of mini-modules with single cells of 3 cm^2. (a) IV curves. (b) standard deviation of PV parameters. Statistic of 2 modules per type.

5.3.3 Low temperature compact TiO_2

An important issue that needs to be addressed before the fabrication of large area modules, is the deposition of the bLayer. According to the standard procedure, the bLayer is sprayed on a hot plate at 300 °C and then fired at 550 °C after the deposition of the $mTiO_2$ (Section 2.2.1). However, most hot plates, including those in our laboratories, do not allow a homogeneous heating over a large area. This inhomogeneous heating can thermally stress the glass, with consequent substrate bending or even cracking. The need to overcome this technical issue, however, led to an unexpected observation in the compact TiO_2 film formation.

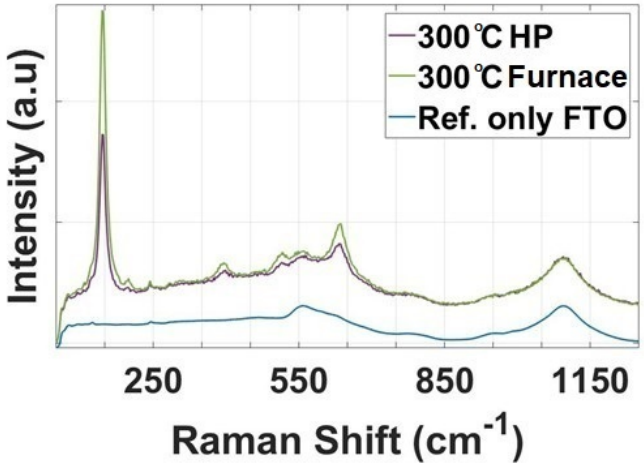


Figure 5.8: Raman data to compare different bLayers that were sprayed at 300 °C and then fired either on a hot plate or in a muffle furnace at 550 °C for 30 minutes.

The issue of the substrate heating can be split in two parts: the spray deposition at 300 °C and the subsequent heating at 550 °C. Due to the difficulty of heating the substrates homogeneously at high temperature on hot plates, the second step at 550 °C was carried out in a muffle furnace, where the closed environment could give a more homogeneous heating all over the glass substrate. When the bLayer is annealed in a furnace, the crystallinity increases, as revealed by Raman in Fig 5.8. The crystalline anatase phase that generates the striking peak at around 144 cm^{-1} Raman shift [14; 15] is present in both samples after the firing either on the hot plate or in furnace. However, the crystal phase is much more abundant when the bLayer is annealed in the furnace. This different crystallisation that occurs in the internal chamber of the furnace can be the result of the uniform heat. On the hot plate the heat comes from the bottom, leaving the surface of the substrate slightly colder than the measured temperature. The use of the furnace, in conclusion, should not negatively affect the blocking properties of the bLayer

and was employed to prepare large modules.

The spray step at high temperature must be done on the hot plate due to the need to have an open space to operate. However, the glass can easily bend or crack in such a condition. To overcome this, the spray step needs to be done at a lower temperature. The bLayer was, therefore, sprayed at 150 °C. Two observations need to be mentioned:

- A longer time between sprays must be given in order to let the solvent to evaporate.
- After the spray of the TAA solution on FTO glass, no anatase phase is observed even after annealing at 550 °C in the furnace (Fig 5.8b).

The lack of crystallinity that was observed when the bLayer was deposited at a lower temperature than the standard one is unexpected, because the amorphous TiO_2 that resulted from the sol-gel reaction during the spraying deposition should crystallise into the anatase phase at between 400 and 480 °C [16]. It might be that the spraying at low temperature does not give enough time for the precursors to cross link in the film due to a high energy barrier. The final annealing process at 550 °C should give enough thermal energy to allow a proper reorganisation of the crystals. However, the TiO_x groups are not connected in all four directions, resulting in an amorphous phase even after high temperature firing.

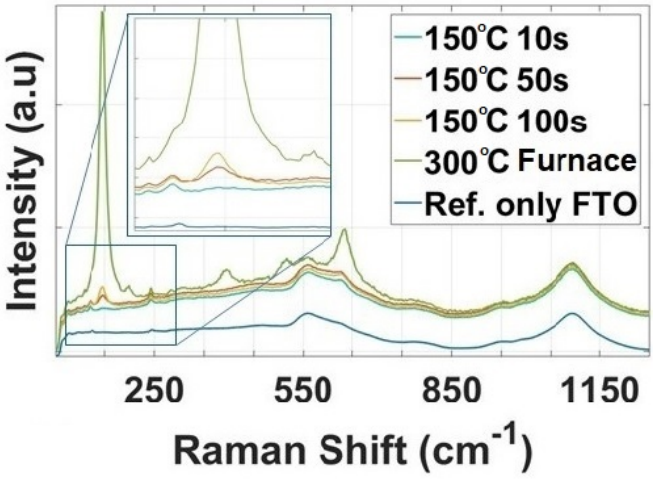


Figure 5.9: Raman data to compare different bLayers sprayed at 150 °C with different waiting time between sprays. All the layers were then fired at 550 °C in a muffle furnace prior analysis.

In order to test the kinetic effect in the reaction, films of TiO_2 with different waiting time between sprays, 10 s, 50 s and 100 s, were prepared. As expected, the TiO_2 phase starts appearing with more time between sprays (Fig 5.9). With

longer waiting time, the system has better kinetics to cross-link the TiO_x groups and overcome the energy barrier during the chemical reaction. More precisely, it is proposed that the system requires longer time to ensure a proper cross linking between the molecule for the 4 chemical sites of the $Ti(\text{-}O\text{-})_4$ due to kinetic effects. Without this additional time, some sites remain unlinked, forming a Ti-O-ligands bond, i.e. with either isopropoxide or acetylacetonate. If the $Ti(\text{-}O\text{-})_4$ is not fully linked with another Ti^{IV}, the annealing at 550 °C cannot result in a full crystallization, but the phase remains instead amorphous or partially amorphous. The organic ligands are expected to burn to form Ti-O-H bond. This speculation could explain the lack of crystal formation even after the annealing at 550 °C.

These results can raise questions about the effectiveness of the blocking properties of the low temperature process. Amorphous bLayer was reported to be successfully used to prepare PSC [17], but the performance of C-PSC single cells with the low temperature bLayer needs to be tested. The results are shown in Fig 5.10, as well as the JV curve of representative cells with different bLayers (Fig 5.10a).

The PCE of cells sprayed at 150 °C do not show the same PCE of the control cells (300 °C, 10 s waiting time). When the cells are sprayed with a short waiting time, the performance is significantly reduced compared to the control cells. With longer waiting time, by contrast, the performance can be comparable to the control cells, although the standard deviation is significantly larger (Fig 5.10b).

The J_{sc} is strongly affected by the bLayer (Fig 5.10c). When the spray occurs at low temperature and short waiting time, the film looks hazy. The haziness of the film could be attributed to an incomplete evaporation of the solvent between sprays, with consequent deposition of material while the solvent was evaporating. The 10 s waiting time seems insufficient to allow a proper drying of the film before the second spray. The hazy film can explain the low current, since it reduces the light reaching the active layers.

The FF and the V_{oc} are not affected by the bLayer when long waiting time between sprays is considered, but they decrease significantly when a short waiting time is taken into account (Fig 5.10d and e). The fact that both FF and V_{oc} are lower for the low temperature and short waiting time bLayer suggests that the R_{sh} is significantly low, likely due to the layer's poor hole barrier behaviour.

The bLayer prepared at 150 °C with a long waiting time presents much better performance for all the PV parameters than the bLayer prepared with a short waiting time. The results suggest that there is a need for a longer waiting time, to allow the bLayer precursor solution to evaporate between sprays. Comparable

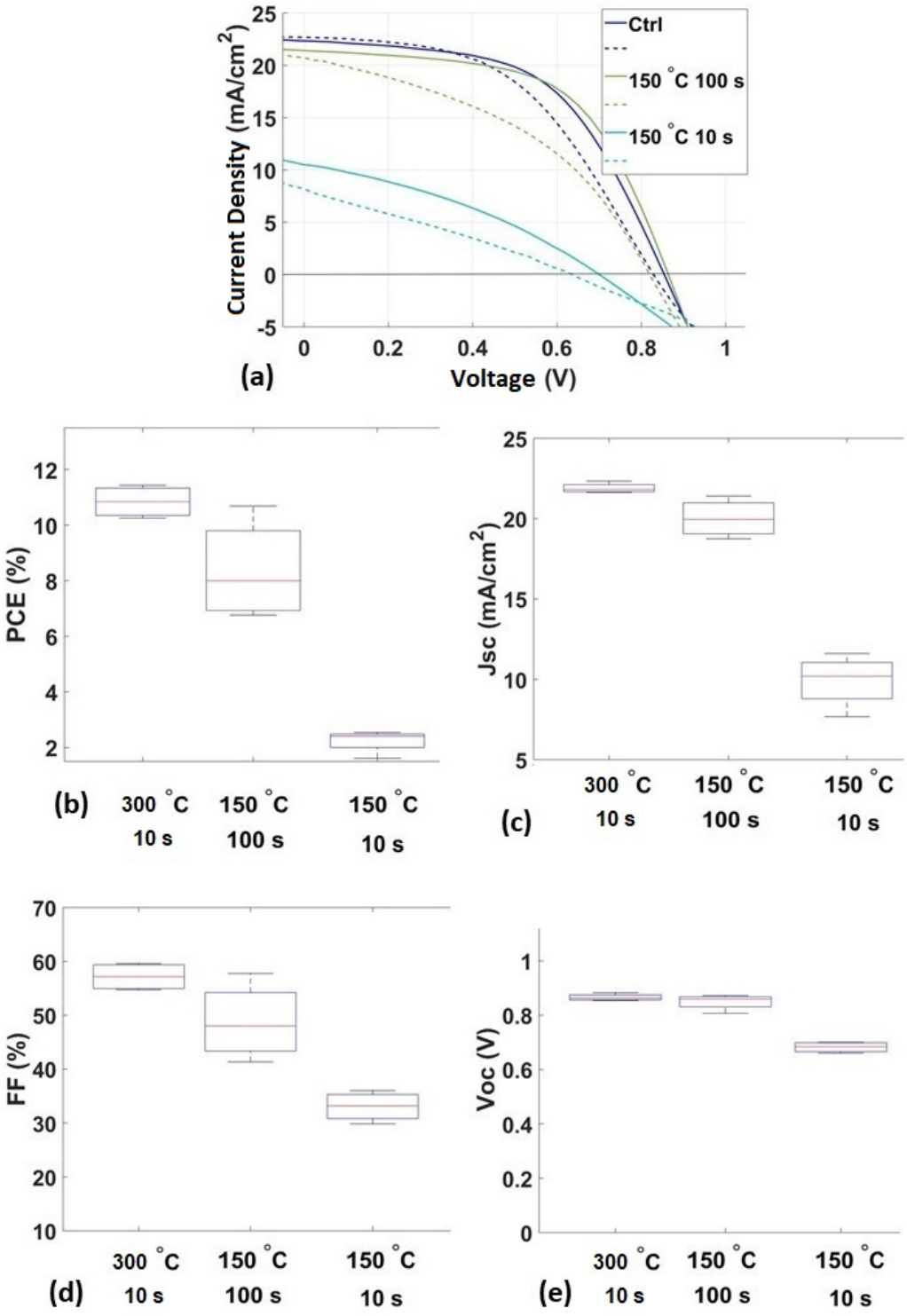


Figure 5.10: JV characteristic for cells prepared with different bLayers. (a) JV curves showing reverse (bold line) and forward (dashed line) scans of representative devices. (b) Standard deviation of PCE in reverse scan; (c) J_{sc} in reverse scan; (d) FF in reverse scan; (e) V_{oc} in reverse scan. Statistic with 4 cells per parameter.

performance to the device prepared at 300 °C is achievable, unlocking the possibility of depositing the bLayer at a lower temperature, overcoming some of the handling issues for large glass substrates.

5.3.4 Large area module

Module fabrication

A large area module with 198 cm^2 active area was designed and fabricated in this work. With our laboratory equipment, the preparation of modules with approximately an A4 size, i.e. 21.0 × 29.7 cm, is possible. The maximal printable area for the screen printer used in this study (Section 2.2.1) is around 200 × 250 mm^2. Considering a lateral frame for the encapsulation, it was planned to prepare devices on 210 × 275 mm^2 substrates, nearly an A4 size. The modules were prepared with stripe-shaped cells, which can be either perpendicular or parallel to the substrate. When the cells are oriented perpendicularly, the length of the cells is limited by the short edge of the substrate, but a large n_c (number of cells) can fit in the design. When the cells are oriented the other way around, i.e. in parallel to the substrate, the length of the cells is limited by the long edge of the substrate, but n_c is smaller. In the first case, the voltage is maximised, in the latter, the current is maximised. Both orientations can be adopted and for this first study it was decided to orient the cells perpendicularly to the substrate to obtain the largest n_c per substrate. The cell size was decided for 5 mm in W_a and the contact area for 3 mm, based on the outcomes of Section 5.3.1 and 5.3.2.

A safe area to avoid any short-circuits in case of misalignment of each layer was necessary. The safe area was ensured by overlapping the insulating ZrO_2 layer, which protects TiO_2 and FTO from unwanted contacts (Fig 5.11).

The design of the module considers the following points:

- The substrate includes a lateral frame to allow for easy handling without touching the active area and to encapsulate the device.

- Registration marks are used to register the screen to the substrate. These are placed on a second extra frame that can be chopped off at the end of manufacture (Fig 5.11a). This gives extra safety during the printing process and handling. The substrates before chopping this frame were 250 × 300 mm^2; the total space occupied by a single cell (W_a + W_d) is 11 mm.

- mTiO_2: 5 mm wide and 180 mm long (Fig 5.11b). The active area of a single cell is, therefore, 900 mm^2.

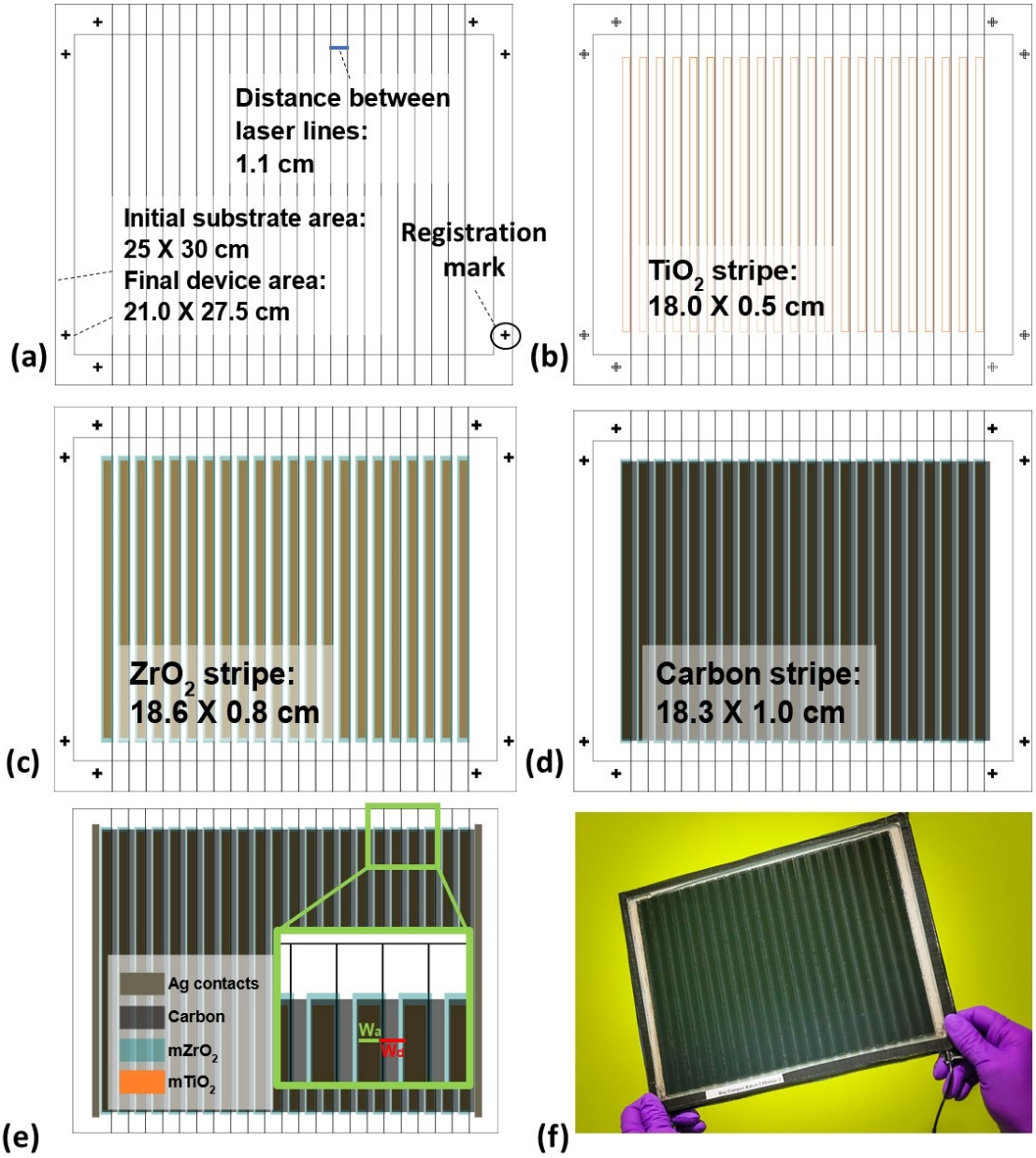


Figure 5.11: Large area module design. (a) The FTO substrate with the laser lines and marks. (b) The $mTiO_2$ layer. (c) The $mZrO_2$ layer. (d) The carbon layer. (e) Fully finished module with Ag contacts. (f) A photograph of a working module.

- $mZrO_2$: 8 mm wide and 186 mm long. In this way, $mZrO_2$ covers completely the $mTiO_2$ from the top and bottom parts of the stripe for 3 mm and the lateral sides for 1.5 mm (fig 5.11c).

- Carbon: 10 mm wide and 183 mm long. Carbon is longer than $mTiO_2$ from the top and bottom parts (1.5 mm each). The conductive layer is shorter than ZrO_2 to avoid short-circuits at the top and bottom of the cells. Furthermore, the carbon layer is much wider than the $mTiO_2$ layer to ensure 3 mm of contact (fig 5.11d).

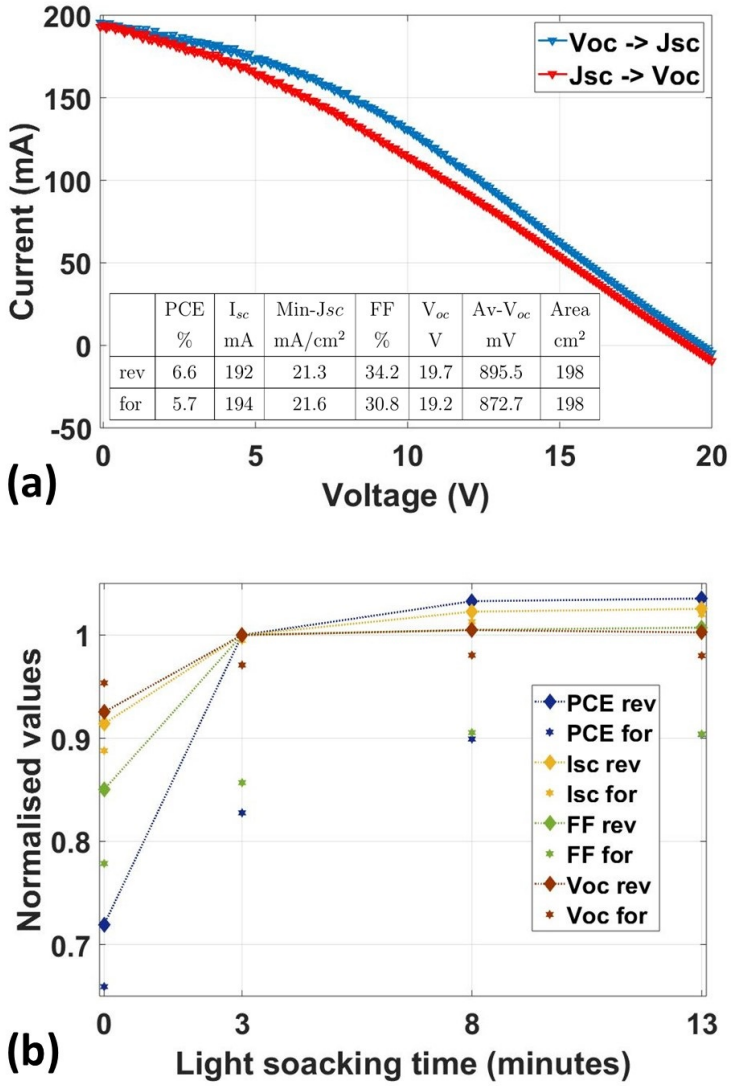
Considering the characteristics of each single cell and the available printing area, a module was designed with 22 single cells (fig 5.11e and f) which should give $V_{oc} > 18$ V and $I_{sc} > 180$ mA, as calculated considering single cells with $V_{oc} > 800$ mV and $J_{sc} > 20$ mA/cm^2.

The bLayer was either sprayed on the entire substrate or patterned, using kapton tape on the contact area. Fig 5.12a shows the JV curve of a module with patterned bLayer, which presents the highest performance in the batch of modules. It may be that this removal can improve the interconnection and, thus, the FF, as pointed out in reference [18]. The best large area module was with patterned bLayer and the result of this will be discussed below in a comparison with modules without patterning.

Module characterisation

Large area devices with more than 3 % PCE were achieved, and more than 6 % after around 2000 h from the fabrication. The Min-J_{sc} and the Av-V_{oc} were comparable with the expected single cell J_{sc} and V_{oc} (Fig 3.8b). The large area modules show a lower PCE compared to single cells because of the FF. The main issue, probably, is the large W_d, through which the current must travel before being collected by the next cell. The FF, however, is just lower than the FF that was observed in small modules for comparable W_d. The result is encouraging for the up-scaling, because in spite of the larger number of interconnects from small to large area modules, comparable FF is still achievable (Section 5.3.2). Furthermore, the fact that the FF is not very dissimilar to that of small modules is a sign that the R_c, which is multiplied by the number of interconnects, does not significantly affect the module performance.

An optimisation of the distance between cells with a more accurate method to create interconnects is necessary. This is because the contact area should not excessively limit the minimisation of W_d. The W_d, furthermore, affects the g-FF.



	PCE %	I_{sc} mA	Min-Jsc mA/cm^2	FF %	V_{oc} V	Av-V_{oc} mV	Area cm^2
rev	6.6	192	21.3	34.2	19.7	895.5	198
for	5.7	194	21.6	30.8	19.2	872.7	198

Figure 5.12: IV characteristic of the best large area 198 cm^2 module and PV parameters. (a) The IV curve after 3 minutes light soaking and after around 2000 h from the fabrication. (b) PV parameters at different light soaking time. Normalisation for the standard 3 minutes light soaking time.

In this design, for example, more than half of the substrate is not active, with a g-FF of around 45.5 %. The optimisation of W_d and of the active area is beneficial to both PCE and g-FF.

The measurement of these modules allows the observation of special peculiarities for the C-PSCs. Large area modules were used to study the effect of the light soaking on the PCE (Fig 5.12b). The increase in PCE after 3 minutes light soaking is around 30 %. The effect is observed mainly on FF but also on I_{sc} and V_{oc}. The FF, which is mostly affected in the first 3 minutes, seems to be stabilised and does not increase further with longer light soaking effect. After 3 minutes, the PCE can increase but only slightly, especially due to the increase in the I_{sc}.

After 13 minutes, the module can generate nearly 10 % more power than with 3 minutes light soaking, due to a small increase in I_{sc}. The slow response of the AVA-MAPI C-PSC was widely discussed in Section 3.3.4, here it is included to emphasise the effect of the light soaking and the need to standardise the measurement. The 3 minutes light soaking proposed in [19] is not the optimal time, but it is a compromise to measure the optimal device performance in a reasonable time.

The performance of the modules tends to improve with ageing (Fig 5.13). When the modules are just manufactured, the PCE is always below 4 %. Following humidity treatment, the PCE increases and eventually goes above 6 %. Ageing effects have been reported when the devices where stored in high humidity conditions [20]. The modules, however, were stored in different environments, from high to low humidity [15]. This continuous change of environment seems not to give a direct effect on the module performance. The moisture could increase the mobility of the ions in the crystal structure of the perovskite allowing better crystallisation. After a drying step, the moisture might not be not completely remove from the thick triple mesoscopic stack and, thus not a neat effect on the PCE at different ambient conditions was observable.

5.4 Conclusion

The registration method can be successfully utilised to make series-connected C-PSC modules. Whereas the expected PCE for single cells is above 10 %, large area modules present just over 6 % after ageing time. The optimal W_a was estimated by calculation, while the contact area was optimised experimentally. The W_a was estimated to be around 5 mm as optimal stripe width for single cells when electrodes of around 15 Ω_{sq} are utilised. Modules with different contact areas were prepared, showing that a relatively large contact in the order of mm is necessary for the porous carbon electrode.

The bLayer can be prepared by low temperature spray, allowing a simpler manufacturing process with less thermal stress applied to the glass substrate. The crystallinity of the bLayer, however, depends enormously on the temperature of the substrate during spraying, in spite of the very high temperature heating after the deposition.

A large area module with 198 cm^2 active area was tested to understand the feasibility of a large-scale process and the possible impact that the design might have on the PCE of the device. A more thorough study on the behaviour of modules with different designs is necessary to minimise W_d and maximise g-FF.

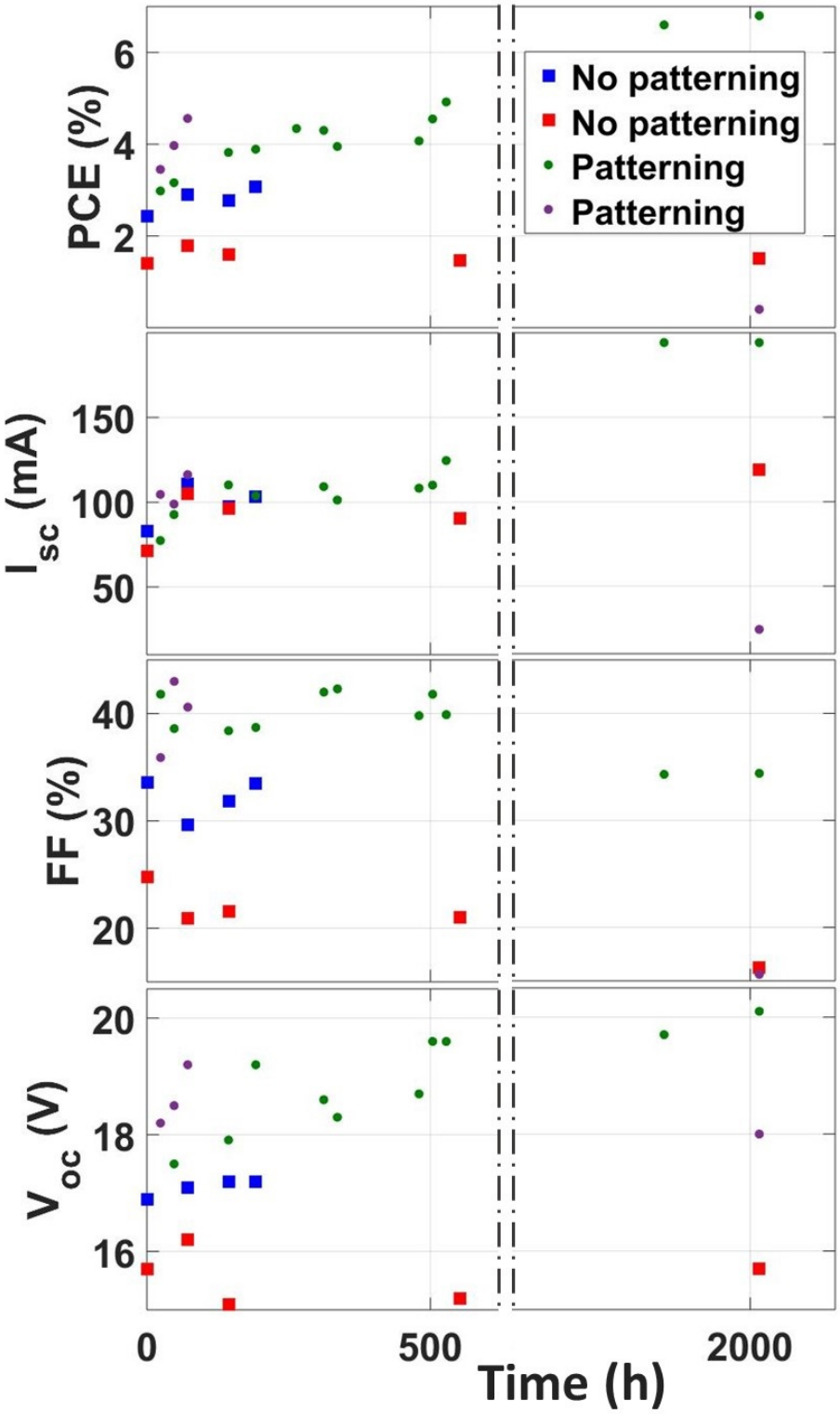


Figure 5.13: The PV parameters of the large area modules measured over time. Storage of the modules in different humidity conditions and in the dark as reported in [15].

Observations about the light soaking and ageing effects on the AVA-MAPI C-PSC modules are also reported. The storage conditions of the modules after annealing, in particular, can have a strong influence on the module performance.

After this study, the importance of the minimisation of W_d is clear, and the issues that can be faced during the up-scaling are known. High precision patterning is necessary to remove all the safe areas that the registration method requires to avoid any short-circuits in case of misalignment. The contact area needs to be minimised as well, in order to avoid any waste of space. In Chapter 6, a scribing method will be investigated to minimise W_d with an optimal contact area, and to achieve both high PCE and high g-FF. A new set of modules with even more than 200 cm^2 active area will be fabricated as a result of the experience accumulated in this work.

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Chapter 6

Increasing geometric fill factor

A key factor to achieve a successful transition from lab to fab scale is the high g-FF (geometric fill factor) of the module. This will maximise the power generation per unit area and, thus, reduce the cost of the device and installation. At present, series-connected C-PSC modules have been achieved using the registration method. In this method, W_d (dead area width) can be wide, as it is taken up not only by the interconnects between cells, but also by some additional blank space, designed to avoid any short-circuits in case of misalignment of the layers. To minimise this blank space, a material removal approach can be used.

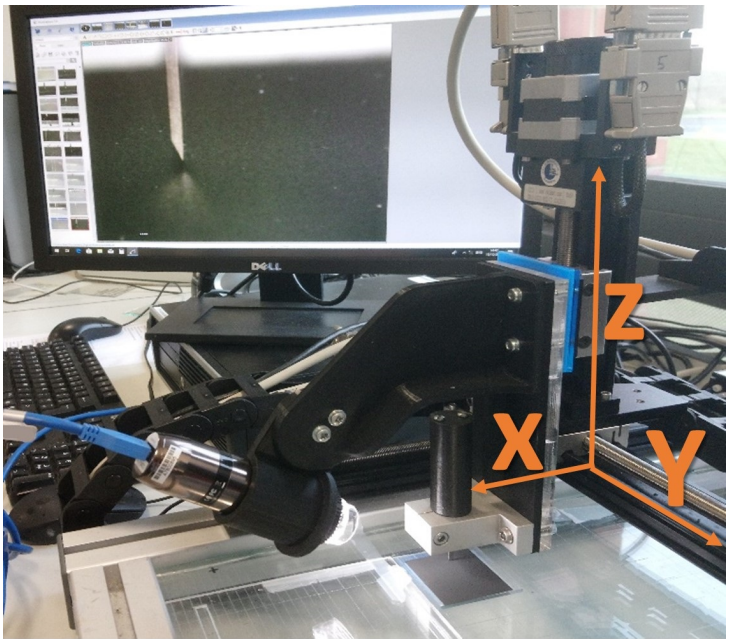


Figure 6.1: Experimental set-up to scribe mechanically the devices with an X-Y stage and camera system.

Here we present an automated and low cost scribing method to selectively remove materials. With this method, the module pattern of series-connected cells

can be created through tiny scribes, with consequent reduction in the inactive area. The impact of the scribing process on different layers is characterised in terms of morphology and chemical composition, and shows the feasibility of patterning each layer without damaging the bottom FTO electrode by using an inexpensive steel blade with an automatic mechanical scriber (Fig 6.1). Laser scribing was also tested, to compare it with the mechanical approach. A systematic study of the interconnection between cells shows the key role of the FTO/carbon contact for the optimisation of the design in terms of both PCE and g-FF. A fully printable and scribed C-PSC module with PCE of over 10 % and g-FF of 71 % on 10 × 10 cm^2 substrate is demonstrated. Modules with more than 200 cm^2 active area will be also presented.

6.1 Introduction

The preparation of C-PSC has been proved feasible from small single cells to modules and 198 cm^2 active area module was also presented in Chapter 5. And yet, the successful commercialisation of a perovskite module is not only governed by PCE, cost and lifetime. Another important factor to consider is also the coverage of the substrate with active material, so that the available space is fully exploited. To improve the performance of the module and the g-FF, it is important to achieve:

- High PCE of the single cells.
  If the single cells suffer from low performance, the large device will not perform better. A possible strategy to improve PCE is to control the crystal growth of the perovskite. The charge is transported through perovskite, especially at the ZrO_2 layer. Large, well-connected crystals can improve the internal conductivity of the device in order to reduce the vertical R_s in the cell. To optimise the crystallisation of the perovskite the Petri dish method was adopted to achieve a slow crystal growth (Section 3.3.5).

- Short distance between cells.
  W_d was observed to have a negative effect on both g-FF and R_s, but it is limited by the precision of the deposition of each layer. This is particularly challenging when using low-cost deposition techniques. Using the registration method, C-PSC modules have been reported to have a g-FF of between 45 and 60 % [1; 2; 3; 4]. The use of camera systems and fiducial points can maximise the accuracy of the printing, but can also slow down the production process.

Higher g-FF of above 90 % has been demonstrated with the so-called scribing method. Here, three different scribes, or patterns, are applied on different layers of the device to make the interconnections. These scribes are called P1, on the bottom electrode, P2, on the active layers, and P3, on the top electrode. The scribing method has been demonstrated only for perovskite architectures when evaporated metal top electrodes are employed [5; 6; 7; 8; 9; 10; 11]. To use this material removal approach for C-PSC the following manufacturing steps would be necessary:

1. The P1 scribe patterns the electrode on the substrates (FTO in this case) and should be as narrow as possible to maximise the g-FF (Fig 6.2a).

2. After layer deposition between the bottom and top electrodes ($mTiO_2$ and $mZrO_2$ in this case, Fig 6.2b), P2 is applied as close as possible to P1. This opens an area where the electrodes are connected to obtain cells in series (Fig 6.2c).

3. After the deposition of the top electrode (carbon in this case, Fig 6.2d) P3 is applied as close as possible to P2 to disconnect the adjacent cells. This directs current through the series connected cells without any short-circuits through the carbon top electrodes of adjacent cells (Fig 6.2e).

Selective material removal is key in this method, because the P2 and P3 scribes must not damage the bottom electrode (in this case FTO), which is crucial for current flow between cells. The P1 and P3 scribes define W_a and W_d, whereas P2 ensures the connection in series between cells (contact area, Fig 6.2f). The area between P1 and P2 is named "S1" (space 1) whereas the space between P2 and P3 is named "S2" (space 2), as shown in Fig 6.2g.

The scribes can be made with a laser or blade (i.e. mechanically) [12; 13], in a sheet-to-sheet or roll-to-roll process, although this has not been previously demonstrated for C-PSC [14]. For high volume PV module manufacture, laser technology is typically used. Lasers allow fine scribes, less than 50 μm and therefore permit a reduced distance between scribes. This is possible by exploiting the different absorption of each layer to selectively scribe the P1, P2, and P3 in a single process, with three different wavelengths. As a result, the three-laser process can avoid issues related to the misalignment of the substrate (or web in a roll-to-roll process). However, high precision lasers can be very expensive, and three different lasers are needed. Therefore, this approach requires a large initial investment, which is in contrast with the principle of low capital cost of C-PSC. The mechanical

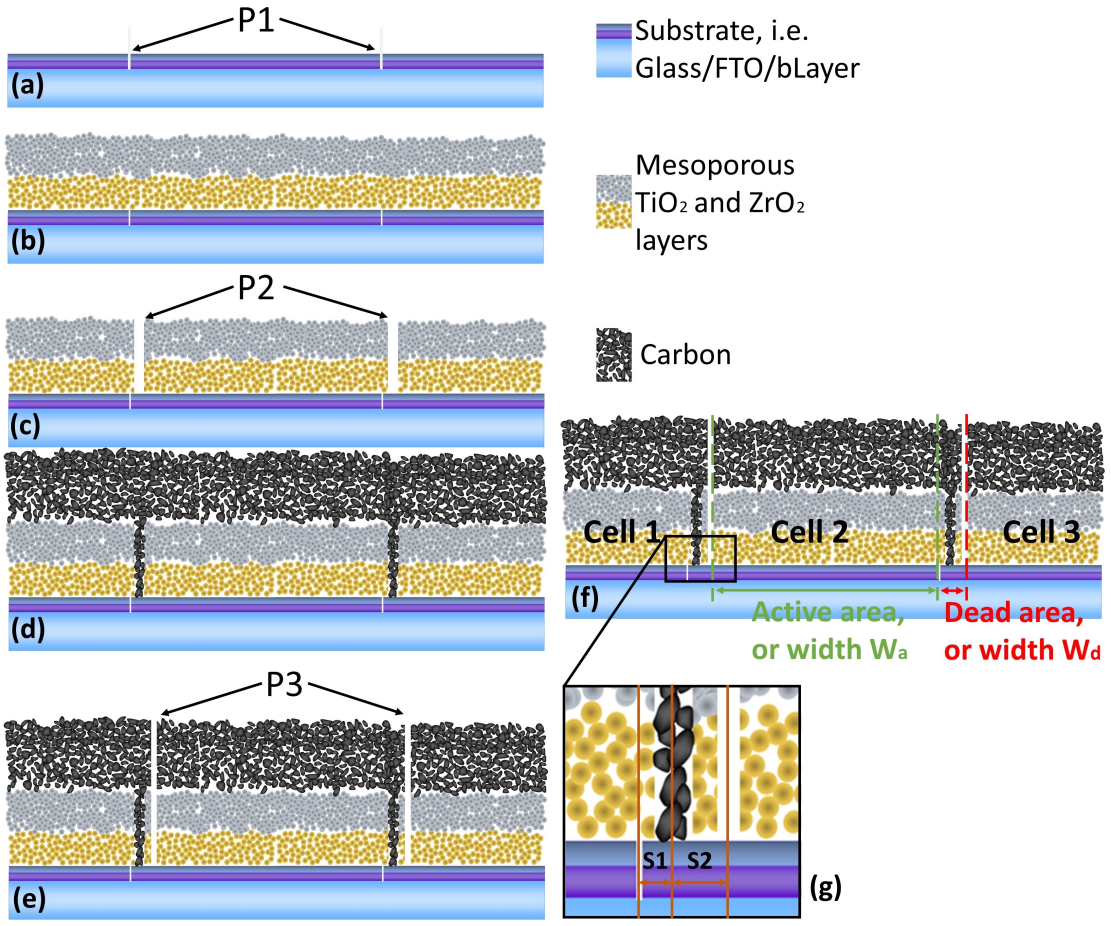


Figure 6.2: The fully printed series-connected solar module based on the scribing method. (a) P1 on a substrate of glass/FTO/bLayer. (b) Deposition of $mTiO_2$ and $mZrO_2$. (c) P2 on the two mesoporous layers to open an aperture for the interconnects. (d) Deposition of the top carbon electrode. (e) P3 to insulate the cells in series. (f) Description of W_a and W_d. (g) Blow-up of the interconnect area with description of the space between P1 and P2 (S1) and the space between P2 and P3 (S2).

approach uses a blade to scribe each layer in three different steps. This does not produce the same as laser technology, but the capital cost is significantly reduced.

In this chapter, the interconnections were characterised to ensure a successful scribe. Because of the importance of a complete but selective material removal, the scribes were optimised and characterised in terms of morphology and chemical composition. Both laser and mechanical methods were used to remove material at the scribe areas.

When the mechanical approach was used for the P2, partial removal of the bLayer was observed, without FTO damage. This could allow for the bLayer patterning via material removal, which would improve the contact area (R_c) [15; 4]. Because the bLayer patterning may add an extra step in the fabrication process, the ability to remove it via scribing reduces the complexity of the device fabrication. The patterning of bLayer by scribing has already been reported for soft layered materials such as TiO_2/perovskite/Spiro OMeTAD [16; 17] and here it is further characterised.

Herein, C-PSCs in series-connected modules prepared by the scribing method will be demonstrated for the first time. The P2 size, which decides the contact area in the interconnects, was varied to study only the effect of the contact area on module performance. Furthermore, modules from 62.5 to 83.3 % g-FF were studied. The interspace between cells was varied in order to study the effect of the distance between two adjacent cells, in order to maximise the g-FF without sacrificing the device performance. A systematic study was carried out on 5×5 cm^2 substrates. The optimal design found in this set of experiments was then used to prepare a 10×10 cm^2 module, showing comparable performance to the 5×5 cm^2 modules. Larger modules with 224.2 cm^2 active area were also prepared, with g-FF = 80 %.

6.2 Experimental

The main steps of module preparation, including layer deposition and perovskite annealing, are described in Section 2.2.3. Special steps for the fabrication of modules based on the scribing method will be described below.

Scribe tests

The scribes were made either with a laser or mechanically. The laser was the green Nd:YVO_4 that was used for the patterning of the FTO glass (Section 2.2.1), while scribing occurred with an automated X-Y-Z stage, adapted with a camera system (Fig 6.1). The blade was attached to a 31 mm steel alloy spring which could be compressed to 0.54 N/mm. A compression of 14 mm (for P2) and 5 mm (for P3) was applied.

The dye that was infiltrated in the stack for the test with laser (Section 6.3.3) was the D205 (97 %, Sigma). A substrate of FTO/mTiO_2/mZrO_2 (no blocking layer) was dyed with 1.5 mM D205 in toluene (waiting time around 12 minutes at room temperature in Petri dish). Then the substrates were rinsed with ethanol and dried with an air gun.

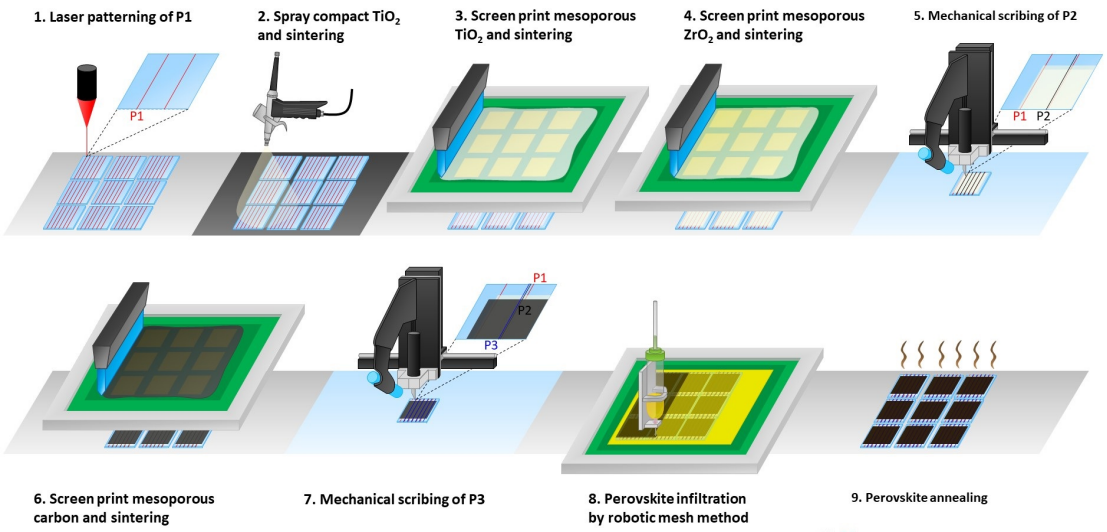


Figure 6.3: Schematic representation of module manufacure, including layer deposition, scribes and perovskite infiltration.

Module fabrication and characterisation

The P1 scribe was carried out using a laser (as for the patterning of FTO utilised for small devices, Section 2.2.1 and 2.2.1) and the P2 and P3 scribes were made mechanically with a steel blade. P2 was either scribed with a single passage

or multiple passages (raster mode) when larger contact areas were tested. The perovskite solution concentration and annealing is described in Section 2.2.3. The deposition of perovskire occurred by RbM (Chapter 4), shown in schematic in Fig 6.3. The characterisation was carried out with the equipment described in Section 2.3.

6.3 Results and discussion

6.3.1 The impact of the design on the g-FF

An important aim of this work was to optimise the design for C-PSC modules, especially in terms of g-FF, without affecting the PCE. Therefore, having a clear idea on how the g-FF can vary with the different designs was crucial. The effect of the design parameters that were defined in Section 1.6.3, i.e. g-FF, Cv (coverage), and A_r (aperture ratio), will be calculated and discussed here. The definition of Cv, A_r, and g-FF were given in Section 1.6.3 and are expressed again in Eq 6.1.

$$\begin{aligned} Cv &= \frac{Active\ area}{Substrate\ area} \\ A_r &= \frac{W_a\ n_c}{W_a\ n_c\ +\ W_d\ (n_c - 1)} \\ g-FF &= \frac{W_a}{(W_a\ +\ W_d)} \end{aligned} \tag{6.1}$$

As discussed in Section 1.6.3, Cv is the real and main parameter to define the coverage of the active area on the device substrate. Eventual lateral frames around the Ap (aperture area) give an effect on the coverage that is not investigated here, because its effect is reduced with the size of the device and can be minimised with precision printing. In this work, the effect of the cell interspace is investigated and minimised.

The Eq 6.1 in function of W_a at different n_c (number of cells) is shown in Fig 6.4a. Both Cv and A_r depend on the device size and geometry. When n_c increases, the Cv increases because the external frame occupies only a smaller portion of the substrate. The A_r is instead maximised when n_c is small. This inverted trend is because no external frame is considered, and the factor -1 in the denominator is negligible only when $n_c \gg 1$. When $n_c \longrightarrow 1$, Cv and A_r have opposite trends. A_r does not represent the real Cv in small scale modules, which are the most commonly fabricated lab scale modules. The definition of g-FF in Eq 6.1 is independent on n_c and represents Cv and A_r when n_c is very large (i.e. large area modules). The effect is more striking when very long cells are used.

Fig 6.4b shows the effect of the length of cells on Cv. For longer cells, Cv tends to be closer to g-FF when n_c is high (i.e. large area modules).

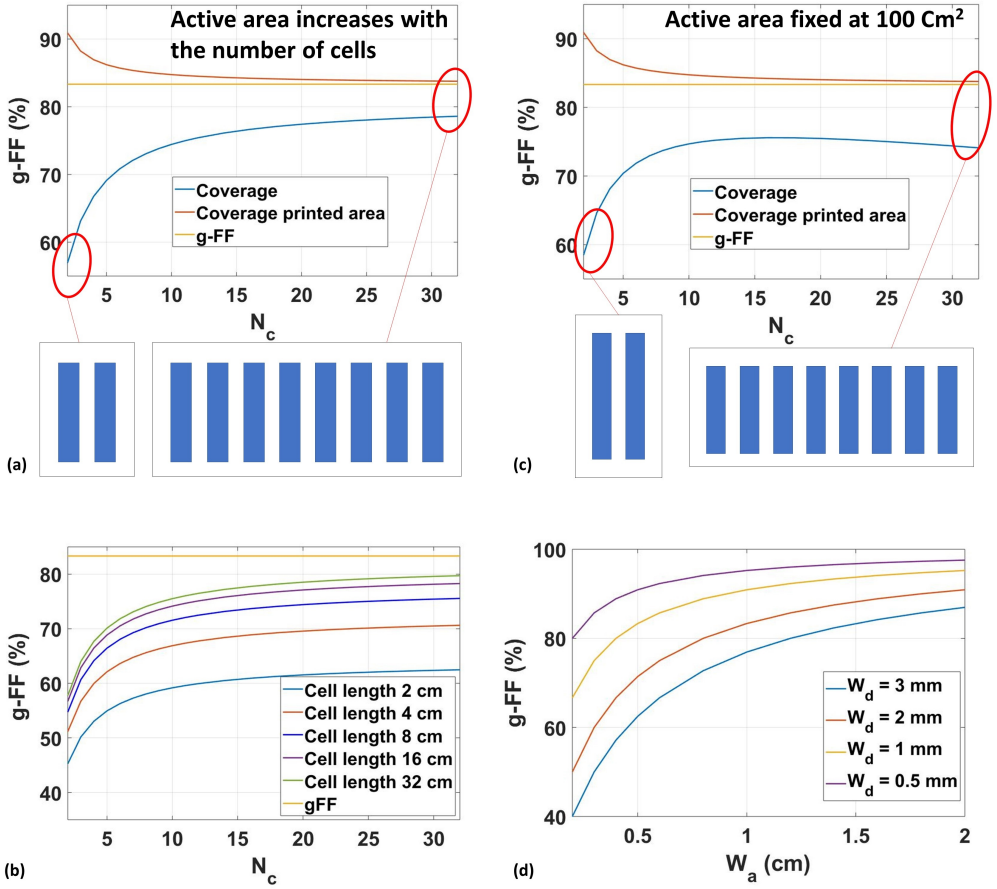


Figure 6.4: The Cv, Cv Ap, and g-FF trends for different designs. (a) When n_c increases (W_a = 5 mm; W_d = 1 mm; cell length = 18 cm). (b) When n_c increases and the active areas is fixed (W_a = 5 mm; W_d = 1 mm). (c) When n_c increases at different values of cell length: effect on the Cv and g-FF (W_a = 5 mm; W_d = 1 mm). (d) When W_a increases at different values of W_d: effect on g-FF. For the definition of Cv, the active area is the area of all the single cells and the substrate area is calculated as Ap = (W_a n_c + W_d (n_c-1)) × cell length + a frame of 5 mm around it.

High values of A_r can be achieved when n_c is small because of the small number of interconnects. This observation leads to the assumption that large area modules should be manufactured with few and very long single cells, resulting in a rectangular module. Fig 6.4c shows the trend of g-FF, Cv and A_r with increasing n_c and constant active area of the module. This is possible when the length of the cells is adjusted to compensate the effect of the variation in n_c. In this case, Cv finds a maximum point when the device is approximately squared and the n_c is not necessary minimised. Again, the g-FF is independent also from the geometry of the module and not only on the n_c, making this parameter an effective figure of

merit to describe the impact of the interspace between cells on the design. When W_a is large the g-FF increases, but W_a is limited by the conductivity of the electrode, as already discussed in Section 5.3.1. In order to increase g-FF, W_a cannot be excessively increased, or it will have a negative effect on the PCE. Thus a parameter that can be better used to maximise the g-FF is W_d. The effect of W_d on the g-FF is enormous, as shown in Fig 6.4d. For modules with 5 mm W_a, the g-FF can increase nearly 50 % when W_d is decreased from 3 to 0.5 mm (from 62.5 to 91 % g-FF). The minimisation of W_d is advantageous because of two reasons: it reduces the resistance between the cells (see Section 5.3.1) and it increases the g-FF.

After a systematic study of the scribes and the characterisation of each one's width, some considerations of realistic W_d will be done by preparing of modules with the dimensions resulting from this investigation.

6.3.2 P1: FTO removal

The P1 scribe is required to electrically isolate the bottom electrode and separate the different domains of each cell (W_a + W_d). This is achieved via the complete removal of the FTO layer in the scribe area. The scribe should not penetrate more than a few nm into the underlying glass, as this can become fragile during the subsequent heating processes. Ideally, a narrow scribe is desirable to reduce W_d and maximise the g-FF.

For the P1 scribe both mechanical and laser scribing methods were demonstrated. The laser process for the removal of the FTO, already introduced in this work for the preparation of the first C-PSCs (Section 2.2), can achieve full material removal and complete isolation (Fig 6.5a). A similar P1 scribe carried out using the mechanical process is around 100 μm wide, due to the size of the diamond tip. The total occupied area is larger, up to 250 μm due to accumulated material on the side of the scribe (Fig 6.5b). As a result, a mechanical scribed line occupies much more space than that from a laser, and leaves a very rough profile. Furthermore, the mechanical scribe requires a depth of penetration of the order of a few μm to achieve complete isolation, thus removing the FTO and part of the glass substrate. Consequently, the substrate becomes more susceptible to thermal stress and can succumb to cracking. The P1 laser scribe, by contrast, allows greater control and can achieve penetration of around 0.65 μm matching the thickness of the FTO layer. The removal of FTO using the laser method is observed using EDX mapping, and shows the complete removal of Sn (FTO) on the P1 scribe (Fig 6.5c).

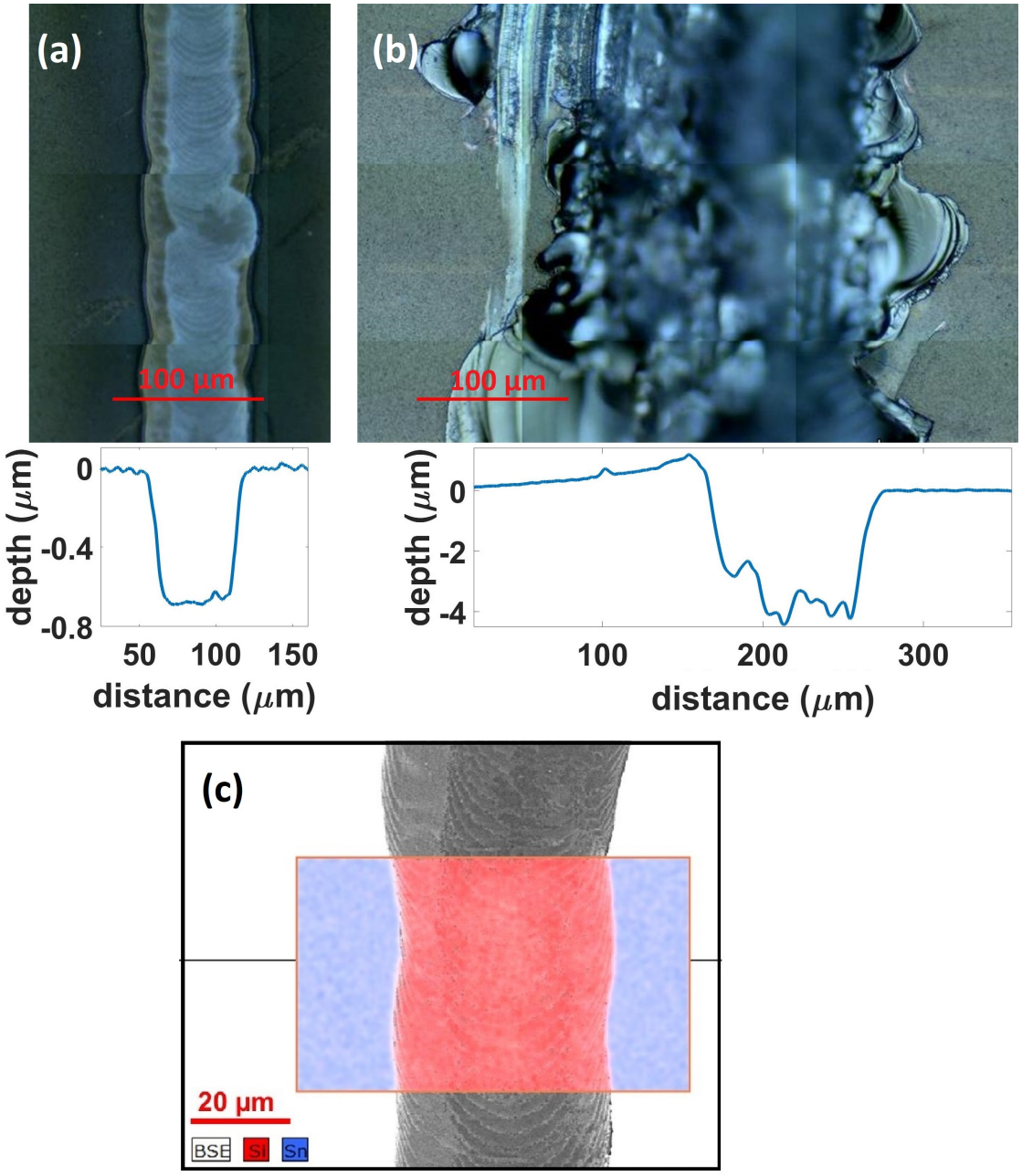


Figure 6.5: P1 laser and mechanical scribes. Optical microscope image of (a) laser and (b) mechanical scribes on the FTO substrate. The relative profilometer plot of each scribe is shown below the image of the scribe. For the mechanical approach, both the microscope image and profilometer show material accumulation on the left side of the scribe. (c) SEM and EDX map of Si (glass) and Sn (FTO) for the P1 laser scribe.

The advantage of using the mechanical approach is the low capital cost. However, the laser method is advantageous in that, as it can obtain narrow P1 scribes without affecting the stability of the substrate. Therefore, a laser process will be adopted for the substrate preparation (P1) from this point on.

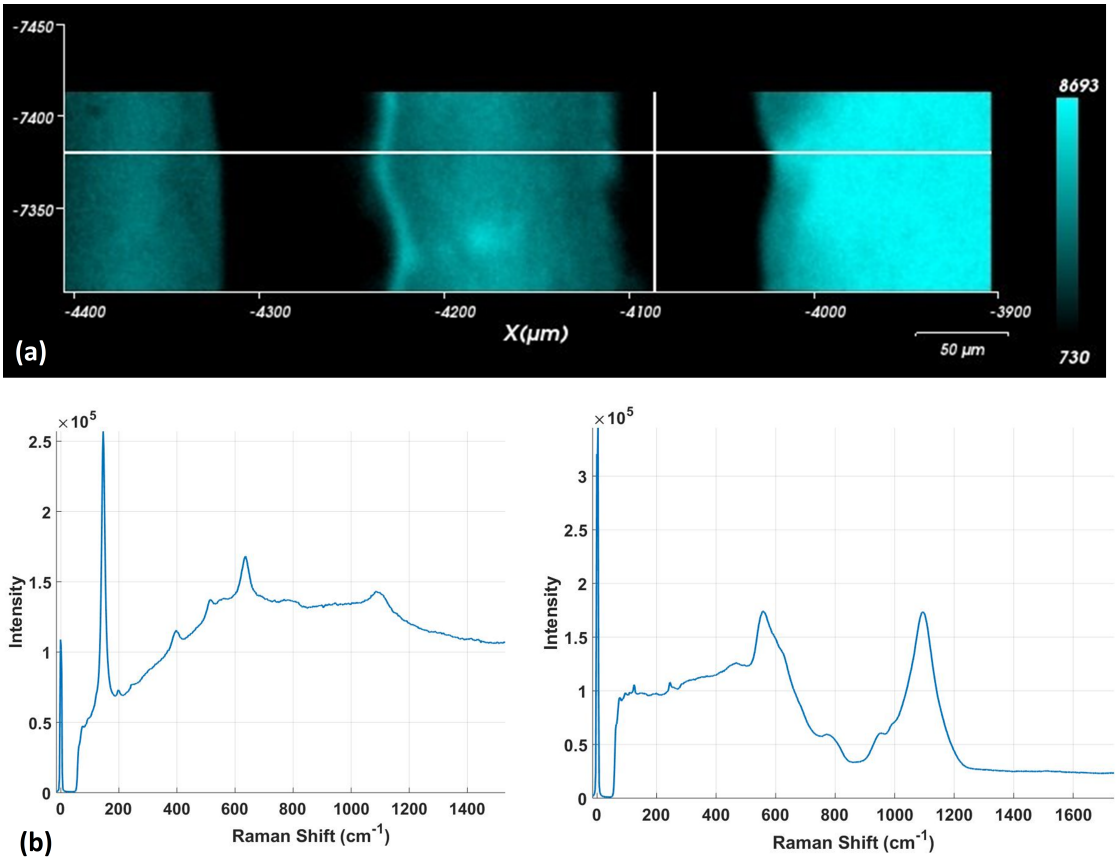


Figure 6.6: Raman on FTO substrate with P1 and subsequential bLayer deposition. (a) Chemical mapping using the anatase signal (144 cm^{-1}). (b) Spectra on the scribed area (right) and not scribed area (left). Note that the anatase phase is not observed on the scribed area.

After the P1 and the substrate cleaning, the bLayer was deposited. It was observed that no anatase phase is present in the scribed area (Fig 6.6). It is possible that the TiO_2 precursors solution (TAA in IPA) does not wet the scribed area. In terms of module design, the presence or absence of bLayer on the P1 area should not play a significant role. However, the effect of the laser on the deposition of TiO_2 is highlighted here because it could be utilised for self-patterning applications.

6.3.3 P2: TiO_2/ZrO_2 removal

The P2 scribe is performed after the deposition and heating of the TiO_2 (bLayer and $mTiO_2$), and $mZrO_2$ layers. All layers need to be removed apart from the FTO.

This is because the P2 opens an aperture where the top electrode can, after the deposition of the carbon layer, get in contact with the bottom FTO electrode. This makes the P2 crucial in the module design because its width defines the FTO/carbon contact area.

Laser scribing for the P2

The green Nd:YVO_4 laser showed several advantages over the mechanical scribing approach for the P1 and was studied here to determine its suitability for the P2 scribe. The same laser was utilised to create interconnects for modules with different architectures [18; 10] in order to find which parameters supply enough energy to the system for complete removal of TiO_2 and ZrO_2 without damaging the underlying FTO. The parameters that can be varied are the laser power, which is modulated with the applied current, the laser speed and the frequency. Moreover, it was discussed that to obtain a proper interconnect, the P2 scribe may need a relatively large area to reduce R_c. Larger scribes can be obtained by a raster process. In this case, the resolution of the raster, or the line distance between the single scribes plays a role in the patterning.

Samples of glass/FTO/TiO_2/ZrO_2 were scribed with the green laser (Fig 6.7). Despite varying the different laser parameters, homogeneous and selective ZrO_2 and TiO_2 removal was not achieved without damaging the FTO. This is because TiO_2 and ZrO_2 do not exhibit high enough absorption in the green region to protect the FTO from the laser: the single pulses give the surface enough power to create spots that completely remove all layers above the glass. This can be clearly observed at 32 A and 50 KHz, where a single pulse mark is enlarged (Fig 6.7). The single pulse also caused additional cracking, observable from the top view. In order to achieve a proper selective pattern, it would be necessary to have a laser that can be absorbed by the TiO_2 and mZrO_2 layers. The wavelength of such a laser would be in the UV region.

Efficient PSC modules with different architecture can be prepared with the green laser [18; 10]. This is possible because the perovskite, which absorbs visible light, can protect the FTO to achieve selective patterns. Perovskite can protect the FTO but, in the standard C-PSC architecture, no absorbing materials are infiltrated into the stack until the carbon layer is deposited and fired.

To prove that a protective layer would be necessary for a selective P2 scribe, a red dye with absorption peak at around 530 nm, typically used in DSSC (D205), was infiltrated in the mTiO_2/mZrO_2 layers before the laser scribe. The dye could be added in the stack and burnt at 400 °C, leaving no by-products, such as Pb-

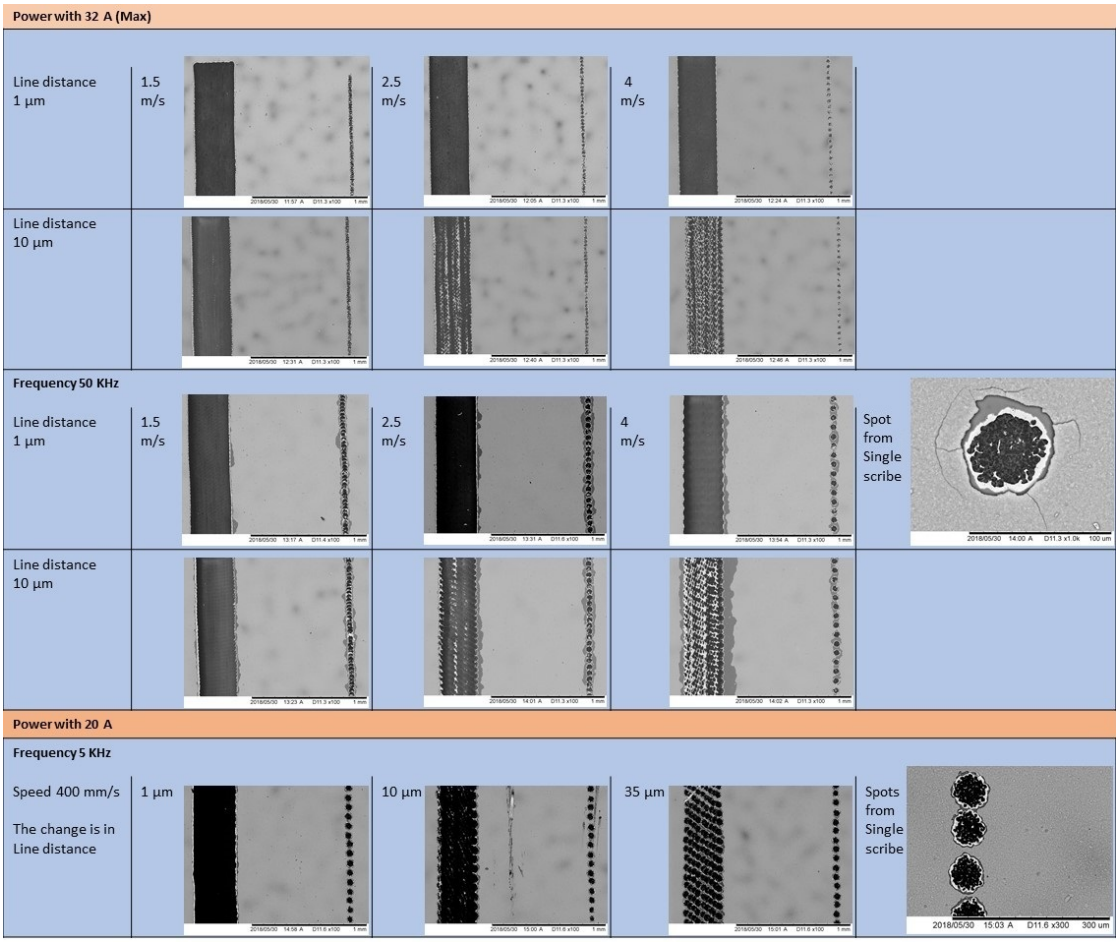


Figure 6.7: SEM images of the most significant laser tests on glass/FTO/TiO_2/ZrO_2. The frequency and the speed of the beam have been varied. The test was run on single scribes or on rastered area. The line distance in the rastered area has been varied. No selective scribe was achieved. Note that where FTO is damaged, the area is not conductive and it appears dark in SEM.

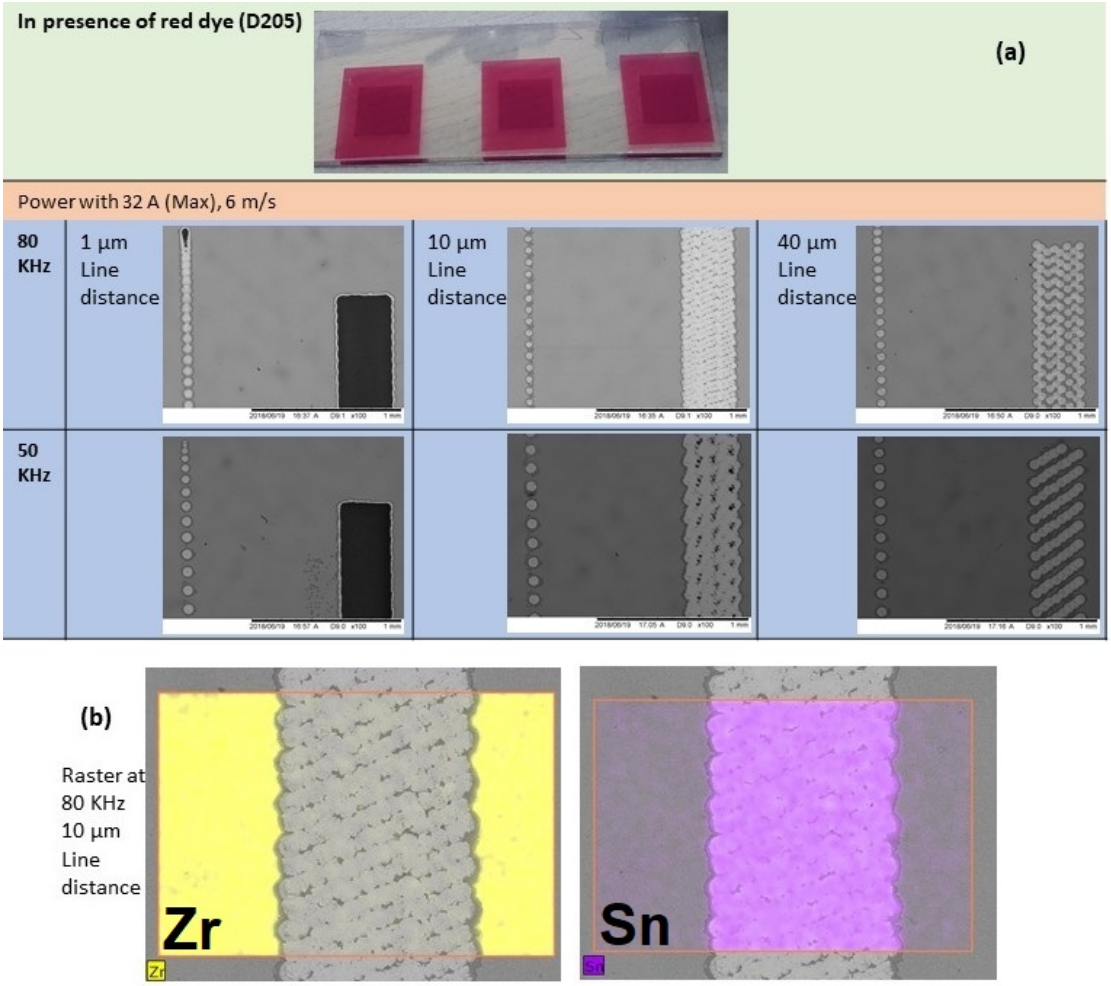


Figure 6.8: SEM images of the most significant laser tests on glass/FTO/TiO_2/ZrO_2 infiltrated with a red dye. (a) The frequency and the speed of the beam have been varied. The test was run on single scribes or on rastered area. The line distance in the rastered area has been varied. Selective scribes were achieved. Note that where the FTO is damaged, the area is not conductive and it appears dark in SEM. (b) EDX image of the rastered area at 32 A, 80 KHz and 10 μm line distance as example of proper material removal and the presence of Sn (FTO) in the scribe.

based compounds, either in the stack or in the environment. The use of the dye allowed the preparation of selective P2 scribes by using different laser parameters as shown in Fig 6.8a. The brightness of the scribe in the SEM image is a sign of the conductivity of the area, thus, the FTO is not damaged. An EDX image can confirm the proper material removal and the presence of FTO in the scribe (Fig 6.8b). The use of the dye, however, leads to some questions related to the low capital cost of the manufacture. The infiltration before the deposition of carbon is an additional step that increases the time and material consumption in the production. Moreover, when a larger investment for the production is possible, the use of a UV laser would be a preferable choice. Therefore, despite the feasibility of patterning the P2 by laser the possibility of mechanically patterning the interconnects was investigated.

Mechanical scribing for the P2

The selectivity of the material removal is determined mostly by the hardness of the blade. A diamond tip, for example, is not suitable for the P2 and P3 scribes because it can easily scratch the FTO layer. A metal (steel) tip was adopted for the P2.

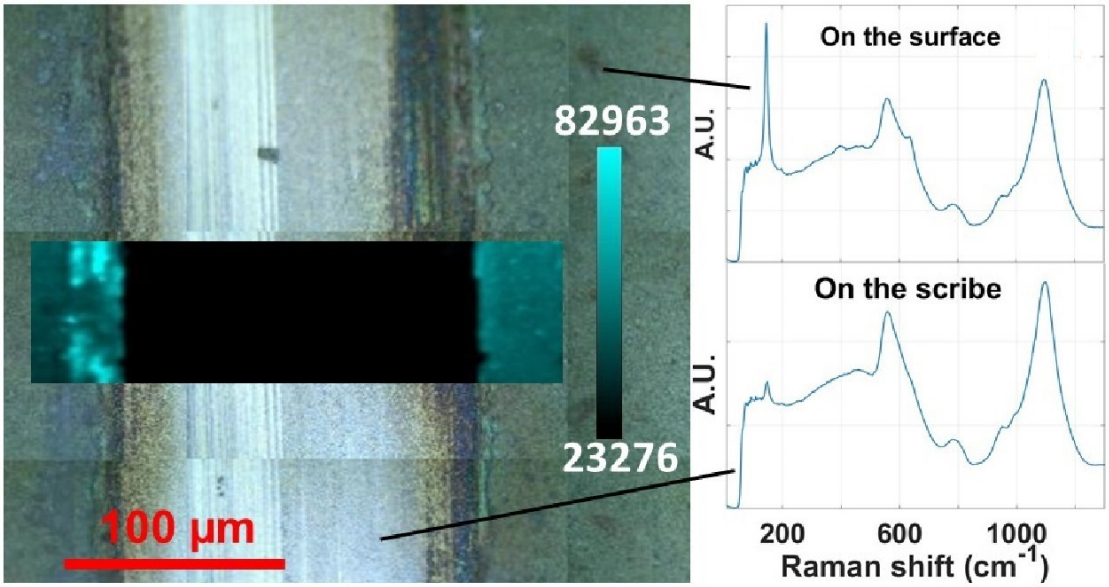


Figure 6.9: P2 characterisation. (a) Optical microscope image and Raman map of the peak at 144 cm^{-1} showing an anatase phase (TiO_2); inset, a false colour map of Raman signal intensity at different positions; (b) SEM image and EDX map of Zr (ZrO_2) and Sn (FTO).

The tip of the blade was scraped along the device surface, creating the P2 scribe. The P2 scribe should remove both $mTiO_2$ and $mZrO_2$ as well as the

underlying bLayer, creating an aperture for the final deposited carbon layer to be in contact with the FTO of the next cell. The P2 scribe must be as close as possible to the P1 without overlapping it, to avoid short-circuits between adjacent cells. The positioning of the P2 scribe is a trade-off between maximising the g-FF and ensuring the interconnects are large enough to ensure proper electrode contact between adjacent cells.

Raman showed that the scribe completely removed the mesoporous layers without damaging the FTO (Fig 6.9). The bLayer also appeared to have been removed, as the characteristic anatase signal (144 cm^{-1}) at the scribing position seemed to be more dampened than expected for a compact TiO_2 layer (Section 3.3.1 and Fig 3.4), raising some questions on the possibility of complete removal of this layer.

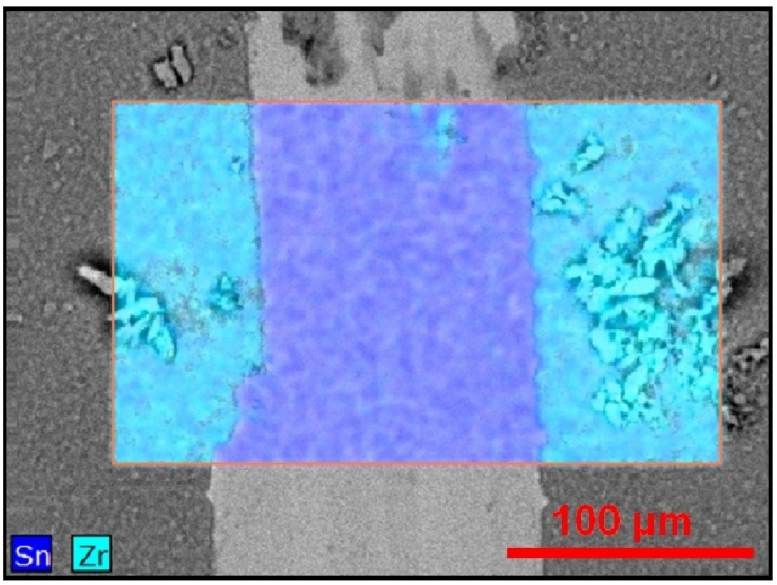


Figure 6.10: P2 characterisation. (a) Optical microscope image and Raman map of the peak at 144 cm^{-1} showing an anatase phase (TiO_2); inset, a false colour map of Raman signal intensity at different positions; (b) SEM image and EDX map of Zr (ZrO_2) and Sn (FTO).

The EDX also confirmed proper material removal (Fig 6.10) or the mesoporous layers. The presence of Ti in the scribe was difficult to determine, due to a possible overlap with a satellite signal of Sn. It was possible that the bLayer was still present in the scribe but strongly damaged by the mechanical removal. The mechanical removal of all the layers, including the bLayer, allows direct contact between a subsequent carbon deposition and the FTO, which is necessary for current flow through the module [15; 4]. The possibility of a mechanical removal of the bLayer would simplify the manufacture and benefit to the alignment. A proof of the bLayer removal was therefore crucial for the proceeding with the work.

Cross-sectional SEM images show the extent of removal of the bLayer, which was limited by the roughness of the FTO (Fig 6.11a). The carbon layer was shown to have a direct access to the FTO without having TiO_2 in the interface. The bLayer was partially removed, leaving a direct contact between FTO and carbon (Fig 6.11b). In other words, the removal of the bLayer is possible, and so is a direct FTO/carbon contact.

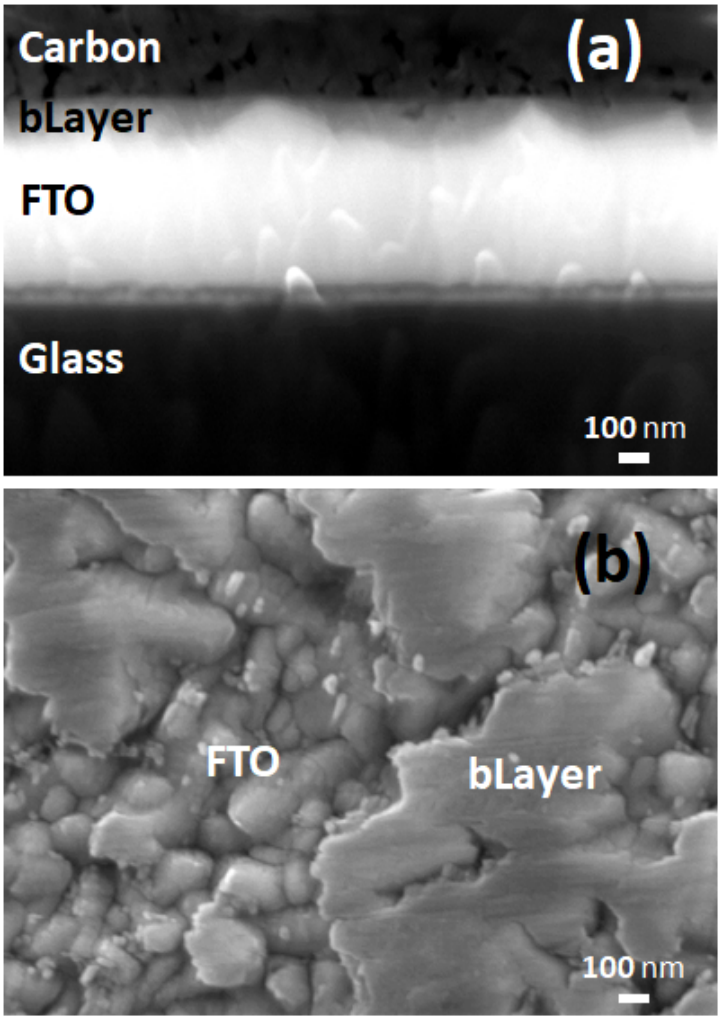


Figure 6.11: (a) SEM cross sectional image of the FTO/carbon interconnect at the mechanically scribed P2 area. The bright and conductive FTO touches directly the carbon layer. The cross section shows that the bLayer is partially removed but TiO_2 is still present in the roughness of the FTO. (b) SEM top view of the P2 scribe. The rough area is the FTO partially covered by a smoother area of bLayer.

6.3.4 P3: TiO_2/ZrO_2/carbon removal

The P3 scribe should penetrate the mesoporous layers to pattern the top electrode without affecting the bottom electrode. With the P1 scribe, the P3 defines W_a and W_d (Fig 6.2). There is no need to have wide scribes in this instance if a

complete electrical insulation is achieved. Therefore, the P3 scribe can be a single narrow line to maximise the g-FF.

In choosing an appropriate analytical method, EDX is unsuitable as the elemental analysis for carbon can suffer from several possible contaminants due to organic compounds. Conversely, Raman mapping can discriminate between the presence of graphite and other C-based compounds, due to the the excitation of the sp^2 bonds in carbon, which generate the so-called G band at around 1570 cm^{-2} [19; 20; 21] (Section 3.3.1).

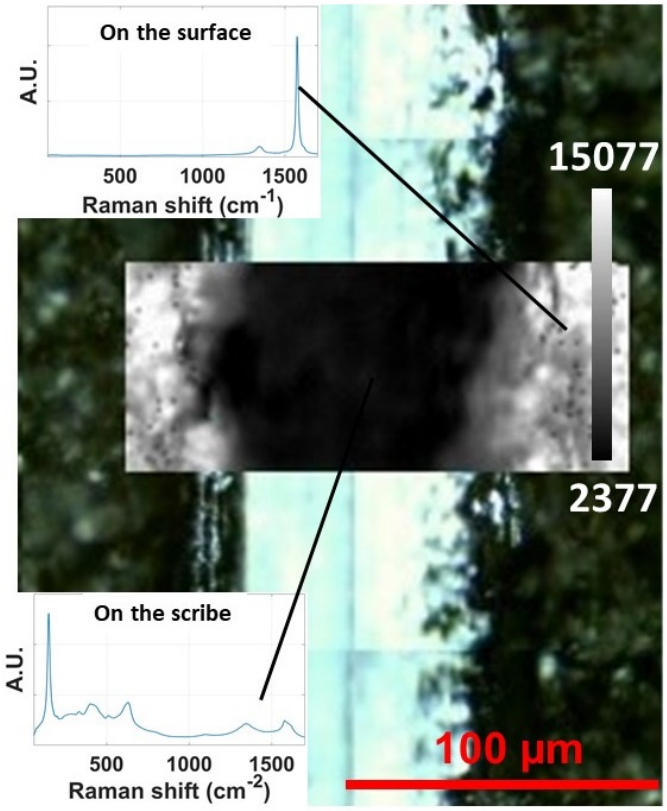


Figure 6.12: Carbon and P3 characterization. Optical microscope image and Raman map of the peak at 1570 cm^{-1}; inset, the Raman signals at different positions.

The chemical map of the P3 scribe by Raman showed a complete removal of the conductive layer; no graphite peak was detected (Fig 6.12). This is a sign that proper electrical insulation has been achieved. In contrast to the P2 scribe, the bLayer still seems still present in the P3 scribe. This observation comes from the Raman mapping, which shows the characteristic anatase phase in the scribed area (Fig 6.12). The bLayer is not removed, probably due to the presence of the carbon layer or the reduced pressure of the blade for the P3 scribe (Section 6.2). However, residual bLayer within the P3 scribe does not cause an issue as the purpose is only to disconnect the top electrodes of adjacent cells. The result shows that an effective P3 scribe, around 200 μm wide, can be achieved by mechanical scribing.

6.3.5 The contact resistance

Low R_c in the interconnects is crucial in series connected modules. In a typical architecture with a metal top electrode, the effect of R_c is negligible due to the higher conductivity of metals over carbon. In this case, the P2 width can be in the order of 100 μm or slightly more [10]. That is not the case for C-PSC modules, which have more resistive porous carbon top electrodes. It should be emphasised that carbon is less conductive than metal and that the porosity of the carbon reduces the effective contact between cells due to the presence of large voids in the interconnection area, as widely discussed in Section 5.3.2.

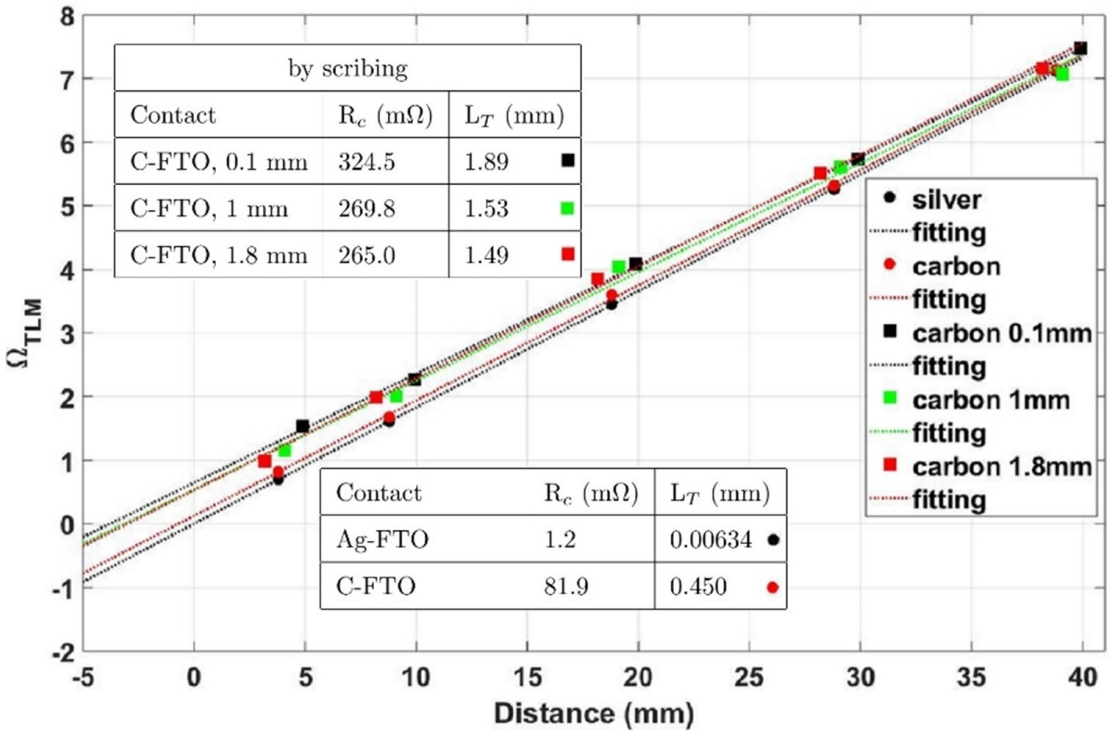


Figure 6.13: TLM measurement of FTO/Ag and FTO/carbon contacts. The plot shows the fitting of: FTO/Ag contact and the FTO/carbon contact with printed carbon lines; the FTO/carbon contact with scribed lines at different P2 width. In the inset, the tables with full data set: above FTO/carbon contacts prepared with different areas with the scribing method; below FTO/Ag and FTO/carbon contacts measured with the standard TLM method. A full description of the experiment is available in Section 2.3.1.

To quantify the effect of using carbon instead of metals, the R_c for both silver and carbon on FTO was measured by TLM (Section 2.3.1). The resistance was plotted over the distance between the lines. The intercept with the y-axis is twice R_c, whereas the intercept with the x-axis is twice L_T (transfer length). The L_T is the average distance that carriers travel underneath the contact before being collected [22]. The measurement shows that the R_c of FTO/carbon contact is

nearly 100 times larger than the one for FTO/Ag (Fig 6.13). The investigation of the minimal contact area is therefore paramount for producing efficient modules with high g-FF.

An additional experiment based on the TLM was designed to simulate actual P2 scribes in modules, and to evaluate the R_c of FTO/carbon interface. This was for typical P2 widths that might be used in a module structure. The experiment is described in Section 2.3.1. For consistency, a scribing method was used to isolate the electrodes in the TLM experiment. All three layers were printed and then P2 scribes of different width performed. Finally, P3 scribes were made to insulate the contact lines, as the TLM layout is shown in Fig 2.7 (Section 2.3.1). The results show a decrease in resistance with increasing P2 width as might be expected (Fig 6.13). The L_T of carbon directly on FTO, is lower than the FTO/carbon prepared with the scribing method, increasing from 450 μm to around 1.5 mm. This is likely due to an incomplete removal of the layers, as described in Section 6.3.3.

It is clear that the P2 width should be in the range of 1 mm or more in order to minimise the R_c. However, large P2 scribes require large W_d, which gives an effect on R_s and, overall, on g-FF. In the next sections, the effect of the P2 width on the PCE of modules, and the effect on the g-FF will be investigated.

6.3.6 Module design: a study on the contact area

To further explore the influence of the P2 scribe width, a set of modules was prepared using three different widths: 0.15 mm (similar to the P2 scribe employed for modules with metal contacts), 1 mm and 1.85 mm (in the range of the L_T that was measured by TLM in Section 6.3.5). The P1 and P3 scribes were kept fixed at around 50 μm and 200 μm respectively (Sections 6.3.2 and 6.3.4). For consistency, cell to cell distance was fixed at 3 mm for all P2 widths. This was chosen because it fits even the larger scribe and avoids the introduction of additional variables other than the contact area, which is defined by the P2 width. This experiment was designed to observe the effect of the interconnects on the R_c and not the R_s, due to the distance between the cells. The three designs are described in Tab 6.1 and the relative interconnects are shown in Fig 6.14.

As the only variable parameter is the P2 width, which is included in the fixed dead area W_d, the g-FF does not change (62.5%) and the cell number (n_c) is equal for the three different module layouts M1, M2, and M3 with increasing P2 width. The optimisation of the g-FF will be discussed in the next section.

The IV curves for the average of three 5 $\times$ 5 cm^2 modules with varying P2 width show an improvement in PCE when the P2 scribe is increased from the M1

Table 6.1: Module designs for the investigation of the contact area effect. PCE is the average of 3 modules with data derived from the reverse scan.

Design	P1 (μm)	P2 (mm)	P3 (mm)	g-FF (%)	W_a (mm)	W_d (mm)	S1 (mm)	S2 (mm)	n_c	PCE (%)
M1	50	0.15	0.2	62.5	5	3	0.3	2.3	5	5.8
M2	50	1	0.2	62.5	5	3	0.3	1.45	5	8.3
M3	50	1.85	0.2	62.5	5	3	0.3	0.6	5	8.9

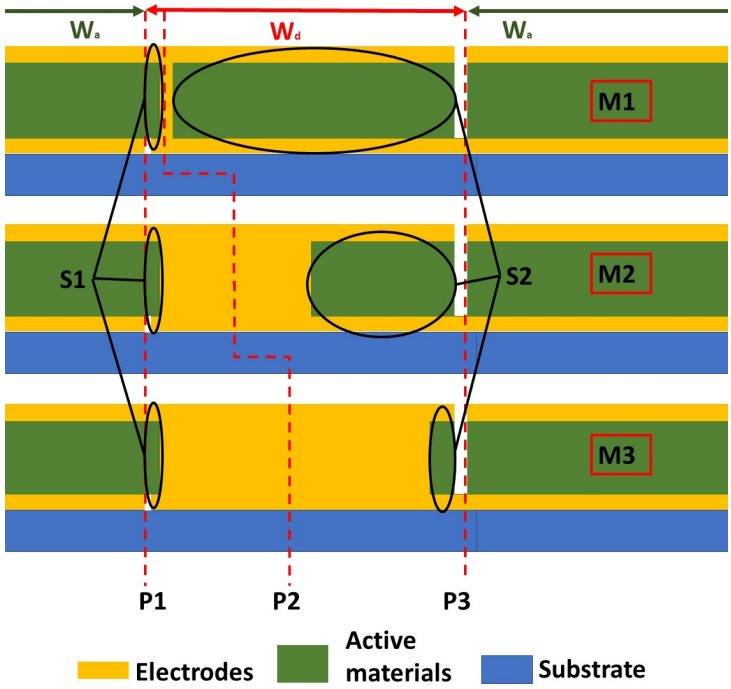
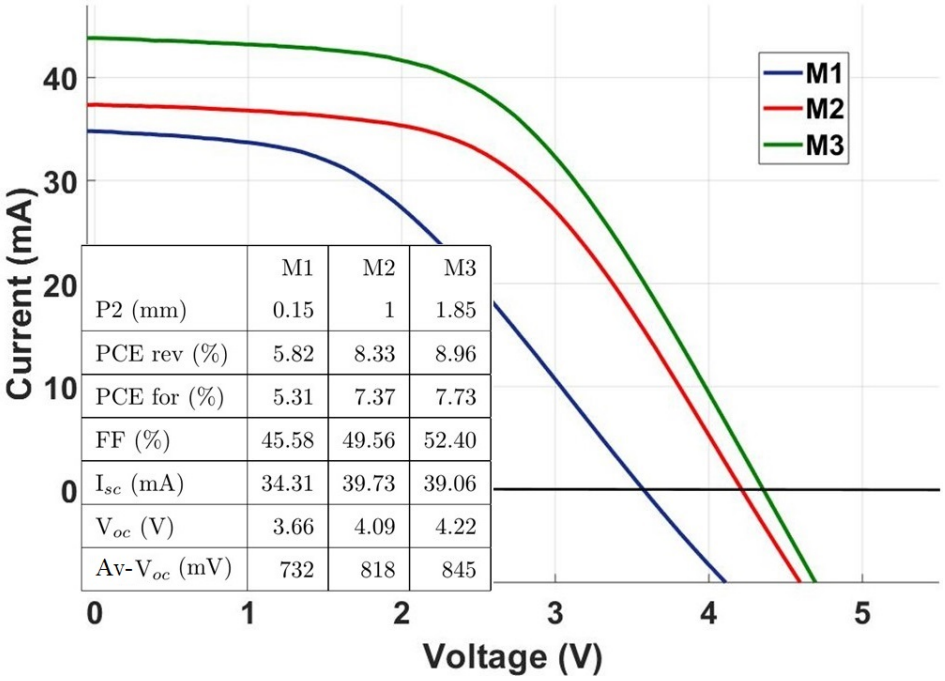


Figure 6.14: Schematic representation of the interconnection areas of generic modules with design M1, M2 and M3 in lateral view. The W_a and W_d are constant in all the three modules. The P2 width is changed as the only parameter under study in this set of modules. The S2 varies accordly to the P2 to conserve the distance between the cells constant.

to the M3 layouts (Fig 6.15 and Tab 6.3). On average, the PCE increases from around 5.8 % to 8.3 % from M1 to M2, and goes up to 8.9 % from M2 to M3, achieving 10.3 % for the M3 best module (Tab 6.3).

The I_{sc} increases slightly from M1 to M2 (from 34.3 mA to 39.7 mA) but it remains constant from M2 to M3 (39.7 and 39.1 mA respectively). The I_{sc} should not be affected by the resistance unless the R_s or R_c are too high (Section 1.5.3). The fact that the I_{sc} tends to be lower in M1 than in M2 and M3 could be a sign that the R_c in M1 is much higher than one in M2 and M3, as the P2 width in M1 (0.15 mm) is too small. The TLM measurement also suggested this (Section 6.3.5).

The fill factor (FF) is strongly affected by both the R_s and the R_c. The average FF is 45.6 % for M1 modules, it increases in M2, 49.6 %, and continues to grow in



	M1	M2	M3
P2 (mm)	0.15	1	1.85
PCE rev (%)	5.82	8.33	8.96
PCE for (%)	5.31	7.37	7.73
FF (%)	45.58	49.56	52.40
I_{sc} (mA)	34.31	39.73	39.06
V_{oc} (V)	3.66	4.09	4.22
Av-V_{oc} (mV)	732	818	845

Figure 6.15: IV curve in reverse scan of representative modules with increasing P2 size, 0.15, 1, and 1.85 mm for respectively M1, M2, and M3 (Tab 6.1 and Fig 6.18). The full set of data can be seen in Tab 6.3. In the inset, the table describing the average values of the device parameters for each kind of device. Statistic of 3 modules per parameter.

the M3 modules, to 52.4 %. The improvement in FF observed with the increase in the P2 size width is a strong sign of a decrease in the R_c.

The open circuit voltage V_{oc} increases with the increase in the P2 size. Av-V_{oc} in the modules is as follows: 732 mV for M1, 732 mV for M2, 819 mV and 845 mV for M3. This parameter was not expected to be related to the P2 width and the R_c, and will be further discussed in the next section.

6.3.7 Module design: geometric fill factor optimisation

An increase in the P2 scribe width improves the C-PSC module performance when W_d is constant. Further improvements in PCE can be expected when the W_d is decreased because shorter distance between cells can reduce R_s, as discussed in Section 5.3.1. Because the decrease in W_d also enhances the g-FF (Section 5.3.1 and 6.3.1) the expected result is a net improvement in PCE × g-FF. For W_a = 5 mm, as in this work, the decrease in W_d from 3 to 1 is expected to improve the PCE by nearly 10 % and the g-FF by nearly 40 % (from 62.5 to 83.3 %, Fig 5.4b).

Table 6.2: Module designs with maximised g-FF at a given P2 width. PCE is the average of 3 modules with data derived from the reverse scan.

Design	P1 (μm)	P2 (mm)	P3 (mm)	g-FF (%)	W_a (mm)	W_d (mm)	S1 (mm)	S2 (mm)	n_c	PCE (%)
M1max	50	0.15	0.2	83.3	5	1	0.3	0.3	6	7.6
M2max	50	1	0.2	71.4	5	2	0.3	0.45	5	9.1
M3	50	1.85	0.2	62.5	5	3	0.3	0.6	5	9.0

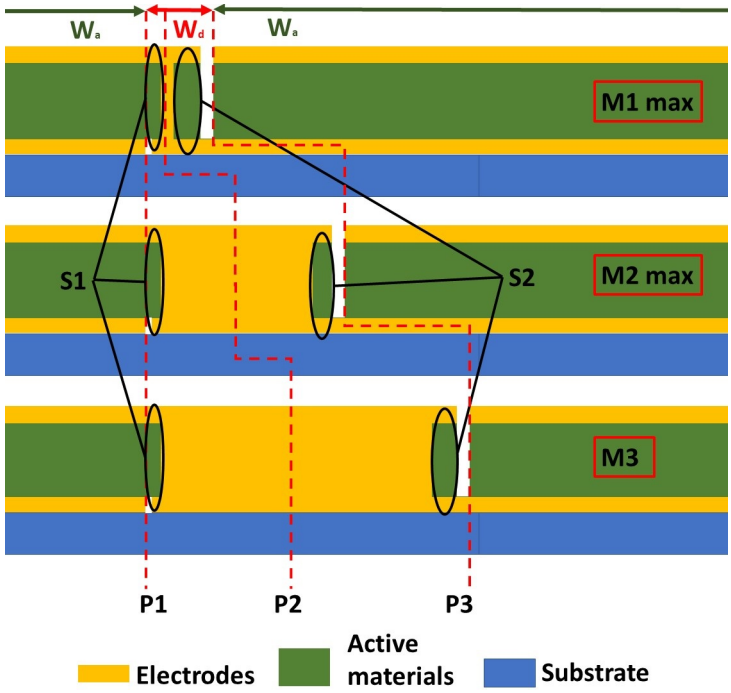


Figure 6.16: Schematic representation of the interconnection areas of generic modules with design M1max, M2max and M3 in lateral view. The W_a is constant in all the three modules but the W_d is minimised according to the P2 width of each design. The g-FF, therefore, increases from M3 to M1max. Note that the S2 does not need to be enlarged as in Fig 6.14.

Section 6.3.6 focuses on modules with g-FF = 62.5 % (M1, M2 and M3 layouts), i.e. with W_d = 3 mm; whereas here are shown a different set of modules with

the aim of exceeding 62.5% g-FF. Keeping W_a constant, i.e. 5 mm, two module designs were tested, namely M1max (P2 = 0.15 mm, W_d = 1 mm) and M2max (P2 = 1 mm, W_d = 2 mm), as equivalent to M1 and M2 but with maximised g-FF (Tab 6.2 and Fig 6.16). It should be noted that the P2 width limits the minimisation of W_d and, thus, the g-FF of M2max is 71.4 % and that of M1max is 83.3 %. As an example, the maximisation of the g-FF from M1 to M1max layouts is shown in Fig 6.17. A detailed schematic of each module layout, i.e. M1, M2, M3, M1max and M2max, can be found in Fig 6.18.

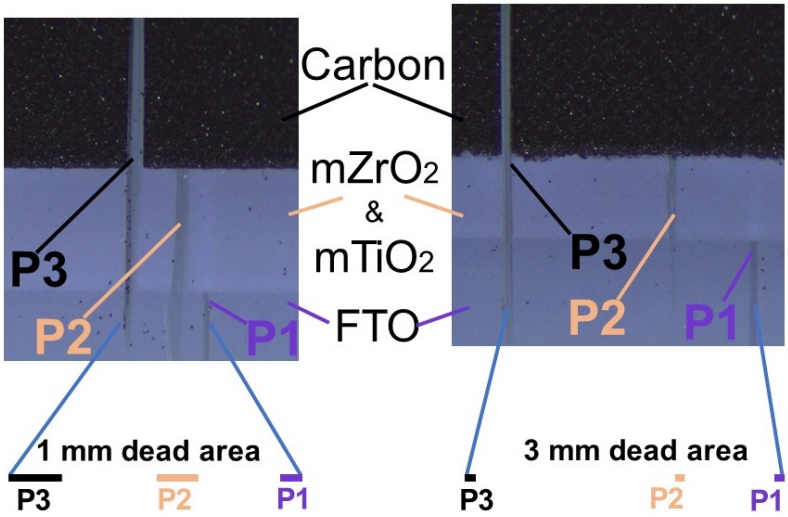


Figure 6.17: Optical microscope image of the scribes for M1 and M1max designs.

All the modules (M1, M2,1max, M2max and M3) were prepared in the same batch, so M3 could be used as a control device for the experiments in both this and previous sections. The primary purpose of the optimised layouts (M1max and M2max) was to investigate the effect of reducing W_d whilst keeping both W_a and the P2 width the same as the original designs, i.e. M1 and M2 respectively. These modules were also compared with M3 (P2 = 1.85 mm, W_d = 3 mm). The average performance of the M1max, M2max and M3, and representative JV curves are shown in Fig 6.19, whereas the full set of data is shown in Tab 6.3. The modules improve significantly with minimisation of W_d. With the same P2 scribe width, M1 improves from 5.8 % (W_d = 3 mm) to 7.6 % (W_d = 1 mm, M1max design), whereas M2 goes from 8.3 % (W_d = 3 mm) to 9.1 % (W_d = 2 mm, M2max design).

The I_{sc} is comparable between M1max, M2max, and M3 in spite of the trend observed for M1, M2 and M3. In detail, the I_{sc} of M2 was similar to that to M3 as well as M2max. The I_{sc} of M1 was lower but M1max recovered with an improvement by 3 mA between the two layouts with the same P2 width (M1 and M1max). It could be that the reduction in W_d can partially compensate the poor contact with the narrow P2 scribe, resulting in a comparable overall effect on R_s.

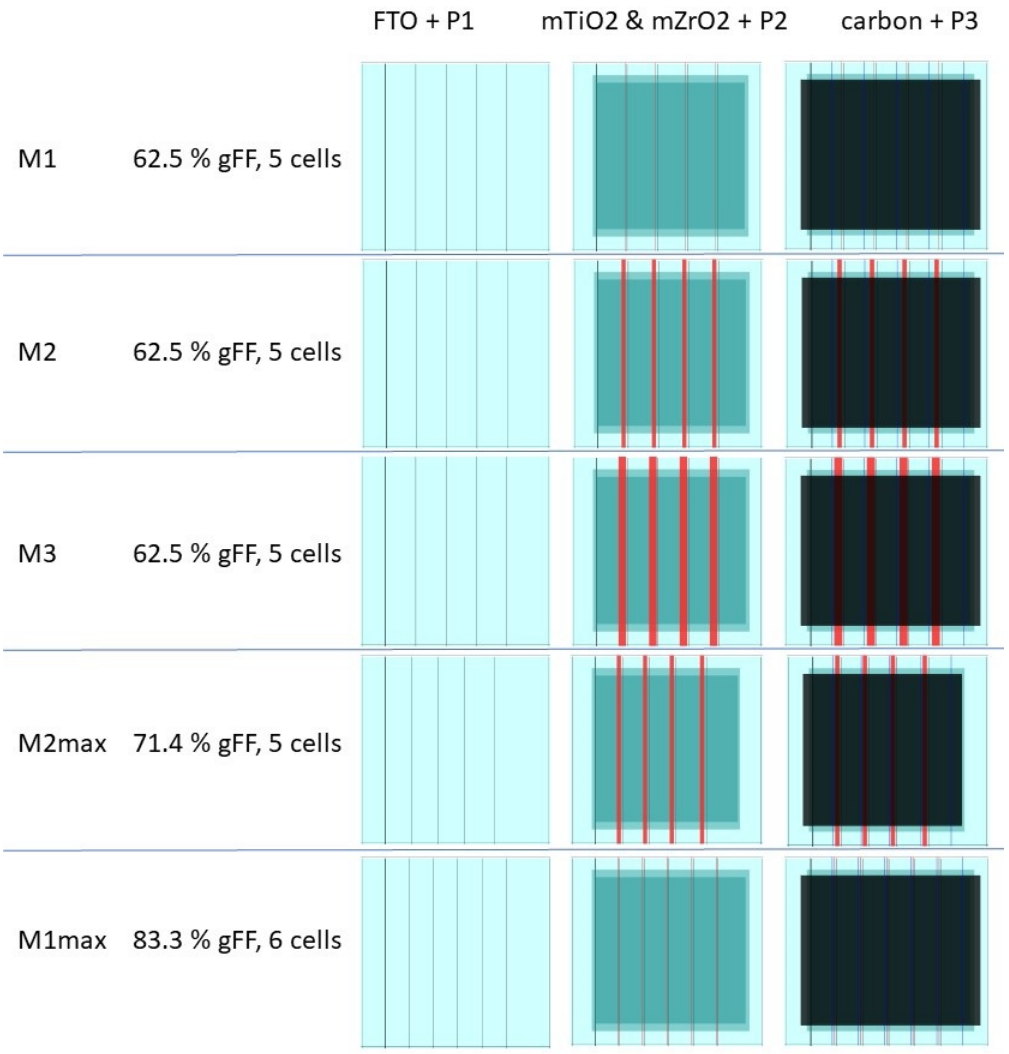
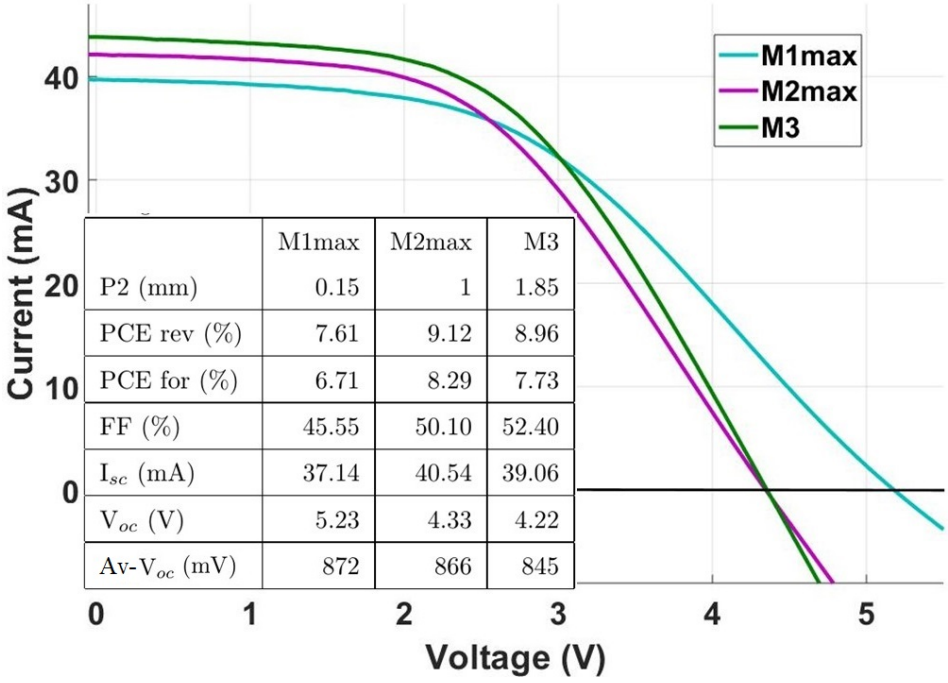


Figure 6.18: Top view of the design M1, M2, M3, M1max, and M2max.



	M1max	M2max	M3
P2 (mm)	0.15	1	1.85
PCE rev (%)	7.61	9.12	8.96
PCE for (%)	6.71	8.29	7.73
FF (%)	45.55	50.10	52.40
I_{sc} (mA)	37.14	40.54	39.06
V_{oc} (V)	5.23	4.33	4.22
Av-V_{oc} (mV)	872	866	845

Figure 6.19: IV curve in reverse scan of representative modules with increasing P2 size and maximised g-FF (M1max, M2max, and M3, Tab 6.2 and Fig 6.18). In the inset, the table describing the average values of the device parameters for each kind of device. The full set of data are in Tab 6.3. Statistic 3 modules per parameter.

The V_{oc} increased significantly when the cells were brought closer together. The improvement in Av-V_{oc} from M1 to M1max was by 140 mV. The same trend was observed from M2 to M2max, where the improvement was around 50 mV. It should be noted that Av-V_{oc} was comparable in M1max, M2max, and M3 modules, i.e. when W_d was reduced for the relative P2 width. In this case the width of the P2 scribe (related to R_c) balanced out the reduction in W_d, which is related to R_s. However, V_{oc} should not be affected by R_s but by R_{rec} (recombination resistance) [23] that is reflected in G (shunt resistance) (Section 1.5). The fact that the V_{oc} improved with the increase of the P2 scribe and the decrease of the W_d may have different reasons. The size of the S2 area was very different for M1, M2 and M3 layouts, but were comparable for M1max, M2max and M2 (Fig 6.14 and Fig 6.16). S1 and S2 are the spaces between the scribes and might act as active cells that generate current, but are not connected in series with the principal cells of the device. This current generation might cause recombination and, therefore, a reduction in V_{oc}. The mechanism might not be negligible when S1 and S2 are large, for example around a half of the active area, as in the case of M1 and M2 modules. The minimisation of S1 and S2 is beneficial for the minimisation of the recombination phenomena.

Table 6.3: Device performance of 5 × 5 modules. Active area of single cells 1.95 cm^2 (3.9 cm × 0.5 cm)

		PCE (rev) (%)	PCE (for) (%)	FF (%)	I_{sc} mA	V_{oc} V	Av V_{oc} mV	n_c
	A	6.22	4.95	53.02	28.25	4.01	801.3	5
M1	B	5.58	5.54	39.67	39.91	3.41	681.0	5
	C	5.67	5.43	44.04	34.77	3.57	714.8	5
	A	6.71	5.56	47.12	31.19	5.29	881.5	6
M1	B	7.79	6.99	42.61	40.50	5.23	870.9	6
max	C	8.33	7.57	46.92	39.72	5.18	863.3	6
	A	8.70	7.26	53.29	37.38	4.21	843.0	5
M2	B	8.04	7.40	46.48	42.48	3.93	786.8	5
	C	8.24	7.46	48.92	39.34	4.13	826.9	5
	A	9.88	8.97	50.13	43.73	4.35	870.1	5
M2	B	9.49	8.88	49.99	42.14	4.35	869.5	5
max	C	7.99	7.03	50.18	35.76	4.30	859.3	5
	A	8.24	7.13	52.27	35.35	4.30	860.6	5
M3	B	8.34	6.93	52.90	38.00	4.01	802.5	5
	C	10.29	9.12	52.02	43.82	4.35	871.0	5

The investigation of this chapter aims to minimise g-FF, so the design quality should be related not only to PCE but also to PCE × g-FF. As it was discussed, the maximisation of the g-FF improves the PCE because of the reduced distance between the cells and the minimisation of the S2 space. However, when the PCE are plotted in function of the P2 width, it seems that the P2 should be as large as possible (Fig 6.20a). When the comparison between the different designs is done in terms of PCE × g-FF, an optimum can be found (Fig 6.20b). In the case of M3 modules, the g-FF of 62.5 % is too low to achieve high PCE × g-FF. The highest g-FF is for M1max modules at 83.3 %; however, the PCE is not as high as M2max and M3. M2max modules have comparable performance to M3 and the g-FF is 71.4 %, which is higher than M3. This was considered a sensible compromise in this set of experiments.

In conclusion, it was found that:

- The contact area between cell must be relatively large for C-PSC. In this set of experiment it is around 1 mm when the PCE × g-FF is considered.
- The minimisation of the W_d, which is limited by the P2 width, is always beneficial for the module design. This is because:
    1. it reduces the distance between the cells;

2. it reduces the S1 and S2 spaces, which can cause recombination phenomena and a reduction in V_{oc}.

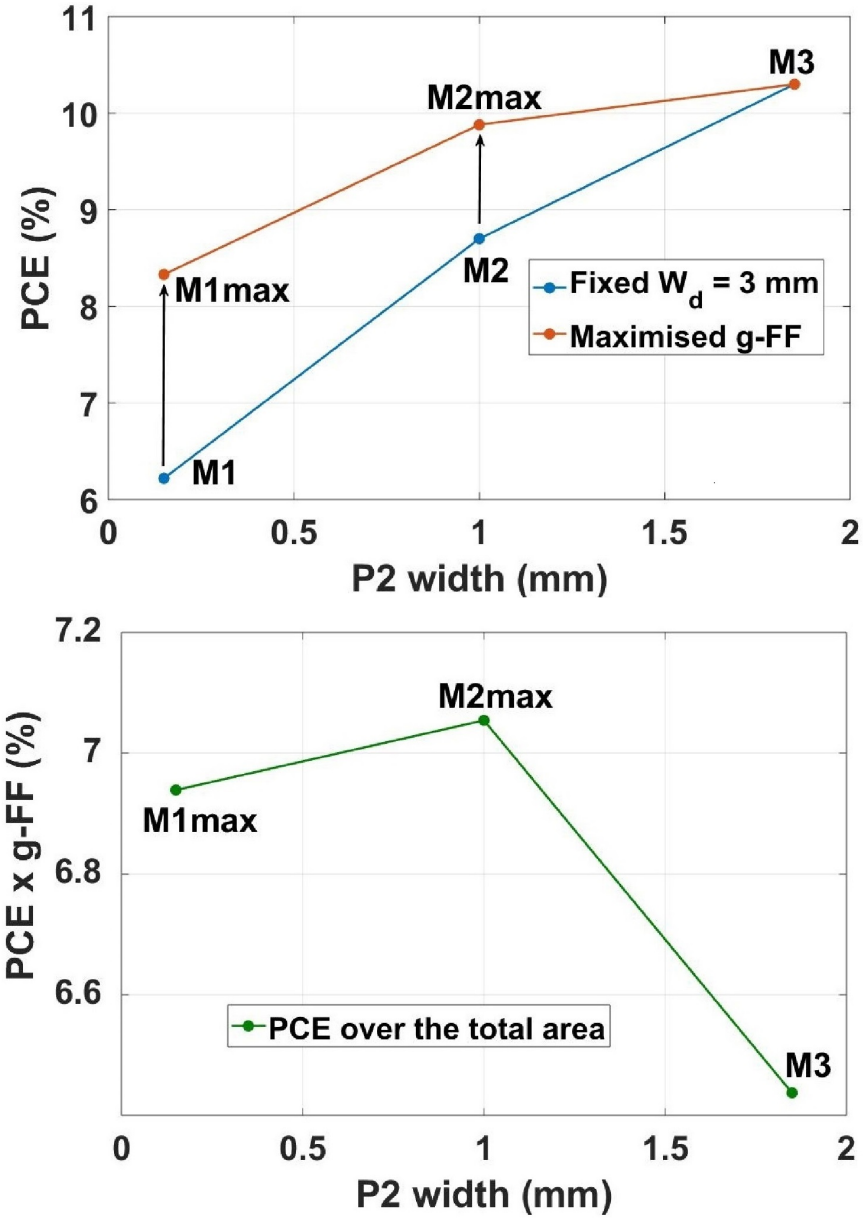


Figure 6.20: (a) The PCE of the best modules over the P2 size. The modules improve with the increase of the P2 scribe width and the minimisation of W_d. (b) The PCE over the total area (PCE × g-FF) of the best modules from M1max, M2max, and M3.

6.3.8 10 × 10 cm^2 module

It was decided to use the results obtained in Section 6.3.7 to further expand the size of the modules, from 5 × 5 cm^2 to 10 × 10 cm^2. The optimum design, i.e. M2max, was therefore utilised to prepare a 10 × 10 cm^2 device with 84-mm-long cells (n_c = 12) connected in series (P2 = 1 mm, W_d = 2 mm, W_a = 5 mm, P1 = 50 μm, P3 = 0.2 mm).

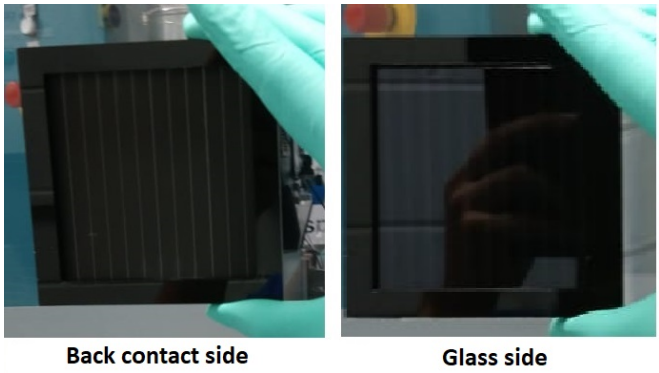


Figure 6.21: The 10 × 10 module, back and front.

The module with 50.04 cm^2 active area is shown from the back and front sides in Fig 6.21, and the results are shown in Fig 6.22. Despite the increased size of the device, the same design shows comparable performance from 5 × 5 cm^2 to 10 × 10 cm^2, i.e 10.37 %. All the PV parameters are comparable to the M2max layout, with Av-V_{oc} ∼ 870 mV, Min-J_{sc} ∼ 22.06 mA/cm^2, and FF ∼ 50 %.

This result demonstrates that the C-PSC modules can be easily scaled-up when homogeneous and defect-free layers are deposited.

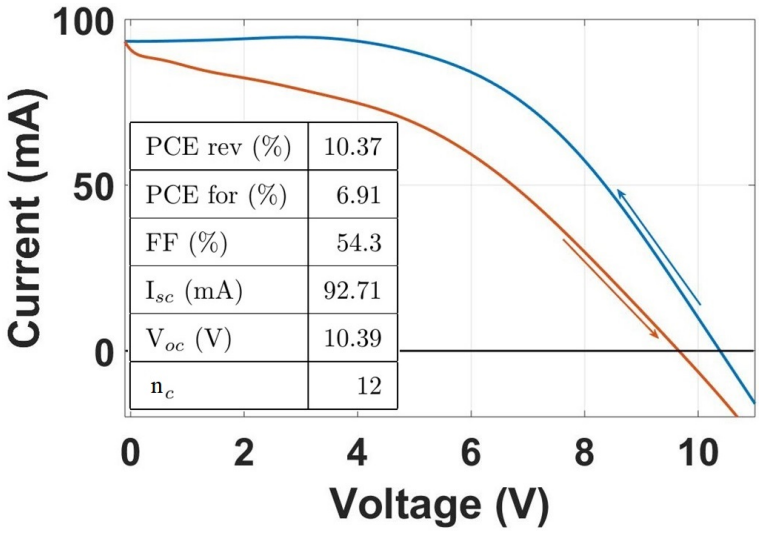


Figure 6.22: IV curve of the 10 × 10 cm^2 module with the M2max design. In the inset, the table describing the device parameters.

6.3.9 Large area module

Modules with over 200 cm^2 active area were also fabricated with the scribing method. The design criteria were:

- P2 width of around 1 mm;
- high g-FF at least over 70 %;
- W_a of around 5 mm;
- S1 and S2 as small as possible.

Because of the very high g-FF that is achievable, a smaller substrate can be employed. The substrate was 175 × 230 cm^2 to achieve around 200 cm^2 active area, comparable to the large area module in Section 5.3.4. The choice of the substrate size was also driven by need of using a flatter hot plate compared to that in Chapter 5. In this way, the bLayer could be sprayed at 300 °C as per the optimised method. The cells can be oriented along the substrate or perpendicularly. For the large area module in Section 5.3.4, the cells were oriented perpendicular to achieve the highest number of cells possible. Because of the high g-FF achievable with the scribing method, the module was designed to be oriented along the substrate, since a similar number of cells can fit on the short side of the module due to the small W_d. S1 and S2 spaces were minimised after the observation of the negative effect that they have on the PCE of modules. In order to achieve the round number 80 % g-FF, the W_a was slightly broadened (from 5 to 5.2 mm) and the P2 slightly narrow (from 1 to 0.8 mm). The design is shown in Tab 6.4 and Fig 6.23.

Table 6.4: Module design for large area modules.

P1 (μm)	P2 (mm)	P3 (mm)	g-FF (%)	W_a (mm)	W_d (mm)	S1 (mm)	S2 (mm)	n_c
50	0.8	0.2	80.0	5.2	1.3	0.11	0.13	22

The n_c in this design is the same of that of the module in Section 5.3.4 (i.e. 22) while the active area is increased, from 900 mm^2 to 1,019.2 mm^2 per cell, resulting in a total active area of 224.2 cm^2. The substrate is however around 30 % smaller than the substrate that was used in Section 5.3.4 (from 21 × 27.5 cm^2 to 17.5 × 23 cm^2), with a significant reduction in material consumption and manufacture complexity. Whereas the substrates for the large modules in Chapter 5 were around A4-size, the substrates for the large modules of this section were in the order of a large electronic device size, such as a tablet or an iPod. The fabrication of modules with higher active area on much smaller substrate was possible

because of the higher g-FF, from 45.5 % in Section 5.3.4 to 80 % for the module presented here.

Two large area modules were prepared with this design. The performance of the modules as fabricated, i.e. without any post-annealing treatment, was between 5 and 6 %, much higher than the modules presented in Section 5.3.4. Because the light soaking gives an enormous effect on AVA-MAPI C-PSC, the modules were measured at different illumination times (Fig 6.24).

As already known from the experience with the small single cells and modules, the PCE increases with the light soaking time. The main parameter that improves is the I_{sc}. The FF tends to increase until it reaches a plateau. The light soaking likely has a positive effect on the FF, but the increase in the current affects the FF, due to the iR-drop (Section 1.5.3). An improvement in FF only sometimes observed, in some cases FF can even decrease. The V_{oc} decreases in the first seconds of light soaking and then it stabilises over time. It could be that the V_{oc} suffers from the high temperature that the module reaches under illumination, due to thermal promotion of charge carriers into the conduction band. The use of a chiller would be beneficial for the V_{oc}.

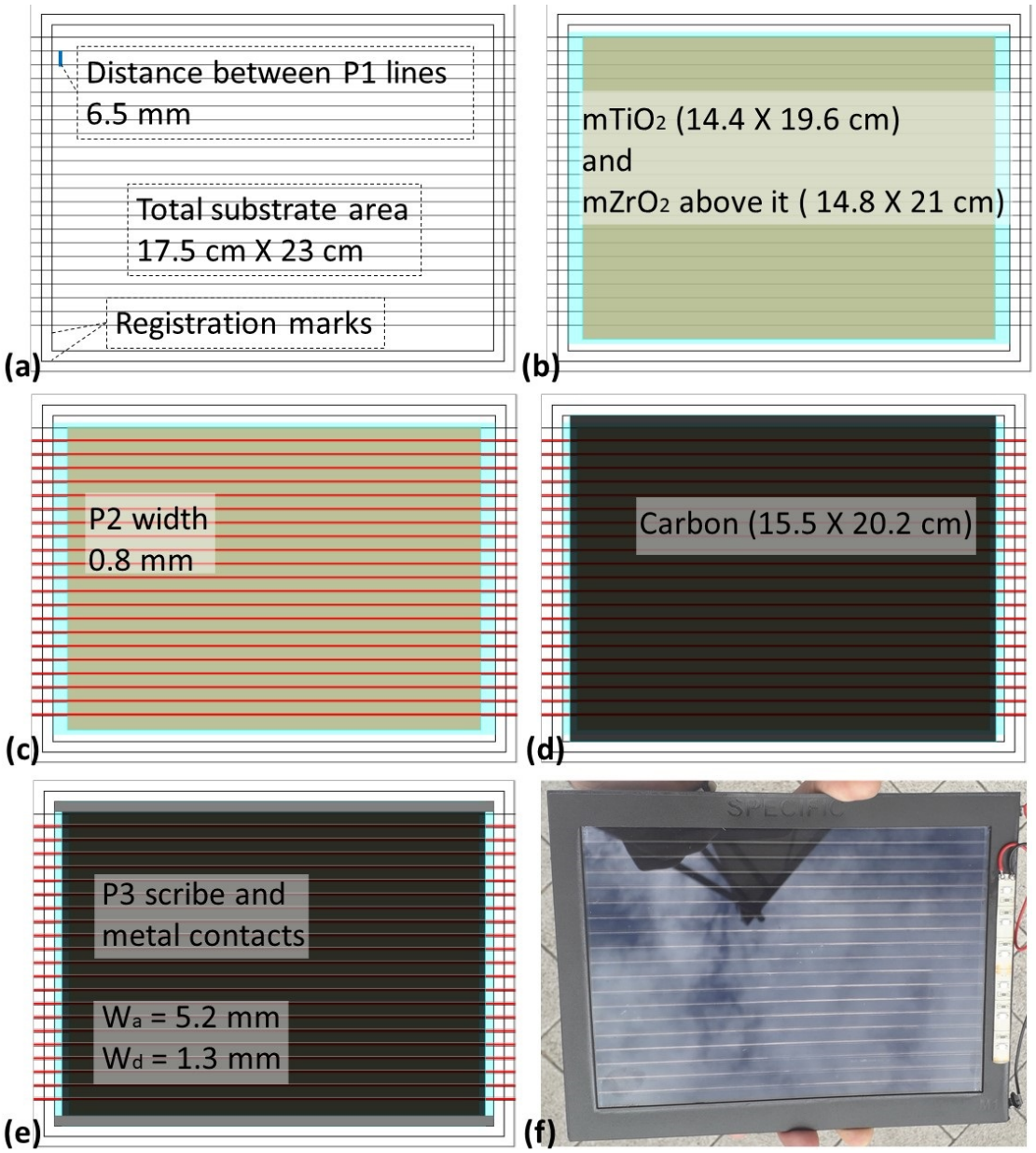
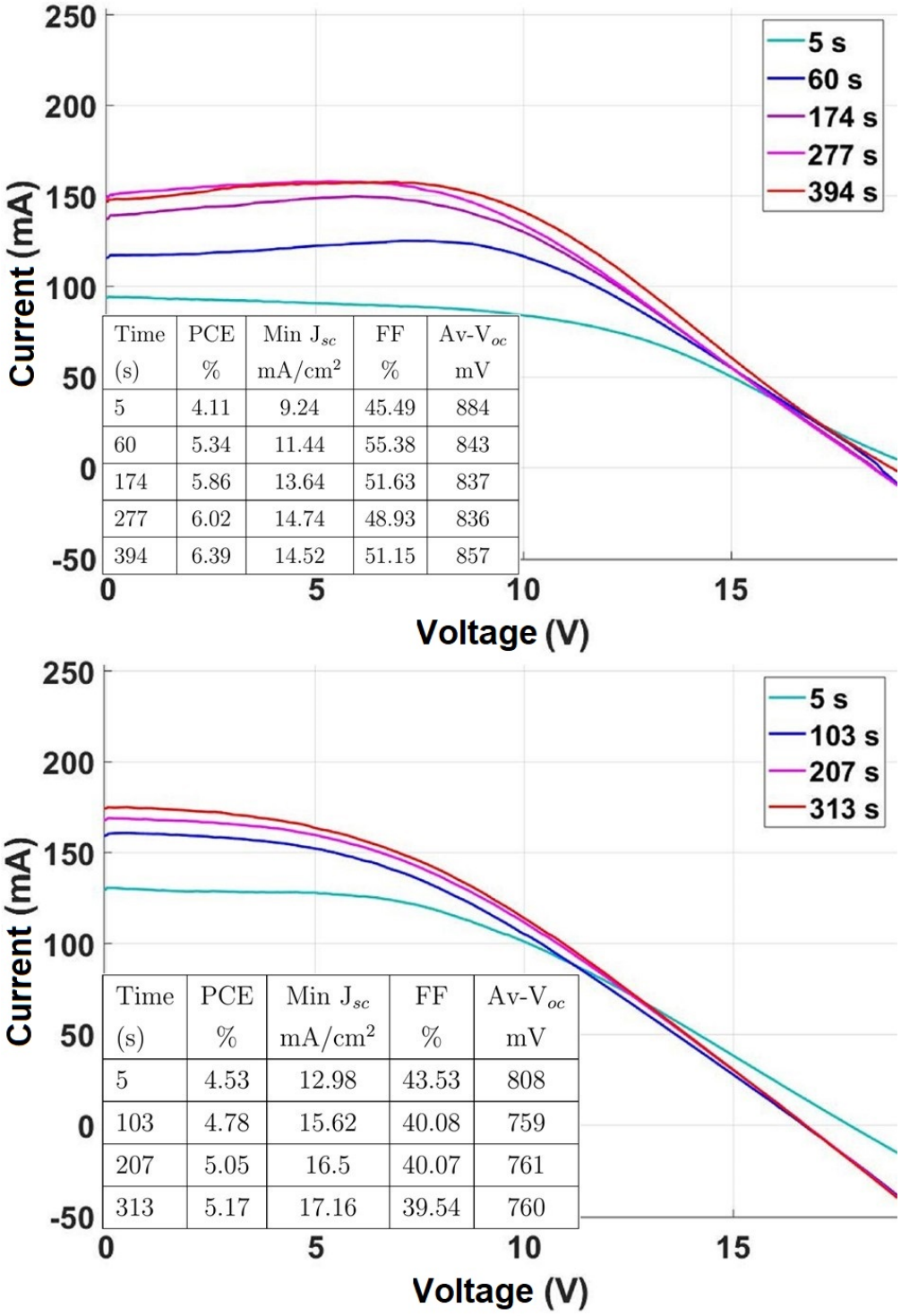


Figure 6.23: Large area module design via the scribing method (224.2 cm^2 active area). (a) FTO substrate with laser lines and marks. (b) $mTiO_2$ and $mZrO_2$ layers one over the other. ZrO_2 is slightly longer and larger than TiO_2 to completely cover it. (c) P2 scribes, 0.8 mm wide. (d) Carbon layer. The carbon layer is larger than ZrO_2 to allow the connection on the edges, but shorter than ZrO_2 to avoid short-circuits between cells. (e) Full finished module with P3 scribes and Ag contacts. (f) A photograph of a working module.



Time (s)	PCE %	Min J_{sc} mA/cm^2	FF %	Av-V_{oc} mV
5	4.11	9.24	45.49	884
60	5.34	11.44	55.38	843
174	5.86	13.64	51.63	837
277	6.02	14.74	48.93	836
394	6.39	14.52	51.15	857

Time (s)	PCE %	Min J_{sc} mA/cm^2	FF %	Av-V_{oc} mV
5	4.53	12.98	43.53	808
103	4.78	15.62	40.08	759
207	5.05	16.5	40.07	761
313	5.17	17.16	39.54	760

Figure 6.24: IV curves of large area modules. Each plot represents a different device with the same design. The evolution of the IV during the time while the module is kept under illumination is shown and the table reports the relative PV parameters.

6.4 Conclusion

The scribing method can be successfully utilised to achieve series connected modules with improved g-FF, by reducing the distance between the cells.

The three P1, P2, and P3 scribes were studied and optimised to find the best approach to obtain complete and selective material removal. For the P1, either the laser or the mechanical scribe can be utilised. However, the laser is by far the best option to achieve material removal in a narrow line space without affecting the thermal susceptibility of the substrate. For the P2, the mechanical approach can achieve selective material removal to open an aperture for the contact area. Only a laser that can be completely absorbed by the inter-electrode layers (here, TiO_2 and ZrO_2) could be used for the P2. In the case of the C-PSC architecture, a UV laser is likely most appropriate. For the P3, the mechanical scribe can achieve selective removal needed to disconnect the top carbon electrode between cells.

For the P2, a large scribe is required to enhance the FTO/carbon contact. The R_c was measured, proving the FTO/Ag contact superior to FTO/carbon, particularly for the way the contacts are scribed in the module design. Large P2 scribes with increased width were tested on real devices, confirming that the presence of large interconnects is beneficial for the module performance. When the cells are placed as close as possible, both g-FF and PCE improve, due to the geometry of the design and the reduced R_s between cells respectively. However, a large P2 has the opposite effect on R_c, which positively affects PCE but limit the minimisation of W_d. These conflicting effects called for an optimisation of the P2 width. Furthermore, the safe spaces between scribes (S1 and S2) have been shown to affect on recombination phenomena, making necessary their minimisation. The optimal design in terms of PCE $\times$ g-FF was found with P2 width = 1 mm, W_a = 5 mm and g-FF = 71.4 % in this set of experiments.

The C-PSC with optimal design was up-scaled to substrates of 10 $\times$ 10 cm, showing comparable performance to the 5 $\times$ 5 cm modules. This demonstrates the simplicity of up-scaling C-PSCs once both the architecture and design are optimised.

A very large module with an active area of 224.2 cm^2 was also manufactured. Mainly because of the minimisation of S1 and S2, 80 % g-FF was achieved. While the registration method resulted in modules on a record A4-sized substrate (Chapter 5), the scribing method allows the preparation of modules with the same number of cells and larger active area, but on much smaller substrates (a tablet or iPod size). The manufacture of the large area module via the scribing method is

the main outcome of this C-PSC up-scaling project, and proves that fabricating low capital cost and large area perovskite solar modules with high g-FF is feasible.

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Chapter 7

Conclusion

In this work, fully printable and low-cost carbon perovskite solar cells (C-PSC) were successfully manufactured from small 1 cm^2 single cells to large area 224.2 cm^2 series-connected modules.

The preparation of single cell devices was investigated in Chapter 3. The printing of the layers was assessed and the inorganic triple-mesoscopic stack was characterised. Baselines for C-PSC with infiltrated MAPI ($CH_3NH_3PbI_3$) or AVA-MAPI ($[NH_3(CH_2)_4COOH]_x(CH_3NH_3)_{1-x}PbI_3$) were established as starting point for the progress of this work. Some peculiar characteristics of AVA-MAPI were observed and reported in this thesis, including their higher stability and slower response compared to MAPI. The superior stability of AVA-MAPI was the reason for this work's main focus on 2D/3D perovskite, whereas MAPI was utilised for few specific studies. In addition, investigations on the effect of perovskite annealing, the bLayer deposition method and the thickness of mesoporous ZrO_2 ($mZrO_2$) on the AVA-MAPI C-PSC were also reported, showing the special nature of the 2D/3D perovskite in the triple mesoscopic stack.

For a successful up-scaling, the deposition of the materials is crucial. While the triple-mesoscopic stack can be prepared with scalable deposition methods, such as screen printing, perovskite is usually deposited via manual drop casting. This approach needed to be overcome for the fabrication of large area devices and the relative investigation is reported in Chapter 4. The investigation of the infiltration was simplified with the use of the 2-step deposition method for MAPI, so that the PbI_2 phase could be visually monitored. Because of the reorganisation of the solution on the hydrophobic carbon layer, the manual drop casting and the use of a robotic dispenser were not sufficient to achieve homogeneous infiltration. A fine mesh was utilised to aid the infiltration into the triple-mesoscopic stack. This infiltration method, that combines the use of a low-cost robotic dispenser and a

mesh, was named robotic mesh (RbM). Chemical mapping (Raman) and XRD sampling of the devices confirmed the higher homogeneity of this deposition when compared to the drop method. Moreover, this work added a new technique to the array of deposition methods for thin film technology, which was demonstrated successful for low viscosity inks on porous materials. The successful manufacture of cells via RbM confirmed the possibility of using the automatized method and unlocked the opportunity to deposit perovskite on modules.

The first trial of module manufacture was based on the registration method (Chapter 5). The optimal contact area was estimated by calculating the effect of the geometry and the sheet resistance of the electrode on the diode equation. The results were compared with values found in the literature, and a 5 mm stripe width was set for the single cells. The effect of the contact area was experimentally estimated, showing that relatively large contacts in the order of mm were necessary for the FTO/carbon interface. In terms of feasibility of manufacture of large area glass substrates, the deposition of the blocking Layer (bLayer) was modified, to avoid thermal stress and eventual cracking of the rigid substrate. A lower temperature was applied during the spray deposition of the bLayer precursor solution, but the final heating was performed at the same temperature as that used for smaller substrate. Despite the same final heating treatment, the crystallinity of the bLayer deposited at low temperature was much lower compared to the conventional one. With the outcome of the preliminary work on the registration method, it was possible to design and fabricate large area modules with 198 cm^2 active area and more than 6 % PCE.

The registration method suffers from the poor coverage of the substrate with active layers, evaluated with the geometric fill factor (g-FF). This is due to the presence of large interspace between the cells. This interspace was necessary to have a forgiving design in case of any misalignments of the layers. The scribing method allows a higher control over the manufacture of the interconnects and a better accuracy in the module fabrication. This higher control is beneficial to reduce the gap between the cells and enhance the design of the module. Laser and mechanical scribes were characterised. High quality scribes with width of around 50 μm on the FTO glass were achieved with the use of a green μs laser. Selective scribes on TiO_2 and ZrO_2 were not possible, due to the poor absorption of these layers in the visible light. The mechanical approach was successful for the patterning of TiO_2 and ZrO_2, showing also the possibility of mechanical removal of the bLayer. The modules were screen printed on substrates of glass/FTO/bLayer with laser pattern, whereas the porous layers were patterned mechanically. The

contact resistance in the interconnects was investigated via transmit line measurement (TLM) and module manufacture. The g-FF was also maximised and an optimal design to manufacture modules was estimated. As final step of the whole work, fully printable large area modules with 224.2 cm^2 were fabricated with 80 % g-FF and more than 6 % PCE. This was done with 5.2 mm cell width and 0.8 mm contact width.

This work also showed which are the critical points to be taken into consideration in order to improve the design quality of C-PSC modules. More conductive electrodes would be necessary to increase the cell width and reduce the contact area, with benefit for the g-FF. The mere increase of the carbon layer thickness is not a viable approach, because it could hinder the infiltration of perovskite and does not improve the vertical conductivity. Alternative or additional materials would be necessary. Metal bus bars could also be deposited at the interconnects to reduce the contact resistance. Furthermore, if expensive laser technology can be used for the low capital cost C-PSC, higher g-FF would be achievable because the width of the scribe can be reduced, especially the last pattern on the carbon layer. However, in this case a UV laser would be more indicated to allow a proper absorption from TiO_2 and ZrO_2. When the reduction in contact area and also the widening of the active cells are achievable without a consistent effect on the PCE, modules with more than 90 % g-FF would have potential for C-PSC architecture.

Thanks to the use of screen printing and mechanical scribing, modules based on inexpensive materials could be fabricated on pre-patterned FTO/bLayer glass substrates by any company that wants to produce high volume PV with low capital cost.

List of contributions

Journal publications at Swansea University:

- K. Hooper, H. Lee, M. Newman, S. Meroni, J. Baker, T. Watson, W. Tsoi, "Probing the degradation and homogeneity of embedded perovskite semiconducting layers in photovoltaic devices by Raman spectroscopy", Physical Chemistry Chemical Physics, 19 (2017), 5246-5253.

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- F. De Rossi, J. A Baker, D. Beynon, K. Hooper, S. Meroni, D. Williams, Z. Wei, A. Yasin, C. Charbonneau, E. Jewell, T. Watson, "All Printable Perovskite Solar Modules with 198 cm2 Active Area and Over 6% Efficiency", Advanced Materials Technologies, 3 (2018), 1800156.

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- H. Yates, S. Meroni, D. Raptis, J. Hodgkinson, T. Watson, "Flame assisted chemical vapour deposition NiO hole transport layers for mesoporous carbon perovskite cells", Journal of Materials Chemistry C, (2019), in press.

Oral presentations:

- PVSAT April 2017, Bangor (UK), "Novel deposition method to print binder-free inks on large scale carbon perovskite solar cells". Awarded with the best paper prize.
- PVSAT April 2018, London (UK), "Perovskite solar modules with 198 cm^2 active area: a study on the deposition of the compact Titania layer on large scale".
- ISFOE July 2018, Thessaloniki (Greece), "Design and optimisation of fully printable perovskite solar modules by scribing method".
- IMRC August 2018, Cancun (Mexico), "Scribing method for fully printable perovskite solar modules with large active area".

Poster presentations:

- Next Generation Materials for Solar Photovoltaics January 2016, London (UK).
- Hybrid and Organic Photovoltaics (HOPV) July 2016, Swansea (UK)
- Next Generation Materials for Solar Photovoltaics January 2018, London (UK).
- Hybrid and Organic Photovoltaics (HOPV) May 2018, Benidorm (Spain).
- International Workshop and Conference on Perovskite and Hybrid Photovoltaics (ICPHPV) February 2019, Delhi (India).
- Perovskite Solar cell and Optoelectronics Day June 2019, Oxford (UK).
- UK-China Workshop July 2019, Swansea (UK).

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