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Electrothermal simulations of Si and III-V nanowire field effect transistors: A non-equilibrium Green's function study

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Electro-thermal simulations in ultrascaled Si and InGaAs nanowire field effect transistors have been carried out. Devices with $2.2 \times 2.2\,nm^2$ and $3.6 \times 3.6\,nm^2$ cross-sections have been investigated. All the standard phonon scattering mechanisms for Si and InGaAs such as optical, polar optical (only for InGaAs), and acoustic phonon mechanisms have been considered. The Non-Equilibrium Green's Function formalism in concomitance with a renormalised 3D heat equation has been used to investigate the effect of self-heating. In addition, locally resolved electron power dissipation and temperature profiles have been extracted. The simulations showed that the heat dissipated inside the transistor increases as the nanowire cross-section decreases. It is also demonstrated that the commonly assumed Joule-heat dissipation overestimates the power dissipated in the transistors studied. It was found that in comparison with standard scattering simulations, electro-thermal simulations caused a 72% and 85% decrease in the current in $2.2 \times 2.2\,nm^2$ cross-section Si and InGaAs core NanoWire Field Effect Transistors , respectively, when compared with ballistic simulations. The corresponding decrease for scattering without self-heating was 45% and 70% respectively. *Published by AIP Publishing*. [http://dx.doi.org/10.1063/1.4998681]

I. INTRODUCTION

NanoWire Field Effect Transistors (NWFETs) are one of the potential candidates for replacing bulk MOSFET in nanoscale CMOS because of their superior electrostatic integrity.[1] Several groups have demonstrated the growth of nanowires of cylindrical, triangular, and rectangular cross-section[2–4] with cross-sections as small as 1 nm[5] and channel lengths below 10 nm.[6] Silicon (Si) is commonly used as a channel material in NWFETs, but III-V materials such as Indium Gallium Arsenide (InGaAs) are being considered due to their high mobility in comparison to Si.[7] In addition to this, digital circuits composed with 10 nm channel length nanowire transistors have been demonstrated.[8] The power dissipation in extremely scaled nanowire transistors due to series resistance has yet to be investigated in great detail. The power dissipation is of particular importance in small cross-section devices. This is because as the cross-section of the nanowire decreases, the effective electron-phonon coupling increases.[9] Therefore, it is expected that small cross-section nanowire transistors will have a short cooling time. After entering the drain the hot electrons will relax at a shorter distance, when compared with large cross-section devices.

Usually, the power dissipated inside the device is approximated by the well known Joule heating I·V, where I and V are the current and the voltage drop through the device, respectively.[10] For large devices, the aforementioned expression is correct as the device is considered in local equilibrium, i.e., the drift-diffusion approximation.[11,12] However, in the case of small devices and high electric fields, the power dissipated inside the transistor could be much less, as electrons travel a shorter distance than the energy mean free path. Therefore, a substantial amount of energy is dissipated deep in the drain region. This requires an energy-resolved carrier transport formalism.

The majority of work on power dissipation still uses the drift-diffusion formalism or Monte Carlo.[13] The drift-diffusion formalism cannot describe strong non-equilibrium conditions, as the distribution is always assumed to be in local equilibrium. Monte Carlo simulations are an energy-resolved transport methodology; however, it is assumed that the Broglie electron wavelength is much smaller than the dimension in which the electric field changes.[14] For transistors with sub-10 nm channel lengths, the electric field should change by one volt in a few nanometres, to keep the CMOS design specifications of power supply.

In addition, when the cross-section of the active region of the transistor is under 4 nm, the electron energy due to confinement is in the order of, or larger than, the thermal voltage. So the use of a subband structure in drift diffusion is required. In addition, Monte Carlo models are needed to accurately account for quantum confinement. However, the description of tunnelling requires a quantum mechanical description. It should also be noted that the Non-Equilibrium Green's Function (NEGF) formalism automatically takes into consideration the renormalisation of the Local Density Of States (LDOS) due to scattering processes, and the Pauli exclusion principle.

As a consequence of this, it is essential to use full quantum mechanical simulations to describe the carrier transport at these scales. Lake and Datta have calculated local power using the NEGF formalism in resonant tunnelling structures and other test structures but limited to the frozen field approximation.[16] Rhyner and Luisier have investigated self-heating in ultra-small Si NWFETs.[17,18] However, a detailed study of local power dissipation and self-heating using dissipative quantum transport formalism for III-V NWFETs and Si NWFETs of different dimensions is lacking in literature.

In this work, a self-consistent electro-thermal methodology using a renormalised Fourier law has been implemented in concomitance with the NEGF formalism. The aim of this paper is to the calculate the spatially resolved power dissipation and self-heating effects for Si and InGaAs in ultrascaled nanowire FETs, using a quantum transport formalism with a renormalised effective mass Hamiltonian. The relaxation of hot electrons in the drain has been investigated for various device dimensions. The temperature profile inside the nanowire has been computed and the reduction in drain current due to self-heating effect is also studied.

A 3D heat equation has been used to describe the heat transport, with the appropriate thermal conductivities and boundary conditions (BCs). Although simple, our model produces similar results to more sophisticated tight binding methodologies,[17] which include non-linear processes. Such methodologies are quite complex, as phonons and electrons are treated with the same degree of accuracy and the Hamiltonian matrix contains a large number of orbitals per atom. The calculation requires huge computational resources. The model presented here aims to be used as a designing tool in which speed and flexibilities are paramount. Our model intends to keep a measured amount of relevant physics without substantially compromising the accuracy of the results. Another advantage of our model is that the set of input parameters are smaller. The use of the heat equation in this smaller dimension has been encouraged by the qualitative success of a simpler model using a 1D heat equation in concomitance with NEGF to describe transport in similar dimension wires.[19] As will be presented later, our model produces the same maximum temperature and a similar temperature profile when compared with similar case using more sophisticated techniques.[17] It is important to mention that the local temperature considered here as well as in the previous mentioned papers is just the local average energy of the phonon system, as it is meaningless to talk of temperature at these smaller dimensions.[11]

The outline of the paper is as follows: Sec. II gives a brief description of the NEGF formalism and heat transport methodology, Sec. III A the self heating and local power dissipation results for Si NWFETs, Sec. III B the corresponding results for InGaAs NWFET, and Sec. III C a comparison of the results for Secs. III A and III B. The findings and conclusions are summarised in Sec. IV.

II. THEORY AND SIMULATION METHODOLOGY

The Non-equilibrium Green's Function (NEGF) formalism was introduced by Schwinger[20] and has been widely used to study dissipative quantum transport (i.e., inelastic electron-phonon transport) in nanotransistors.[21–25] The retarded Green's function is given by

$$[E-H_\nu(\vec{r}_1)]G^r_\nu(\vec{r}_1,\vec{r}_2;E)-\int d\vec{r}\,\Sigma^r_\nu(\vec{r}_1,\vec{r};E)G^r_\nu(\vec{r},\vec{r}_2;E) = \delta(\vec{r}_1,\vec{r}_2), \tag{1}$$

and the lesser-than and greater-than Green's functions by

$$G^{\lessgtr}(\vec{r}_1,\vec{r}_2;E)=\int d\vec{r}\int d\vec{r}'G^r_\nu(\vec{r}_1,\vec{r};E)\Sigma^{\lessgtr}_\nu(\vec{r},\vec{r}';E)G^a_\nu(\vec{r}',\vec{r}_2;E), \tag{2}$$

where ν denotes the valley index. In the NEGF formalism, the energy resolved electron current is given by

$$\vec{J}(\vec{r},E)=\frac{q\hbar}{4\pi m}lim_{r\to r'}(\nabla-\nabla')G^<(\vec{r},\vec{r}',E), \tag{3}$$

where E is the carrier energy, and q and m are the electron charge and effective mass, respectively. The energy current can then be written as

$$\vec{J}_{Energy}(\vec{r})=\int E\vec{J}(\vec{r},E)dE. \tag{4}$$

The divergence of Eq. (4) gives local power transfer from the electron to the lattice

$$P(\vec{r})=-\nabla\cdot\vec{J}_{Energy}(\vec{r}), \tag{5}$$

this can be broken down to show the Joule power and kinetic energy components

$$P(\vec{r})=-\nabla\cdot\vec{J}_K(\vec{r})+E(\vec{r})\cdot\vec{J}(\vec{r}). \tag{6}$$

The first term of the RHS of Eq. (6) is the change in the kinetic energy current of the electron ensemble. The second term is the local Joule power. If there are no hot electron phenomena, then the first term is zero; in this scenario, the electrons would follow the shape of the potential profile, hence the electron energy relative to the conduction band minima would not change (i.e., the electrons are in equilibrium). A negative change in the kinetic energy current would indicate the electron system was cooling and a positive change would indicate heating in the electron system. Using Eqs. (1) and (2), the local power dissipation can also be written as

$$-\nabla\cdot\vec{J}_{Energy}(\vec{r})=P(\vec{r})=\int E(G^<(\vec{r},\vec{r},E)\Sigma^>(\vec{r},\vec{r},E) - G^>(\vec{r},\vec{r},E)\Sigma^<(\vec{r},\vec{r},E))dE. \tag{7}$$

In our previous work,[26] it has been demonstrated that for a thin Si Gate-All-Around (GAA) nanowire, hot electrons require a very long drain in order to be thermalised. This length was around 100 nm. So, for a shorter drain region a substantial amount of electrons enter the broadened lead or the contact with energy larger than the thermal. Therefore, a fraction of joule power [the second term of Eq. (6)] is dissipated inside the drain of the transistor.

The Self-Consistent Born Approximation (SCBA) with local self-energies has been deployed. The Effective Mass Approximation (EMA) has been used, decomposing the 3D problem and allowing phonon scattering to be implemented efficiently. In practice, for a discrete system the NEGF equations are matrix equations. Only phonon scattering has been considered.

In the Si core NWFETs, X-X intervalley (for f-type and g-type phonons) and elastic acoustic phonon scattering have

TABLE I. InGaAs scattering parameters.

Acoustic scattering		
	Deformation potential (10^8 eV/cm)	
	5.24	
Non-polar optical phonon scattering (L-valley)		
	Deformation potential (10^8 eV/cm)	Phonon energy (meV)
	2.84	33.3
Polar optical phonon scattering (L-valley)		
	Phonon energy (meV)	
	36.0	
Intervalley phonon scattering		
	Deformation potential (10^8 eV/cm)	Phonon energy (meV)
Γ-L	7.55	28.9
Γ-X	6.0	31.2
L-L	6.2	31.9
L-X	5.4	28.6
X-X	3.25	31.7

been simulated. Even if the energy of the acoustic phonons plays a role in the thermalisation of hot electrons, the introduction of inelastic acoustic phonon will make the computation cumbersome. The implementation of the inelastic acoustic phonon in the NEGF formalism will require the separated inclusion of many phonon mechanisms as different acoustic phonon energies are considered. However, previous calculations using the phonon models of this paper have been shown to produce similar mobilities and current reductions to Ref. 27, which consider all phonon modes as inelastic and calculated the phonon dispersion law using tight-binding (TB) simulations. In addition, the impact of self-heating in the current voltage characteristic in this paper agrees with those in Ref. 17. This indicates that our model reproduces the essential trends of more sophisticated models.

In the III-V core devices, optical intervalley (Γ-L, L-X, Γ-X, X-X, L-L), optical and polar optical intravalley, and elastic acoustic phonon scattering have been considered.[14,15] The scattering parameters for InGaAs are collected in Table I. It is known that the polar optical matrix element does not evolve into a delta function. So, in principle, polar optical phonon scattering is intrinsically a non-local mechanism. This implies that the self-energies are non-diagonal in the spatial representation; however, the use of non-local energies will invalidate the recursive algorithm[28] which is used in this work, making the calculation almost intractable computationally. A preliminary study of non-local self-energies was carried out by Datta[29] and Price.[30] It was shown that for a simple Einstein phonon model, the off-diagonal element of the self-energy has a small contribution to the current. In addition, a short communication by Nikonov *et al.*[31] gives some insight into the plausibility of using local self-energies for polar optical phonons. The bandstructure of bulk InGaAs is shown in Fig. 1. In order of increasing energy, the valleys are Γ, L, and X. The effective masses have been extracted from tight-binding (TB) simulations and scaled to the cross-section of the NWFETs (see Table II).[32]

In order to study self-heating effects, a 3D Fourier heat equation is solved. The source term is obtained by Eq. (7). This allows the calculation of the 3D temperature profiles self-consistently with the NEGF equations. The metal gate

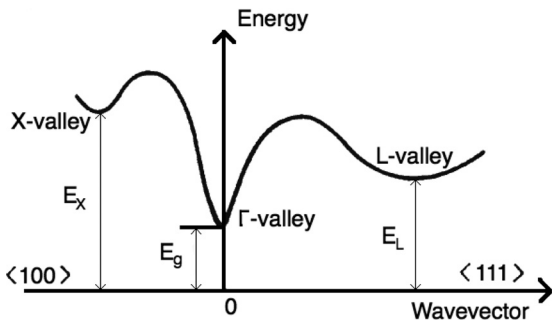

FIG. 1. Approximation of bandstructure of III-V materials in bulk.

TABLE II. Confinement effective masses for InGaAs (m_0).

	Γ-valley	L-valley	X-valley
$2.2 \times 2.2\,nm^2$	0.13	0.54	1.62
$3.6 \times 3.6\,nm^2$	0.108	0.45	1.35

contact planes are set to room temperature (300 K), i.e., Dirichlet's Boundary Conditions (BCs). All other planes are set to Neumann's conditions.[33] In addition, the bulk values for the thermal conductivity of Si and InGaAs are not valid

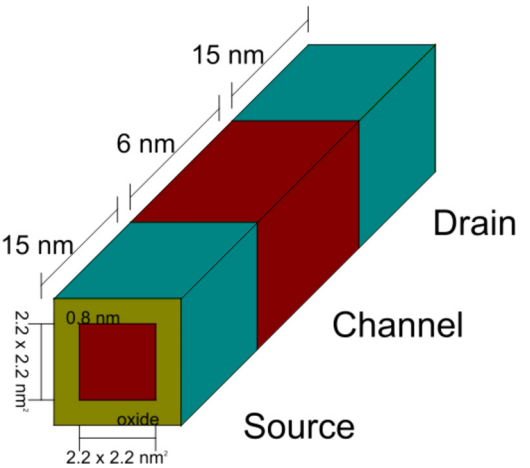

FIG. 2. Schematic of simulated NWFETs.

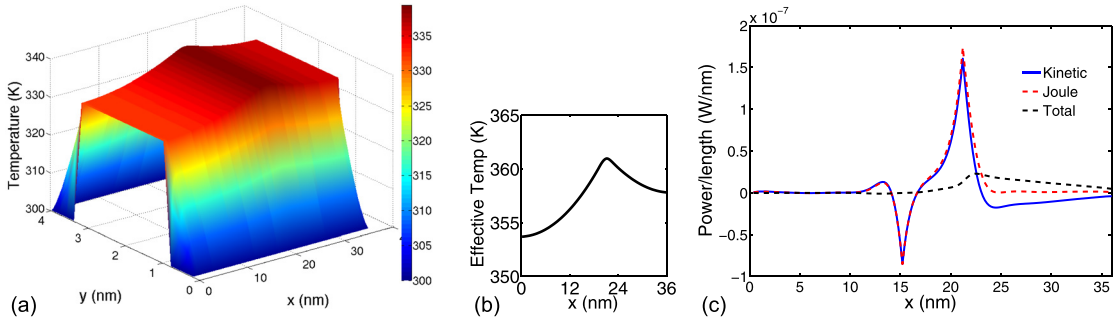

FIG. 3. Effective temperature profile in (a) 3d and (b) 1d. (c) Power dissipation for a $2.2 \times 2.2\,\text{nm}^2$ cross-section Si core NWFET at $V_D = 0.6\,\text{V}$, $V_G = 0.9\,\text{V}$.

at these dimensions. For the Si NWFET, a thermal conductivity of 28 W/m K has been assumed.[19] For the InGaAs NWFET, a thermal conductivity of 8 W/m K has been assumed.

In Ref. 19, the source and the drain are kept at 300 K, which is not what has been observed in more sophisticated calculations,[17] so our BCs in the source and the drain allow for increases in the source/drain temperatures. However, in Ref. 17 there is no heat flowing through the oxide when some heat should be flowing throughout the oxide. Therefore, our BCs provide some compromise between the two works.

III. RESULTS

Si and InGaAs core NWFETs with a $2.2 \times 2.2\,\text{nm}^2$ and $3.6 \times 3.6\,\text{nm}^2$ cross-section and a 6 nm channel length have been simulated. A schematic of the device is shown in Fig. 2. First, the power dissipation of the electrons and the 3D temperature profile inside the nanowire are presented for the different dimension devices, we then investigate the effect the self-heating has on the current by comparing with the current from standard scattering processes. Finally, the results of the Si and InGaAs core NWFETs are compared.

A. Si NWFET

Figure 3 shows the temperature profile and power dissipation for a $2.2 \times 2.2\,\text{nm}^2$ cross-section, Si core NWFET. The total power and the Joule power are $2.16 \times 10^{-7}\,\text{W}$ and $3.44 \times 10^{-7}\,\text{W}$, respectively. The peak temperature is 339 K. The I_D-V_G for this device is presented in Fig. 4(a). In comparison to ballistic simulations, standard scattering causes a 45% decrease in the current, whereas electrothermal simulations cause a 72% decrease in the current when compared to the ballistic case. The temperature profile and the power dissipation for the simulated $3.6 \times 3.6\,\text{nm}^2$ cross-section, Si core NWFET are presented in Fig. 5. The total power and the Joule power are $3.7 \times 10^{-7}\,\text{W}$ and $9.89 \times 10^{-7}\,\text{W}$, respectively. The peak temperature is 361 K. The I_D-V_G for this device is presented in Fig. 4(b). In comparison to ballistic simulations, scattering causes a 41% decrease in the current at high drain, whereas electrothermal simulations cause a 68% decrease in the current when compared to the ballistic case. The percentage reduction in the current decreases with increasing cross-section. This is because the strength of the electron-phonon coupling decreases as the cross-section increases. The greater decrease in the current for electrothermal simulations is because scattering processes increase with increasing temperature.

B. InGaAs NWFET

Figure 6 shows the temperature profile and the power dissipation for a $2.2 \times 2.2\,\text{nm}^2$ cross-section, InGaAs core NWFET. The total power and the Joule power are $5.48 \times 10^{-7}\,\text{W}$ and $7.69 \times 10^{-7}\,\text{W}$, respectively. The peak temperature is 350 K. The I_D-V_G for this device is presented in Fig. 7(a). In comparison to ballistic simulations, scattering causes a 70% decrease in the current, whereas electrothermal simulations cause a 85% decrease in the current when compared to the ballistic case. The temperature profile and the power dissipation for the simulated $3.6 \times 3.6\,\text{nm}^2$ cross-section, InGaAs core NWFET are presented in Fig. 8. The total power and the Joule power are $7.53 \times 10^{-7}\,\text{W}$ and $1.91 \times 10^{-6}\,\text{W}$, respectively. The peak temperature is 420 K. The I_D-V_G for this device is presented in Fig. 7(b). In comparison to ballistic simulations, scattering causes a 67% decrease in the current at high drain, whereas

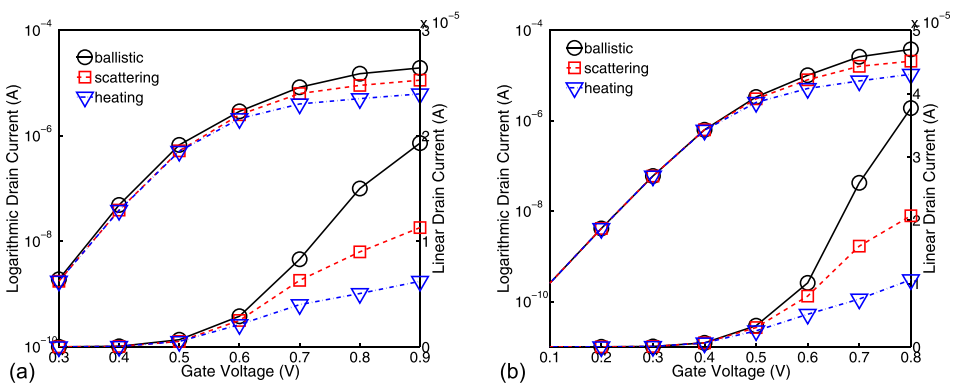

FIG. 4. I_D-V_G characteristics for (a) $2.2 \times 2.2\,\text{nm}^2$ and (b) $3.6 \times 3.6\,\text{nm}^2$ cross-section Si core NWFET at $V_D = 0.6\,\text{V}$, showing ballistic, electrothermal, and standard scattering simulations.

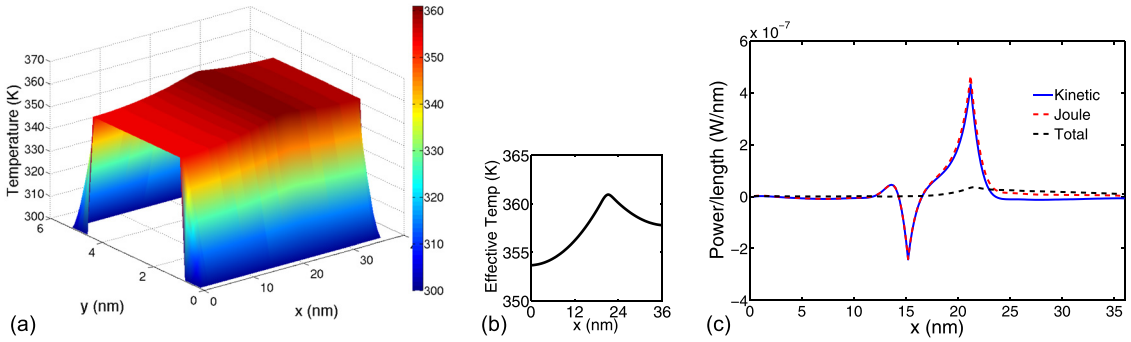

FIG. 5. Effective temperature profile in (a) 3d and (b) 1d. (c) Power dissipation for a $3.6 \times 3.6\,\mathrm{nm}^2$ cross-section Si core NWFET at $V_D = 0.6\,V$, $V_G = 0.9\,V$.

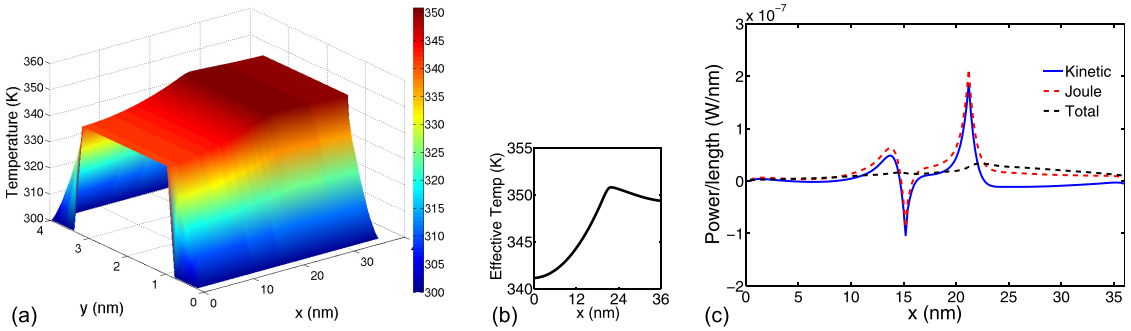

FIG. 6. Effective temperature profile in (a) 3d and (b) 1d. (c) Power dissipation for a $2.2 \times 2.2\,\mathrm{nm}^2$ cross-section InGaAs core NWFET at $V_D = 0.6\,V$, $V_G = 0.9\,V$.

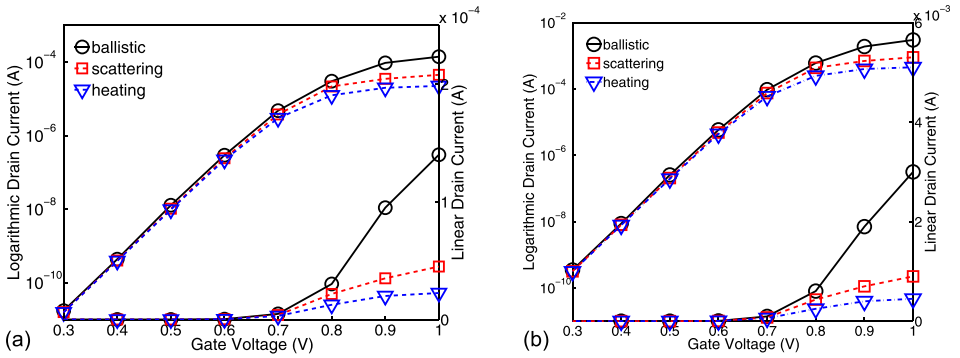

FIG. 7. I_D-V_G characteristics for (a) $2.2 \times 2.2\,\mathrm{nm}^2$ and (b) $3.6 \times 3.6\,\mathrm{nm}^2$ cross-section InGaAs core NWFET at $V_D = 0.6\,V$, showing ballistic, electrothermal, and standard scattering simulations.

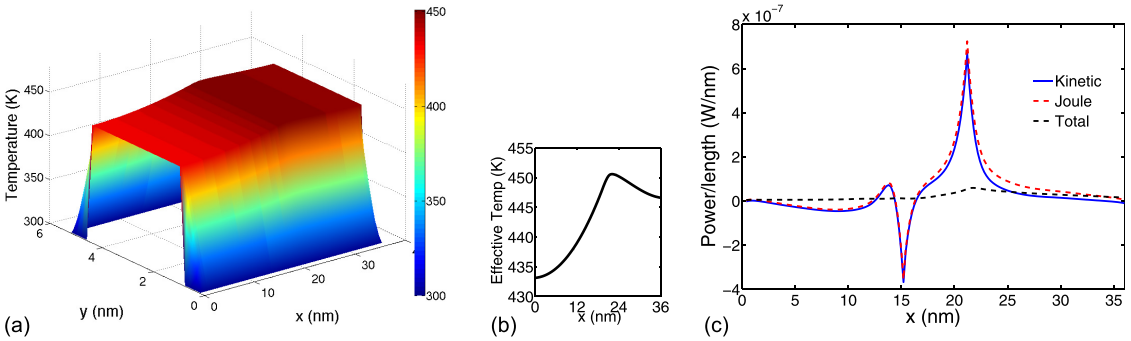

FIG. 8. Effective temperature profile in (a) 3d and (b) 1d. (c) Power dissipation for a $3.6 \times 3.6\,\mathrm{nm}^2$ cross-section InGaAs core NWFET at $V_D = 0.6\,V$, $V_G = 0.9\,V$.

electrothermal simulations cause a 80% decrease in the current when compared to the ballistic case.

C. Comparison between the Si and InGaAs NWFETs

For the $2.2 \times 2.2\,\mathrm{nm}^2$ cross-section InGaAs, scattering and heating cause a 25% and 13% greater decrease in the current in comparison to the same dimension Si NWFET. The current spectra along the length of the nanowire for the $2.2 \times 2.2\,\mathrm{nm}^2$ cross-section, Si and InGaAs core NWFETs are shown in Fig. 9. The average current energy is denoted by the solid white line. The average current energy decreases with distance within the drain as expected, due to the energy

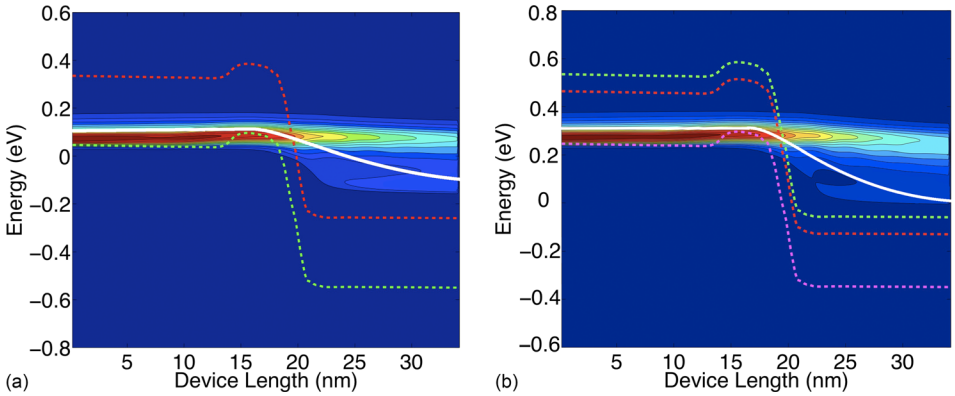

FIG. 9. Energy-resolved current spectra for a $2.2 \times 2.2\,\mathrm{nm}^2$ cross-section: (a) Si and (b) InGaAs core NWFET with the average current energy (solid white line).

TABLE III. Current reduction and peak effective temperature for all simulated NWFETs.

	Total × 100/J	Current reduction scattering %	Current reduction heating %	Peak temperature (K)
Si $2.2 \times 2.2\,\mathrm{nm}^2$	63	45	72	339
Si $3.6 \times 3.6\,\mathrm{nm}^2$	37	41	68	361
InGaAs $2.2 \times 2.2\,\mathrm{nm}^2$	71	70	85	350
InGaAs $3.6 \times 3.6\,\mathrm{nm}^2$	39	67	80	420

TABLE IV. Total power and Joule power in all simulated NWFETs.

	Total power (W)	Joule power (W)
Si $2.2 \times 2.2\,\mathrm{nm}^2$	2.16×10^{-7}	3.44×10^{-7}
Si $3.6 \times 3.6\,\mathrm{nm}^2$	3.70×10^{-7}	9.89×10^{-7}
InGaAs $2.2 \times 2.2\,\mathrm{nm}^2$	5.48×10^{-7}	7.69×10^{-7}
InGaAs $3.6 \times 3.6\,\mathrm{nm}^2$	7.53×10^{-7}	1.91×10^{-6}

relaxation of the hot electrons as they move through the drain.

Tables III and IV highlight the main results of this paper; the power dissipation and the current reduction percentage due to scattering and heating relative to the ballistic simulations are shown. The peak temperatures are also shown. Overall, the InGaAs NWFETs show a greater reduction in the current than the Si NWFETs. Strong polar scattering in InGaAs is the reason behind the large scattering rates for this material. The current reduction changes just slightly between the two cross sections studied. Large current reductions have been observed but for a much larger difference in cross-section.[24] However, due to the short channel length, tunnelling should play a role at large cross section compensating for the decrease of electron-phonon scattering due to the increased cross-section. The change in momentum is the major driver of current reduction and occurs mainly in the channel region where tunnelling dominates. However, power dissipation is more directly related with inelastic phonon scatterings or dissipative processes and is mainly located at the drain extensions in which a large potential drop occurs. This implies that small cross section devices have a substantially larger percentage of power dissipation than their large cross section counterparts.

As seen from the table, the effect of self-heating in the transport is large in the silicon devices even if the temperature rise is lower than the III-V counterpart. This is a result of the fact that the dominant scattering mechanism in Silicon is acoustic phonons in which electron-phonon coupling is directly proportional to the temperature. However, in III-V materials, the relevant process is polar scattering, which have weaker temperature dependence. The large temperatures in III-V devices as compared to Si ones are a result of various reasons: (i) dissipation is stronger and (ii) thermal conductivity is smaller. The above descriptions need to be taken with care, as they are only valid for the device dimensions explored in this paper. Changes in masses due to confinement; tunnelling; and variations in thermal conductivities, in concomitance with changes in local density of states, are some of the factors which strongly affect small devices.

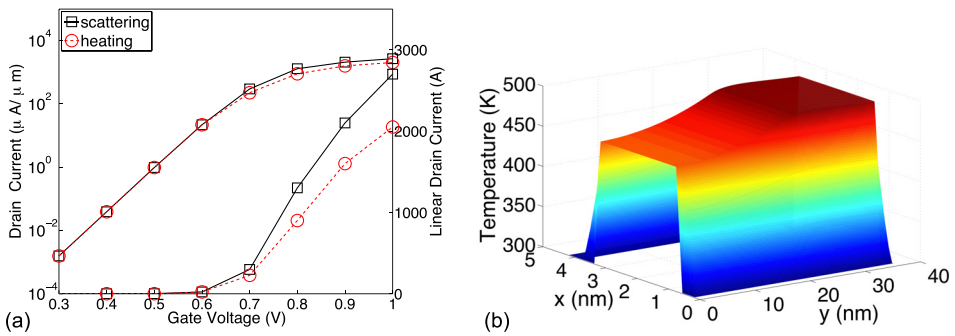

FIG. 10. (a) I_D-V_G characteristics for a Si core NWFET at $V_D = 0.6$ V matched to Fig. 3 in Ref. 17 showing electrothermal and standard scattering simulations and (b) the corresponding effective temperature profile.

Finally, it would be desirable to compare the model used in this work with much more complex models.[17] It is not expected that both models will agree as one is using a renormalised heat equation and the other the full NEGF formalism to describe phonon as well as electrons and also the using a full band approach. For this case, we considered the results obtained from the effective temperature profile of a 3 nm diameter cylindrical Si GAA NWFET with a 0.6 nm oxide, as presented in Ref. 17. This reference shows a peak effective temperature of 480 K. Figure 10 shows the corresponding I_D-V_G and effective temperature at high gate, for our $3.6 \times 3.6\,nm^2$ Si NWFET, which has a similar level of current as given in Fig. 3 of Ref. 16. In addition, the reduction of the drain current due to self-heating is 66%, in good agreement with the results of Ref. 17, Fig. 3. The peak effective temperature is 485 K, showing a good agreement with Fig. 5 of Ref. 17. The fact that the profile and the peak temperature are similar for this particular case is an indication that at least from a design point of view, this simple model could potentially be used to evaluate electrothermal effects at the nanoscale. It should be noted that the thermal conductivities used are those provided in the literature, so in this case, no attempt to calibrate our results with these in Ref. 17 has been carried out.

IV. CONCLUSION

The NEGF formalism has been used to perform electrothermal simulations of Si and InGaAs NWFETs. Two cross-sections were considered. It was found that electrothermal simulations caused a 72% and 85% decrease in the current in the $2.2 \times 2.2\,nm^2$ cross-section Si and InGaAs core NWFETs, respectively. At high drain and gate bias, the total power dissipation was 2.16×10^{-7} W and 5.48×10^{-7} W for the $2.2 \times 2.2\,nm^2$ cross-section Si and InGaAs core NWFETs, respectively.

For the $3.6 \times 3.6\,nm^2$ cross-section, electrothermal simulations caused a 62% and 80% decrease in the current in the Si and InGaAs core NWFETs, respectively. At high drain and gate bias, the total power dissipation was 2.16×10^{-7} W and 5.48×10^{-7} W for the Si and InGaAs core NWFETs, respectively. Overall, there was greater power dissipation and therefore a greater effective temperature in the InGaAs NWFET, with a peak temperature 420 K in the $3.6 \times 3.6\,nm^2$ cross-section device in comparison to a peak temperature of 350 K in the equivalent Si NWFET. Finally, we have presented a model combining the NEGF with the heat equation that could be used for nanoscale electrothermal simulations. The results obtained are in qualitative agreement with some of the results obtained using more sophisticated models. This brings the possibility to use this model, if properly calibrated, to study the impact of self-heating in nanoscale devices.

[1]See http://www.itrs2.net/ for the section of scaled device in International Technology Roadmap for Semiconductors (ITRS) Emerging Research Materials (ERM) White Paper Rev 2 [03/14/2014].
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