Analysis of Potential and Electron Density Behaviour in Extremely Scaled Si and InGaAs MOSFETs Applying Monte Carlo Simulations

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Abstract. Scaling of Silicon and InGaAs MOSFETs of a 25 nm gate length till shortest gate length of 5 nm, simulated this nano-device by Monte Carlo (MC) with quantum corrections. The transistors are scaled-down only in lateral dimensions in order to study electron transport approaching a ballistic limit along the scaled channel following experimental works. These MC simulations are able to give detailed insight into physical behaviour of electron velocity, electron density, and potential in relation to the drive current. We found that electron peak velocity increases during the scaling in Si MOSFETs till the 10 nm gate length and then dramatically declines due to a strong long-range Coulomb interaction among the source and the drain [16]. This effect is not observed in the equivalent InGaAs MOSFETs in which electron peak velocity exhibits double peak which steadily increases during the scaling [16]. However, the increasing of current in the equivalent InGaAs MOSFETs is moderate, by about 24 %, by comparing of current in the Si MOSFETs of 74 % delivered by 5 nm channel transistor.

1. Introduction

CMOS (Complementary Metal-Oxide-Semiconductor) Si (Silicon) technology must to accommodate numerous non-standard solutions for the scaling of MOSFETs to continue. These non-standard solutions include a channel strain [1], raised source/drain contacts [2], metal gate--high-κ dielectric material [3], and multi-gate non-planar architectures [4]. One of intensively researched non-standard solutions is a replacement of the Si channel with a high-mobility semiconductor material and the winning choice emerges to be InGaAs for an n-type channel [5]. However, the International Technology Roadmap for semiconductors (ITRS) [6], IMEC [7] estimates that the gate length in multiple processor units (MPUs) will target less than 5-nm in 2021. The goal is to reach close to ballistic transport with scaling down [8] and thus to increase the drive current and to decrease the switching time. However, experiments indicate that electron mobility and drift velocity into the channel will substantially decline by scaling of 25-nm gate length thus preventing to reach not just the ballistic transport regime but also the desired close-to-the-ballistic regime [9,10].

In this simulation work, we investigate the finite element ensemble MC device simulation toolbox MC/MOS [11, 12, 13] to obtain the characteristics I_D -V_G for 25 nm gate length of Si MOSFET [14, 15] and for the 25 nm InGaAs MOSFET [16]. The I_D -V_G characteristics of the Si MOSFET are compared against the other work of MC simulations while the characteristics of the III-V MOSFET are predicted by the MC code verified by experimental work from multiple low and high Indium

content channel MOSFETs and HEMTs [12, 13]. After this verification of the MC/MOS, we do scaling the Si and InGaAs transistors from a gate length of 25 nm scaling down to gate lengths of 5 nm only in intervals of 5. This systematic lateral only scaling follows the experimental works [8, 9, 10] aiming to determine how the carrier transport approaches a ballistic limit with the channel scaling [13, 16]. In order to have a detailed insight into non-equilibrium carrier transport at nanoscale under extremely high electric fields, we study the physical mechanisms for determining the average carrier velocity [16], 2D electrostatic potential, and electron density profiles across the channel with reducing gate length at the drive bias at which transistors operate in on-regime [8]. We have observed the electron density at the area of the source and drain side remains almost unchanged throughout the scaling process in Si nano-transistors when compared with III-V materials. While scaling, the depletion area will be decreased whereas the electron density along channel gradually increases near drain of the nano-transistor as observed in that of 5 nm gate length. Alternatively, the same scaling process that is carried out on $In_{0.3}Ga_{0.7}As$ MOSFETs, will not result in a remarkable increase of the electron density along the channel near the drain of the transistor even the increase of the electron density at the source. The drain on-current for InGaAs MOSFET is comparatively high when compared with Si MOSFET due to strong injection velocity.

2. MOS Structures for Si and InGaAs MOSFETs

Initial investigations of the Si and InGaAs MOSFETs are carried out on respective MOS structures obtained in the middle of the gate through the channel. The MOS structures are studied using 1D Poisson-Schrödinger solver which are solved self-consistently. The obtained energy states (eigen level) and electron wavefunctions (eigen function) are applied to compute electron density which results bring to sheet density across the gate length at applied biasing [17]. A device structure with the gate length of 25 nm Si MOSFET which has a p-type semiconductor, dielectric material of oxynitride (ON) with a diameter of 1.6 nm and a dielectric constant of ε_{ON} = 7, used metal gate is shown in Figure 1. Energy levels, wavefunctions, conduction band profile, and electron concentration in the respective MOS structure are shown in Figure 2. The electron density which is classically developed, where we observed maximum peak at the interface, shows larger electron density comparing to electron density in quantum-mechanically. We observed the electron density in quantum-mechanically, which is smaller and the displacement of the peak from the interface after comparing to the classical development [17, 21].

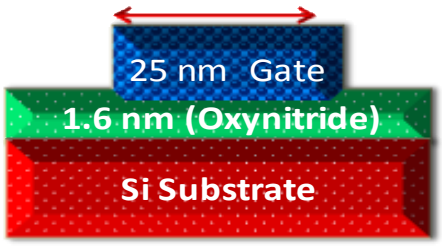


Figure 1. A schematic MOS structure of 25 nm gate length Si MOSFET with p-type Si substrate.

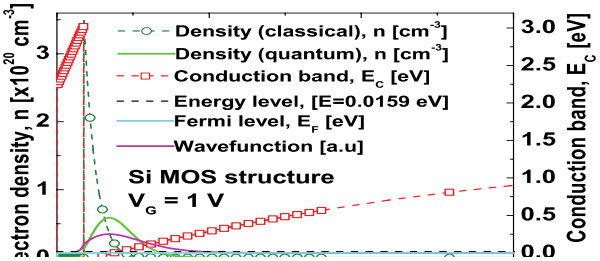


Figure 2. Conduction band and electron density, energy level, Fermi energy level and a wavefunction across the channel for the Si MOS structure.

The InGaAs MOSFET structure which has InGaAs channel with a diameter of 5 nm, Gadolinium Gallium Oxide (GGO) as a gate dielectric, whose diameter is 1.5 nm and dielectric constant is ε_{GGO} = 20. The channel is positioned within 1.5 nm thick AlGaAs layer and the 3 nm thick AlGaAs layer. A δ-doping level is positioned under the channel with a concentration of 7 x 10^{12} cm^{-2}. The AlGaAs layer at the foundation is developed with a thick buffer level of 50 nm as shown in Figure 3. The entire structure is extended on a GaAs substrate.

Figure 4 shows the conduction band, electron density (classical and quantum-mechanical), energy levels and Fermi energy for the 15 nm gate length InGaAs MOSFET biased at V_G = 1.0 V. We observe five discrete energy levels at this high bias with one deep ground level and four levels close

to the well edge. The classically developed electron density which has maxima of density at edges of the quantum well as expected. The electron density is developed in quantum-mechanically which maxima displaces apart from the gate towards the bottom of the channel [21].

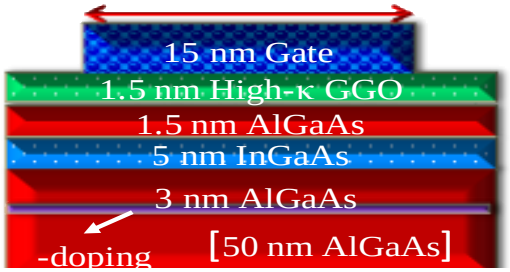


Figure 3. A schematic MOS heterostructure for InGaAs of 25 nm gate length.

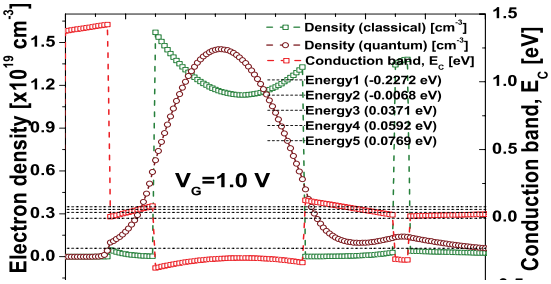


Figure 4. Conduction band and electron density, energy level, Fermi energy level and a wavefunction across the channel for InGaAs.

3. Monte Carlo Engine

A core of analysis including predictions of I_D-V_G characteristics during extreme lateral scaling to 5 nm gate length is performed with the heterostructure MC device simulator MC/MOS [11, 12, 13]. The MC simulation uses non-parabolic analytical bandstructure model with anisotropic valleys (Γ, L, and X). The most appropriate scattering mechanisms in Si [18, 19] are included in the simulation of Si MOSFET, such as acoustic phonons, non-polar optical phonons, interface roughness established on Ando's model [12] intra-valley, inter-valley and ionized impurity scattering. The electron scattering with polar optical phonons, inter-valley and intra-valley optical phonons, non-polar optical phonons, acoustic phonons, interface roughness, and interface phonons [20], and ionised impurity scattering in the simulation of InGaAs MOSFET. The effect of strain is also included in the InGaAs channel using a phenomenological model for tensile strain induced on the lattice direction in the channel along x-y axis, the so-called biaxial strain [22]. The model affects bandgap, band-offset, electron effective mass, energy position of L and X valleys, polar optical deformation potential and phonon energies. Finally, the alloy scattering is also applied in the channel of InGaAs MOSFET [24, 11, 23]. Source/drain of the MOSFETs are heavily doped, MC device simulations include Fermi-Dirac statistics by self-consistently developing Fermi level and electron temperature in the device mesh at MC time step [13, 25]. The determined electron temperature and Fermi level are then applied in a static screening model for the ionised impurity scattering [26]. Finally, quantum corrections is considered in the MC device simulations [16, 27].

4. $I_D - V_G$ Characteristics

Figure 5 exhibits the specimen of a n-channel Si MOSFET (25 nm gate length) with an oxide-nitride (ON) dielectric gate stack and a metal gate (workfunction of 4.05 eV) which was designed as a arrangement of transistor for the SiNANO consortium [14, 15] in order to compare different simulation techniques and tools. The device consists of source/drain (n-type) and extensions regions, both with heavily doped concentration of 1 x 10^{20} cm^{-3}, a halo p-type doping with a concentration of 8 x 10^{18} cm^{-3}, and a p-type substrate doping concentration of 3 x 10^{18} cm^{-3}.

Fig 6 shows the comparing results of MC simulated I_D - V_G characteristics for the 25 nm gate length Si MOSFET with drain biases of 0.1 V and 1.1 V, respectively. The stars show the outcome from the obtaining codes of CNRS, the squares are those from ETHZ, circles and triangles are the outcomes from our obtained simulation results (MC/MOS/QC and MC/MOS). The properties developed from our MC/MOS simulation compared to those developed from MC simulations executed with ETHZ and CNRS MC codes [14], which are exhibiting an excellent uniformity. The ETHZ and CNRS MC codes originates from i) Eidgenoeessische Technische Hochschule Zurich, a MC device code which implements a full-band structure of Si, the transport is simulated along the <100> direction but quantum corrections are not considered into account [29, 30], and ii) Centre National de la Recherche and Scientifique, a MC device code which implements an anisotropic X-

valley analytical model for the Si bandstructure and quantum corrections have also not been taken into account [31, 32]. The open diamonds show the results of MC simulator with implemented quantum corrections applying the effective quantum potential method (MC/MOS/QC) [28].

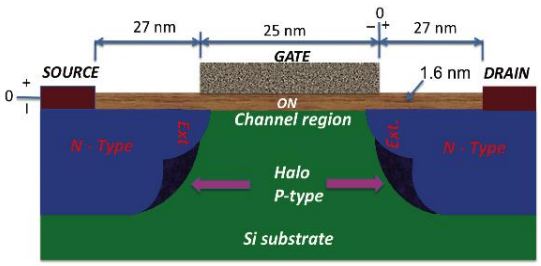


Figure 5. Illustration of the verified 25 nm gate length, n-channel Si MOSFETs.

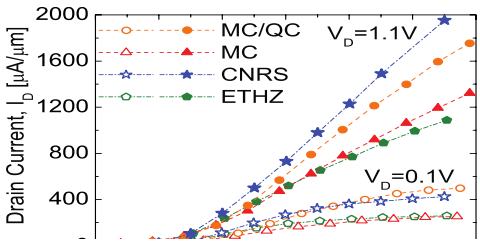


Figure 6. I-V properties of 25 nm gate length Si MOSFET biased at V_D = 0.1 V, and V_D = 1 V, contrasting with others MC simulations.

Figure 7 shows n-channel InGaAs MOSFET of 25 nm gate length with a spacer of 26 nm. This transistor be made up of a GaAs substrate, 7 nm layer InGaAs channel, a 4.6 nm layer of high dielectric (GGO, $\kappa = 20$) material dividing the channel from a metal gate (workfunction of 4.05 eV). The formation has a foundation consistent p-type doping of 1 x 10^{18} cm^{-3} and n-type peak doping of 2 x 10^{19} cm^{-3} in the S/D contacts [34]. The doping and geometrical profile of Si and InGaAs MOSFETs have been selected to be as close as possible. For both devices, the gate lengths are equal in measurement (25 nm), only the spacers differ by 1 nm (see Figures 5, 7). The major contrast are in doping because III-V semiconductors has lower maximum doping activation [13] comparing to Si whereas they contribute very close electrostatics. Figure 8 shows the characteristics of I_D - V_G for the case of 25 nm gate length InGaAs MOSFET, at drain biases of 0.05 V and 1.0 V. The device of InGaAs MOSFET delivers an on-current of 2200 μA/μm at the overdrive of 1.0 V, which is more than 20% larger than the on-current delivered by the equivalent Si MOSFET (1800 μA/μm). The observed larger drain current at the high drain bias in the III-V MOSFET is caused by the strong injection velocity even shows lower carrier density in the channel of the nano-device. The higher injection velocity assurance a faster switching speed, as a result this is one of the main drivers of the current research into III-V MOSFETs [33].

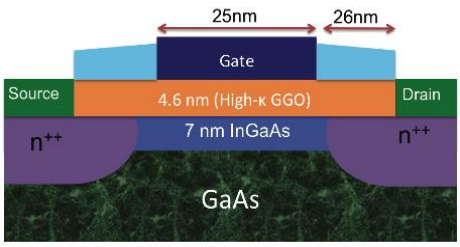


Figure 7. Cross-section of the verified 25 nm gate length, n-channel Si MOSFETs.

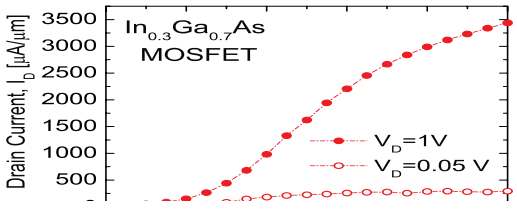
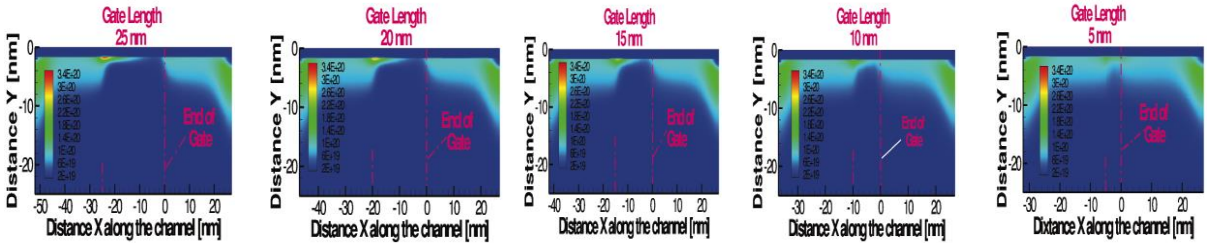


Figure 8. I-V characteristics of 25 nm gate length InGaAs channel MOSFET, biasing at V_D = 0.1 V, and V_D = 1 V

5. Carrier Density and Potential Profile

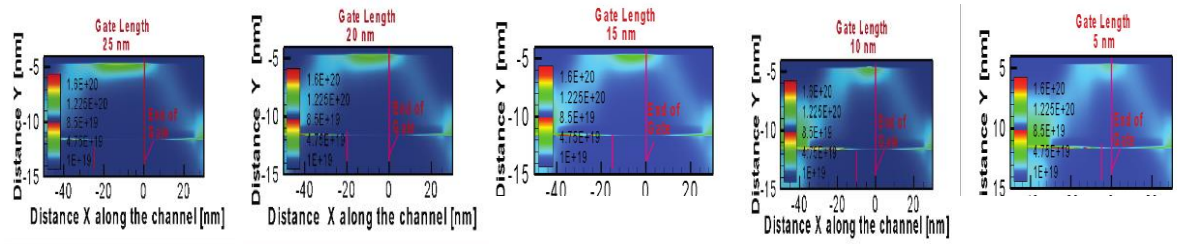
Figures 9 show an electron density profile in the scaled Si MOSFETs, biased at V_G -V_T = 1.0 V and V_D =1.0 V. The width of the large density gradually increases with decreasing gate length (from 25 nm to 5 nm) as expected. The channel thickness is quite narrow for the 25, 20, and 15 nm gate length transistors indicating that the gate keeps a good control over electron transport. However, when the gate is scaled down to 10 and 5 nm, the channel starts to leak as the gate is losing control over flow of the electrons through the channel due to a lack of the vertical scaling. During the scaling process, the depletion region is decreased and the carrier density in the Si channel moderately enhances resulting in increase in the drive current. The increase of the electron concentration in the channel promotes to

the enhance in electron scattering, which result brings a decreasing of electron velocity. We can also observe a high density region at the beginning of the gate, close to the interface, in every scaled transistor which is the result of electron injection and backscattering.



(a) (b) (c) (d) (e)

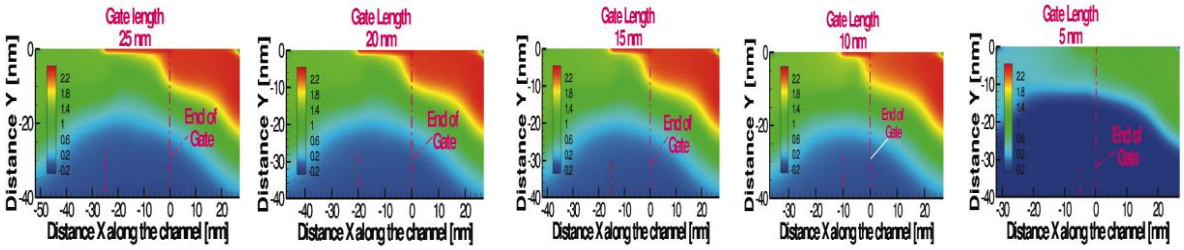
Figures 9. [a, b, c, d, e] : The carrier density profile for Si MOSFETs laterally scaled down from the 25 nm to 5 nm gate length, for all cases biased at V_G -V_T=1.0 V and V_D =1.0 V. The dot dashed/solid lines indicate the gate beginning and the gate end. The inset exhibits scale of the electron density in cm^{-3}.



(a) (b) (c) (d) (e)

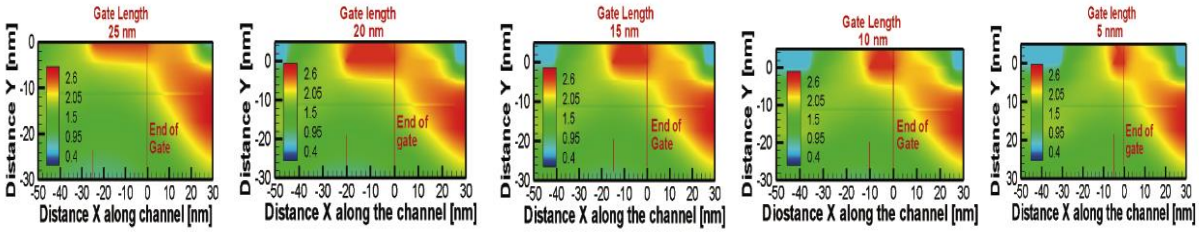
Figures 10. [a, b, c, d, e]: The carrier density profile for InGaAs MOSFETs laterally scaled down from the 25 nm to 5 nm gate length, for all cases biasing at V_G -V_T=1.0 V and V_D =1.0 V. The dot dashed/solid lines indicate the gate beginning and the gate end. The inset exhibits scale of electron density in cm^{-3}.

Figures 10 show a carrier density profile for the case of scaled InGaAs MOSFETs at the same applied bias. During channel length scaling, the electron sheet density will not increase significantly into the channel at the drain side in spite of enhance of the density at the source side of the device. This is induced by a source starvation due to minimum density of states (the heavily doped III-V material source will have a smaller density of states compared to the heavily doped Si source) appearing in many III-V semiconductors [38] but the starvation will not be increased during scaling. Note here that the starvation means inability of the source region to supply carriers into a channel [34, 35].



(a) (b) (c) (d) (e)

Figures 11. [a, b, c, d, e]: The potential profile for Si MOSFETs laterally scaled down from the 25 nm to 5 nm gate length, for all cases biasing at V_G -V_T=1.0 V and V_D =1.0 V. The dot dashed/solid lines indicate the gate beginning and the gate end. The inset exhibits scale of the potential in eV.



(a) (b) (c) (d) (e)

Figures 12. [a, b, c, d, e]: The potential profile for InGaAs MOSFETs laterally scaled down from the 25 nm to 5 nm gate length, for all cases biased at $V_G - V_T = 1.0$ V and $V_D = 1.0$ V. The dot dashed/solid lines indicate the gate beginning and the gate end. The inset exhibits scale of the potential in eV.

Figures 12 show a potential profile in the scaled Si MOSFETs at the same applied bias. The potential in the drain region shows almost unchanged behaviour in the transistors with gate lengths scaled from 25 nm to 10 nm. When the gate length is scaled to 5 nm, the potential in the drain region starts to strongly decrease as the mutual Coulomb interaction between the source and the drain takes over. This potential behaviour is a new, exceptional effect exclusively attributed to ultra-short channel transistors (gate length of 5 nm) [35]. Figures 12 show a potential profile in the scaled InGaAs MOSFETs, again, at the same applied bias. We observe that the potential profile increases steeply along the channel in all scaled transistors (from 25 nm to 5 nm). The potential is almost a constant in the drain region except for 10 nm and 5 nm gate length transistors. The potential at drain region shows almost unchanged behaviour when transistors are scaled from 25 nm to 10 nm. If the gate length is scaled down furthermore to 5 nm, the potential at drain region strongly decreases as the mutual Coulomb interaction among the source/drain enhances because of their close vicinity as mentioned before.

6. Conclusions

Ensemble MC device simulations using the MC/MOS toolbox have accomplished to analyse the behaviour of n-channel Si and $In_{0.3}Ga_{0.7}As$ MOSFETs scaled down from a gate length of 25 nm to 5 nm successively. The simulations are based on comparison of $I_D - V_G$ performance for the 25 nm gate length Si MOSFET which satisfy very good with the outcomes from another developed simulation MC codes [14]. The simulations of $I_D - V_G$ performance for the III-V transistors are based on the previous verifications against experimental data from various sub-100 nm gate length transistors [11, 12, 13]. We have also investigated the influence of carrier confinement in nano-scaled transistor using 1D simulations through cross-sections of the devices, determining conduction band outline, carrier density, energy states and eigenfunctions under external applied bias.

Moreover, we have noticed that the current in Si MOSFETs is gently increasing during scaling system in spite of a dramatic decay of maximum velocity at 5 nm gate length. The intrinsic drain current effectively enhances, gratefulness to the uniform enhance of the velocity at the drain of nano-transistors. We have also investigated the physical mechanisms which establish the carrier density, and potential profile along the channel of MOSFETs with scaling-down of the 25 nm gate length Si MOSFET. The behaviour of the electron density in the scaled Si and InGaAs transistors reflects the behaviour of electron velocity [16], the gate is progressively losing control of the electron transport in the channel. The overall electron density along the channel of the all scaled Si devices is larger than in the equivalent InGaAs ones. The high density region at the beginning of the gate, close to the interface, is the result of electron injection and backscattering. The maximum electron density in this region gradually decreases in the scaling process. The potential in the scaled Si devices is maintaining a very good control of the electron transport in the channel till the 5 nm gate length when the control is lost due to the previously mentioned strong long-range Coulomb interaction. This potential behaviour is a new, exceptional effect exclusively attributed to ultra-short channel transistors [34]. The potential distribution in the equivalent InGaAs MOSFETs is weaker but it is not lost even at the gate length of 5 nm.

7. References

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