SiC/Al_4SiC_4 Based Heterostructure Transistors

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Abstract

Wide band gap SiC/Al_4SiC_4 heterostructure transistor with a gate length of 5 μm is designed using a ternary carbide of Al_4SiC_4 and its performance simulated by Silvaco Atlas. The simulations use a mixture of parameters obtained from ensemble Monte Carlo simulations, DFT calculations, and experimental data. The 5 μm gate length transistor is then laterally scaled to 2 μm and 1 μm gate length devices. The 5 μm gate length SiC/Al_4SiC_4 heterostructure transistor delivers a maximum drain current of 168 mA/mm, which increases to 244 mA/mm and 350 mA/mm for gate lengths of 2 μm and 1 μm, respectively. The device breakdown voltage is 59.0 V which reduces to 31.0 V and to 18.0 V in the scaled 2 μm and the 1 μm gate length transistors. The scaled down 1 μm gate length device switches faster thanks to a higher transconductance of 65.1 mS/mm compared to only 1.69 mS/mm by the 5 μm gate length device. Finally, a sub-threshold slope of the scaled devices is 197.3 mV/dec, 97.6 mV/dec, and 96.1 mV/dec for gate lengths of 5 μm, 2 μm, and 1 μm, respectively.

Keywords: *Heterostructure; Ternary Carbide; Al_4SiC_4; Silvaco; transconductance; Breakdown, HEMT*

Introduction

Al_4SiC_4, a wide band gap (WBG) ternary carbide semiconductor material, has attracted a great deal of interest from the electronics industry over the past few decades, due to its emerging semiconductor properties, a departure from its previous classification as a ceramic material.[1,2] Although Al_4SiC_4 was first predicted as having a band gap of only 1.05 eV,[3] the band gap has been revised in previous publications to be 2.78 eV.[4] This has led to Al_4SiC_4 being classified as a wide band gap semiconductor, with a band gap close to that of, for instance, 3C-SiC and thus potentially addressing similar fields of applications. Other material properties of significance include superior oxidation resistance,[5,6] superior wear resistance, low weight, high strength, and high thermal conductivity.[7] These material properties mean that Al_4SiC_4 could became a very useful and versatile material in applications for opto-electronic and power electronic applications.

Al_4SiC_4 might have many potential applications as a WBG semiconductor material if we are able to synthesize it in large enough crystals. As Al_4SiC_4 has a smaller band gap of 2.78 eV than a SiC band gap of 3.4 eV, this ternary semiconductor might be used to design carbide heterostructures, carbide heterojunctions, or carbide quantum well devices such as a SiC/Al_4SiC_4 heterostructure transistor. The density of interface states between Al_4SiC_4s and SiC might be reduced when compared to the density of the interface states between oxide based dielectric layers and SiC[8] due to the close matching of the lattice constants between the two materials. These heterostructure SiC/Al_4SiC_4 transistors could compete with such devices as a lateral SiC LD MOSFETs and AlGaN/GaN HEMTs[9] in high energy efficiency applications.[10]

The heterostructure $SiC/Al_4SiC_4/SiC$ material system can allow to tailor the lowest electron ground state and the highest hole ground state in the Al_4SiC_4 quantum well within the conduction and valence band offsets determined by the two band gaps of the two components of 2.78 eV and 3.4 eV by adjusting the width of the quantum well. Opto-electronic applications of Al_4SiC_4 could take advantage of its very distinct bandgap which might pro-

duce light with a wavelength of around 446 nm (blue light) based on a bandgap of 2.78 eV[4] where it could compete with GaN[11] based LEDs. The light absorption of Al_4SiC_4 around the blue light spectrum could have a potential to be used in photovoltaics as thin films and as photo-electro-chemical water splitting as the high-energy light absorber. Al_4SiC_4 also has a potential to work as an X-ray detector where it could either replace the SiC X-ray detectors[12] or work in parallel with them, due to its high tolerance to radiation and ability to absorb at a different energy value to that of SiC. On top of these applications, Al_4SiC_4 is compatible with the 4H-SiC or the 6H-SiC technology by having a close crystal lattice constant and by having a chemical compatibility with 4H-SiC and 6H-SiC giving way to many SiC/Al_4SiC_4 heterostructure or quantum well based devices such as heterostructure transistors or LEDs.

In this work, we have employed a commercial TCAD Silvaco software by using two-dimensional (2D) Atlas simulations to foresee device characteristics of a SiC/Al_4SiC_4 heterostructure transistors for the first time. The device simulations use a combination of material properties of Al_4SiC_4 obtained from physically based simulations and calculations[4,13] along with other published material properties.[14] Where the material properties are unknown, we use the material properties of 4H-SiC as the closest material system.[15] The initial device architecture is designed with a gate length of 5 μm to meet requirements of power applications. The initial architecture is then scaled down to gate lengths of 2 μm and 1 μm in order to access the device potential to increase its performance by scaling, mainly to increase the switching speed by increasing transconductance.[16] We have enlisted a conventional HEMT-like design[9] with a 4H-SiC layer on the top of an Al_4SiC_4 buffer layer in order to promote a creation of the 2-D electron gas (2DEG) at the interface between the two materials. The transistor characteristics that are investigated are DC current-voltage (I-V) characteristics, transconductance, device breakdown, and a comparison between three devices scaled laterally.

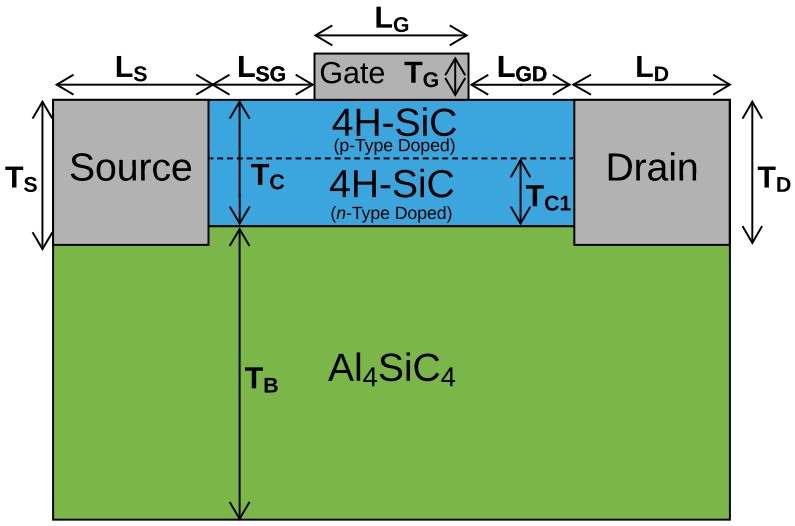

Figure 1: Cross-section of the SiC/Al_4SiC_4 heterostructure transistor designed for power applications with see device dimensions summarised in Table 1. The concentration of n-type doped 4H-SiC layer is $2.5 \times 10^{18}\,\mathrm{cm}^{-3}$ and the p-type doped part of the 4H-SiC layer is $1.0 \times 10^{16}\,\mathrm{cm}^{-3}$.

Transistor Simulations

Transistor simulations have been run in a commercial TCAD Silvaco software where a transistor heterostructure was designed considering a Al_4SiC_4 3 μm buffer layer topped with a partially n-type doped 4H-SiC layer and a Shottky metal gate. The heterostructure device was modeled with a V_D ranging from $1 - 40$ V.

Device Structure

A cross-section of the SiC/Al_4SiC_4 heterostructure transistor aiming for power applications is illustrated in Figure 1. The device heterostructure, which has been optimised for a large channel electron density, comprises of a thin layer of n-type doped 4H-SiC with a concentration of $2.5 \times 10^{18}\,\mathrm{cm}^{-3}$, on the top of a p-type doped Al_4SiC_4 buffer with a concentration of $1 \times 10^{16}\,\mathrm{cm}^{-3}$. The purpose of the thin layer of n-type doped SiC is to provide supply of carriers into the device channel which occurs at the interface between the SiC and

Table 1: Corresponding dimensions of the scaled heterostructure transistors schematically shown in Figure 1. Note that L_S and L_D dimensions are assumed to be a large enough to make good Ohmic contacts. All the dimensions are given in nanometers.

Dimensions (nm)	Gate length (nm)		
	5000	2000	1000
Source-to-gate spacer (L_{SG})	2500	1000	500
Gate-to-drain spacer (L_{GD})	2500	1000	500
SiC layer thickness (T_C)	20	20	20
n-type doping depth in SiC (T_{C1})	10	10	10
Al_4SiC_4 thickness as buffer (T_B)	3000	3000	3000
Source depth (T_S)	25	25	25
Gate height (T_G)	5	5	5
Drain depth (T_D)	25	25	25

the Al_4SiC_4. Figure 2 illustrates that the increasing electron sheet density as a function of n-type doping concentration in the thin layer of 4H-SiC (see Figure 1) starts to saturate from a concentration of about $2.5 \times 10^{18}\,\mathrm{cm}^{-3}$. Therefore, we choose this n-type doping concentration as sufficient to provide the large electron sheet density in the device channel considering also technological difficulties to implant a very large n-type doping concentration into a 4H-SiC layer. The SiC/Al_4SiC_4 heterostructure device has a gate length of 5 μm, a channel length from source-to-drain of 10 μm, a source-to-gate distance of 2.5 μm and a gate-to-drain distance of 2.5 μm. The thickness of the layers is fixed to 20 nm for SiC and to 3 μm for Al_4SiC_4.

The initial 5 μm gate length SiC/Al_4SiC_4 heterostructure transistor is laterally scaled to gate lengths of 2 μm (4 μm channel length from the source to the drain) and 1 μm (2 μm channel length from the source to the drain). The source-to-gate and the gate-to-drain dimensions are scaled to 1 μm for the 2 μm gate length device and to 0.5 μm for the 1 μm gate length, see Table 1.

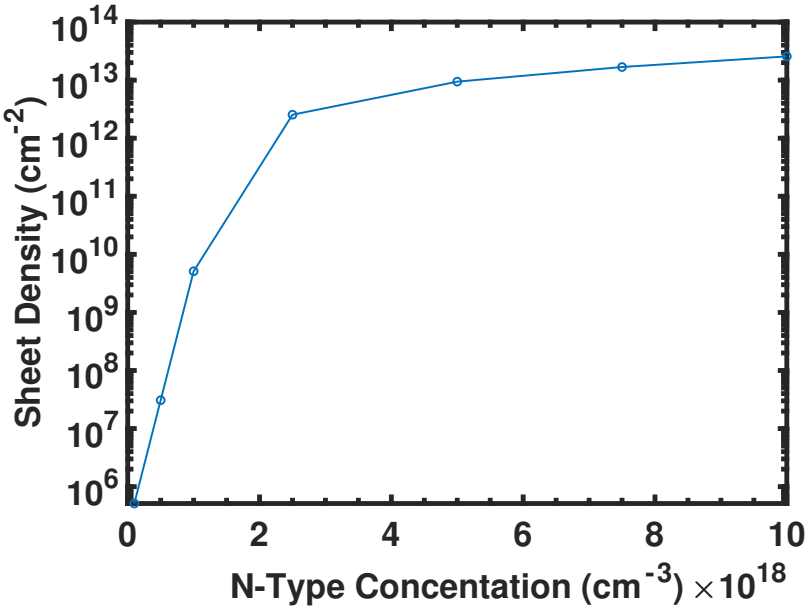

Figure 2: Electron sheet density in the SiC/Al_4SiC_4 device heterostructure as a function of the n-type concentration in the bottom of the SiC layer as illustrated in Figure 1.

Device Model

All simulations are carried out with the 2D TCAD Software Silvaco V5.26.1.R by Silvaco using a 2D drift-diffusion transport model with field dependent mobility model[17] and Auger recombination[17] simulating both holes and electrons. The solution technique that is used in the simulations is the combined Gummel-Newton algorithm. The material parameters for Al_4SiC_4 are summarized in Table 2. We also assume a very low interface density of states between SiC/Al_4SiC_4.

Scaled SiC/Al_4SiC_4 Heterostructure Transistors

The $I_D - V_G$ (transfer) characteristics of each heterostructure transistor are simulated for a gate bias (V_G) from 0 V to 20 V, and for the drain bias (V_D) from 1 V to 40 V as depicted in Figures 3-5. When V_D is increased, the drain current starts to saturate due to a limitation of the maximum electron density in the channel which is determined by the conduction band offset as seen in Figures 6-8. The drain current saturation exhibits itself as inability to

Table 2: Al_4SiC_4 material parameters considered in the simulations of heterostructure transistors. The electron mobility is extracted from an ensemble Monte Carlo simulations[13] at an applied electric field of 0.01 kV/cm.

Parameter (unit)	Value
Electron mobility (cm^2/Vs)	242.5 [a]
Electron saturation velocity (cm/s)	8×10^6 [a]
Bang gap at 300°C (eV)	2.78 [a]
Permittivity	8.32 [b]
Affinity (eV)	3.546 [a]
Conduction band effective density of states at 300°C (cm^{-3})	7.887×10^{19} [a]
Valence band effective density of states at 300°C (cm^{-3})	1.2×10^{19} [a]
Electron recombination coefficient (cm^6 s^{-1})	5×10^{-31} [c]
Hole recombination coefficient (cm^6 s^{-1})	2×10^{-31} [c]

[a]Obtained from Ref.[13] [b]Ref.[14] [c]Ref.[18]

substantially increase saturation current at higher V_D (between 15 V to 40 V). The $I_D - V_G$ characteristics show a linear region, an on-set of the saturation, a saturation region. At V_D=40 V, the complete drain current saturation occurs determining the maximum drain current. The scaled transistors can deliver at approximately 168 mA/mm, 244 mA/mm, and 350 mA/mm for gate lengths of 5 μm, 2 μm, and 1 μm, respectively. The decrease in the maximum drain current in the devices is due to the distance between the source and the drain. The larger is the source-to-drain distance the larger is resistance limiting the maximum drain current. A slight decline in the drain current saturation region of its slope in the 5 μm gate length transistor is caused by the Fermi level being very close to the edge of the conduction band. This allows electrons to be able to escape from the channel into the surrounding layers reducing the electron density in the channel and therefore impacting on the current.

The maximum drain current of 168 mA/mm (110 mA/mm) from the 5 μm gate length SiC/Al_4SiC_4 heterostructure transistor is just 40% (45%) lower than the maximum drain current of 240 mA/mm (200 mA/mm) delivered by a 4H-SiC vertically diffused metal oxide

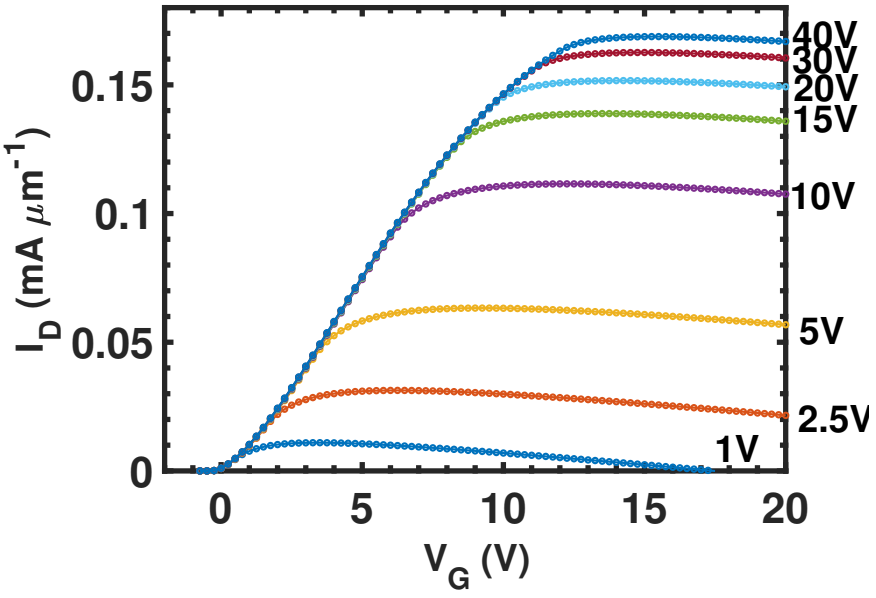

Figure 3: Drain current vs. gate bias ($I_D - V_G$) characteristics at indicated drain biases (V_D) for the 5 μm gate length SiC/Al_4SiC_4 heterostructure transistor.

semiconductor field effect transistor (VDMOSFET) with a channel length of 6 μm[19] at a gate voltage of 10 V (10 V) and a drain voltage of 20 V (10 V), respectively.

The metal-gate workfunction that is used in the simulations is assumed to be 3.9 eV. The 3.9 eV metal workfunction on the gate can be achieved by using various metals like (116) Nb (a workfunction of 3.95 eV[20]), Mn (a workfunction is 3.95 eV[21]), or $Ti_{30}Al_{70}/Ti_{20}Al_{80}$ (a workfunction of 3.95 eV[22]/3.97 eV[22]). The threshold voltage is determined from the drain current-gate voltage ($I_D - V_G$) characteristics at a large fixed drain voltage (V_D) where a linear fit is taken against the linear region. The threshold voltage is found to be 71.0 mV, 28.3 mV, and 28.3 mV for the 5 μm, 2 μm, and 1 μm gate length transistors, respectively. This decrease in threshold voltage is caused by an increase in electron density during the scaling. The sub-threshold slope has been extracted from the $I_D - V_G$ characteristics on a semi-logarithmic scale by fitting a linear line at a low drain bias of $V_D = 5$ V. The sub-threshold slope is 197.3 mV/dec, 97.6 mV/dec, and 96.1 mV/dec for devices with gate lengths of 5 μm, 2 μm, and 1 μm, respectively, all of which are much larger than the ideal sub-threshold slope of 60 mV/dec.[23,24]

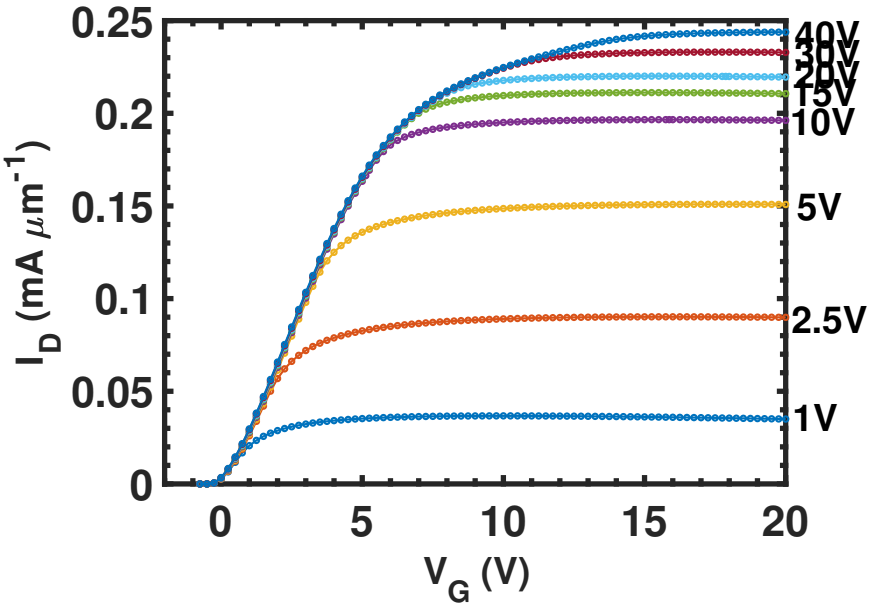

Figure 4: Drain current vs. gate bias ($I_D - V_G$) characteristics at indicated drain biases (V_D) for the scaled SiC/Al_4SiC_4 heterostructure transistor with the 2 μm gate length.

Figures 6 to 8 show the conduction and valence band profiles with overlap of the electron concentrations at device off and on operating conditions. When the device is in the off-state, the Fermi level is located between the conduction band and the valence band. When in the on-state, the Fermi level shifts up so that the level is located within the conduction band of the device and the electron concentration increases by a factor of six creating a 2DEG at the interface between 4H-SiC and Al_4SiC_4 due to a bandgap offset of 350meV between the two semiconductors.

Breakdown of the devices is determined from simulated $I_D - V_D$ characteristics seen in Figures 9-10 when the transistors are off. The bias at which the device breaks down becomes smaller as the gate length decreases from 59.0 V at the 5 μm gate length to 31.0 V for the gate length of 2 μm, and to 18.0 V for the gate length of 1 μm.

The 5 μm gate length heterostructure transistor exhibits a non-equilibrium stage between holes and electrons in a form of a kink[25] in its $I_D - V_D$ characteristics at approximately 35 V followed by the device breakdown at 59.0 V. The kink and the device breakdown voltage, when the drain current sharply rises, is presented in Figure 9. A similar kink is seen in the

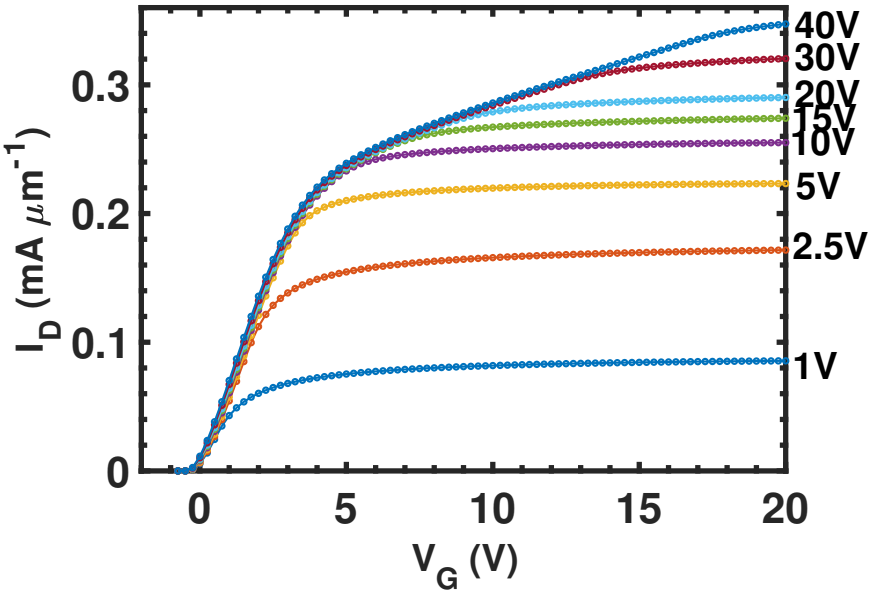

Figure 5: Drain current vs. gate bias ($I_D - V_G$) characteristics at indicated drain biases (V_D) for the scaled SiC/Al_4SiC_4 heterostructure transistor with the 1 μm gate length.

2 μm gate length heterostructure transistor where a sharp rise occurs at approximately 25 V followed by the device breakdown at 31.0 V as shown in Figure 10. Figure 11 illustrates that no kinks occur in the smallest device where the breakdown voltage is only 18.0 V.

Finally, a good figure of merit for semiconductor transistors is a transconductance which relates the current through an output to the voltage across the input of a device.[26] The transconductance indicates what will be the switching speed of a device and how quickly a signal can be transmitted through the device. The higher the transconductance the better the performance of a device. Therefore, we extract transconductance at a low drain bias of 2.5 V and a high drain bias of 30 V in order to ascertain how well the device will be performing in a switching operation. As the device gate length decreases, the transconductance increases from 1.25 mS/mm (1.69 mS/mm) to 31.90 mS/mm (36.5 mS/mm) and 59.3 mS/mm (65.1 mS/mm) at a low drain bias of 2.5 V (at a high drain bias of 30 V) as summarized in Table 3 and, in turn, the switching speed of the device will improve. This increase in the switching speed is mainly govern by a capacitance between the gate and the channel. As the gate dimension become smaller, the smaller the gate-to-channel capacitance

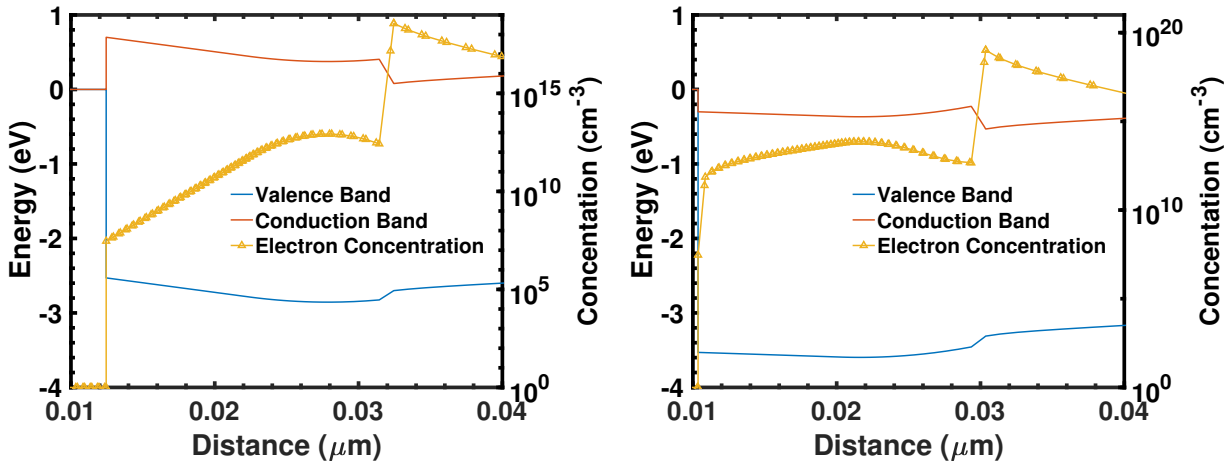

Figure 6: Conduction and valence band profiles (left) overlapped with electron density (right) across the middle of the 5 μm gate length device in an off-state with zero bias applied (a), and in an on-state at V_D=5 V and V_G=1 V (b).

and thus faster the switching. The decline of the transconductance in the 1 μm gate length transistor at the high drain bias of 30 V is caused by a kink at around 13 V at a drain bias of 30 V, detectable in the $I_D - V_G$ characteristics shown in Figure 5. The kink separates two transport regimes in the transistor operation. The first transport regime is a standard electron accumulation in the channel giving a linear regime of the $I_D - V_G$ characteristics. The second transport regime occurs when an additional channel is created by electrons spilling into a conduction band minimum in the SiC layer (see the conduction band in the SiC layer in Figure 8(b)).

The maximum drain currents and the transconductance of scaled SiC/Al_4SiC_4 HEMTs can be compared with the typical performance of AlGaN/GaN HEMTs[27] despite these two transistor technologies aim for different application areas.[10] The first 1.5 μm gate length $Al_{0.15}Ga_{0.85}N$/GaN HEMTs delivered maximum drain currents of 150 − 400 mA/mm and a transconductance up to 140 mS/mm.[28] The HEMT heterostructure optimisation led to a maximum drain current of 500 mA/mm and a transconductance of 160 mS/mm by the 1.0 μm gate length $Al_{0.15}Ga_{0.85}N$/GaN HEMT.[27] This maximum drain current of the 1 μm gate length SiC/Al_4SiC_4 heterostructure transistor of 350 mA/mm is 30% lower and its

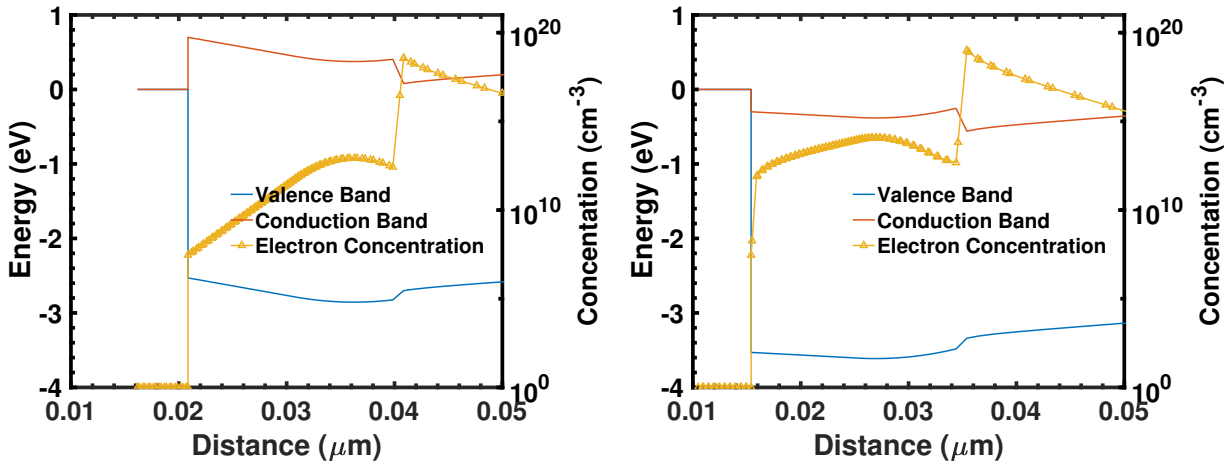

Figure 7: Conduction and valence band profile (left) overlapped with electron density (right) across the middle of the 2 μm gate length device in an off-state with zero bias applied (a), and in an on-state at V_D=5 V and V_G=1 V (b).

best transconductance of 65.1 mS/mm is 59% lower than the equivalent gate length AlGaN/GaN HEMTs. However, the maximum transconductance from the 1.0 μm gate length AlGaN/GaN HEMTs with a 7.0 μm source-to-drain distance grown on commercially viable Si substrates will be reduced to 120 mS/mm.[29] The much better transconductance of AlGaN/GaN HEMTs is related to a larger electron saturation velocity which allows for a larger velocity overshoot in the scaled AlGaN/GaN HEMTs[30] but the carbide heterostructure technology offers a very good and competitive figures of merit (FoM) in a low frequency, a high power area of 1 kW.[10]

On top of proportional lateral scaling of the device, we also performed an asymmetric scaling in order to distribute a large electric field occurring at the drain side of the scaled transistors when a very large drain voltage is applied.[29,31,32] The 1.0 μm gate-to-drain spacer of the scaled 2.0 μm and 1 μm gate length heterostructure transistors is increased to 2.5 μm in

Table 3: Maximum transconductance of the scaled heterostructure transistors.

Drain Bias (V)	5 μm	2 μm	1 μm
2.5	1.25 mS/mm	31.9 mS/mm	59.3 mS/mm
30	1.69 mS/mm	36.5 mS/mm	65.1 mS/mm

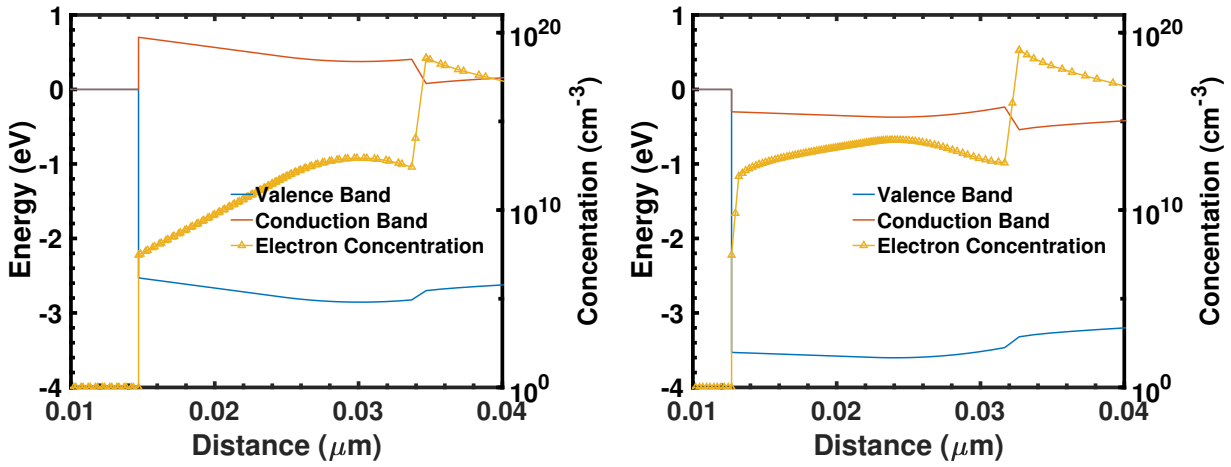

Figure 8: Conduction and valence band profile (left) overlapped with electron density (right) across the middle of the 1 μm gate length device in an off-state with zero bias applied (a), and in an on-state at V_D=5 V and V_G=1 V (b).

order to re-distribute electric field between the gate and the drain along the longer distance. The rest of device sizes stayed the same as per Table 1. A breakdown voltage increased by 17.25 V, that is from 31.0 V to 48.25 V. We also look at increasing the breakdown voltage of the 1 μm gate length heterostructure transistor by creating an asymmetric design of the device where the source-to-gate spacer is fixed to 0.5 μm but the gate-to-drain spacer is increased to 1.0 μm and to 2.5 μm. The 1 μm gate length asymmetric heterostructure with a 1.0 μm gate-to-drain spacer exhibits an increase in the breakdown voltage of 4.75 V, that is from 18.0 V to 22.75 V. The 1 μm gate length asymmetric heterostructure with a 2.5 μm gate-to-drain spacer exhibits an increase in the breakdown voltage of 11.25 V, that is from 18.0 V to 29.25 V. Therefore, lateral scaling of the SiC/Al_4SiC_4 heterostructure transistor can deliver increase in the device transconductance.

However, a consequence of the lateral scaling, which induces an increase in the electric field in the device heterostructure because a decrease in the source-to-gate and the gate-to-drain distances, is also a decrease in the device breakdown voltage. This breakdown decrease can be mitigated by using the asymmetric device structure where the distance between the gate and the drain is increased in order to spread a distribution of the electric field induced

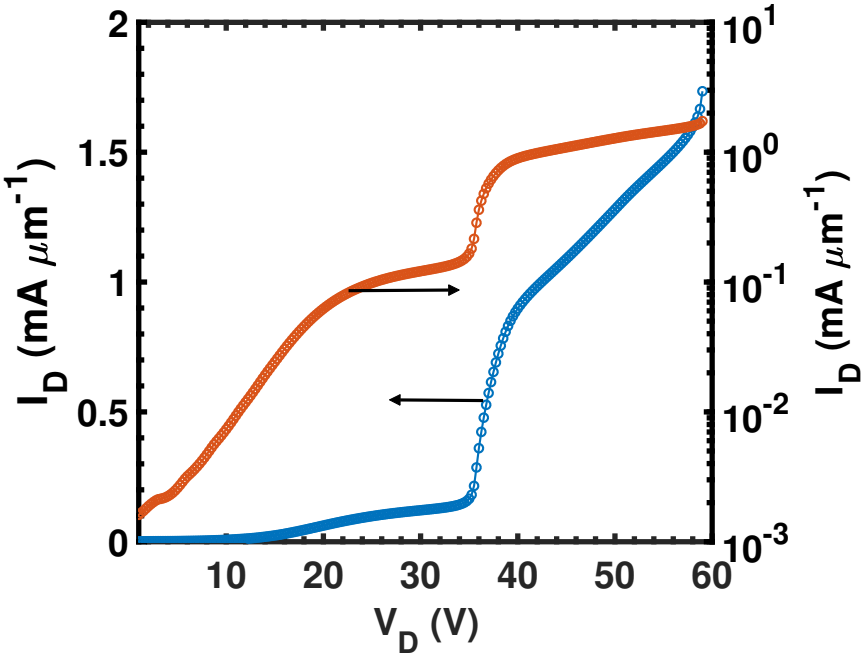

Figure 9: Breakdown of 59.0 V for a heterostructure device with a 5 μm gate length on a linear scale (left) on a log scale (right).

by a large potential at the drain (at a large applied drain bias). However, this increase in the breakdown voltage is still small compared to a breakdown voltage of 350 V obtained in the 1.5 μm gate length AlGaN/GaN HEMT grown on a highly resistive 4H-SiC substrate with a gate-source and gate-drain distances of 1.5 μm and 5.0 μm, respectively, and a 1.5 μm field plate over the gate.[32]

Conclusions

A performance of heterostructure transistor made of SiC/Al_4SiC_4 material system with a ternary carbide of Al_4SiC_4 has been simulated in Silvaco Atlas using known experimental[4] and theoretical data.[13] The heterostructure transistor with a gate length of 5 μm and two heterostructure transistors laterally scaled to gate lengths of 2 μm and 1 μm with a respective lateral scaling of the source-to-gate distance, the channel length, and the gate-to-drain distance have been simulated using a drift-diffusion transport model in commercial simula-

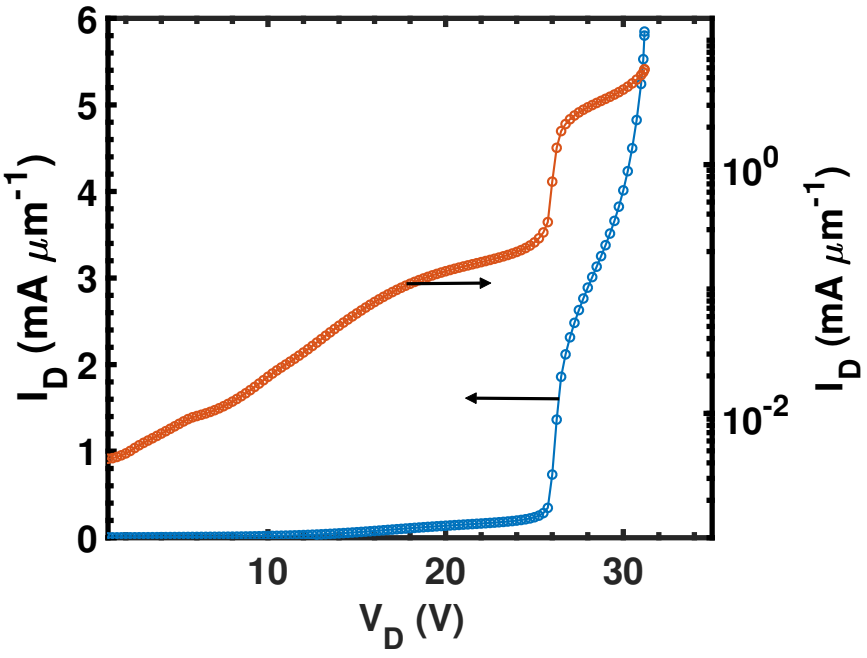

Figure 10: Breakdown of 31.0 V for a heterostructure device with a 2 μm gate length on a linear scale (left) on a log scale (right).

tor Atlas by Silvaco. The variants of asymmetrically scaled heterostructure transistors with the increased gate-to-drain distance to achieve a larger breakdown voltage have been also studied.

The threshold voltage reduces as the gate length is reduced from 71.0 mV to 28.3 mV, and to 28.3 mV for 5 μm, 2 μm, and 1 μm gate length transistors, respectively, when a metal gate workfunction is assumed to be 3.9 eV. Therefore, the device remains off unless a gate bias is applied and all the scaled SiC/Al_4SiC_4 heterostructure transistors provide a n-channel enhancement-mode, normally-off device operation. Sub-threshold slopes of 197.3 mV/dec, 97.6 mV/dec, and 96.1 mV/dec for gate lengths of 5 μm, 2 μm, and 1 μm, respectively, are observed which are, in all cases, much larger than the ideal value of 60 mV/dec at 300 K. This sub-threshold slope is also higher than the 64 mV/dec average that is observed in AlGaN/GaN HEMTs.[33]

The bias point at which the device breakdown occurs reduces from 59.0 V, to 31.0 V, and to 18.0 V as the gate length reduces from 5 μm to 2 μm and to 1 μm, respectively.

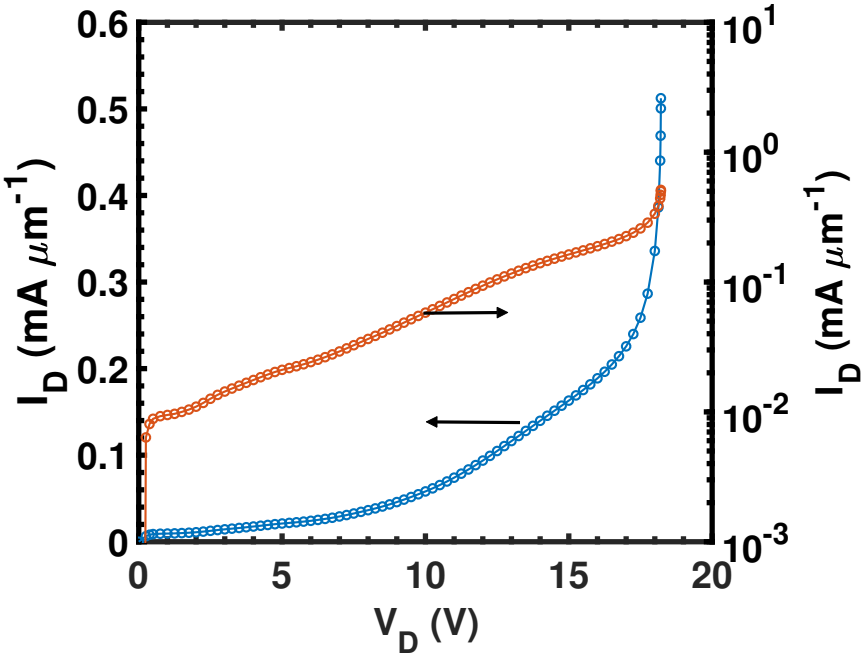

Figure 11: Breakdown of 18.0 V for a heterostructure device with a 1 μm gate length on a linear scale (left) on a log scale (right).

These breakdown voltages for SiC/Al_4SiC_4 heterostructure transistors are lower than what is reported for AlGaN/GaN HEMTs at between 90 V[34] to 600 V.[32] The breakdown voltage can be increased to 48.25 V when we increase the gate-to-drain spacer to 2.5 μm in the 2 μm gate device, and to 22.75 V and to 29.25 V in the 1 μm gate device when the gate-to-drain spacer is increased to 1.0 μm and to 2.5 μm. The drain current saturation point increases with the reduction of the gate length and increase of the drain voltage. At a large drain voltage of 40 V, a drain current saturation appears at 1.68×10^{-4} mA/mm, 2.44×10^{-4} mA/mm, and 3.50×10^{-4} mA/mm for gate lengths of 5 μm, 2 μm, and 1 μm, respectively.

A larger drain current and transconductance of AlGaN/GaN HEMTs compared to the carbide SiC/Al_4SiC_4 heterostructure transistors originate from a higher electron saturation velocity in scaled AlGaN/GaN HEMTs[30] but the carbide heterostructure technology offers a competitive FoM in a low frequency, a high power area of 1 kW[10] while not suffering from reliability issues.[35]

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