The Role of SiN/GaN cap Interface Charge and GaN Cap Layer to Achieve Enhancement Mode GaN MIS-HEMT Operation

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Abstract

The thickness increase of gallium nitride (GaN) cap layer from 2 nm to 35 nm to achieve an enhancement mode GaN MIS-HEMT (Metal-Insulator-Semiconductor High-Electron-Mobility Transistor) with a threshold voltage (V_{th}) of +0.5 V is studied using TCAD simulations. The simulations are calibrated to measured I-V characteristics of the 1 μm gate length GaN MIS-HEMT with the 2 nm thick GaN cap. A good agreement at low and high drain voltages (V_{DS}=1 V and 5 V) between simulations and measurements is achieved by using a quantum-corrected drift-diffusion transport model. The enhancement mode GaN MIS-HEMT with a GaN cap thickness of 35 nm achieves V_{th} = +0.5 V thanks to positive interface traps occurring between the SiN passivation layer and the GaN cap as reported experimentally. The simulations indicate that a parasitic channel is created at the interface between the SiN layer and the 35 nm GaN cap. Our study also shows an increase in the breakdown voltage from 100 V to 870 V when a thickness of the GaN cap layer increases from 15 nm to 35 nm.

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1. Introduction

The ongoing research activities on III-Nitrides are driven by the development of advanced types of GaN based devices for decisive optical, sensor, power, and RF applications with an excellent performance and a good energy consumption. One of the most perspective GaN based devices is a High Electron Mobility Transistor (HEMT) [1, 2] for power amplifiers, radar monitoring, and wireless communications. GaN has exclusive material properties such as an energy bandgap of 3.4 eV, a great breakdown electric field of 3.3 MV/cm, a large value of electron mobility in a two-dimensional electron gas (2DEG) of 2000 cm^2/Vs, a high saturation velocity of 2.5×10^7 cm/s, a low relative permittivity of 8.9, and a large thermal conductivity (κ) of 130 $Wm^{-1}K^{-1}$ [3, 4]. Furthermore, a 2DEG at the interface of an $Al_xGa_{1-x}N$ barrier and a GaN substrate might have a sheet density exceeding 10^{13} cm^{-2} which occurs without doping of the $Al_xGa_{1-x}N$ barrier due to a combination of the spontaneous and the piezoelectric polarization. This polarisation creates the 2DEG making an $Al_xGa_{1-x}N$/GaN HEMT to operate in the depletion mode (a normally-on device operation) which then requires first to apply a negative bias in switching circuits [5]. Therefore, intensive research is underway to achieve an enhancement mode GaN HEMT (a normally-off device operation) to improve the reliability of the transistor in switching circuits and thus to meet the stringent requirements in power circuit operations, for example, for automotive applications [6]. The enhancement mode of GaN HEMT operation can be achieved by various changes in the device architecture or in the manufacturing process like i) reducing the AlGaN barrier down to 3 nm [7], ii) making a recessed gate [8], iii) using a dual-gate [9], iv) using a *p*-type doping of the GaN gate [10], v) making an *N*-polar GaN [11], vi) using the carbon tetrafluoride (CF_4) plasma treatment technique [12], or vii) introducing an InGaN cap layer of about 5 nm to achieve the polarisation induced electrostatic potential rising the conduction band [13]. However, many of these solutions result in decrease in a drive current and negatively affect device reliability [14]. For example, the introduction of GaN cap layer, in order to protect a surface of GaN HEMT against surface trap generation, will substantially decrease the drain current [15].

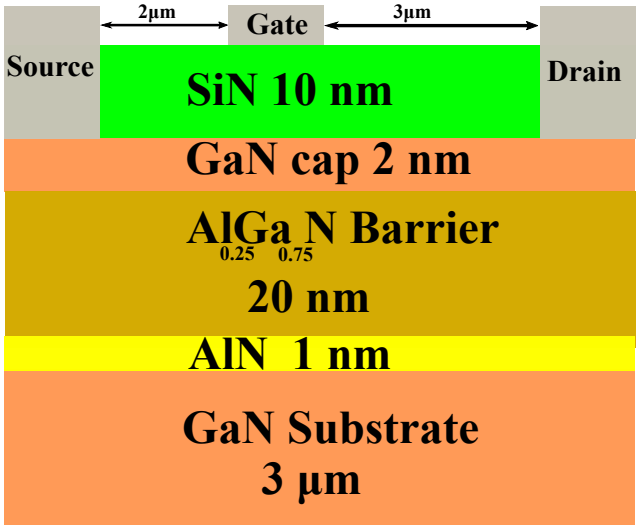

Figure 1: Cross-section of the simulated i-GaN capped MIS-HEMT.

In this paper, we investigate the impact of increasing cap layer thickness aiming to achieve the enhancement mode transistor operation. We reported that the increase in a cap layer thickness can lead to drop in the drain current [15]. Modifying the cap layer thickness together with the gated recess etching led to an increase in a contact resistance from 1.0 Ω.mm to 4.0 Ω.mm [16] and an increase in a drain current [17]. The reason is that the capped layer changes the spread of electric field increasing the electric field in the AlGaN layer while reducing the electric field in the GaN cap [18]. Thus, the thin GaN cap layer minimizes the surface related current collapse when applying a high electric field stress [19]. However, further increase of the GaN cap layer limits the electron density in the 2DEG channel [20].

2. Simulation Method

Figure 1 presents device architecture of the 1 μm gate length GaN MIS-HEMT. This device is passivated with a 10 nm SiN, has a 2 nm thick n-type uniformly doped GaN cap, a 20 nm $Al_{0.25}Ga_{0.75}N$ barrier layer thickness, a 1 nm AlN spacer layer to improve channel quantum confinement, and a 3 μm GaN substrate. The distance between the drain and the gate is 3 μm and the distance between the source and the gate is 2 μm. Ohmic contacts made of a composite metal consisting of Ti/Al/Ni/Au 30/180/40/100 nm

are deposited directly on the SiN_x passivation layer [21, 22] followed by the Rapid Thermal Annealing (RTA) at an optimized temperature of 800^{o}C for a duration of 30 s. The 1 μm gate length GaN MIS-HEMT has a background n-type doping concentration of 1×10^{16} cm^{-3}. We assume that iron (Fe) traps at an energy level of $E_T = E_C - 0.36$ eV and with a density of 5×10^{17} cm^{-3} are present in the GaN substrate [23].

The SiN_x passivation layer contains shallow donor-like traps with energy levels in the range of $E_C - E_T \leqslant 0.30$ eV [24] (referred to also as the border traps) in SiN-passivated AlGaN/GaN HEMTs. These interface traps can be unoccupied or occupied [25] and thus behave at the interface either as a positive charge when the donor traps are unoccupied or be neutral when the traps are occupied. Unoccupied shallow donor-like traps will induce a positive charge at the interface of the SiN layer and the AlGaN barrier which compensates a large negative polarization present normally at the surface of the AlGaN barrier in a Ga-face AlGaN/GaN heterostructure. The compensation of this large negative polarization at the interface of the AlGaN barrier leads to a 2DEG formation in the channel as opposed to free surface states at the AlGaN barrier in heterostructures with a Schottky gate metal [26]. The experimental evidence for this interface donor-like traps in a SiN layer is based on the fact that comparable 2DEG density values from 0.8×10^{13} cm^{-2} to 1.2×10^{13} cm^{-2} [27] in the SiN passivated AlGaN/GaN HEMTs can be achieved by the Si deposition on the surface of AlGaN. The SiN interface is therefore believed to have a high positive interface charge density of 2×10^{13} cm^{-2} [28].

This positive interface charge between a dielectric layer (Al_2O_3, SiON, SiN_x) and an III-nitride material has been widely reported in the literature [29, 30, 31, 32, 33]. Different dielectric layer materials used as a passivation layer induce various positive interface charge densities [32, 33]. For example, the SiON has a higher fixed charge density of 1.3×10^{13} cm^{-2} [34] than a pure SiN or SiO_2 density of 1×10^{11} cm^{-2} [35] owing to the increase of Si dangling bonds at the interface which act as ionized donors [33]. These ionized donors incompletely neutralize the negative polarization charge at a barrier surface [27]. This positive interface charge between a passivation layer and III-nitride materials also helps to minimise the current collapse [30].

As the GaN cap thickness is only 2 nm and the interface donor traps exist at the interface between the SiN passivation layer and the GaN cap layer, we have used a volume representation model to represent the donor interface traps. The assumed donor trap concentration in the 2 nm GaN

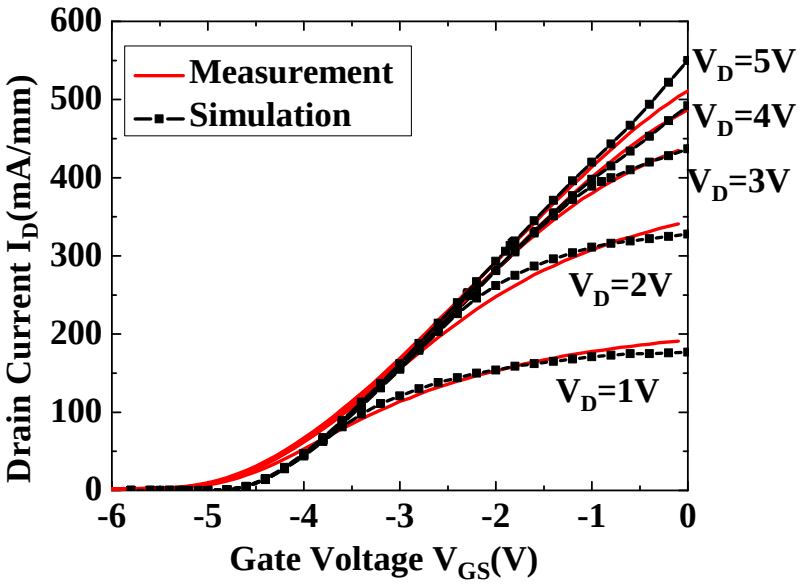

Figure 2: The calibration of I_{DS}-V_{GS} characteristics obtained from drift-diffusion simulations against experimental data at V_{DS} from 1 V to 5 V with a step of 1 V

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cap is 4.5×10^{19} cm^{-3} at an energy level of $E_T = E_C - 0.5$ eV [36], which is equivalent to a sheet concentration of 9×10^{12} cm^{-2} at the interface. Figure 2 shows a calibration of the simulated I_{DS}-V_{GS} characteristics at V_{DS}=1 V, 2 V, 3 V, 4 V, and 5 V against the actual measured data. These transfer characteristics exhibit a very good agreement between the measurement and the calibration obtained from simulations using Atlas, a commercial tool by Silvaco [37].

In the calibration of the device I_{DS}-V_{GS} characteristics to experimental data, we employed a drift-diffusion transport model. In these drift-diffusion simulations, we use a combination of the parallel field mobility model and the Albrecht mobility model [38]. The parallel field mobility model is calibrated using a low-field effective electron mobility of 925 cm^2/V.s which embeds also the impact of source/drain resistance, and an electron saturation velocity of 1.15×10^7 cm/s. The Albrecht mobility mode reproduces Monte Carlo simulations of electron transport for a wurtzite GaN [38]. The Albrecht

mobility model reads:

$$\frac{1}{\mu} = a\left(\frac{N_1}{10^{17}cm^{-3}}\right)\ln\left(1+\beta_{CW}^2\right)\left(\frac{T}{300K}\right)^{-\frac{3}{2}} + b\left(\frac{T}{300K}\right)^{\frac{3}{2}} + \frac{c}{\exp\left(\frac{\Theta}{T}-1\right)} \tag{1}$$

where:

$$\Theta = \frac{\hbar\omega_{LO}}{\kappa_B} = 1065\ K$$

$$\beta_{CW}^2 = 3\left(\frac{T}{300K}\right)^2\left(\frac{N_I}{10^{17}cm^{-3}}\right)^{-\frac{2}{3}}$$

The quantities in Eq. (1) are defined as follows:
$N_I = (1+\kappa_c)N_D$, $a = 2.61\times10^{-4}$ V.s.cm^{-2}, $b = 2.90\times10^{-4}$ V.s.cm^{-2}, and $c = 1.70\times10^{-2}$ V.s.cm^{-2}, N_D is the ionized donor concentration, T is the ambient temperature, and $\kappa_c = \dfrac{N_A}{N_D}$ is the compensation ratio. In addition, our simulations employ Shockley-Read-Hall (SRH) model for carrier generation and recombination together with Fermi-Dirac statistics, and quantum corrections using Schrödinger equation solutions across the channel.

3. Proposed Enhancement Mode GaN MIS-HEMTs

Enhancement mode MIS-HEMTs are required to avoid the need for a negative voltage supply in power switches or in MMICs which leads to unnecessary power loss and impairs circuit safety requirements [39]. Therefore, in this work, we carried out a research on the effect of the positive interface charge between the SiN passivation layer and the GaN cap on the device performance to achieve an enhancement mode operation by increasing the thickness of the GaN cap layer up to 35 nm. The positive interface charge at the interface between dielectric (Al_2O_3, SiON, SiN_x) and III-nitride materials such as GaN, $Al_xGa_{1-x}N$, and AlInN [29, 30, 31, 32, 33] leads to the increase of a 2DEG density and improves the switching performance of GaN MIS-HEMTs. The relationship between V_{th} and the positive interface charge is given by [31, 33]:

$$V_{th} = V_{th}(\text{MIS-HEMT}) - V_{th}(\text{HEMT}) = -\frac{Q_f}{C_{\text{dielectric}}} \tag{2}$$

Figure 3: The architecture of a new proposed enhancement mode GaN MIS-HEMT.

where Q_f is the positive fixed charge at the interface between the passivation dielectric layer and the III-nitride layer, V_{th}(MIS-HEMT) stands for the threshold voltage of a metal-insulator-semiconductor high-electron mobility transistor and $C_{\text{dielectric}}$ is the capacitance of a dielectric layer.

The cross-section of a proposed enhancement mode device is shown in Figure 3. The device architecture is optimized to obtain a normally-off (the enhancement mode operation) transistor by increasing the GaN cap thickness from 2 nm to 15 nm, 20 nm, 25 nm, 30 nm and 35 nm in the 1 μm gate length GaN/$Al_{0.25}Ga_{0.75}N$/GaN/$Al_{0.075}Ga_{0.925}N$/$Al_{0.1}Ga_{0.9}N$ MIS-HEMT but the SiN passivation layer is reduced to 5 nm [40]. However, a two-dimensional hole gas (2DHG) exists between the GaN cap layer and the AlGaN barrier alongside the 2DEG when the cap layer increases more than 10 nm [41]. As the GaN cap thickness is increased, the AlGaN barrier is kept at the same thickness of 20 nm. The GaN channel thickness is reduced to 20 nm and two layers of AlGaN back-barriers are added with different compositions to increase the quantum confinement of the 2DEG. The GaN channel thickness reduction to 20 nm and the two layers of low aluminium

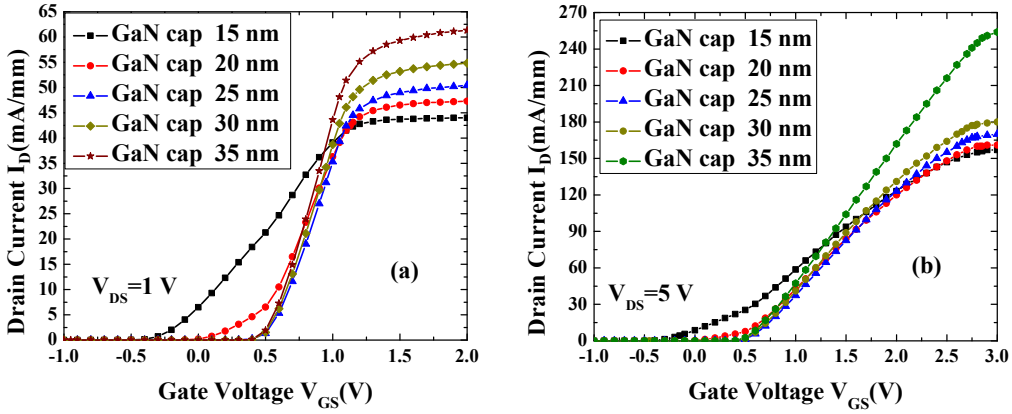

Figure 4: Simulations of transfer (I_{DS}-V_{GS}) characteristics at low and high drain voltages of V_{DS}=1 V (a) and V_{DS}=5 V (b) for the 1 μm gate length GaN MIS-HEMT with a varying thickness of the GaN cap layer of 15 nm, 20 nm, 25 nm, 30 nm, and 35 nm assuming a positive interface charge of 5.25 $\times 10^{12}$ cm^2.

content back-barriers help to achieve the normally-off operation [42, 43]. The GaN channel is assumed to have an unintentional background doping concentration of 1×10^{16} cm^{-3}.

An iron (Fe) doped GaN channel will inevitably have Fe induced acceptor energy levels of traps (E_T) which can vary from 0.28 eV to 1.0 eV [44, 45, 23] and have been reported to reduce the substrate-related current collapse when compared to a carbon (C) doped GaN channel [46, 47]. In our study, the Fe induced acceptor traps are located in the GaN channel at an energy level of E_T=E_C-0.36 eV with a concentration of 7×10^{17} cm^{-3} [23] and electron and hole capture cross-sections of $\sigma_{n,p} = 1\times10^{-15}$ cm^2 [48]. The hole concentration in the AlGaN back-barrier is achieved using a polarization doping by ionized Mn acceptors [49, 50]. A Mn concentration of 3×10^{16} cm^{-3} with an energy level at E_T=E_V + 1.4 eV [51] above the valence band is assumed in the $Al_{0.075}Ga_{0.925}N$ with a thickness of 20 nm. This layer with a low aluminium concentration is chosen to avoid any mismatch between the GaN substrate and the AlGaN back-barrier layer. Finally, the $Al_{0.1}Ga_{0.9}N$ double back-barrier layer has a thickness of 3 μm and is p-type doped with a concentration of 1.25×10^{18} cm^{-3}.

The proposed device structure is simulated at a low drain voltage of V_{DS} = 1 V and a high drain voltage of V_{DS} = 5 V as shown in Figure 4(a) and Figure 4(b), respectively. Shockley-Read-Hall (SRH) generation and

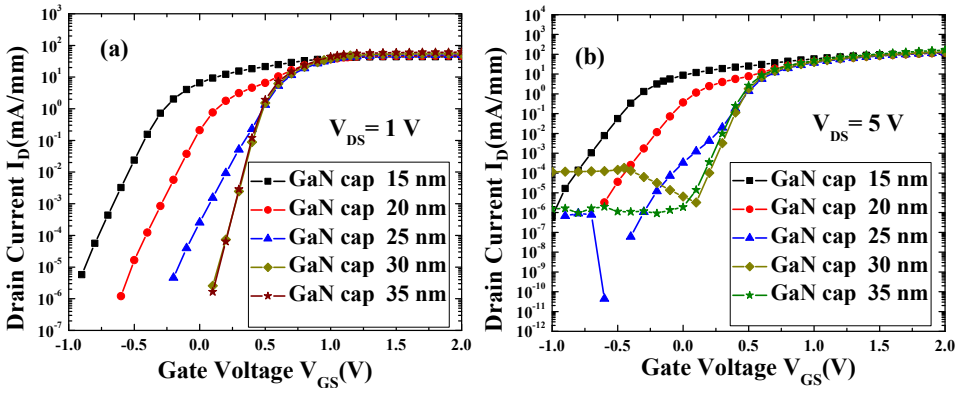

Figure 5: Transfer characteristics (I_{DS}-V_{GS}) of the 1 μm gate length GaN MIS-HEMT, showing the sub-threshold region, as a function of gate voltage and the different GaN cap layer thicknesses at a low drain voltage of V_{DS}=1 V (a), and a high drain voltage of V_{DS}=5 V (b).

recombination, Fermi-Dirac statistics, and quantum corrections via solutions of Schrödinger equation are consistently used as before. The positive interface charge with a concentration of 5.25×10^{12} cm^{-2} (or 0.84 μCcm^{-2}) is placed at the interface between the 5 nm SiN passivation layer (dielectric layer) and the GaN cap layer for all cap thicknesses. A capacitance of the SiN dielectric layer can be calculated as $C_{\text{dielectric}} = \varepsilon_{\text{SiN}}/t$. Assuming the SiN permittivity (ε_{SiN}) of 7.0 and $t = 5$ nm, $C_{\text{dielectric}} = 1.24\,\mu\text{Fcm}^{-2}$. Eq. (2) would thus predict an increase in a threshold voltage shift of -0.68 V relative to the threshold voltage of a Schottky gate HEMT, a desirable improvement that brings the device closer to the enhancement mode operation. The calculated threshold voltage shift for a density of positive interface charge of 5.25×10^{12} cm^{-2} is consistent with the results in [33] where shifts in the threshold voltage of -4.0 V and -10.0 V were obtained for GaN transistors having a density of positive interface charge of 1.54×10^{13} cm^{-2} and 2.71×10^{13} cm^{-2}, respectively.

The positive interface charge, due to Si donors at the interface of the SiN passivation and the GaN cap, was reported experimentally with the value ranging from 8×10^{12} cm^{-2} to 2×10^{13} cm^{-2} [28]. Our simulations assume that the positive interface charge is 5.25×10^{12}cm^{-2}, the value close to that reported in Refs. [28, 33].

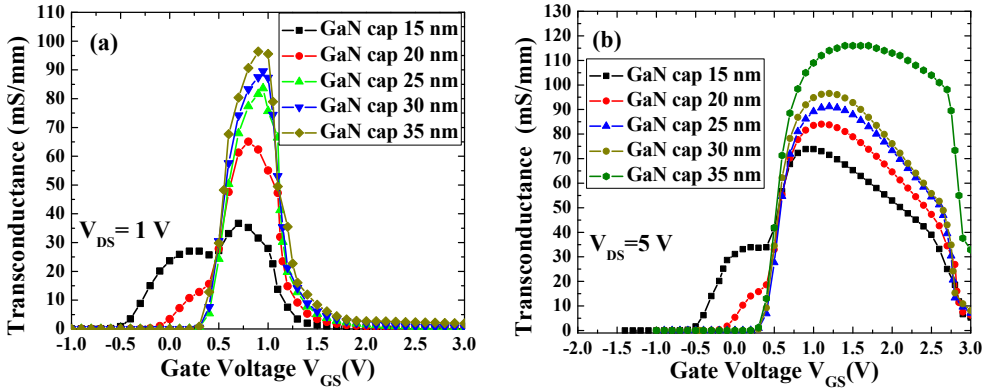

Figure 6: Transconductance of the 1 μm gate length GaN MIS-HEMT as a function of gate voltage and different GaN cap layer thicknesses at a low drain voltage of V_{DS}=1 V (a) and a high drain voltage of V_{DS}=5 V (b), respectively.

4. The Impact of GaN Cap

The threshold voltage V_{th} of the original experimental GaN MIS-HEMT is about -4.5 V as shown in Figure 2. Figures 4(a) and 4(b) show transfer (I_{DS}-V_{GS}) characteristics of the proposed enhancement mode transistors at low and high drain voltages of V_{DS}=1 V and V_{DS}=5 V, respectively. The threshold voltage shifts from -0.5 V, when using the 15 nm GaN cap, up to 0.5 V when using the 35 nm GaN cap layer. We see also an increase in the drain current from 40 mA/mm when using the 15 nm GaN cap to 60 mA/mm when using the 35 nm cap. It was reported that increasing the thickness of GaN cap layer would reduce the electron density in 2DEG channel [41].

To test this approach, we place a positive interface charge between the SiN and the GaN cap layer by varying of the cap thicknesses in simulations. As the result, the drain current increases by 62% and 60% at low and high drain biases which corresponds to the increase from 150 mA/mm at the 15 nm GaN cap up to 240 mA/mm at the 35 nm GaN at V_{DS} = 5 V as shown in Figure 4(b).

Figure 5 shows a sub-threshold leakage current for the 1 μm gate GaN MIS-HEMT as a function of gate voltage for a different GaN cap layer thicknesses at a low drain voltage of V_{DS} = 1 V in Figure 5(a) and at a high drain voltage of V_{DS} = 5 V in Figure 5(b). Figure 6 presents transconductance simulations for the 1 μm gate length GaN MIS-HEMT for several GaN cap

layer thicknesses. Figure 6(a) shows the simulations of transconductance at a low drain voltage of V_{DS} = 1 V giving its highest values at 95 mS/mm for the 35 nm thick GaN cap. Figure 6(b) shows the simulations of transconductance at a high drain voltage of V_{DS} = 5 V giving its highest value at 120 mS/mm for the 35 nm thick GaN cap. The increase in transconductance originates from the creation of a parasitic 2DEG channel at the interface of the SiN layer and the GaN cap because a conduction band offset increases as the thickness of the GaN cap increases. This parasitic 2DEG channel also contributes to the increase in the drain current. A low value of positive interface charge improves the performance of GaN MIS-HEMT [52]. The reduction in the positive interface charge can be achieved by oxygen plasma and post metallization annealing (PMA) treatment which enables to engineer the threshold voltage (V_{th}) from -7 V to -4 V [28].

Figures 7 and 8 show the conduction band profiles for different thickness of the GaN cap layers at the equilibrium together with electron and hole concentrations at a surface potential of 1.25 eV. A two-dimensional hole gas (2DHG) is created at the interface between the GaN cap and the AlGaN barrier after the thickness of the GaN cap layer increases above 10 nm [41] and further as shown in Figure 8. The 2DHG remains very close to the surface and effectively works as a potential barrier between the gate and the channel [41]. However, the 2DHG channel that was reported in the literature does not play a role in the proposed enhancement mode device as its concentration is very low. There is a shift up in the conduction band energy profile which is visible at a GaN cap thickness of 35 nm with no 2DEG channel created at the equilibrium. However, the occurrence of a positive interface charge at the interface between the SiN passivation layer and the GaN cap creates there an extra parasitic electron channel.

The shallow donor-like traps responsible for the positive charge at the interface of the SiN/GaN-cap can get occupied by electrons and become neutral. Therefore, we also simulate the 1 μm gate length GaN MIS-HEMT assuming that only the deep donor interface traps at an energy level of E_T=E_C-0.5 eV [36] are present at the interface of the SiN passivation layer and the GaN cap. Figure 9 shows the simulations of transfer (I_{DS}-V_{GS}) characteristics for the 1 μm gate length GaN MIS-HEMT with varying cap layers with a thickness of 15 nm, 20 nm, 25 nm, 30 nm, and 35 nm with the deep donor interface traps at a low drain voltage of V_{DS}=1 V. We assume an interface trap density of 9×10^{12} cm^{-2} because the electron sheet density has to be the same for various GaN cap layer thicknesses. The electron sheet density (N_s)

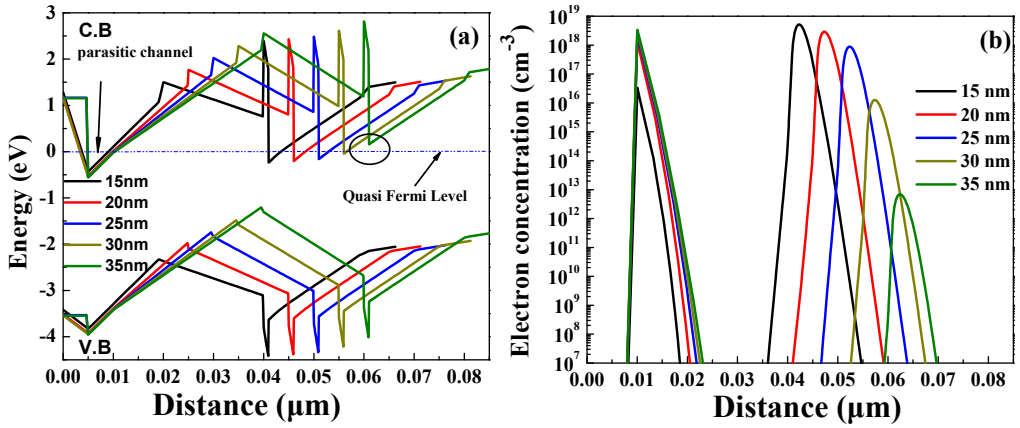

Figure 7: (a) Conduction (C.B) and valence (V.B) band profiles of the proposed enhancement mode HEMT at equilibrium (V_{DS}=0 V and V_{GS}=0 V), and (b) electron concentration for increasing thickness of the GaN cap from 15 nm to 35 nm with a step of 5 nm. No 2DEG channel is formed at the GaN cap thickness of 35 nm as indicated by the black circle. The location of a parasitic electron channel (black arrow) and the quasi Fermi level (blue dash-dot line) is also indicated.

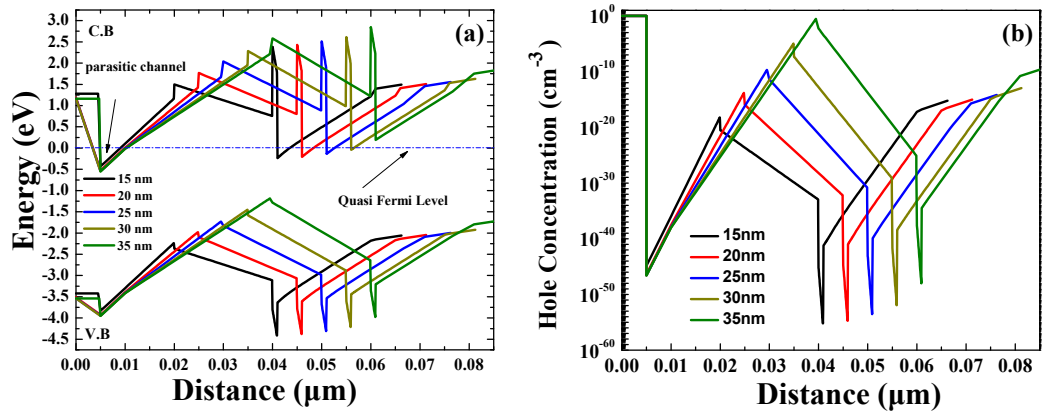

Figure 8: (a) Conduction (full red lines) and valence (full black lines) band profile of the proposed enhancement mode MIS-HEMT at equilibrium (V_{DS} = 0 V and V_{GS} = 0 V), and (b) hole concentration for increasing thickness of the GaN cap from 15 nm to 35 nm with a step of 5 nm. The location of a parasitic electron channel (black arrow) and the quasi Fermi level (blue dash-dot line) is also indicated.

is given by $N_s = N_i.d$, where N_i is the donor density in the GaN cap layer and d is the thickness of GaN cap layer.

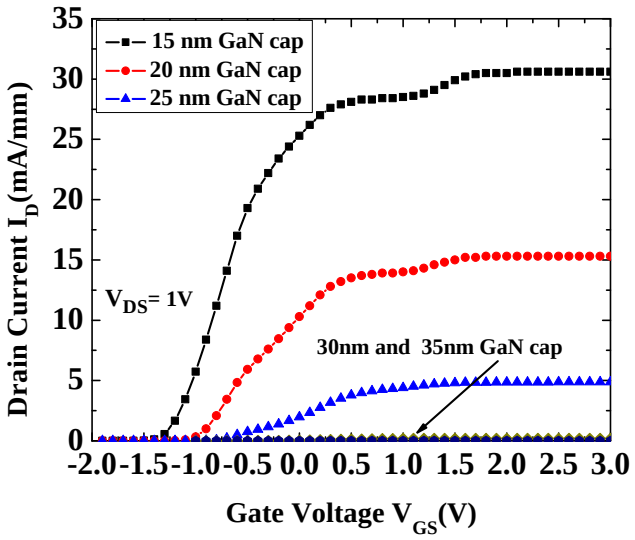

Figure 9: Simulations of transfer (I_{DS}-V_{GS}) characteristics at a low drain voltage of V_{DS}=1 V for the 1 μm gate length GaN MIS-HEMT with a varying cap layer with a thickness of 15 nm, 20 nm, 25 nm, 30 nm, and 35 nm and a deep donor interface trap concentration of 9$\times$ 10^{12} cm^{-2} located at the interface of the SiN passivation layer and the GaN cap

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Increasing the cap thickness will cause a lowering of 2DEG density in the channel and a formation of the higher 2DHG density [41], and leading to a drop in the drain current and a slight shift of the threshold voltage to more positive values as shown in Figure 9. Figure 9 also demonstrates that these donor interface traps have a detrimental impact on the drain current because the maximum drain current (at V_{DS}=1 V) decreases by 50%, 84%, and, finally, practically by 99% and 99.9%, with respect to the drain current in the 15 nm thick GaN cap transistor, when the cap layers thickness increases from 15 nm to 20 nm, 25 nm, 30 nm, and 35 nm, respectively.

5. The Effect of Parasitic Channel

The increasing of a thickness from 15 nm to 20 nm, 25 nm, 30 nm, and 35 nm of the GaN cap with the positive interface charge presents between

SiN passivation layer and GaN cap layer creates a parasitic channel. The formation of the parasitic channel at the interface between these two layers is due to increase of the potential applied on the drain [53]. Experimental work confirms the presence of a parasitic channel induced by the on-state stress, originating from applied external fields, which occurs after ageing the device for many hours [54]. The location of the parasitic channel is assumed to be between the gate and the source but not under the gate. However, our simulations reveal that the location of the parasitic channel is between the dielectric layer and the GaN cap layer. The existence of the parasitic channel explains the drain current increment as the GaN cap layer is increased as shown in Figures 4 and 5. This can be contributed to electrons moving from the interface between the SiN passivation layer and the GaN cap into the 2DEG channel. Our simulations show that electron concentration in the 2DEG channel is reduced while the GaN cap thickness is increased. This leads to the increase of electron concentration in the parasitic channel. This increase of electron concentration has a crucial impact on the increase in the drain current and the transconductance.

6. Breakdown Voltage

One of the most important figures of merit in power devices is the breakdown voltage (BV) required for a reliable performance at high temperatures and in high power applications [55]. Several research studies in the literature have been reported to improve and optimize the breakdown voltage (BV) such as a floating gate [56], an increase in the thickness of the epitaxial-layer [57], a source extended field plate, several field plates [58], and Schottky contact in the drain [59].

A simulation of the device breakdown voltage requires to establish impact ionization coefficients needed for an impact ionisation model. Impact ionization coefficients for electrons (α_n) and holes (α_p), we have used, are given by [60, 61, 62]:

$$\alpha_n(E) = A_n \, exp\left(-\frac{B_n}{E}\right) \tag{3}$$

$$\alpha_p(E) = A_p \, exp\left(-\frac{B_p}{E}\right) \tag{4}$$

where E (V/cm) is the electric field. The constants used in the GaN breakdown voltage model are: $A_n = 2.81 \times 10^8$ cm^{-1}, $B_n = 3.43 \times 10^7$ Vcm^{-1},

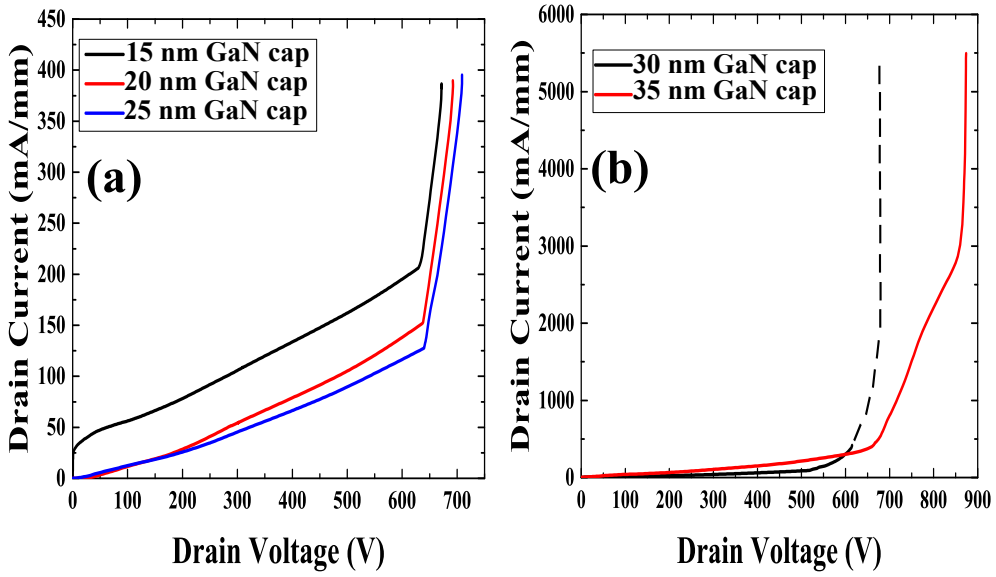

Figure 10: (a) Simulations of a breakdown voltage for the 1 μm gate length GaN MIS-HEMT with the 15 nm, 20 nm and 25 nm, and (b) with the 30 nm and 35 nm GaN cap layer thicknesses assuming a positive interface charge of 5.25×10^{12} e/cm^{-2}.

$A_p = 5.41\times10^6$ cm^{-1}, and $B_p = 1.96\times10^7$ Vcm^{-1} [63]. The breakdown voltage of the original 1 μm gate length GaN/AlGaN HEMT is 100 V (Figure 4 in Ref. [64]). The breakdown characteristics are simulated at the device pinch-off as shown in Figure 10. Our simulations show an improvement in the breakdown voltage from 100 V to 870 V. The breakdown voltage is 650 V for the 15 nm GaN cap layer, 670 V for the 20 nm GaN cap layer, 690 V for the 25 GaN cap layer as shown in Figure 10(a). Figure 10(b) shows the breakdown voltages of 670 V and 870 V for the 30 nm and 35 nm cap layer thicknesses, respectively.

7. Conclusions

Our study based on a meticulous calibration between measurements and simulation results of the 1 μm gate length GaN MIS-HEMT examines the effect of the increase in the GaN cap layer thickness accounting for a positive interface charge between the GaN cap layer and the SiN passivation layer. We have proposed a new enhancement mode device by using the thickness increase in the GaN cap layer and by adding two AlGaN back-layers with

different compositions. The first back-layer of $Al_{0.075}Ga_{0.925}N$ has a very low aluminium concentration to lattice match closely the GaN substrate. The second back-layer has still a low aluminium concentration in ternary alloy of $Al_{0.1}Ga_{0.9}$ to increase the electron confinement in the channel. The threshold voltage of the new enhancement mode GaN HEMT with a 35 nm GaN cap layer is about 0.5 V delivering a maximum drive current of 245 mA/mm. The existence of a parasitic channel is observed in the proposed device between the SiN passivation layer and the GaN cap layer with a minor impact on a transconductance of 118 mS/mm for the 1 μm gate length GaN MIS-HEMT with a 35 nm thick GaN cap. The interface donor traps located at the surface of the GaN cap layer result in a negligible drain current for the GaN cap thicknesses larger than 25 nm as shown in Figure 9.

Finally, our study shows an increase in the breakdown voltage from 100 V to 870 V. The breakdown voltage is 650 V for the 15 nm thick GaN cap layer, 670 V for the 20 nm thick GaN cap layer, 690 V for the 25 nm thick GaN cap layer. For the 30 nm and 35 nm GaN cap layer thicknesses, the breakdown voltages are 670 V and 870 V, respectively. Therefore, the enhancement mode AlGaN/AlN/GaN/AlGaN MIS-HEMT with the 35 nm GaN cap delivers the best performance in terms of on-current, maximum transconductance, and breakdown voltage.

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