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Impact of gate edge roughness variability on FinFET and gate-all-around nanowire FET

G. Espiñeira, D. Nagy, G. Indalecio, A. J. García-Loureiro, K. Kalna and N. Seoane

***Abstract*—The effect of gate edge roughness (GER) in the sub-threshold region is studied for two state-of-the-art architectures: a 10.7 nm Si FinFET and a 10 nm Si gate-all-around (GAA) nanowire (NW) FET using an in-house 3D quantum corrected drift-diffusion simulation tool. The GER is applied to the device gate using characteristic values of root mean square amplitude (RMS) and correlation length (CL). The GER induced variability results in a standard deviation (σ) for the threshold voltage (V_T) of 7 mV for the FinFET when CL/Gate Perimeter = 0.66 and RMS = 0.80 nm, which is 20% greater than that of the GAA NW FET. GER is a less damaging source of variability than metal grain granularity (MGG), line edge roughness (LER) and random dopants (RD) for both devices. When compared to LER variations, σV_T due to the GER is 62% and 86% lower for the FinFET and GAA NW FET, respectively. However, although GER affects more the FinFET than the GAA NW FET, the combined variability effect of GER, MGG, LER and RD ($\sigma V_{T,comb}$) on the FinFET is 30 mV, a value approximately 50% smaller than that of the GAA NW FET.**

***Index Terms*—FinFET, Gate-all-around nanowire FET, Gate Edge Roughness, Variability**

I. Introduction

FinFETs are the preferred device architecture in industry for the 10 nm technology node as they fulfill the requirements for both gate control and suppression of short-channel effects [1][2]. For future technology nodes, other multi-gate architectures need to be considered to be able to keep up with industry requirements [3][4]. In this context, the GAA NW FET presents itself as a viable substitute to previous architectures as its cylindrical geometry further improves the gate control [5]. However, due to the progressive scaling of CMOS technology, variability issues intensify making a necessity to develop means to minimize them [6]. During the transistor fabrication, as a result of lithography and etching processes, gate edge roughness (GER) might be a considerable source of variability affecting device performance as it does not scale down with technology [7]. Previous works covering the effect of GER for bulk MOSFETs [8] and FinFETs [9] have been presented but they lack a study comparing the effect of this variability in state-of-the art FinFET and GAA NW FETs. In this work, we present a comparative study of the impact of GER variability on a 10.7 nm gate length Si FinFET and a 10 nm gate length Si GAA NW FET. Two of the main figures of merit (FoM) describing the sub-threshold region: the threshold voltage (V_T) and the OFF current (I_{OFF}), have been studied using an in-house-built 3D density gradient quantum corrected drift-diffusion (DG-DD) simulator [10]. The obtained GER results are compared to the some of the major variability sources affecting these devices: MGG [11][12], LER [13][14] and RD [15][16]. This information could help in the design of fluctuation resistant architectures.

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Table I
DEVICE DIMENSIONS AND MAIN FOM FOR THE 10.7 NM GATE LENGTH FINFET AND THE 10 NM GATE LENGTH GAA NW FET.

Symbol	FinFET 10.7 nm	GAA NW FET 10 nm
Gate length (L_G)[nm]	10.7	10.0
S/D length ($L_{S/D}$)[nm]	10.7	14.0
Channel width (W_{CH})[nm]	5.8	5.7
Channel height (H_{CH})[nm]	15.0	7.17
Equivalent oxide thickness (EOT)[nm]	0.62	0.80
Channel p-type doping (N_{CH})[cm^{-3}]	10^{15}	10^{15}
S/D n-type doping ($N_{S/D}$)[cm^{-3}]	10^{20}	10^{20}
S/D doping lateral straggle (σ_x)	3.45	3.23
S/D doping lateral peak (x_p)[nm]	11.0	7.8
Channel perimeter [nm]	35.8	20.3
Gate perimeter [nm]	45.4	25.0
SS [mV/dec]	77	71
V_T [V]	0.255	0.250
I_{OFF} [$\mu A/\mu m$]	0.0341	0.0267
I_{ON} [$\mu A/\mu m$]	1774	1770
I_{ON}/I_{OFF} ($\times 10^4$)	5.202	6.629

II. Device structure and simulation methodology

The devices that have been used for this study are two state-of-the-art transistors based on experimental data [17][18] scaled down following the ITRS guidelines [19]. The main dimensions and doping values can be seen in Table I. The device channel has been uniformly doped whereas the source/drain (S/D) regions have a Gaussian doping. These Gaussian doping profiles, reverse engineered from experimental data [20] and scaled accordingly, are characterized by the S/D doping lateral straggle (σ_x), that describes the slope of Gaussian profile, and the S/D doping lateral peak (x_p), that indicates a position where the Gaussian decay starts measured from the middle of the channel (see Table I). Our in-house-built 3D DG-DD simulator is based on the finite element (FE) approach that accurately describes complex three-dimensional geometries [10]. The DG-DD includes Caughney and Thomas doping dependent low-field electron mobility model [21], combined with lateral (saturation velocity) and perpendicular (critical field) electric field models [22]. The DG quantum corrections

Table II
CALIBRATION PARAMETERS: v_{sat} IS THE SATURATION VELOCITY, E_{CN} IS THE PERPENDICULAR CRITICAL ELECTRIC FIELD, m_x AND $m_{y,z}$ ARE THE DG ELECTRON MASSES IN THE TRANSPORT AND CONFINEMENT DIRECTIONS.

	FinFET 10.7 nm	GAA NW 10 nm
v_{sat} [cm/s]	1.00×10^9	1.30×10^7
E_{CN}[V/cm]	5.00×10^4	9.95×10^5
$m_x[m_0]$	0.25	0.50
$m_{y,z}[m_0]$	0.10	0.10

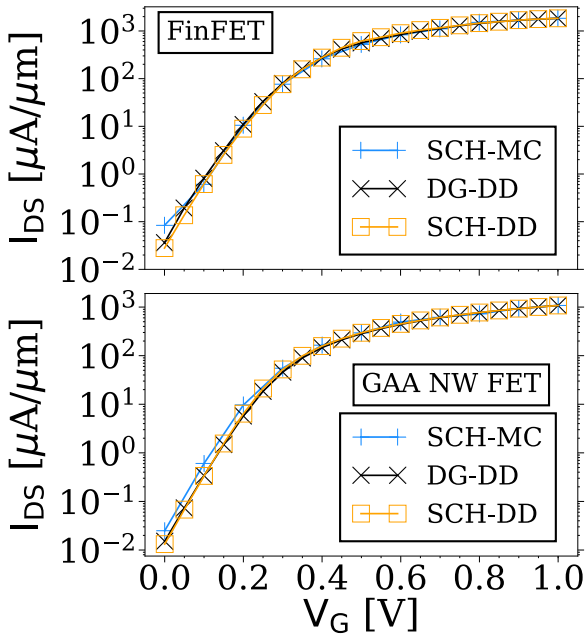

Figure 1. DG-DD simulated I_D-V_G characteristics for: the FinFET (top) and the GAA NW FET (bottom), compared against SCH-DD and to SCH-MC simulations, at $V_{D,sat}$ = 0.70 V.

use calibrated electron effective masses to account for source-to-drain tunneling and quantum confinement [23]. All the calibration parameters are summarised in Table II.

The DG-DD I_D-V_G characteristics have been meticulously calibrated (see Fig. 1) at a high drain bias ($V_{D,sat}$) of 0.7 V. They have been matched to DD simulations including anisotropic Schrödinger equation (SCH) based quantum corrections (SCH-DD) in the sub-threshold region and to SCH quantum-corrected Monte Carlo simulations (SCH-MC) [24] in the on region, as the SCH-MC may produce noisy results at very low gate voltages. In order to compare both architectures from the performance point of view, Table I presents the main FoM that characterize these benchmark devices. A constant current criteria of I_{DCC} = 32.6 [μA/μm] has been used to obtain V_T for both devices. I_{ON} has been extracted as the drain current at $V_G = V_T + V_{D,sat}$ V. The sub-threshold slope (SS) is slightly lower ($\approx$ 8%) for the GAA NW FET which translates to a faster switching speed than that of the FinFET. The GAA NW FET shows lower I_{OFF} (by 22%) and similar I_{ON} (<1% lower) compared to the values yielded by the FinFET, resolving in less power leakage. As a conclusion, the GAA NW FET outperforms the FinFET by

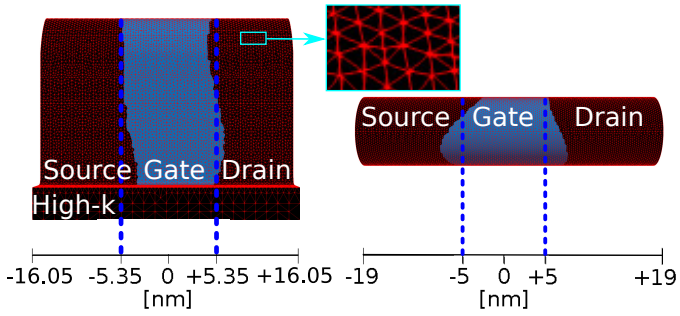

Figure 2. FinFET [17] and GAA NW FET [18] showing a GER deformed gate. A close-up view of the FE mesh used is also shown.

a 20% larger I_{ON}/I_{OFF} ratio. After the ideal, non-deformed device has been calibrated to produce sound results, the GER is applied to the gate of the device. GER has been designed similarly to the line edge roughness (LER) using the Fourier synthesis methodology as previously explained in [7][25]. To parametrize the GER, two variables have been defined: the correlation length (CL), that models the width of the Gaussian filter on the gate long edges, and the root mean square (RMS) height that quantifies the variations in the width of the gate in the transport direction. To properly capture the effect of GER, different CL and RMS values were simulated which were observed experimentally and also shown to produce the greatest variability results [18][26][27]. For each set of CL and RMS parameters, an ensemble of 300 simulations has been performed to obtain a statistically significant prediction on the behaviour of the device. Fig. 2 shows an example of the two studied devices with their gates affected by GER.

III. GER VARIABILITY

In this section, we first study the effect of GER in the sub-threshold region for the 10.7 nm gate length Si FinFET and the 10 nm gate length Si GAA NW FET and later we present a comparison between these results and other variability sources. Fig. 3 (top) shows σV_T and $\sigma log_{10}(I_{OFF})$ versus the CL for a fixed RMS of 0.80 nm. The CL has been normalized by the gate perimeter (see values in Table I), in order to perform a fair comparison of the results. Note that, for both devices, the variability increases linearly with the CL/Gate Perimeter. Results show that, in the sub-threshold region, the GAA NW FET is more resilient to GER than the FinFET. For instance, when CL/Gate Perimeter = 0.66, σV_T and $\sigma log_{10}(I_{OFF})$ are, respectively, 20% and 11% larger for the FinFET than for the GAA NW FET. A comparison of the GER variability versus the RMS with a constant CL/Gate Perimeter of 0.44 for our benchmark devices can be seen in Fig. 3 (bottom). As previously reported for LER [26], GER variability will increase with the RMS. We obtain maximum variability values at a RMS value of 1.0 nm, where σV_T and $\sigma log_{10}(I_{OFF})$ are 34% and 18% larger for the FinFET than for the GAA NW FET, respectively. A reason for the smaller variability yielded by the GAA NW FET is that the GER profiles have to be periodic as the device has a continuous gate whereas, for the FinFET, the trigate structure does not require this boundary condition. Similarly, a decrease in the MGG variability of

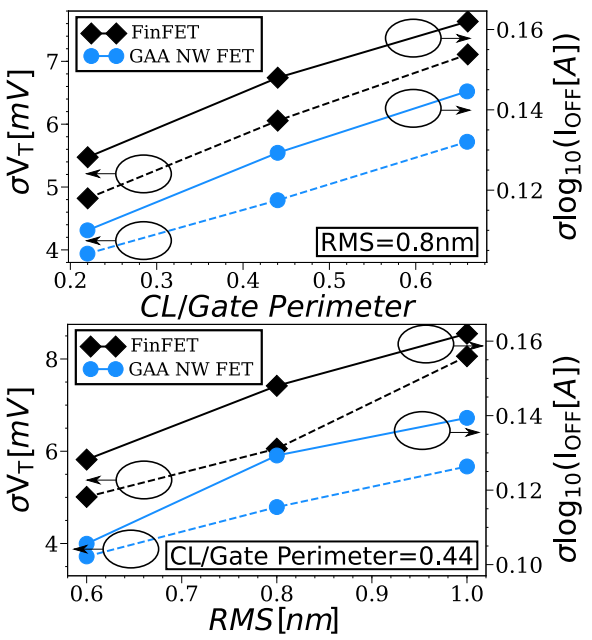

Figure 3. GER variability as a function of: the CL/Gate Perimeter (top) and RMS (bottom) for σV_T (left) and $\sigma log_{10}(I_{OFF})$ (right) at $V_{D,sat}$ = 0.70 V.

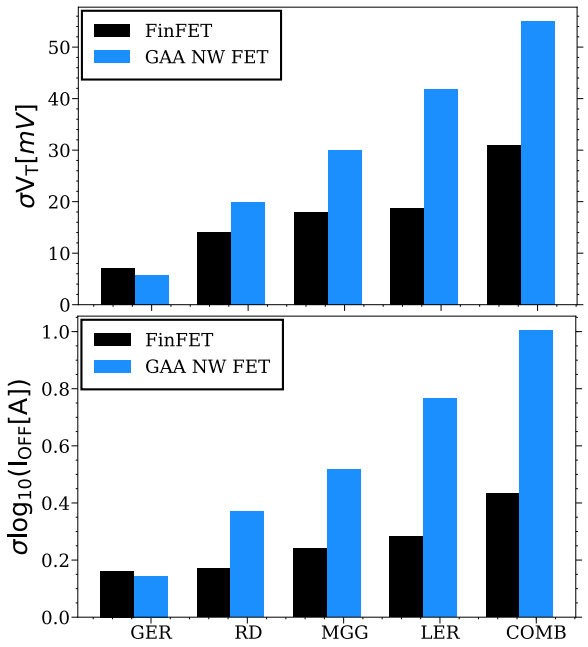

Figure 4. GER variability for σV_T (top) and $\sigma log_{10}(I_{OFF})$ (bottom) compared to other major sources of variability (MGG [25], LER [23][25] and RD) and their combined effect (COMB) at $V_{D,sat}$ = 0.70 V.

GAA NW FETs was previously reported when using periodic Voronoi patches [28].

Finally, we have compared the impact of GER (CL/Gate Perimeter = 0.66, RMS = 0.80 nm) against three of the major variability sources affecting multi-gate devices: MGG, LER and RD. The results for MGG (grain size = 5.0 nm) and LER (CL = 20 nm, RMS $\approx$ 0.80 nm) are taken from previously published DG-DD simulations [23][25], whereas the RD variability is explicitly simulated for this study following the methodology from [29]. Fig 4 shows the impact on σV_T (top) and on $\sigma log_{10}(I_{OFF})$ (bottom) of the aforementioned four sources of variability and the combined effect of them for both the FinFET and GAA NW FET. Comparatively, the GER is the least damaging source of variability affecting σV_T and $\sigma log_{10}(I_{OFF})$ for both devices. σV_T produced by GER is a 49% and a 72% smaller than the corresponding RD variations for the FinFET and the GAA NW FET, respectively. The RD variation is 30% larger for the GAA NW FET than for the FinFET, which partly due to the NW's longer S/D regions and to the different lateral peak positions of the Gaussian doping profiles (see $L_{S/D}$ and x_p in Table I). If $L_{S/D}$ for the GAA NW FET is similar to the FinFET's, there is a 13% decrease in the RD variation. Moreover, x_p is lower for the GAA NW FET, implying that the Gaussian doping will penetrate further into the channel leading to the aforementioned increase in variability. The GER variability for σV_T is around 62% and 86% smaller for the FinFET and the GAA NW FET, respectively, than the LER variations, which is the most damaging source of variability. The LER variability is larger for the GAA NW FET than the FinFET because of its smaller channel height leading to a stronger confinement limiting the device conductivity in the transport direction [25]. Moreover, although the impact of GER on the FinFET is greater than on the GAA NW FET, the statistical combination of the four sources shows that the FinFET device is more resilient to the effect of variability (with a σV_{Tcomb} = 30 mV and a $\sigma log_{10}(I_{OFFcomb}) = 0.44$), a value 46% lower for σV_T and 56% lower for $\sigma log_{10}(I_{OFF})$ than that of the GAA NW FET.

IV. Conclusions

We have studied the impact of GER variability on the performance of a 10.7 nm gate length Si FinFET and a 10 nm gate length Si GAA NW FET using two of the main FoM (V_T, I_{OFF}) in the sub-threshold region. The GER induces standard deviations of σV_T = 7 mV and $\sigma log_{10}(I_{OFF}) = 0.16$ for the FinFET when CL/Gate Perimeter = 0.66 and RMS = 0.80 nm, which are around 20% and 11% greater than those of the GAA NW FET. Moreover, we compared the GER variability versus MGG, LER and RD, yielding up to 62% lower impact for the FinFET and 86% for the GAA NW FET for σV_T. Finally, even though the GER impact is greater on the FinFET, this device is more resilient to the combined effect of variability with results approximately 50% lower (σV_{Tcomb} = 30 mV and $\sigma log_{10}(I_{OFFcomb}) = 0.44$) compared to the ones obtained from the GAA NW FET.

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