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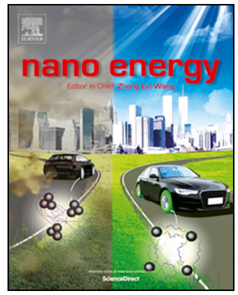

Quantum information memory based on reconfigurable topological insulators by piezotronic effect

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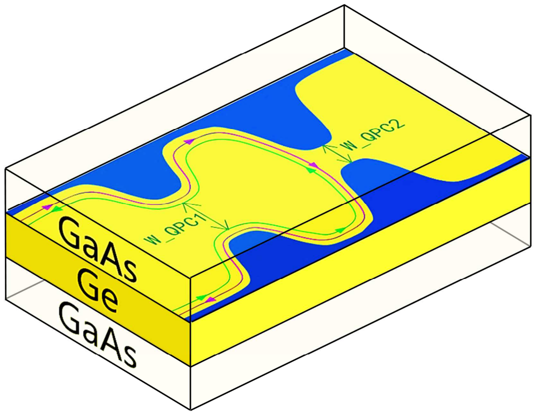

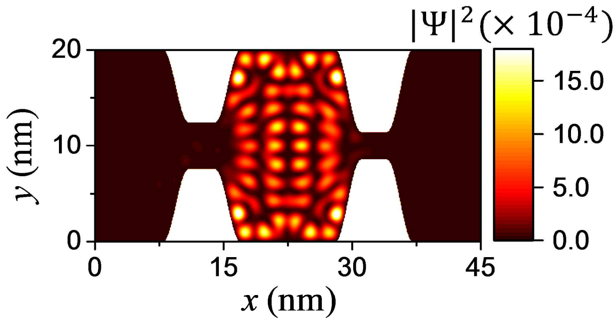

Strain-induced piezoelectric field effectively controls a GaAs/Ge/GaAs quantum well from a normal state to a topological insulator state. The quantum piezotronic device can be used for the low power consumption signal converter and quantum information memory device.

Topological Insulators by Piezotronic Effect

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Abstract

As the emerging fields, piezotronics and piezophototronics have recently attracted extensive attention by the coupling of the semiconductor, photon excitation and piezoelectric properties. Piezopotential can be induced inside a piezoelectric material by applying an external mechanical force, which further adjusts the carrier transport property. In this paper, we theoretically investigate the piezotronic effect on topological insulators based on GaAs/Ge/GaAs quantum well with two quantum point contacts (QPCs). Strain-induced piezopotential can drive a topological phase from normal insulator to topological insulator state. The transport characteristics of edge states and bulk states are studied by calculating the electronic density distribution under various strains. The conductance of the edge states exhibits an excellent switching behavior with the ON/OFF ratio over 10^{10}. By integrating multiple topological insulator systems into a circuit, piezotronic signal converter can be edge state transport of the topological insulator. Besides, at some special circumstances, bulk-state electrons can be trapped by the double QPCs, which can be used to realize quantum information memory devices. This work provides a novel method for developing high-performance piezotronic devices based on topological insulator.

Keyword: piezotronic effect, topological insulator, double quantum point contacts, strain-gated transistors, quantum information memory.

Introduction

Piezoelectric semiconductor materials, such as ZnO, GaN, InN, CdS and monolayer MoS_2, have attracted increasing interests owing to the coupling characteristics of piezoelectric and semiconductor properties [1, 2]. Strain-induced piezopotential can effectively tune the carrier generation, transportation and recombination inside the material [3, 4]. Inspired by ultra-high performance, a variety of piezotronic and piezo-phototronic devices have been developed such as, nanogenerator [5, 6], piezoelectric field effect transistors [7], flexible spintronic devices [8], acoustic wave devices [9, 10], photon detectors [11], solar cells [12, 13] and LEDs (light emitting diodes) [14]. Additionally, utilizing the piezoelectric effect to adjust the quantum states has been proposed for a series of piezotronic devices such as piezotronic strain-gated logic devices [15] and quantum photovoltaic devices [16]. Piezotronic effect is also able to enhance luminescence in ZnO nanowires [17, 18] and the monolayer MoS_2 [19].

Topological insulator, as a new quantum state of matter, has the insulating bulk and conductive surface, which has been demonstrated theoretically and experimentally [20-23]. Its unique edge state is robust in electron transportation process against the nonmagnetic impurity scattering and local perturbation [24-26], making it a promising material to develop non-dissipation devices. Since the discovery of topological insulators in HgTe quantum wells [24, 27], most materials have been witnessed to possess such topological phase under some specific conditions.

Recent studies have suggested that the mechanical force plays an important role to to topological insulator [28, 29]. Furthermore, recent results have demonstrated that in the topological insulator Bi_2Se_3, the Dirac states can be tuned by strain at the atom scale, making it possible to achieve strain engineering in layered topologic insulators [30].

In this paper, we discuss the characteristics of electric switching and charge storage of the quantum structure based on the GaAs/Ge/GaAs quantum well. A thin Ge layer is sandwiched between two GaAs layers to form a quantum well with an inverted band [29]. Double quantum point contacts (QPCs) are formed in the quantum well layer and can be controlled by applying the strain-induced piezopotential on the split gates [15]. Piezopotential effectively manipulates the extension of the Ge layer, hence accurately tuning the width of each QPC [3, 4]. Further, the externally applied strain can change the topological phase of quantum well and effectively modulate the electronic transport property of the system. By calculating the conductance and the electronic density distribution at various applied strains, we observe an electric switching behavior for edge states, which has ultrahigh ON/OFF conductance ratio. In particular, by adjusting the strain and Fermi energy, the electrons can be confined between the double QPCs.

Figure 1 shows the schematic of GaAs/Ge/GaAs quantum well with double QPCs and the band structures. Electronic transport in the middle Ge layer (also named as quantum Hall bar) is strongly dependent of the topological phase that is determined by the QPCs width [31]. Figure 1(a) displays the energy structure for a narrow QPC width of 2 nm. A band gap appears and it corresponds to the normal insulator state. When the Fermi energy is located at the gap region, no quantum states exists and thus the electrons will be blocked in the transport process. Noting that we assume the first QPC width (labeled as QPC1) to be wide and the band structure corresponds to the second QPC (labeled as QPC2). Figure 1(b) shows a gapless case when the QPC width is increased to 8 nm, indicating a topological insulator state. The red line stretching across the conductance and the valence is the gapless edge states [32]. When the Fermi energy is in gapless region, the electrons can travel through the system along its boundaries.

GaAs/Ge/GaAs structure is a good candidate due to the small lattice mismatch between devices and sensors [34, 35].

The transport properties in the GaAs/Ge/GaAs quantum well can be obtained by solving the Schrödinger equation under specific boundary conditions

$$H\psi = E\psi \tag{1}$$

where ψ is wave function with the energy E. H is the Hamiltonian describing the electrons properties in the GaAs/Ge/GaAs quantum well, which are governed by a four-band effective Hamiltonian matrix [29]

$$H = \begin{bmatrix} E_0 + E_1 k^2 & A_1 k_+ & 0 & 0 \\ A_1^* k_- & H_0 + H_1 k^2 & 0 & 0 \\ 0 & 0 & E_0 + E_1 k^2 & -A_1 k_- \\ 0 & 0 & -A_1^* k_+ & H_0 + H_1 k^2 \end{bmatrix} \tag{2}$$

where $k = \sqrt{k_x^2 + k_y^2}$ denotes the in-plane momentum, $k_\pm = k_x \pm i k_y$. Other relevant parameters are $E_0 = -0.19808$ eV, $E_1 = -0.43810$ eV · Å^2, $H_0 = -0.19153$ eV, $H_1 = -0.20810$ eV·Å^2, and $A_1 = 0.028510$ eV·Å [29].

The conductance in GaAs/Ge/GaAs quantum well can be calculated using the Landauer-Büttiker formula [36, 37]

$$G = G_0 \sum_{m,n} | t_{mn} |^2 \tag{3}$$

where $G_0 = e^2 / h$ is conductance unit, t_{mn} is the transmission coefficient for the electrons travelling the system from the *m*th incoming channel to the *n*th outcoming channel.

The boundary of the quantum system has great influence on the transport behavior [38]. Experimental results suggested that the QPC width, as the boundary of the studying system, can be effectively controlled by the applied gate voltage [31]. Hence, the piezopotential arising from the external strain on piezoelectric materials can be used as the gate voltage to modulate the electronic transport.

Piezoelectric charges induced by mechanical strain *S*, can be obtained from the polarization vector *P*, which is given by

The constituting equations can be written as [3, 39]

$$\begin{cases} \sigma = c_E S - e^T E \\ D = eS + kE \end{cases} \tag{5}$$

where E and D represent the electric field and electric displacement vectors. σ and c_E stand for the stress and elasticity tensors. k is the dielectric tensor. Piezoelectric charges polarized by an applied strain induce piezopotential according to the following relationship [3]

$$V_{piezo} = \frac{PL_{piezo}}{\varepsilon_r \varepsilon_0} \tag{6}$$

where L_{piezo} is the length of the piezoelectric material, P is the polarization vector obtained from Eq. (5), ε_r and ε_0 are the relative and vacuum dielectric constants respectively.

For zinc-blende structure grown along the polar direction [111] with shear strain s_{23} along the $y-z$ plane, the piezopotential is given by

$$V_{piezo} = \frac{e_{14} s_{23} L}{\varepsilon_r \varepsilon_0} \tag{7}$$

where e_{14} is the piezoelectric coefficient of zinc-blende piezoelectric material and L is the length of piezoelectric material in the topological insulator.

Results and discussions

1. Transport Properties of the Edge States

Topological insulator has a unique edge state which is topologically protected by the time reversal symmetry and has great potential for developing low power consumption devices [26]. In order to give a direct view of the transportation of the edge state, we plot its electronic density distributions in Figure 2 under different QPCs widths. The Fermi energy is

Figure 2(a) shows that electrons can pass through two QPCs along the top boundary when the QPCs are adequately wide $W_{QPC1} = W_{QPC2} = 8$ nm, corresponding to the full ON state. Figure 2(b) and Figure 2(c) show that the electrons are blocked respectively by the second and first QPC for the width $W_{QPC1} = 8$ nm, $W_{QPC2} = 2$ nm and $W_{QPC1} = W_{QPC2} = 2$ nm. These two blocking cases represent the full OFF state, and no electric current flows through the system. Besides above full ON and OFF cases, electrons can also partially travel through the system under $W_{QPC1} = W_{QPC2} = 5$ nm, as shown in Figure 2(d). In this case, an obvious partial reflection can be observed at QPC2 and is enhanced at QPC1. The above results demonstrate that different QPCs widths can significantly influence the transport behavior of the edge state.

2. Piezotronics Effect on the Topological Insulator

From the previous investigations, the topological phase transition of HgTe quantum well heavily depends on the thickness and width of quantum well [40-42]. A commonly used method to control the width is the usage of the QPC by the split gates [31]. For the GaAs/Ge/GaAs quantum well, the gate voltage is able to broaden or shrink the extension of the depletion region in Ge layer, making it possible to effectively tune the width of each QPC independently. Figure 3(a) shows the side-view schematic of using the strain-induced piezopotential applied on the split gates to modulate the QPC width. The piezopotential is produced at the substrate of GaAs layer. The zinc-blende structure piezoelectric semiconductors, such as CdTe, GaAs, GaP, InSb, and InAs, can be used to form the substrate of the GaAs/Ge/GaAs quantum well. The piezoelectric coefficient e_{14} and relative dielectric constant ε_r are listed in Table I [43].

Figure 3(b) shows the piezopotential as a function of strain for different piezoelectric materials. With the increase of applied strain, the piezopotential increases for CdTe but decreases for GaAs, GaP, InSb, and InAs due to the opposite sign of the piezoelectric

$$W_{QPC} = \alpha(V_{piezo} + V_0) + W_0 \quad (8)$$

where α is the ratio parameter, V_0 is the bias voltage of the split gates, W_0 is the initial QPC width in the absent of piezopotential. The relevant parameters used in the calculation are $\alpha = 225$ nm·V^{-1}, $V_0 = 0.2$ V and $W_0 = 20$ nm [31].

Considering the well width of 20 nm in the system studied, two QPC widths changing with strain s_{23} have upper limit of 20 nm and lower limit of 0 nm, as shown in Figure 3(c). Exceeding the limit leads to unchanged QPC width [15, 44]. By using the quantum transport package KWANT [45], we calculate the conductance in Figure 3(d) as a function of the strain at the fixed Fermi energy $E_F = -0.193$ eV. As mentioned above, this Fermi energy corresponds to the edge states and thus $2G_0$ conductance can be observed. It should be noted that we assume two QPC widths controlled by the same piezopotential and thus only one strain s_{23} can be used in Figure 3(d). However, in Figure 5, we use two independent piezopotentials induced by different strains to control the QPCs. There is a sharp transition between the zero conductance and $2G_0$ conductance in Figure 3(d), behaving as a high-efficienct switching characteristic. For GaAs, the transition occurs at the strain of 0.83%. When the strain is lower than the transition point, the QPC width becomes wide and thus the electrons can travel through the system, leading to the ON state. The electrons can be fully blocked if the strain is larger than the transition point, giving rise to the OFF state. The transition points are -3.46%, 1.23%, 2.78%, and 3.98%, for CdTe, GaP, InSb, and InAs, respectively. Because the electronic backscattering is suppressed for the edge states, ultra-low power consumption can be achieved [25, 26, 32].

Strain-induced piezoelectric field can not only parallelly modulate the conductance in the topological insulator, it can also perpendicularly control the electronic transport in heterojunction devices. Recent reports have demonstrated that by using a perpendicular piezoelectric field in AlGaN/AlN/GaN heterojunction, the electric transport of microwire quantum well devices [33].

3. Piezotronic Signal Converter Based on Edge-state Transport

Due to the excellent switching behavior shown in Figure 3(d), we propose a novel method to design a signal converter that can achieve the conversion from external mechanical stimulus to digital logic output. For simple illustration, we choose three topological insulator systems with different piezoelectric materials including GaP, InSb and InAs, which are respectively labelled as system A, B and C. It is convenient to define the logic signal “1” for ON state and “0” for OFF state [15, 44]. Their conductance is plotted in Figure 4(a). Because of their different switching strains, integrating those three systems into a circuit in parallel connection can be used to design a strain signal converter, as shown in Figure 4(b). We define the output signal of this parallel circuit as “*abc*” where, *a*, *b* and *c* are the logic outputs of the system A, B and C, respectively. Specifically, for the strain varying from 0 to 1.23% in region I, all three systems are at ON state, and thus the output logic signal is “111”. When the strain is in region II from 1.23% to 2.78%, system B and C are at ON state, but system A is at OFF state, resulting in “011” output. With the strain increasing to region III from 2.78% to 3.98%, system A and B are at OFF state and C is at ON state, leading to the output “001”. Further increasing the strain greater than 3.98% in region IV, all three systems are completely blocked and thus have no current, giving rise to the output “000”. Note that external strain is simultaneously applied on three different systems, as shown in Figure 4(b). This strain dependence of output logic signal is the principle of the piezotronic signal converter. The truth table for this converter is shown in Figure 4(c). We can distinguish these four output signals “111”, “011”, “001” and “000” to binary logic signal “11”, “10”, “01” and “00”, respectively.

Because the ON state corresponds to the edge state, such signal converter based on the topological insulator has ultra-low power consumption, which possesses outstanding advantages compared with the conventional strain converter. For instance, for GaN nanobelt-based strain-gated piezotronic logic devices, the currents of ON state and OFF state

ON/OFF ratio over 10 for each subsystem. Even in the "111" state, the power dissipation caused by the edge states is very low [48]. For recently proposed piezotronic logic devices based on strain-gated transistors (SGTs), switching on more SGTs requires a large amount of unnecessary energy wasted on those SGTs already in ON state [49]. By contrast, the piezotronic logic signal converter devices based on topological insulator can perfectly overcome this shortcoming. As a subsystem is once switched on, its energy loss maintains unchanged due to its constant $2G_0$ conductance. Integrating more subsystems with different switching points can realize more precise conversion from mechanical stimulus to logic output signal. Therefore, piezotronic signal converter based on the topological insulator can achieve ultra-low power consumption and high precision devices.

4. Quantum Information Memory Device Based on Charge Trapping Cells in Bulk-state Transport

When the Fermi energy is fixed at some other particular values, bulk states occur. Figure 5(a) shows the conductance as a function of two different strains for CdTe material at the Fermi energy $E_F = -0.189$ eV where seven bulk states (also call channels) are opened. In this case, two QPC widths are independently controlled by different strains. The horizontal coordinate-axis and longitudinal coordinate-axis are the strains imposed on the QPC1 and QPC2, severally. In contrast to edge states, the conductance of the bulk states exhibits some obvious step-like plateaus. For illustrating the origination of those conductance plateaus, we assume one QPC with its maximum width and vary another one by the strain. For the strain lower than -3.47% where the QPC is narrow enough, the electrons in different bulk channels are all blocked and thus zero conductance is observed. When the strain changes from -3.47% to -3.31%, the first bulk channel is opened, leading to one $2G_0$ conductance plateau. As the strain further increases, the QPC width becomes wide. More and more bulk channels will be opened and contribute each $2G_0$ conductance to the total plateau, giving rise to the staircase nm, $W_{QPC2}=3.0$ nm, the electrons will be entirely confined between two QPCs, as shown in Figure 5(b). According to the method in Ref. [34], we calculated the bandstructure, as shown in Figure 1. When the Fermi energy is from -0.191 eV to -0.196 eV, the electronic state is edge state. When the Fermi energy is out of this region, it is bulk state. Figure 5(c) shows another case where the electrons injected from the left lead are completely blocked by the first QPC when the Fermi energy is fixed at -0.191 eV and $W_{QPC1}=4.5$ nm, $W_{QPC2}=3.5$ nm. This charge trapping cell based on the QPCs and topologic insulators provides the possibility of storing information, which is different from the conventional means of charge storage. Figure 5(d) shows the schematic of the charge-trap memory based on GaAs/Ge/GaAs topological insulator. The applied strain can confine the electrons between QPCs in Ge layer. The stored charge effectively shifts the threshold voltage between source and drain, corresponding to the "write" of information [50, 51]. Removing the applied strain, the stored charges are free and threshold voltage changes back, which is the "erase" of information [50, 51].

Conclusion

In this study, we investigate the electronic transport properties based on the GaAs/Ge/GaAs quantum well with double QPCs. The width of QPCs is controlled by the strain-induced piezopotential that leads to the topological insulator transition. The conductance of edge states saturates to $2G_0$ with the increasing of the QPCs width, exhibiting an excellent switching behavior. In this case, a signal converter is demonstrated to realize the transformation from external mechanical stimulus to digital logic output. The converter is based on the electronic transport of the edge states and has an ultrahigh ON/OFF ratio. Besides, the conductance of bulk states presents the staircase shaped plateau with the increase of the new opened bulk channels. In particular, by appropriately controlling the Fermi energy and mechanical strain, a clear charge trapping between the double QPCs can be

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UESTC. He is interested in new semiconductor nanodevices, and focuses on theory of piezotronics and piezophototronics.

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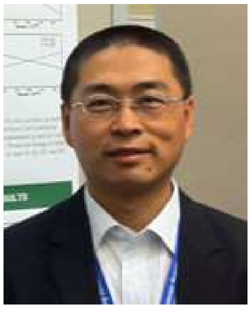
Minjiang Dan is currently pursuing his B.S. degree in the University of Electronic Science and Technology of China (UESTC). He is now simulating piezotronic devices under the guidance of Professor Yan Zhang in School of Physics. His interests focus on the quantum piezotronics, semiconductor device and solar cell.

Lijie Li is a professor at Swansea University, UK. His research interests are design, modeling, fabrication, and characterization of MEMS, NEMS, sensors and actuators. He is Fellow of IET, and senior member of IEEE.



Yan Zhang is a professor at University of Electronic Science and Technology of China. He received his B. S. degree (1995) and Ph.D degree in Theoretical Physics (2004) from Lanzhou University. His research interests include self-powered nano/micro system, piezotronic and modeling of nonlinear dynamics of NEMS. He is senior member of IEEE.

Figure 1. Schematic of the GaAs/Ge/GaAs quantum well with double QPCs and the band structures. The spin-up (purple line) and spin-down (green line) electrons travel along different boundaries. (a) The energy structure for a narrow QPC width of 2 nm. The electrons are blocked in the transport process. (b) Gapless energy structure for a wide QPC width of 8 nm (the red lines express edge states). The electrons travel the system without blocking.

Figure 2. Electronic density distributions of edge states under different QPCs widths. The Fermi energy is fixed at -0.193 eV. (a) Full ON state under $W_{QPC1} = W_{QPC2} = 8$ nm. (b) Full OFF state under $W_{QPC1} = 8$ nm and $W_{QPC2} = 2$ nm. (c) Full OFF state under $W_{QPC1} = W_{QPC2} = 2$ nm. (d) Partial reflection under $W_{QPC1} = W_{QPC2} = 5$ nm.

Figure 3. (a) The side-view schematic of using the strain-induced piezopotential applied on the split gates to modulate the QPC width. (b) Piezopotential as a function of strain for different piezoelectric materials (CdTe, GaAs, GaP, InSb, and InAs). (c) The QPC width as a function of strain. (d) Conductance as a function of strain at fixed Fermi energy $E_F = -0.193$ eV.

Figure 4. (a) Conductance as a function of strain for three different piezoelectric materials (InAs, InSb, GaP). The Fermi energy is fixed at $E_F = -0.193$ eV. Region I is from 0 to 1.23%, region II is from 1.23% to 2.78%, region III is from 2.78% to 3.98% and region IV is over 3.98%. (b) Schematic of piezotronic signal converter based on edge-state transport. (c) Truth table for the converter under strain in different regions.

Figure 5. (a) Conductance as a function of two different strains for CdTe material. The Fermi energy is fixed at -0.189 eV. The horizontal coordinate-axis and longitudinal coordinate-axis

nm and $W_{QPC2} = 3.5$ nm. (d) Schematic of charge-trap memory based on GaAs/Ge/GaAs topological insulator.

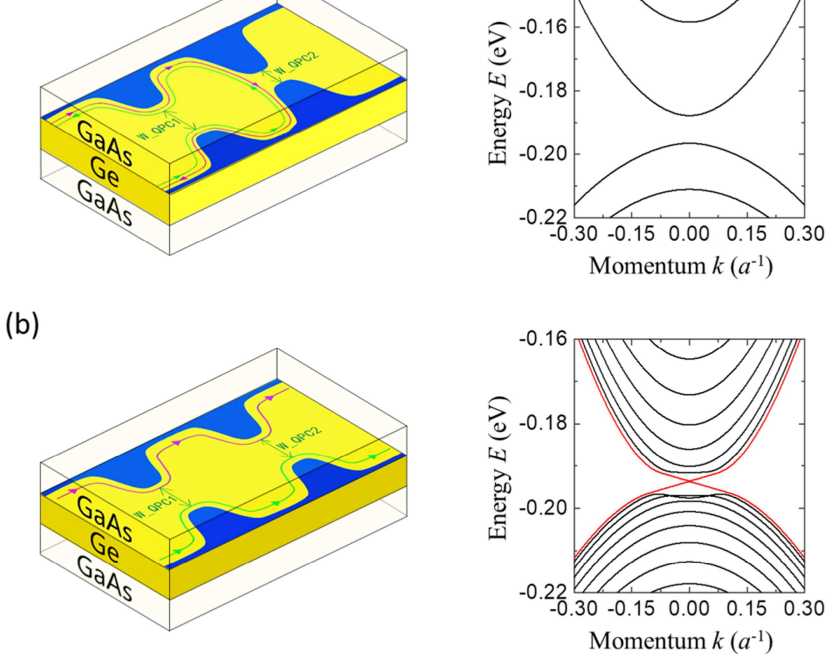


Figure 1

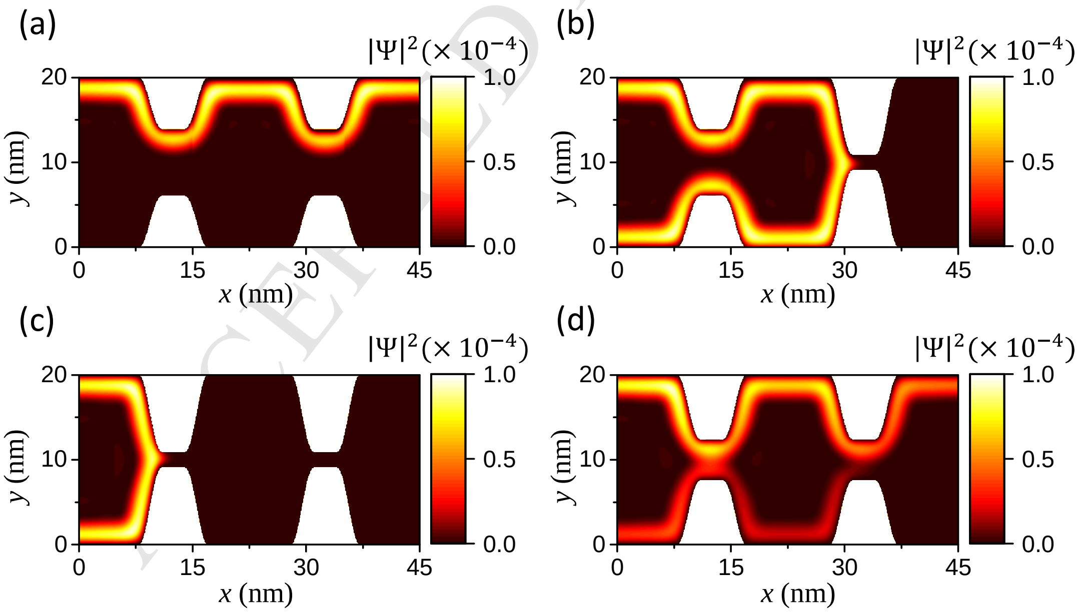


Figure 2

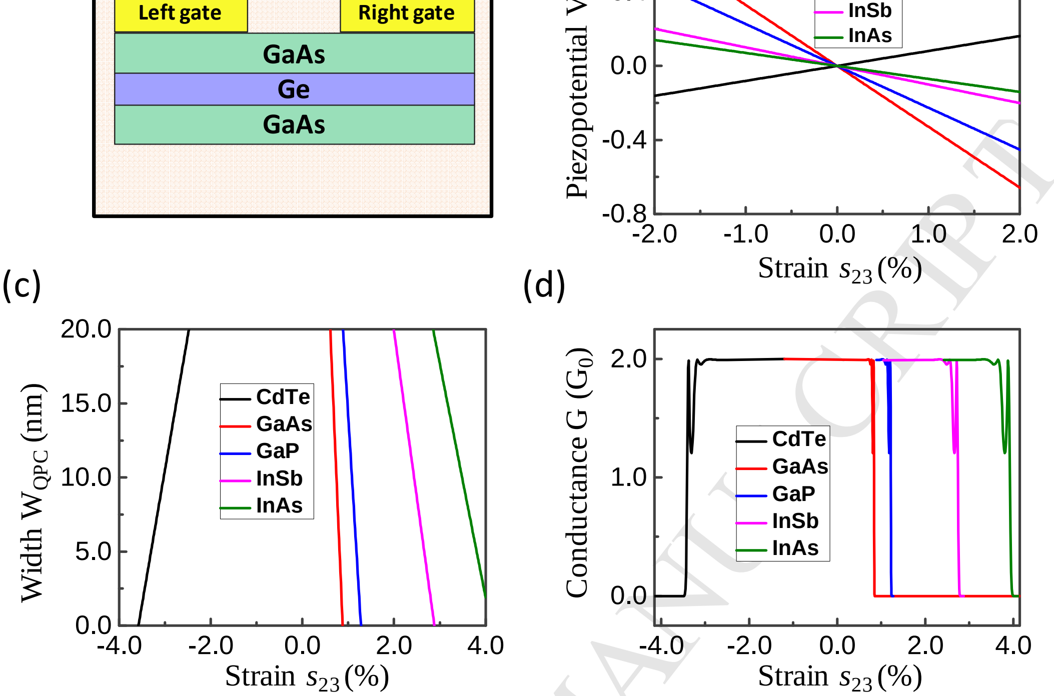
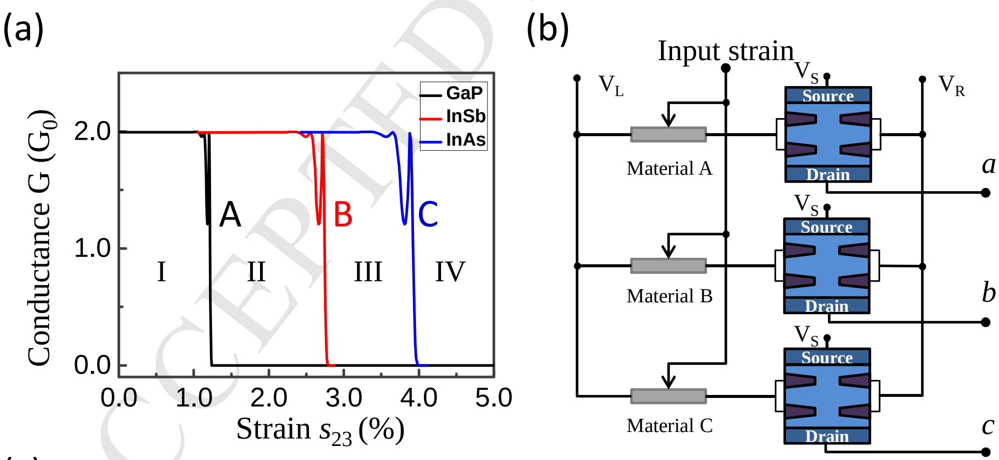


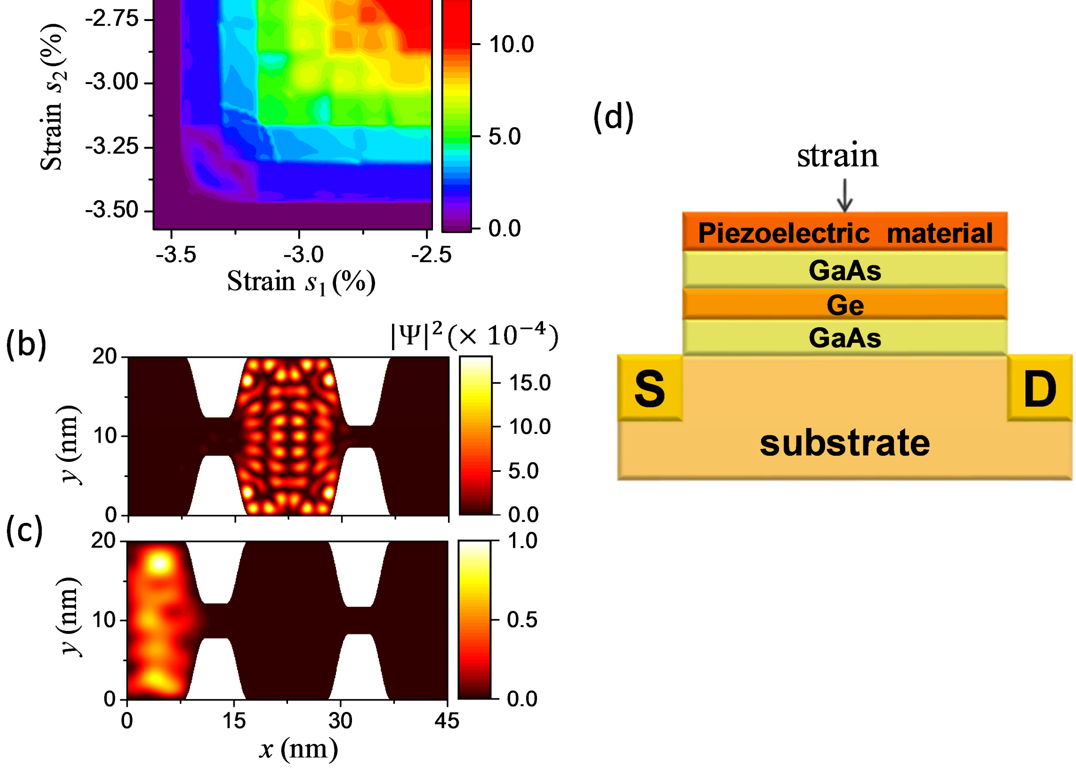
Figure 3



(c)

strain	*a*	*b*	*c*	output
I (0-1.23%)	1	1	1	“11”
II (1.23%-2.78%)	0	1	1	“10”
III (2.78%-3.98%)	0	0	1	“01”
IV (3.98%-)	0	0	0	“00”

Figure 4



-2.75
-3.00
-3.25
-3.50
Strain s_2 (%)
10.0
5.0
0.0
-3.5
-3.0
-2.5
Strain s_1 (%)
(b)
$|\Psi|^2 (\times 10^{-4})$
20
10
0
y (nm)
15.0
10.0
5.0
0.0
(c)
20
10
0
y (nm)
1.0
0.5
0.0
0
15
30
45
x (nm)
(d)
strain
Piezoelectric material
GaAs
Ge
GaAs
S
D
substrate

Figure 5

Table I. Piezoelectric Coefficients and Relative Dielectric Constants for the Zinc Blende Material used in this study

Material	Piezoelectric coefficient e_{14} (C/m^2)	Relative dielectric constant ε_r
CdTe	0.035	9.8
GaAs	-0.16	11
GaP	-0.1	10
InSb	-0.071	16
InAs	-0.045	14.5

investigated.

2. Strain-induced piezopotential modulates the edge-state transport in topological insulators.

3. A piezotronic signal converter and quantum information memory device are demonstrated based on double quantum point contacts.