Design and implementation of digital phase locked loop for single-phase grid-tied PV inverters

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Abstract: In this paper, a synchronous rotating-frame based phase-locked loop (PLL) for a single-phase PV inverter control system is presented. Detailed PLL mathematical model and the digital implementation for a single-phase PV inverter system are presented. A practical solution for transport delay based orthogonal signal generation using first-in-first-out (FIFO) circular buffer is also discussed. Details of implementation for a real-time system using digital signal processor were also described. The performance of the developed PLL was experimentally verified on a developed single-phase PV inverter prototype.

Key worlds: Single-phase PLL, orthogonal signal generator, PI controller, and single-phase PV inverter

1. Introduction

The photovoltaic (PV) technology is now widely applied in industrial, commercial, residential community and grid-connected PV plants. The PV inverters can provide an opportunity to maximizing the energy capture, and control of generating high-quality energy. Figure 1 shows a grid-connected single-phase photovoltaic electric power conversion system [1]. The PV system consists of a solar array, a PV inverter with an output filter, insulation transformer. The PV array is connected to utility system through a PV inverter. For a single-phase PV system, the PV array comprises a number of series connected solar panels to ensure the dc link voltage is higher than the peak ac voltage for converting the dc voltage into a utility grid voltage. It can be seen from Figure 1 that the main elements of the control system of the grid-connected PV converter are the synchronization algorithm based on phase-locked-loop (PLL), the maximum power point tracking (MPPT), and the current controller including the PWM control signal generation. Therefore, the PV inverter controls the PV array's output voltage and current based on the MPPT control algorithm so that the PV array always operate at its maximum power points. The PV inverter is also responsible for the control of the output current to provide a unity power factor operation by synchronizing the inverter output sinusoidal current in phase with the grid voltage. The PLL is used to synchronize the PV inverter output current with the grid voltage to achieve a unity power factor operation of the inverter output as well as to provide a clean sinusoidal reference current i_g^* to the current controller.

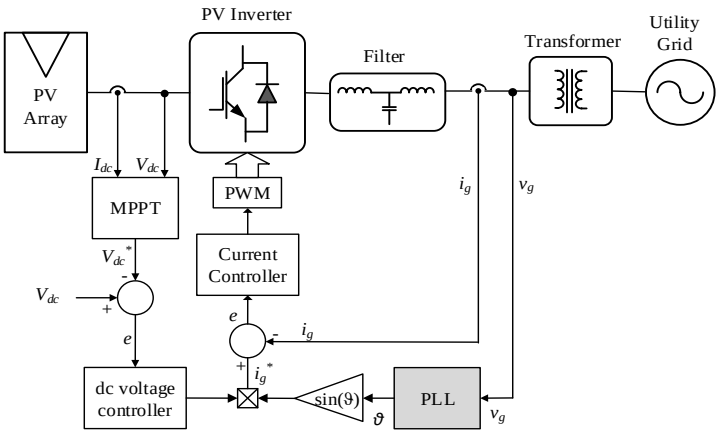


Figure 1 PV system electrical connection

The key to achieving the synchronous with the grid voltage is to detect the phase angle information of the grid voltage. PLL is one of the most common methods to detect the phase angle of grid voltage due to its robustness, effectiveness, simplicity [2-6]. A typical single-phase PLL usually comprises of three parts: a phase detector (PD), a loop filter (LP) and a voltage controlled oscillator (VCO). A proportional-integral (PI) controller usually implements the loop filter, which outputs the estimated angular frequency. The integration of the angular frequency determines the phase-angle, which is conducted by the VCO. A phase detector is a frequency mixer or analog multiplier that generates a voltage signal that represents the difference in phase between two inputs. The phase detector (PD) can be constructed in a stationary frame (SF) [4, 5, 6 and 7] or in a synchronous rotating frame (SRF) [8, 9]. Figure 2 shows the block diagram of a stationary-frame based PLL.

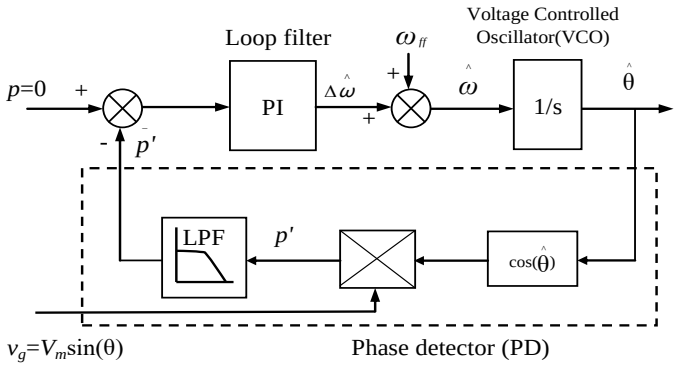


Fig. 2 Block diagram of a stationary-frame based PLL

In Figure 2, v_g is the input voltage signal whose phase angle need to be estimated. A feedforward component ω_{ff} used in improving the initial dynamic performance of the PLL is the nominal value of the angular frequency of the input voltage signal (for 50Hz, ω_{ff} =314 rad). The phase angle θ can be estimated by the integration of the

estimated angular frequency $\Delta\hat{\omega}$ this is achieved by multiplying the grid voltage signal v_g with $\cos(\hat{\theta})$. The virtual power p' is expressed as:

$$p' = V_m \sin(\theta)\cos(\hat{\theta}) = \bar{p}' + \tilde{p}' \tag{1}$$

$$\bar{p}' = \frac{V_m}{2}\sin(\theta - \hat{\theta}), \tag{2}$$

$$\tilde{p}' = \frac{V_m}{2}\sin(\theta + \hat{\theta}) \approx \frac{V_m}{2}\sin(2\omega t) \tag{3}$$

Where equation (2) and (3) represents the dc-component and the double-frequency component, respectively. For small phase-angle difference equation (2) can be approximated by equation (4).

$$\bar{p}' = \frac{V_m}{2}\sin(\theta - \hat{\theta}) \approx \frac{V_m}{2}(\theta - \hat{\theta}) \tag{4}$$

Equation (4) is approximately a constant in steady state and gives the information of the phase difference. The PLL model should be designed to cancel the small dc component so that the output of PLL can represent the phase angle of the grid voltage.

However, it can be seen from the equation (1) that the double-frequency component in the virtual power p', have a relatively high amplitude, the high double-frequency component will degrade the accuracy of the phase angle estimation and therefore must be filtered out.

Reference [7] and [8] present PLL based on the synchronous rotating frame (SRF), in which the fundamental component of the input voltage signal is shifted by 90° to create an orthogonal voltage signal to form a virtual two-phase system so that the Park transformation can be applied. With this method, the entire control signals were transferred into the synchronous rotating d-q frame so that the PLL closed loop can eliminate the steady-state errors with a simple PI regulator. By using the synchronous rotating frame (SRF) based PLL, the double-frequency ripple in the stationary frame is eliminated.

This paper presents the mathematical model and the implementation of a single-phase SRF-PLL. The paper also discussed the generation of orthogonal signals for a single-phase SRF-PLL. In addition, a practical design of the SRF-PLL for a real-time system and experimental results and analysis will be presented.

2 Mathematical models of SRF-PLL

Figure 3 shows the block diagram of a single-phase SRF-PLL.

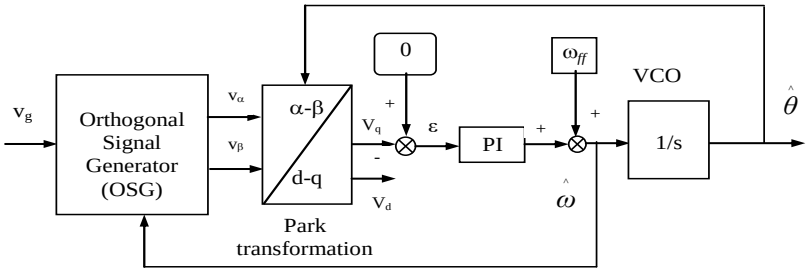


Figure 3 block diagram of single-phase SRF-PLL

Figure 3 shows a synchronous rotating-frame PLL. The Park transformation needs two input voltage signals v_α and v_β. The two-phase voltage signals can be naturally converted in three-phase systems by using Clarke transformation. However, in a single-phase system as there is only one phase voltage signal available so the orthogonal voltage signal must be constructed based on the available one phase voltage signal. There are several algorithms to generate the orthogonal signal for single-phase systems, such as Hilbert Transformer-Based PLL discussed in [18], the transport-delay based method in [19, 20 and 21] and the inverse Park-Transformation based PLL discussed in [13] and [22].

With the PLL based on Hilbert Transformer, the orthogonal signal is generated using the Hilbert transformer. With this method, all the harmonic content is phase-shifted by 90^o, and the process is relatively complicated for real-time application.

The transport-delay based method is easily implemented using a first-in-first-out (FIFO) buffer, with a size set to one fourth the number of samples contained in one cycle of the fundamental frequency. All the harmonic content of the input signal is subjected to the same time delay.

With the inverse Park-transformation based PLL, a single-phase voltage v_β, and an internally generated orthogonal signal v_α are the inputs to a Park transformation block. The v_α is obtained using an inverse Park transformation, the input data of the reverse park transformation is the output of the Park transformation fed through first-order low pass filter. Although the inverse Park transformation based PLL requires only one inverse Park transformation and two first-order low-pass filters, it is not very complicated for practical implementation. However, tuning the time constant of the filters is a complicated process, as compared with the other PLL algorithms.

In this paper, the transport-delay method was implemented using a first-in-first-out (FIFO) buffer, with a size set to one fourth the number of samples contained in one cycle of the fundamental frequency of grid voltage. For a sampling frequency of 25 kHz, there will be 500 sampling points in one period of the fundamental frequency. Assume $v_\beta(k) = v_g(k)$, the voltage of v_α at the *k*th sampling point was constructed by shifting sampled grid voltage signal $v_g(k)$ by 125 points, i.e. $v_\alpha(k) = v_g(k-125)$. The method was implemented by using the circular memory array available in the ADMC401 microprocessor, which can be provided by most microprocessors. Figure 4 shows the practical solution for the transport-delay method.

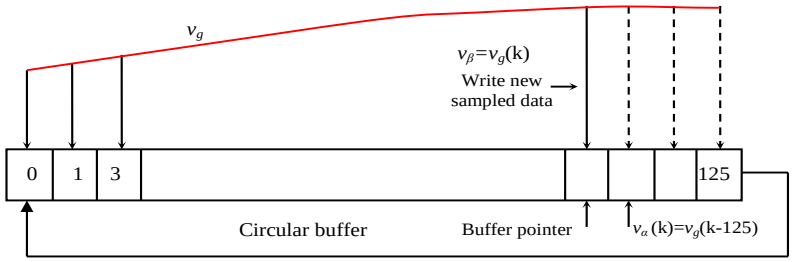


Fig. 4. Practical solution for transport-delay method using first-in-first-out (FIFO) circular buffer

In Figure 4, assume $v_\beta = v_g = \mathrm{V_m}\sin\theta$ and $v_\alpha = \mathrm{V_m}\cos\theta$, where θ is the phase angle of the grid voltage. By applying Park transformation to the virtual two-phase voltage signals, v_α and v_β, the voltage components in the rotating *d-q* frame V_d and V_q can be expressed by equation (5).

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos(\hat{\theta}) & \sin(\hat{\theta}) \\ -\sin(\hat{\theta}) & \cos(\hat{\theta}) \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{5}$$

Where $\hat{\theta}$ represents the estimated phase angle of the grid voltage. By substituting $v_\alpha = V_m\cos\theta$ and $v_\beta = V_m\sin\theta$ to equation (5), the voltage components in the rotating *d-q* frame V_d and V_q can be expressed as (6):

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \mathrm{V_m}\cos(\hat{\theta}-\theta) \\ \mathrm{V_m}\sin(\hat{\theta}-\theta) \end{bmatrix} \tag{6}$$

When the difference of $\hat{\theta}-\theta$ is sufficiently small, the voltage components in rotating frame V_d and V_q can be expressed as (7):

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} V_m \cos(\hat{\theta} - \theta) \\ V_m \sin(\hat{\theta} - \theta) \end{bmatrix} \approx \begin{bmatrix} V_m \\ V_m(\hat{\theta} - \theta) \end{bmatrix} \tag{7}$$

where V_q is proportional to the error between estimated and actual phase angles. If V_q is regulated to zero, the phase angle difference $\hat{\theta} - \theta$ will be zero. This means that the PLL output follows the actual phase angle of the grid voltage.

To effectively achieve the zero-phase difference of the output current against output voltage a PI-controller based loop filter must be appropriately designed. Figure 5 shows the small signal model of the PLL closed loop system.

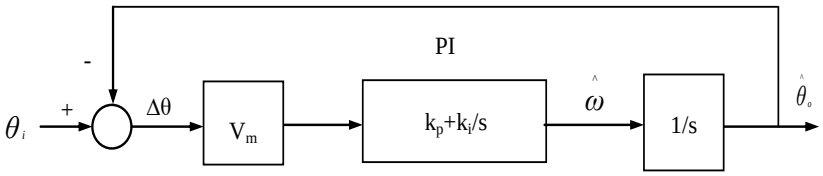


Fig.5 Small signal model of the PLL closed loop

Where V_m is the amplitude of the grid voltage, k_p and k_i are the proportional and integral gains of the PI controller, respectively. The transfer function of the PLL closed loop system is given by equation (8)

$$\frac{\hat{\theta}_o(s)}{\theta_i(s)} = \frac{V_m k_p s + V_m k_i}{s^2 + V_m k_p s + V_m k_i} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{8}$$

Where ω_n represents the natural frequency, and it is expressed by $\omega_n = \sqrt{V_m k_i}$, ζ is the damping ratio of the closed-loop system, and it is expressed by $\zeta = \frac{k_p}{2k_i}\omega_n$.

Equation (8) is a typical transfer function of a second-order system. The damping ratio ζ was set as 0.707. The response speed of the PLL can be determined by the value of natural frequency ω_n. The higher the natural frequency, the faster the dynamic response and less damp effect. Therefore, a trade-off must be considered between response speed and damping effect. For a single-phase PV system with a voltage of 240V/50Hz, the corresponding k_i and k_p of the PI regulator were set as 46.4 and 0.52, respectively. Figure 6. shows the dynamic response of the PLL closed-loop system with different damping ratios and different natural frequencies. In this paper, the natural frequency ω_n was set as $\omega_n = \sqrt{V_m k_i} = 50 \times 2\pi = 314$ rad.

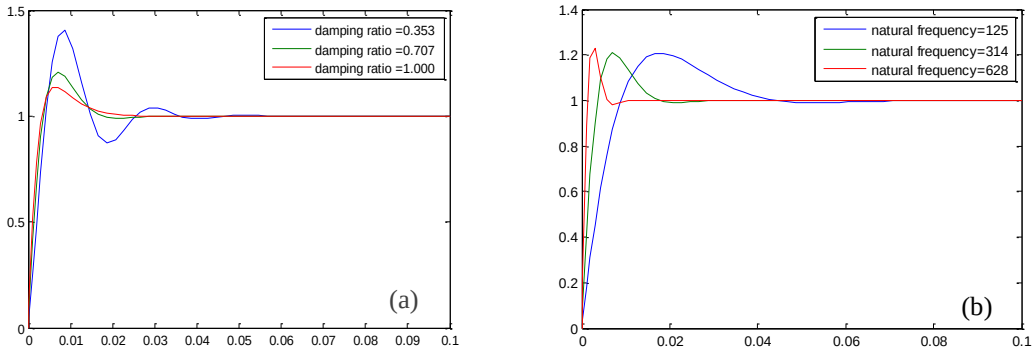


Fig. 6 Dynamic response of PLL closed-loop: (a) with $\omega_n = 314$ and different damping ratios;

(b) with ζ = 0.707 and different natural frequencies

Considering the voltage in the rotating *d-q* frame V_q as the input to the PI regulator, the estimated phase angle of the grid voltage in the practical digital implementation is expressed by equation (9).

$$\hat{\theta}(k+1) = \hat{\theta}(k) + A_1 \cdot V_q(k) + A_0 \cdot V_q(k-1) + \Delta\hat{\theta} \tag{9}$$

where, $\hat{\theta}(k+1)$ is the reference angle for the next sampling step. The coefficients A_1 and A_0 are calculated by equation (10)

$$\begin{aligned} A_1 &= k_i \cdot \frac{T_{sample}}{2} + k_P, \\ A_0 &= k_i \cdot \frac{T_{sample}}{2} - k_P, \\ \Delta\theta &= \frac{f_{fundamental}}{f_{sample}} \cdot 360^o \end{aligned} \tag{10}$$

Where $f_{\text{fundamental}}$ and f_{sample} are the voltage fundamental nominal frequency and digital sampling frequency respectively. The values of sine and cosine for an electrical angle are calculated by equation (11).

$$\sin(\theta) = 3.1406250\theta + 0.0202636\theta^2 - 5.3251960\theta^3 + 0.5446778\theta^4 + 1.8002930\theta^5 \tag{11}$$

The approximation is accurate for any value of θ from 0° to 90° (the first quadrant). However, because $\sin(-\theta) = -\sin(\theta)$ and $\sin(\theta) = \sin(180^o - \theta)$, the sine of any angle can be obtained from the sine of an angle in the first quadrant. On this scale, 180° equals the maximum positive value 7FFFh, and –180° equals the

maximum negative value as shown in Fig.7. The result is accurate to within the least significant bits (LSBs) for sin(θ).

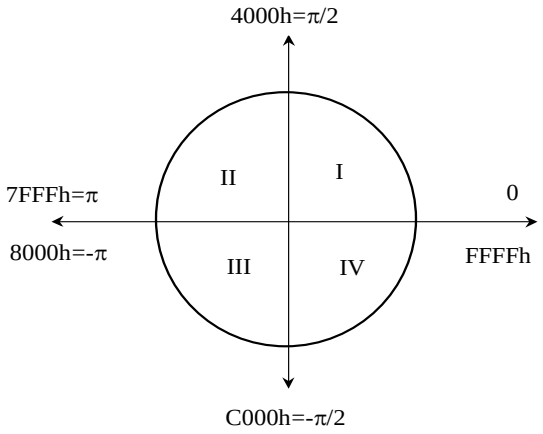


Fig.7 Scaled angle values in microprocessor

The value of cosine can be calculated by using equation (12).

$$\cos(-\theta) = \sin(90^o + \theta) \tag{12}$$

The accuracy is again within two least significant bits (LSBs). In a steady-state single-phase system, the voltage components in the rotating *d-q* frame are represented by equation (13):

$$\begin{aligned} V_d(k) &= V_m \\ V_q(k) &= 0 \end{aligned} \tag{13}$$

where V_m is the peak value of the input voltage signal, *k* represents the *kth* sampling point.

3. Experimental system configuration and test results

An experimental single-phase PV inverter prototype was built in the laboratory for the validation of the developed PLL control algorithm. The experimental system circuit connection and the developed prototype hardware are shown Figure 8 and Figure 9 respectively. The experimental system comprises of four parts: the variable transformer-based power supply unit, PV inverter constructed using ST-STGIPL14K60 IGBT module, a boost DC/DC converter and an emulated PV source.

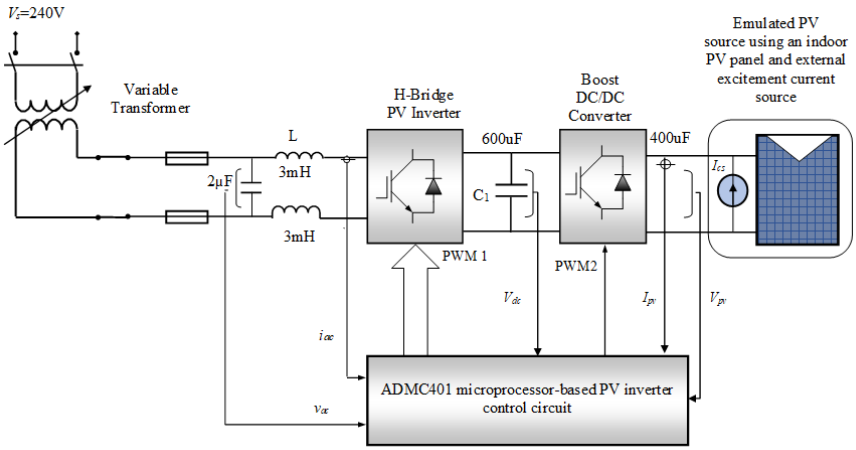
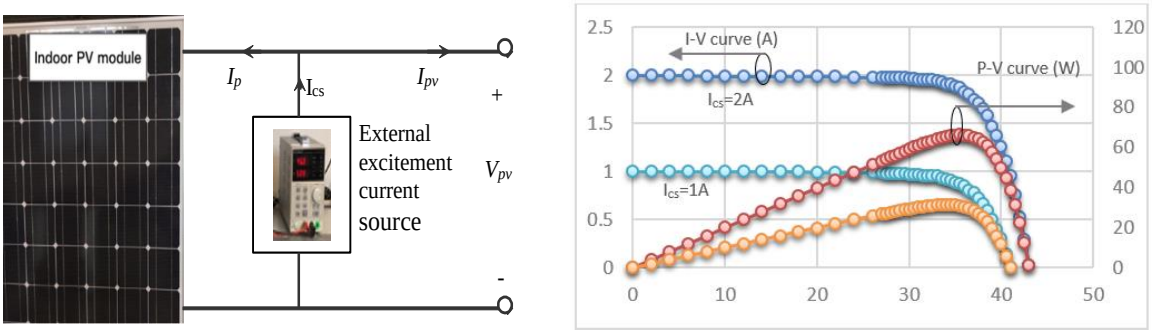


Figure 8 PV inverter experiment circuit connection

The emulated PV source was built by using an indoor PV panel and a DC power supply in the laboratory. Figure 9 shows the circuit connection of the constructed PV source, in which a 175W SUNTEC solar panel and a 1250W DC power supply (TENMA 72-2940) operating in constant current mode is connected in parallel.



(a) (b)

Figure 9 (a) Experiment setup of constructed PV source (b) Measured I-V and P-V curves with different external excitement currents

In Figure 9 (a), I_{CS} represents the external excitement current which is injected into the PV module and the PV converter. The output current of the proposed PV source is given by $I_{pv} = I_{cs} - I_p$.

In the laboratory environment, almost no current can be generated from the solar panel, so the photo-generated current $I_{ph} \approx 0$. In this experiment, the photo-generated current I_{ph} was emulated by the external excitement current source I_{cs}. The voltage of the PV panel will depend on the current injected to the solar panel. The electrical characteristics of the proposed PV source were measured in the laboratory using a 1800W DC electronics load (PRODIGIT 3362F). The measured I-V and P-V curves with 1Amp and 2Amp external excitement currents, respectively, are shown in Figure 9(b).

Figure 10 (a) and (b) shows PV converter experiment test set-up and PV inverter circuit. The single-phase PV inverter bridge was constructed by using ST-STGIPL14K60 IGBT module.

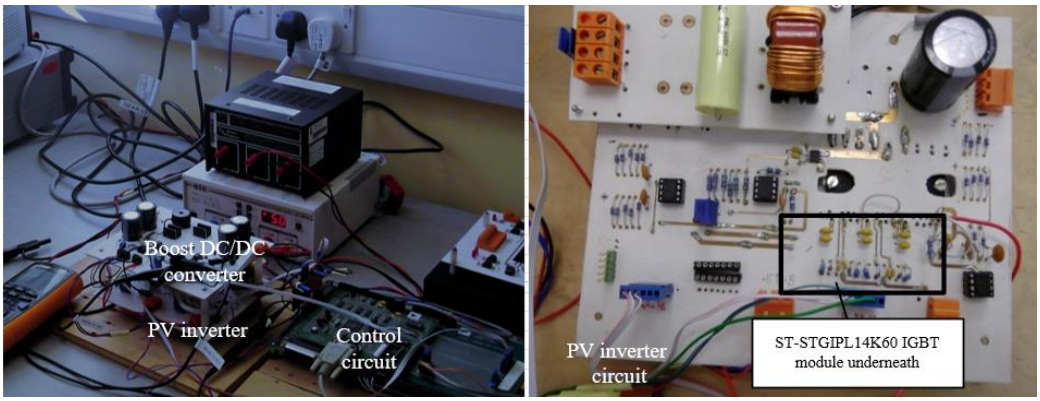
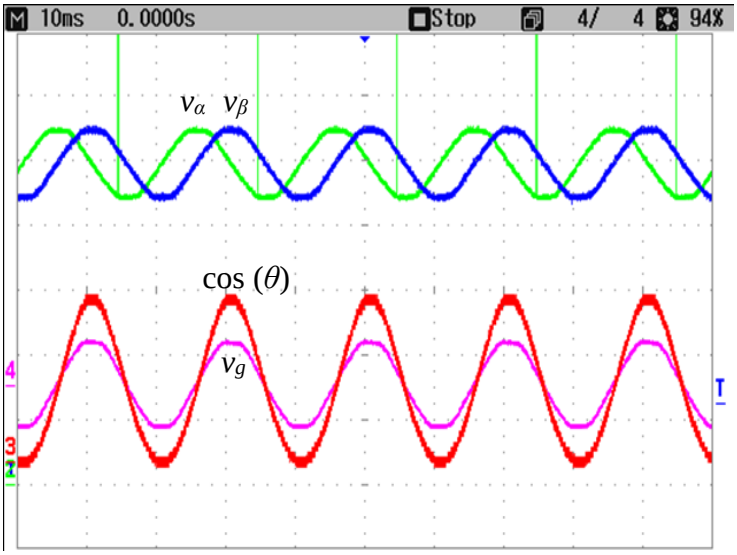


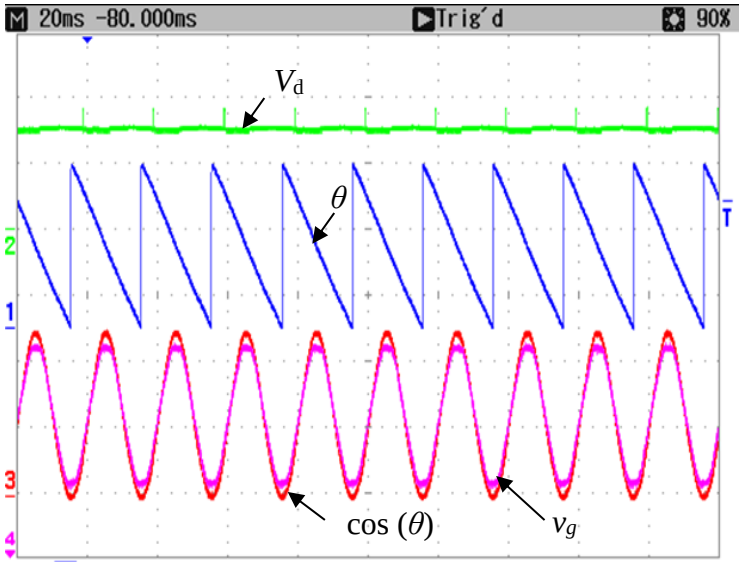
Figure 10 (a) PV converter experiment test set-up (b) PV inverter circuit

The IGBT module is a small and low power loss intelligent module; it is integrated with gate driving circuits and freewheeling diodes. The rating of each IGBT device is 15A/600V. Two aluminum electrolytic capacitors, each rated 300μF/450V, were connected in parallel. One resistor with 10KΩ was used across the capacitors to provide a discharge path for the energy in the capacitors when the circuit is switched off. A 3mH common coupled inductor was employed at the output side of the PV inverter. Two ultra-rapid 5A fuse was used to protect the inverter circuit. Differential amplifier circuit was built for measuring the grid voltage. Line current was measured by a current sensor ACS712 based circuit**.** For evaluating the performance of the developed digital PLL**,** a serial 12-bit DAC AD7568 converter (each of the converters was configured in voltage mode and provides an analog output that is proportional to the applied digital value) was employed to output the signals that was unable to be measured directly, such as the voltage components V_d, V_q in the rotating d-q frame, the estimated grid voltage phase angle θ and cos(θ). The values are treated in the range from -1 to 0 and 0 to +1 and will be displayed as 0V, 2.5V, and 5V on the oscilloscope for the values of 0 -1, 0, and +1 respectively. The utility voltage is 240V/50Hz. The role of the variable single-phase transformer is to obtain a variable ac supply voltage to the PV inverter so that experiment tests can be carried out under relatively low voltage condition for safety reason.

Unipolar PWM switching strategy with 25kHz of switching frequency for the single-phase PV system was implemented for the control of the single-phase PV inverter. A boost DC/DC converter was built to boost the PV source voltage for the PV inverter. Experiments were carried out under low grid voltage by using a single-phase variable transformer. Figure 11 (a) shows the performance of the developed PLL under steady-state operating condition.



(a) Waveforms from top to bottom are virtual two-phase voltage signals, v_α, v_β, grid voltage v_g (55V/Div.) and cos (θ) (2V/div)



(b) Waveforms from the top are V_d in the rotating *d-q* frame, estimated phase angle θ, (144°/div), grid voltage v_g (55V/div) and cos (θ) (2V/div)

Fig.11 Test results in steady state operating condition

The waveforms from top to bottom are the virtual two-phase voltage signals v_α, v_β, the grid voltage v_g, and the cosine value of the estimated phase angle. In the experiment, the cosine value of the grid voltage phase angle is output by DAC-AD7568 of the ADMC401 microprocessor based development board (for the values of ±1, the outputs are ±2.5V). It can be seen from Figure11 that cos (θ) was synchronized successfully to the actual grid voltage phase angle. Although there are harmonics in the grid voltage, the phase angle is still estimated accurately.

Figure 11 (b) shows the characteristics of the developed digital PLL under steady state. Results shown from top to bottom are: the dc component V_d in the rotating *d-q* frame, the estimated grid voltage phase angle θ which varies linearly between 0 to 360°), the grid voltage v_g, and cos (θ) of the input voltage. The dc component V_q is controlled to be zero by the operation of the PLL, and this wasn't shown in the test results.

Fig. 12 shows the transient response of the developed PLL in the start operation. The results shown from top to bottom are: V_d in the rotating *d-q* frame, estimated grid voltage phase-angle, θ, the grid voltage and the cos (θ). The PLL output was well synchronized to the input voltage phase angle within 60 ms of the start operation (i.e., the grid voltage changes from *0* to full voltage).

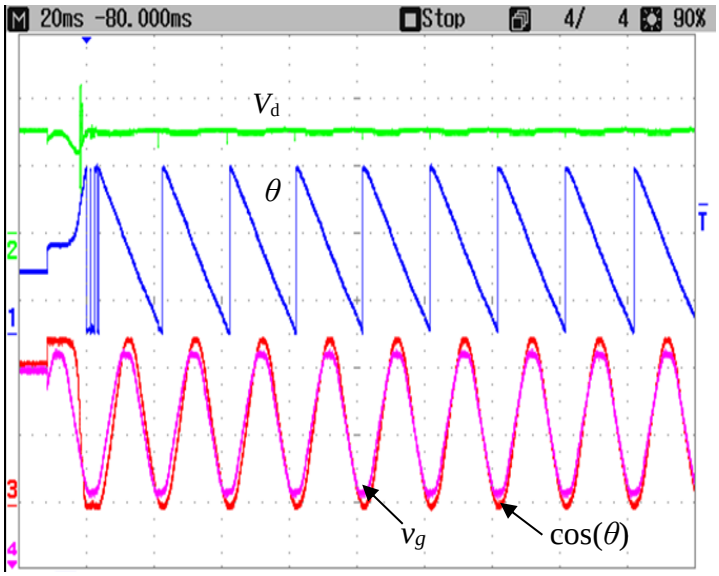


Fig.12 Estimated characteristics of the PLL under initial start-up condition, from top: V_d in the rotating *d-q* frame, estimated phase angle θ, (144 degrees /div), grid voltage v_g (55V/div) and cos (θ) (2V/div).

Fig. 13 shows the transient response of the implemented PLL with step increase of 40% in grid voltage. The results from top to bottom are: V_d in the rotating *d-q* frame, estimated grid voltage phase-angle, θ, grid voltage and the cosine value of the estimated grid voltage phase angle. It can be seen with the step change of 40% in grid voltage, the phase angle of the grid voltage was well tracked by the PLL. Only a small distortion appears in the curve of the estimated grid voltage phase angle.

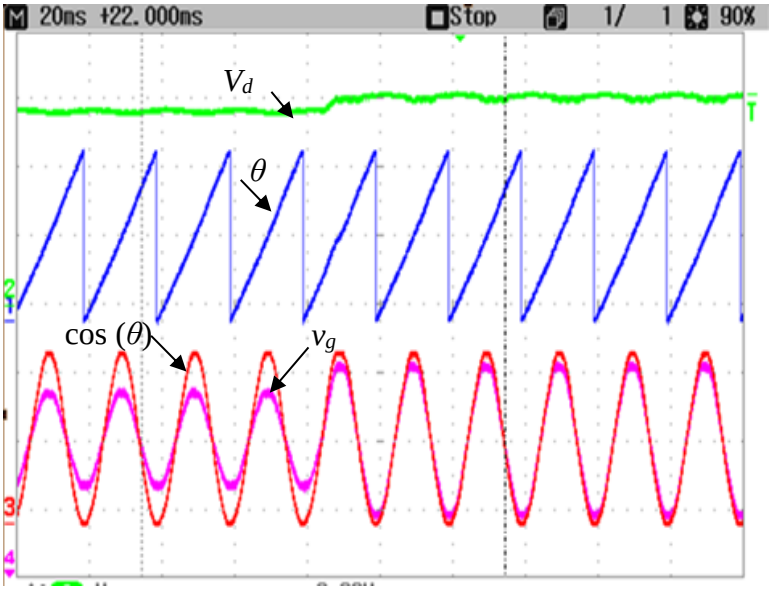
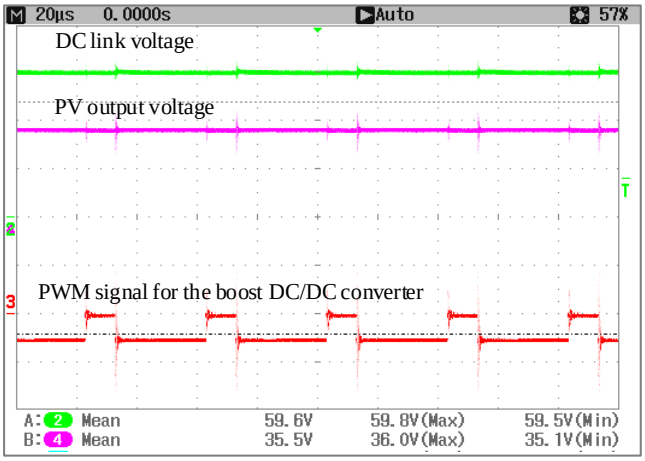


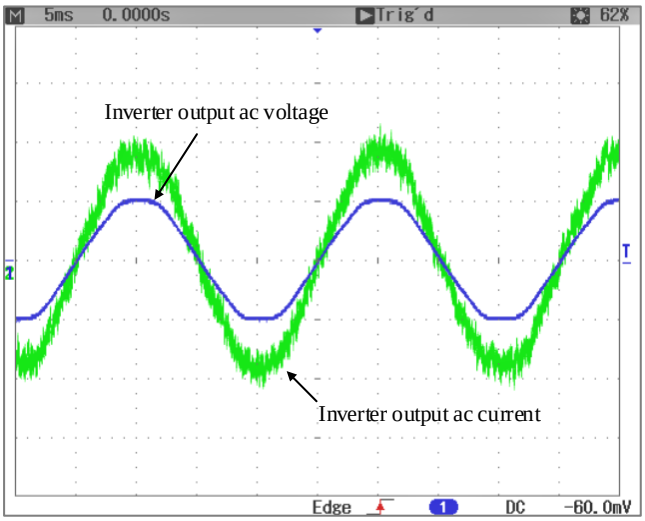
Fig 13. Test results for PLL with input voltage with 40% of input voltage increment, from top: V_d in the rotating *d-q* frame, estimated phase-angle θ (144°/div), grid voltage v_g (55V/div) and cos (θ) (2V/div).

It is worth mentioning that the transient tests were only carried out with step changes in the grid voltage. The response to frequency changes in the input voltage was not tested as it is difficult to change the frequency of the utility system in a laboratory environment.

Figure 14 (a) shows the output voltage of the emulated PV source and the DC link voltage V_{dc} as well as the PWM signal for the boost DC/DC converter. Perturb & Observer (P&O) based maximum power point tracking algorithm was developed to control the PV source operating voltage. Figure 14 (b) shows the PV inverter output voltage and current waveforms; the output current is controlled in phase with the grid voltage based on the PLL presented in this paper.



(a)



(b)

Figure 14 (a) operation voltage of the emulated PV source (20V/Div), (b) PV inverter output voltage v_{ac} (55V/Div) and current i_{ac} (1A/Div)

CONCLUSION

In this work, a rotating *d-q* frame based single-phase PLL was designed and implemented for a single-phase grid-tied PV inverter prototype. Detailed PLL structure, mathematical model, and practical implementation were described in the paper. Detailed orthogonal voltage signal was constructed based on transport-delay algorithm for single-phase systems this was implemented using a circular buffer (FIFO). The designed PLL was implemented in an ADMC401 based control system for a single-phase PV inverter. Experimental results show that the implemented PLL was well designed with a very good dynamic performance in both steady-state and transient conditions.

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