IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received May 31, 2018, accepted July 6, 2018, date of publication July 31, 2018, date of current version August 20, 2018.

Digital Object Identifier 10.1109/ACCESS.2018.2861323

Strain-Reduction Induced Rise in Channel Temperature at Ohmic Contacts of GaN HEMTs

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This work was supported by the Department of Electronics and Electrical Engineering, Liverpool John Moores University, Liverpool L3 3AF, U.K.

ABSTRACT Operating temperature distributions in AlGaN/GaN gateless and gated devices are characterized and analyzed using the InfraScope temperature mapping system. For the first time, a substantial rise of channel temperature at the inner ends of ohmic contacts has been observed. Synchrotron radiation-based high-resolution X-ray diffraction technique combined with drift–diffusion simulations show that strain reduction at the vicinity of ohmic contacts increases electric field at these locations, resulting in the rise of lattice temperature. The thermal coupling of a high conductive tensile region at the contacts to a low conductive channel region is an origin of the temperature rise observed in both short- and long-channel gateless devices.

INDEX TERMS AlGaN/GaN based devices, ohmic contact, self-heating, infrared camera, high-resolution X-ray diffraction.

I. INTRODUCTION

AlGaN/GaN based devices are promising candidates for high-power and high-frequency applications [1]–[3]. These devices can be manufactured onto the existing Silicon substrates, allowing co-integration with conventional Silicon technology. The wide bandgap, high electron velocity saturation, and good thermal conductivity of III-Nitrides (III-N) provide distinctive advantages over the conventionally used Silicon, leading to superior high-power and high-frequency device performance [1], [2]. However, the superior performance of AlGaN/GaN High Electron Mobility Transistors (HEMTs) is hammered by serious reliability issues, which are holding back their widespread commercial and industrial development. Deleterious phenomena such as: (i) self-heating effects, that significantly impact the transport properties in the semiconductor, (ii) charge trapping effects, that are responsible for reducing device lifetime and reliability, and (iii) source/drain Ohmic contact (S/D) resistances increase during device operation, are controversial with unclear physics [4]–[6]. These accelerating factors are behind device performance degradation and persist to be limiting reliability factors [4]–[6]. Maintaining high performance and reliability of the S/D Ohmic contacts in AlGaN/GaN HEMTs is a significant challenge, particularly at high operating voltage, which hinders progress in a large-scale deployment of the technology in applications [4]–[6].

In this work, we investigate the channel temperature distribution in AlGaN/GaN based devices using Infrascope temperature mapping system (IR) accompanied by synchrotron radiation-based High-Resolution X-RAY Diffraction (HRXRD) measurements and physically based TCAD simulations, for the first time. This unique approach demonstrates that compressive and tensile strain around S/D contacts affects temperature distribution during device operation and limiting its performance. Section II overviews devices under investigation and experimental procedure. Section III presents channel temperature profiles in the devices under different configurations and examines physics behind temperature rise at the S/D contacts of gateless devices. Conclusions are drawn in Section IV.

II. DEVICES AND EXPERIMENTAL PROCEDURE

The investigated epi-structure has been grown by molecular beam epitaxy on High-Purity HP-Si(111) substrate (Fig. 1). It consists, from the substrate to the top surface, of low-temperature AlN(40 nm)/GaN(250 nm)/AlN(250 nm) nucleation layers, a 1.7 μm $Al_{0.10}Ga_{0.90}N$ back-barrier to reduce leakage current in the buffer and to improve

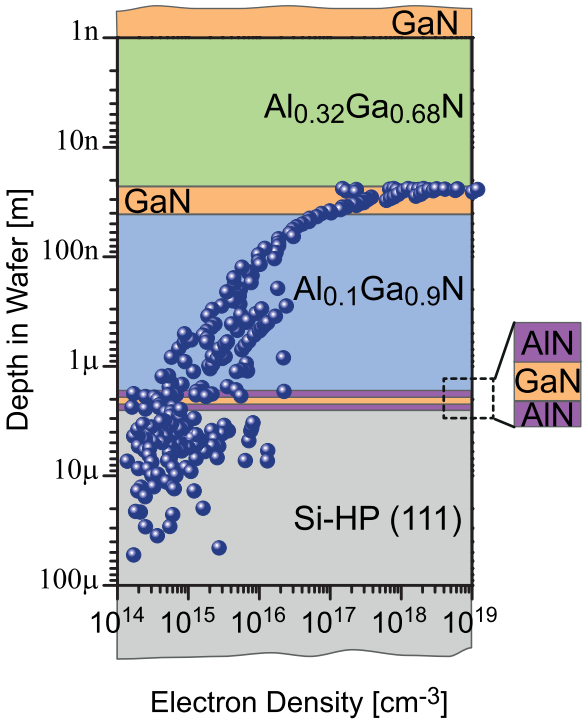

FIGURE 1. Epi-structure and measured electron density profile of the investigated wafer, GaN(1nm)/$Al_{0.32}Ga_{0.68}N$(25nm)/GaN(15nm)/ $Al_{0.10}Ga_{0.90}N$(1.7μm) /NL/HP-Si(111), where NL are nucleation layers that consist of AlN(40nm)/GaN(250nm)/AlN(250nm).

the carrier confinement of the 2-dimensional electron gas (2DEG). A channel is made of a 15 nm thick unintentionally doped GaN buffer followed by a 25 nm undoped $Al_{0.32}Ga_{0.68}N$ barrier and, finally, a 1 nm GaN cap layer. Room temperature Hall measurements yield a 2DEG electron mobility of 1750 $cm^2\ V^{-1}s^{-1}$ and $R_\square$ = 310 $\Omega/\square$. The CV-technique revealed an electron sheet density of $1.18 \times 10^{13}\ cm^{-2}$ in the buffer. The fabrication process flow is similar to that in [7]. To reduce the contact resistance, the S/D terminals are formed by rapid thermal annealing of an evaporated Ti(10nm)/Al(200nm)/Ni(40nm)/Au(100nm) multilayers metallization scheme at 870°C for 30 s under nitrogen atmosphere. The S/D contacts resistance and specific resistivity are 0.39 Ω.mm and $3.8\times\ 10^{-6}\ \Omega.cm^2$, respectively. The devices are electrically isolated by He^+ ion multiple implantations. To reduce trapping effects and dispersion, the surface of the devices are N_2O pre-treated for 2 min followed by SiO_2(100nm)/Si_3N_4(50nm) bi-layer passivation, performed by plasma-enhanced chemical vapor deposition at 340°C. The SiO_2(100nm)/Si_3N_4(50nm) bi-layer is opened by using a CHF_3/CF_4 reactive ion etching plasma. The used gate metallization scheme is Ni(5nm)/Pt(25nm)/Ti(25nm)/Mo(30nm)/Au(250nm).

The electrical I-V characterizations are performed at DC and dark conditions using Agilent B1500A framework. Before taking any measurements, V_{DS} = 0 V is applied for a period of time to fully recover the device from deleterious phenomena of charge trapping and self-heating that would distort further measurements. The trace of drain current is reproducible showing that no permanent degradation of drain current occurs from the experiment, only recoverable degradation, i.e., charge trapping and self-heating.

To measure the temperature profile, our Infrascope temperature mapping system, equipped with 500 × 500 InSb detectors array, is first calibrated. A high emissivity layer is coated over the device and surface radiation of the unbiased AlGaN/GaN device is measured, whilst increasing the temperature from 50°C to 200°C with a step of 15°C using a heated-stage to maintain constant uniform temperature [8], [9]. The surface temperature is then measured from the emissivity by comparing it with the instrument calibration curve (not shown). After the calibration step, each device is first placed on a constant temperature platform (40°C or 45°C) and biased at DC conditions using Agilent B1500A framework. Then, thermal imaging measurements are performed using the calibrated Infrascope system. Pixel resolution of the obtained IR image is about 2.3 μm, giving a total field of view of about 1 mm × 1 mm. This technique is based on measuring the IR radiations emitted at the top surface of the device that are proportional to the temperature.

The strain relaxation in the AlGaN barrier layer of an unbiased device is measured using synchrotron radiation-based High-Resolution X-RAY Diffraction (HRXRD) [21]. This techniques uses 10.4 keV energy at the 2−ID−D microdiffraction beamline of the Advanced Photon Source (APS) at Argonne National Laboratory. The sample device is mounted on an XYZ stage with a 50 nm lateral resolution. The location of the beam spot was monitored by means of simultaneous measurement of Ga−K fluorescence intensities and the diffraction data were collected by a charge-coupled detector. The size of the quasi-circular beam spot is ≈220 nm with 180 arc sec divergence.

The electrostatic of the used devices has been investigated by Drift-Diffusion (DD) simulations. The details of the used device simulation technique can be found in [10] and [24]–[28]. In the past, this simulation technique has been successfully used to predict AlGaN/GaN based device architectures grown on various substrates (i.e., Si, 4H−SiC, diamond, sapphire). The transport parameters such as electron drift velocity, energy relaxation time, and electron effective mass are obtained from Monte Carlo simulation runs at different lattice temperatures [28]. Both simulated I−V characteristics and calculated temperatures have been compared to experimental I−V characteristics and temperature measurements, demonstrating a good agreement [10], [24], [25], [27]. Moreover, this simulation technique has been adapted to deal with both gated and gateless AlGaN/GaN devices.

III. RESULTS AND DISCUSSION

A. AlGaN/GaN GATELESS DEVICES

The I_D-V_D characteristics of the used 100 μm wide gateless AlGaN/GaN Transmission Line Measurement structures (TLMs) with different source-to-drain distances,

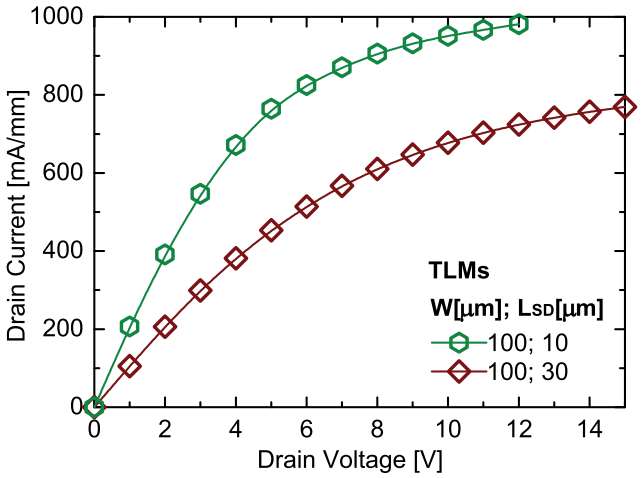

FIGURE 2. Measured I_D-V_D characteristics of the gateless AlGaN/GaN Transmission line measurement structures (TLMs). The source-to-drain distance of the used TLMs are $L_{SD} = 10\ \mu$m (short TLM) and $L_{SD} = 30\ \mu$m (long TLM).

$L_{SD} = 10\ \mu$m (short TLM) and $L_{SD} = 30\ \mu$m (long TLM), are shown in Fig. 2. A lower current and a larger resistance are observed for the long TLM ($L_{SD} = 30\ \mu$m).

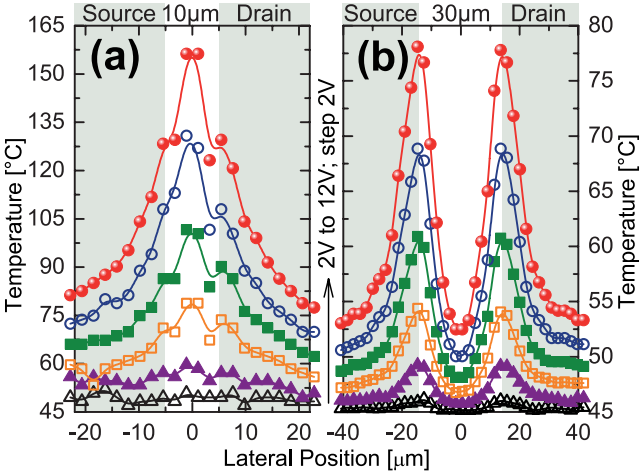

FIGURE 3. Measured temperature profiles along the top surface of the gateless AlGaN/GaN structures at different drain voltages for (a) short TLM ($L_{SD} = 10\ \mu$m) and (b) long TLM ($L_{SD} = 30\ \mu$m).

Fig. 3 shows the temperature distributions along the surface of the short and long TLMs, $L_{SD} = 10\ \mu$m and $L_{SD} = 30\ \mu$m, at $V_{DS} = 2$ V to 12 V by step of 2 V. For the long TLM, temperature peaks are observed at the inner ends of the S/D contacts, for all applied biases (Fig. 3b). These temperature peaks merge when L_{SD} decreases as a result of temperature coupling (Fig. 3a). For $L_{SD} \leqslant 10\ \mu$m, the amount of thermal coupling between the source and the drain sides is even larger making it difficult to observe the temperature peaks at the inner end of the Ohmic contacts (not shown). Note that this thermal coupling induced temperature rise can significantly impact the device performance through increase in the contact access resistance and electron mobility degradation, particularly for small devices, as a result of the source-drain thermal coupling.

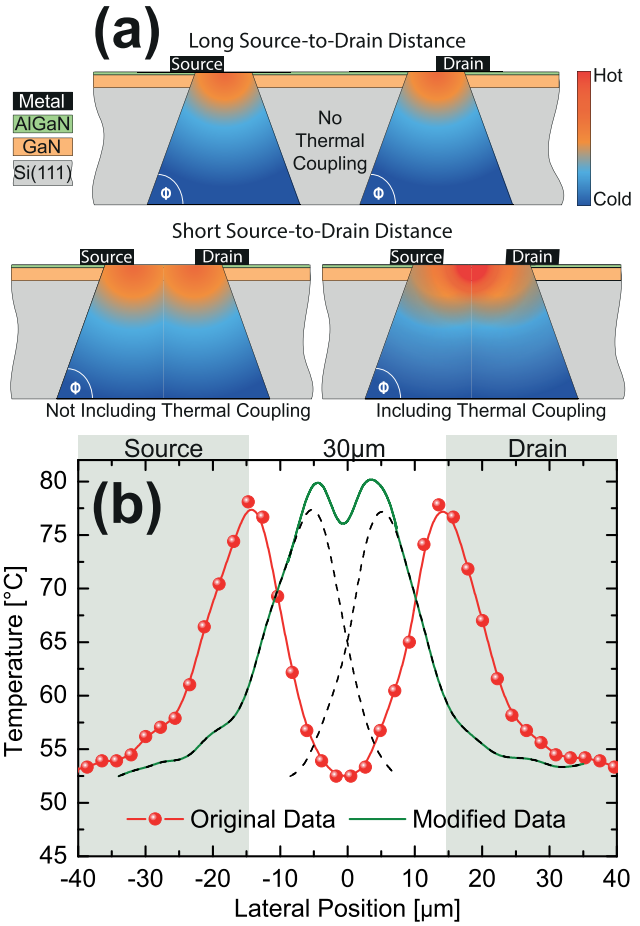

FIGURE 4. (a) Illustration of the heat spreading angle and the source/drain thermal coupling in the short and long TLMs. (b) Measured temperature profile along the top surface of the long AlGaN/GaN TLM ($L_{SD} = 30\ \mu$m) at $V_{DS} = 12$ V. The original measured data are compared to the modified data to show a very negligible thermal coupling between the inner ends of Ohmic contacts in a long L_{SD} device.

Unlike in the long TLM, the channel temperature is at its maximum in the center of the short TLM ($L_{SD} = 10\ \mu$m). This can be explained by a heat spread angle and a strong thermal coupling between source and drain, as illustrated in Fig. 4a. The temperature in the middle of the short TLM is much higher than at the inner ends of Ohmic contacts. To demonstrate the low thermal coupling in the long TLM ($L_{SD} = 30\ \mu$m), we have artificially modified the measured temperature profile by reducing the source-to-drain distance from 30 μm to 10 μm (Fig. 4b). It can be seen that the resultant temperature profile (modified data) is slightly larger than the original data but still present two peaks, in contrary to the measured temperature of the short TLM ($L_{SD} = 10\ \mu$m).

The channel temperatures of the AlGaN/GaN TLMs are plotted against the dissipated power density in Fig. 5. The dissipated power density is controlled via V_{DS}. For a given dissipated power density, the temperature is higher in the

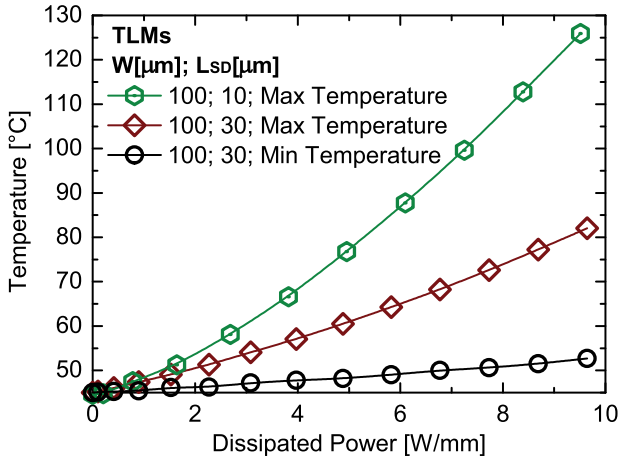

FIGURE 5. Evolution of the channel temperature versus the dissipated power density of the AlGaN/GaN TLMs ($L_{SD} = 10\ \mu$m and $L_{SD} = 30\ \mu$m). The Max Temperatures are extracted at the vicinity of S/D contacts for the long TLM and in the center of the device for the short TLM. The Min Temperature corresponds to the value of temperature at center of the long TLM ($L_{SD} = 30\ \mu$m).

short TLM ($L_{SD} = 10\ \mu$m) due to (i) a higher electric field [10] and (ii) a stronger thermal coupling between source and drain sides (Fig. 4a).

To get a rough estimate of the thermal resistance of each TLM, we have employed an analytical thermal model described by the following equation [11], [12]: $T = T_{SUB} + R_{TH} \times P_{DISS}$; where T is the channel temperature, T_{SUB} is the substrate temperature (45°C), R_{TH} is the thermal resistance, and P_{DISS} is the dissipated power, which is proportional to electric field (E), current (I_{DS}) and source-to-drain distance (L_{SD}): $P_{DISS} \approx E \times I_{DS} \times L_{SD}$. According to this model, the increase of L_{SD} should lead to an increase in channel temperature, due to a larger amount of material for heat to dissipate through. This is in disagreement with experimental observations. Therefore, the temperature increase with the reduction of L_{SD} is mainly caused by the thermal resistance. With respect to the heat spreading angle model [13]–[15], as illustrated in Fig. 4a, the thermal resistance increases with decreased L_{SD} due to the less substrate volume for heat to dissipate. The extracted thermal resistance are 68°C W^{-1} and 38°C W^{-1} for short ($L_{SD} = 10\ \mu$m) and long ($L_{SD} = 30\ \mu$m) TLMs, respectively. These values of R_{TH} are within the typical range of values [16], [17]. Here, we have used the maximum temperatures that occur (i) at the inner-ends of the source and drain terminals for the long TLM ($L_{SD} = 30\ \mu$m) and (ii) in the center of the device for the short TLM ($L_{SD} = 10\ \mu$m), due to thermal coupling. When using temperature values in the middle of the TLM with $L_{SD} = 30\ \mu$m (Min Temperature), the extracted R_{TH} is equal to 9.0°C W^{-1}, over three times smaller than at the inner-ends of the source and drain terminals. This is an indication of a non-uniform distribution of the electric field between source and drain contacts.

It has been reported that the S/D Ohmic contacts process annealing and device operation induce mechanical stress due to (i) a mismatch in thermal expansion coefficients of III-N and Ti/Al/Ni/Au metallization scheme, and (ii) an exacerbation of inverse piezoelectric effect at high temperatures [18]–[20]. These effects result in a change of strain at the vicinity of metal contacts. The deformation of *c*-plane nitride crystal under compressive and tensile strains [22] around the contacts is illustrated in Fig. 6b.

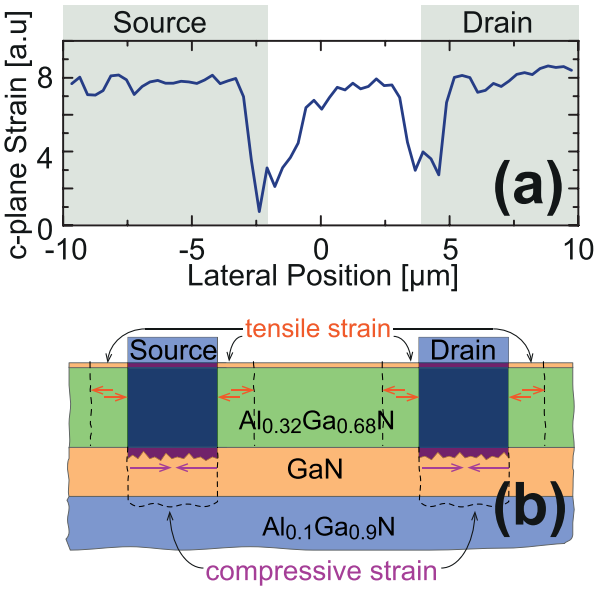

FIGURE 6. (a) Measured strain in the channel along the lateral direction of an AlGaN/GaN TLM using synchrotron radiation-based High-Resolution X-RAY Diffraction (HRXRD), showing a reduction of strain at the inner ends of S/D contacts. (b) The schematic of strain distribution at the vicinity of S/D Ohmic contacts.

The above theory is supported by the strain profile, measured by HRXRD and given in Fig. 6a, that reveals a reduction of strain at the inner ends of S/D contacts. The strain reduction at the inner ends of the contacts diminishes the electron density at these locations which, in turn, increases the electric field locally [23], hence an increase in channel temperature.

The impact of the strain reduction, at the inner ends of S/D Ohmic contacts, on the device electrostatic has been investigated by DD simulations and HRXRD measured data. The lateral 2DEG profile overlapped with corresponding potential distribution at $V_{DS} = 0$ V, when taking into account the measured strain, are shown in Fig. 7a. At least 25 % reduction in 2DEG density is observed at the inner ends of S/D contacts, as result of strain degradation. Figs. 8a and 8b compare the simulated electric field distributions with measured temperature profiles under $V_{DS} = 12$ V for both short ($L_{SD} = 10\ \mu$m) and long ($L_{SD} = 30\ \mu$m) TLMs, respectively. Electric field peaks, that occur at the inner ends of the S/D contacts, are nearly three times larger than that at the middle of the device and directly correlate with the measured temperature profiles. As the electric field and the drain current increase proportionally with V_{DS}, the channel temperature increases near the Ohmic contacts. With the proportional relationship between electric field and temperature,

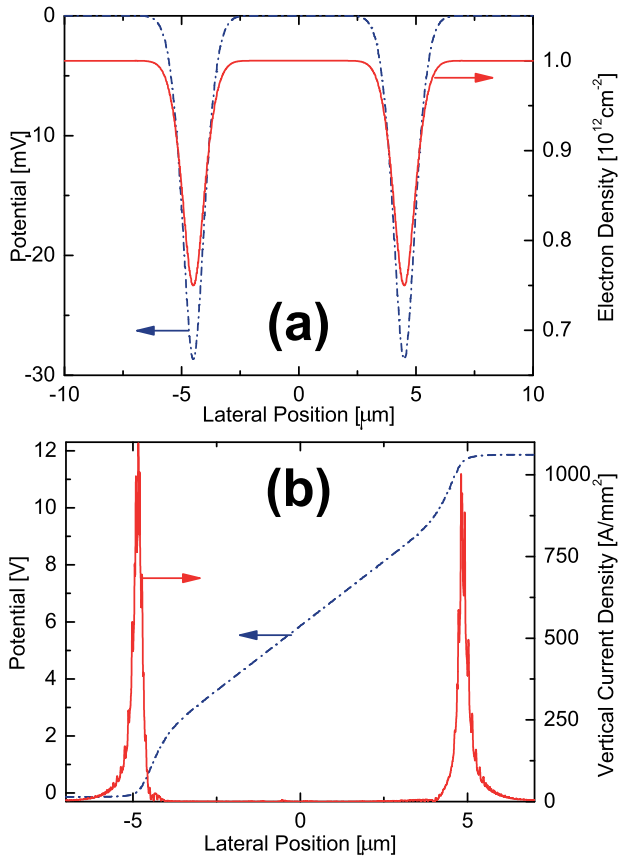

FIGURE 7. Drift-Diffusion (DD) simulation results of the short TLM ($L_{SD} = 10\ \mu m$), when taking into account the HRXRD measured strain. (a) Lateral 2DEG profile overlapped with potential distribution at $V_{DS} = 0$ V in the channel of the TLM. (b) Vertical current density overlapped with potential distribution at $V_{DS} = 12$ V in the channel of the TLM.

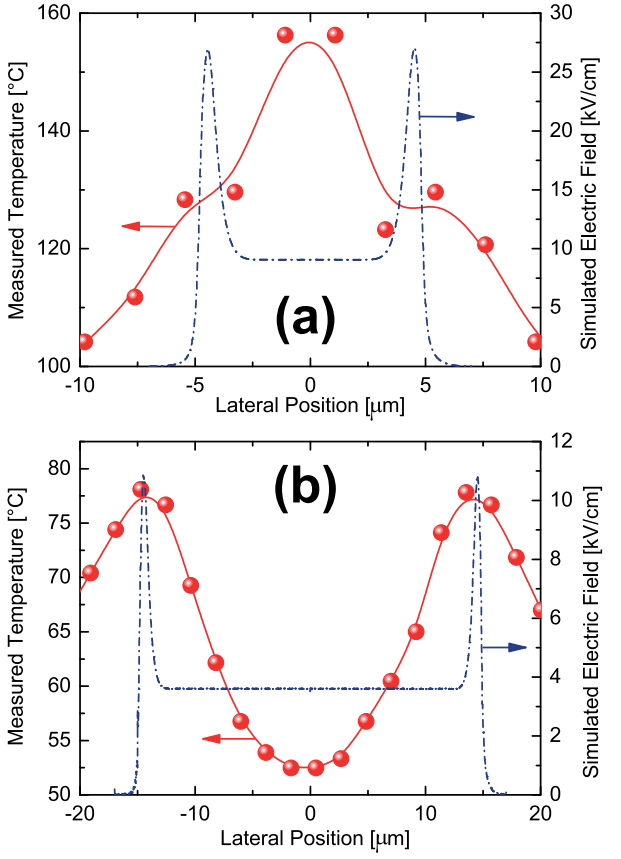

FIGURE 8. Simulated electric field distributions and measured temperature profiles at $V_{DS} = 12$ V of (a) short TLM ($L_{SD} = 10\ \mu m$) and (b) long TLM ($L_{SD} = 30\ \mu m$).

the degradation of strain significantly impacts temperature peaks within the device. Furthermore, the simulated vertical current density, given in Fig. 7b, shows that the majority of current flows in/out of the 2DEG through a small portion of the S/D contacts as suggested by Trilayer-TLM model Ohmic contacts [29]. This attribute could be a cause of a further strain degradation and channel temperature increase.

B. AlGaN/GaN GATED DEVICES

It was not possible to observe the temperature peaks at the vicinity of the Ohmic contacts in AlGaN/GaN HEMTs due (i) to the strong thermal coupling between contacts when $L_{SD} \leqslant 10\ \mu m$, as demonstrated in the previous section; and (ii) to the hot-spot at the end of the gate, as described in this section. However, a temperature rise near source and drain contacts still take place in HEMTs, since the fabrication process of Ohmic contacts in gated and gateless devices are exactly the same. We shall therefore expect to observe temperature rise near the source/drain contacts in HEMTs as in TLMs.

The I_D-V_G characteristics of two AlGaN/GaN HEMTs with different configurations (single or two-finger gate) are presented in Fig. 9. The two-finger gate device 'B' outputs less current than single-finger gate HEMT 'A', a point to be noted in discussion. The same temperature measurement technique is applied to a two-finger gate HEMT with $L_{GD} = 2.5\ \mu m$ and $W = 2 \times 150\ \mu m$ (Fig. 10a). Since L_{SD} of

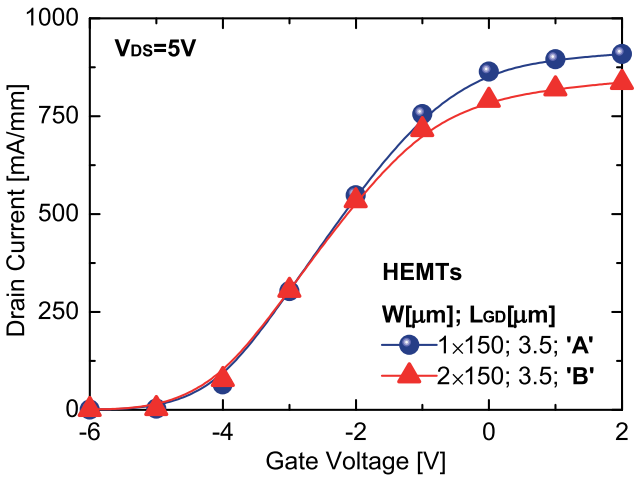

FIGURE 9. Measured I_D-V_G characteristics of single and two-finger gate AlGaN/GaN HEMTs at $V_{DS} = 5$ V. The device dimensions are: $L_{SG} = 1.0\ \mu m$, $L_G = 0.5\ \mu m$, $L_{GD} = 3.5\ \mu m$.

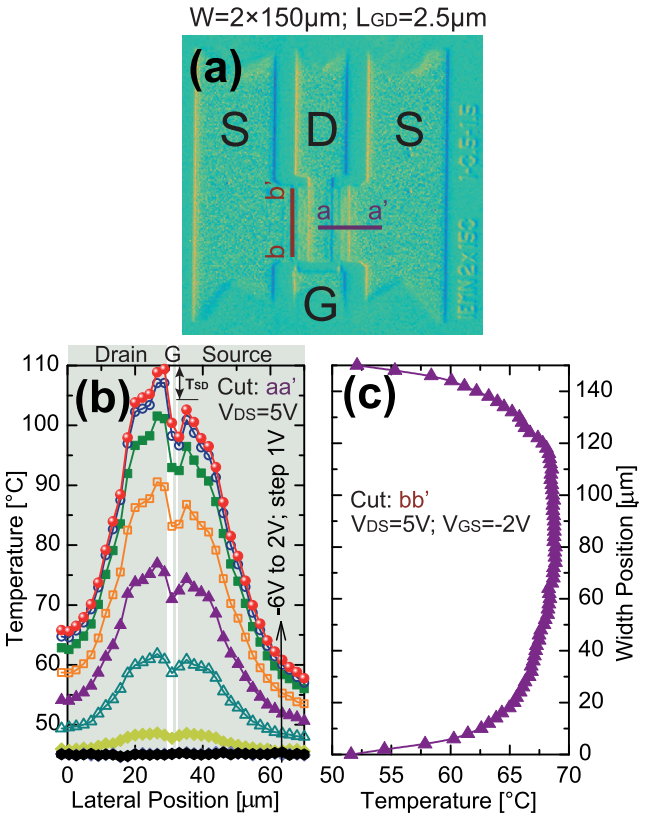

FIGURE 10. (a) Layout of two-finger gate AlGaN/GaN HEMTs. (b) Measured temperature profiles at V_{DS} = 5 V and at different gate voltages (−6 V to 2 V; step 1 V) along the lateral position (Cut: *aa*′). (c) Temperature distribution at V_{DS} = 5 V and V_{GS} = −2 V along the width position (Cut: *bb*′). The device dimensions are: L_{SG} = 1.0 μm, L_G = 0.5 μm, L_{GD} = 2.5 μm. Same phenomena have been observed for HEMT with L_{GD} = 3.5 μm.

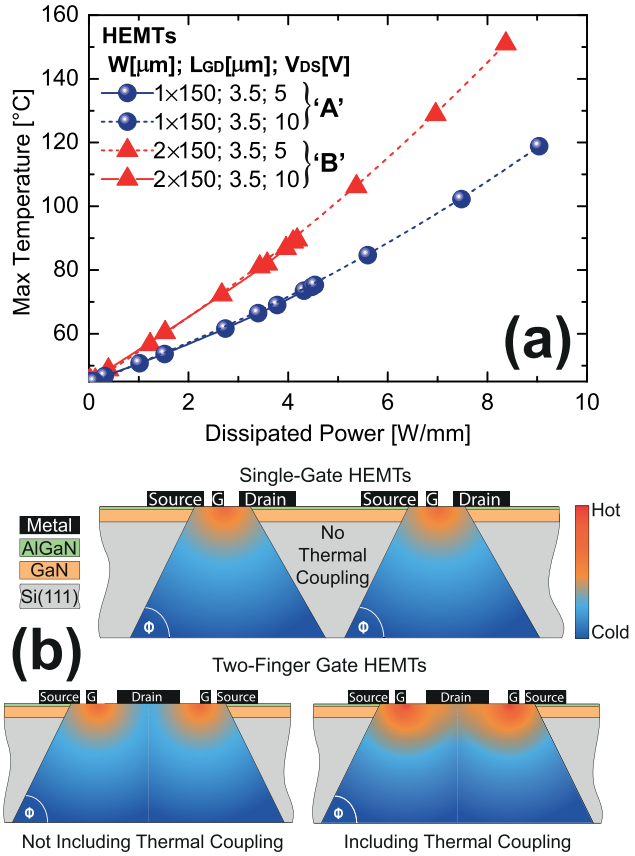

FIGURE 11. (a) Evolution of the maximum channel temperature versus the dissipated power density of single and two-finger gate AlGaN/GaN HEMTs ('A': W = 1 × 150 μm; and 'B': W = 2 × 150 μm. The device dimensions are: L_{SG} = 1.0 μm, L_G = 0.5 μm, L_{GD} = 3.5 μm. (b) Illustration of the heat spreading angle in single and two-finger gate AlGaN/GaN HEMTs.

this device is less than 10 μm, the peaks of temperature at the inner ends of S/D contacts are merged together. This profile is similar to what has already been reported in literature using techniques such as μRaman [30]. The notch between the source and drain sides is caused by the metal gate. In addition, a higher temperature peak can also be seen at the end of the gate (toward the drain side, as marked by T_{SD} in Fig. 10b). This peak may be slightly undervalued, due to the limited resolution of the IR System. The drain-side temperature increase as V_{GS} increases can be explained by the temperature coupling with that of the neighboring HEMT and by the high electron kinetic energy at the end of the gate [31].

The maximum device temperatures of the AlGaN/GaN HEMTs are plotted against dissipated power density in Fig. 11a. The dissipated power density is controlled via V_{GS} and V_{DS}. The presence of temperature coupling between two neighboring HEMTs (two-finger gate HEMT 'B': W = 2 × 150 μm), due to heat spreading angle as illustrated in Fig. 11b, leads to channel temperature increase, when compared with a single-gate HEMT ('A': W = 1 × 150 μm) [32]. As results, the two-finger gate exhibits lower drain current as shown in Fig. 9 [24], opposite to the expected higher current without considering thermal coupling. This experimental observation is in good agreement with heat spreading angle models [13]–[15]. The main cause of temperature rise in AlGaN/GaN HEMT is, therefore, the high value of the electric field at the end of the gate toward the drain side. The electrons that enter the device via the source terminal and crystal lattice of AlGaN and GaN gain significant energy at the drain-side gate edge, due to the large electric field peak in the local area. Consequently, a non-uniform distribution of dissipated power produces a hot spot of temperature to be formed at this location [33]–[35]. This phenomenon happens regardless of the strain reduction near the contact [36], [37]. Therefore, the physics behind temperature rise near the gate and near source/drain contacts are very different. Both mechanisms contribute to the higher temperature at the drain side in AlGaN/GaN HEMTs. Further investigation will be needed to separate the thermal effects of the two mechanisms in this device.

IV. CONCLUSION

Infrascope temperature mapping system measurements have shown a large increase in temperature at the S/D contacts

of AlGaN/GaN-based devices at operating conditions. Temperature coupling of a high conductivity tensile region to the lower conductivity regions is responsible for the temperature rise observed in both short and long gateless devices. The thermal coupling also enhances the peak of temperature at the end of the gate in the AlGaN/GaN HEMTs. In addition, the HRXRD measurement supported by DD simulations have revealed that the change of the strain at the vicinity of S/D Ohmic contacts, due to a difference in expansion coefficients of III-N and S/D metallization, is the reason behind this temperature rise.

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