Silicon integrated circuits for secondary side control of isolated DC-DC converters.

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Silicon Integrated Circuits for Secondary Side Control of Isolated DC–DC Converters

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M.Phil.

2012

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DECLARATION

The following thesis is submitted in part fulfilment of the requirement for the degree of MPhil of the University of Swansea.

This work has not been submitted previously as an exercise for a degree at this or any other University. It is entirely the applicants own work, except where general knowledge and theories are presented or references made to the work of others.

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January 2012

Richard Davies

I wish to thank Dr Salah Khanniche and Dr Timothy Davies, for their support and guidance in completion of this work and Dr J D Williams for his encouragement in the decision to embark on the project.

Summary

This thesis investigates the requirements of a secondary side control strategy for isolated DC-DC switch mode power converters as found in board mounted power systems such as "quarter", "eighth" and "sixteenth" "brick" products used in fixed telecom systems where commercial pressures on cost, size and power efficiency are intense.

Objective specifications for silicon design of the primary and secondary side control circuits are developed. Functional description level circuits are designed for initial simulation testing of system operation and compared to conventional system architectures. Device level circuit designs based on current process technology are created to illustrate the integrated circuit design required to meet the objective specifications.

Simulation results for these circuits showing system level operation including start up sequence, feed forward operation, load step response and over current protection is presented. The operation and parametric performance of specific circuit blocks is also illustrated including the pre regulator function and reference voltage trimming.

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List of Symbols

BVdss	Mosfet breakdown voltage drain to source
C	Electrical capacitance
D	Duty cycle
L	Electrical inductance
V	Voltage
Vin	Line input voltage
Vcc	Positive supply voltage
Vout	Converter output voltage
Z	Electrical impedance

Abbreviations

ASIC	Application Specific Integrated Circuit
BBM	Break before make time
BCD	Bipolar Cmos Dmos
BUCK	Step Down Switching Converter
BST	Boost Voltage
DMAX	Maximum Allowed Duty Cycle
DPA	Distributed power architecture
DRC	Design Rule Check
EA_OUT	Error amplifier output
EA_P	Error amplifier non inverting input
EA_N	Error amplifier inverting input.
FF	Feed Forward
FPGA	Field Programmable Gate Array
GMR	Giant Magnetoresistive
HICCUP	Repeated Turn ON – Turn Off
HV	High Voltage
IBA	Intermediate Bus Architecture
LVS	Layout Versus Schematic

ms	Milli Seconds
MOC	Moderate Over Current
Mosfet	Metal Oxide Silicon Field Effect Transistor *
OCP	Over current protection
OEM	Original Equipment Manufacturer
OVP	Over Voltage protection
OTP	Over Temperature Protection
POL	Point of Load
PWM	Pulse Width Modulator
SIPO	Serial In Parallel Out
SOA	Safe operating area
SOC	Significant Over Current
SOI	Silicone on Insulator.
SS	Soft Start
us	Micro Seconds
UVLO	Under Voltage Lock Out
VCCS	Voltage Controlled Current Source
VCSW	Voltage Controlled Switch

* The use of the term "Metal" is historic, the gate of field effect transistors now being fabricated from PolySilicon.

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1 Introduction

1.1 Background

The expansion of wired and wireless telecommunications infrastructure has been driven by deregulation and technology advances requiring the provision of lower cost, smaller size and higher performance equipment. These telecom and datacom systems typically contain high performance processors, ASIC and FPGAs devices.

Power supplies for this equipment are required to supply ever-lower voltages at higher and faster dynamic currents, at ever-higher efficiencies and lower cost to a load that is predominantly digital circuitry. An analysis of the trends in this area is given in [1].

The general scheme for the supply of power to this equipment comprises an ac-dc front end that down converts utility power to a dc supply for telecoms systems with a voltage range of 36V to 75V.

This voltage range still necessitates galvanic isolation for compliance with safety standards such as IEC/EN/UL60950 [2]. The general configuration is illustrated in fig1.1, shown overleaf consisting of filtering and full wave rectification of the AC mains resulting, for telecoms applications a DC supply range of 36 to 75V. The following DC-DC converter containing transformer isolation.

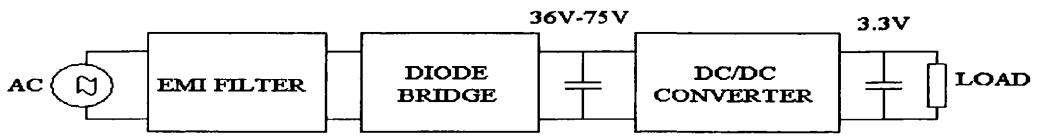


Fig 1.1 AC to Low Voltage DC Block Diagram

These power supplies are therefore categorised as "Isolated dc/dc converters" and may be board mounted "in house" designs by telecoms equipment manufacturers or frequently be power modules available from many leading manufacturers conforming to fixed standards and often referred to as 1/2 , 1/4, $1/8^{th}$ or $1/16^{th}$ "bricks". The power range for such modules is generally up to 350W for a ½ brick to less than 50W for the $1/16^{th}$ brick, examples of which can be found at [3].

An example of an $1/8^{th}$ brick power module is shown in fig1.2 which serves to illustrate the power density achieved by such modules which requires multi layer printed circuit board and planar magnetic technology along with minimum component count.

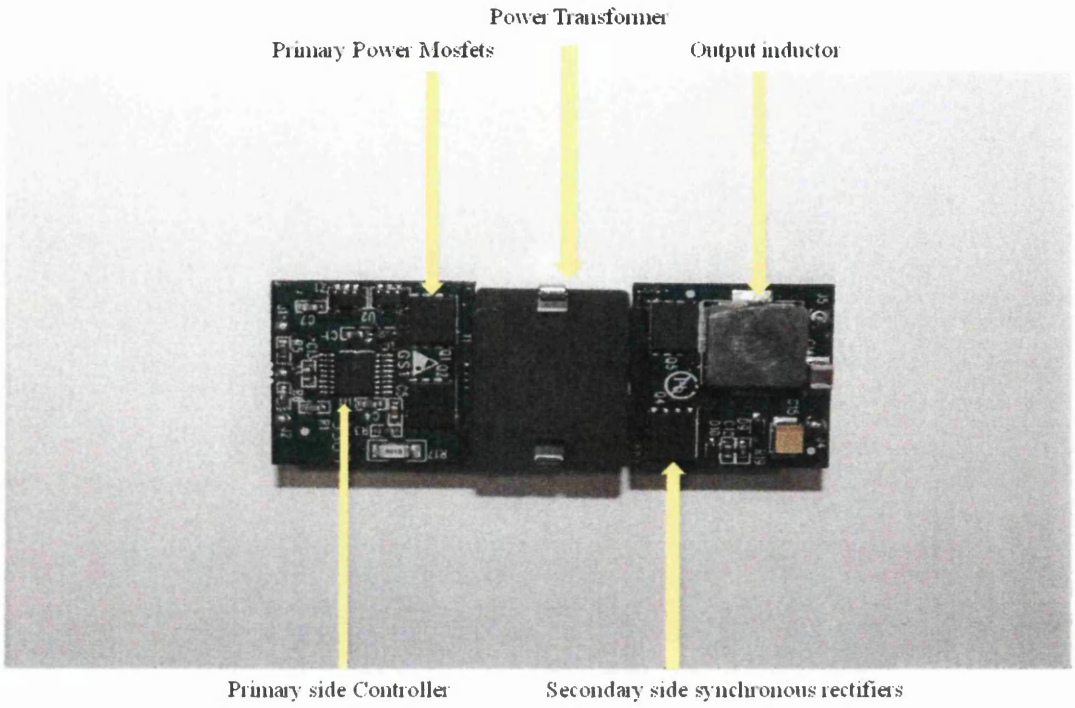


Fig 1.2 Eighth Brick DC-DC Converter

The industry standard dimensions for this power module are 58.4 x 22.7 x 10.1mm or (2.3 x 0.894 x 0.32 in), with the height dimension of 10.1mm or 0.32 in representing a "low profile" product.

The task of designing such products is even more challenging when one considers the sixteenth brick product with dimensions of 33.02 x 22.86 x 7.5 mm or ((1.3 x 0.9 x 0.295 inch) and achieving a power output of 100w representing 312W/in^3 [4].

A relatively recent product announcement in this area is the P13101 from PICOR [31] delivering 60W at a power density of 400W/in^3 with dimensions of 0.87 x 0.65 x 0.265 inch.

1.2 Isolated Power Distribution Architectures

The converter modules referred to above are used in a number of configurations to meet the power demands of telecom equipment [5] [6].
The first generation used the distributed power architecture illustrated below in fig 1.3

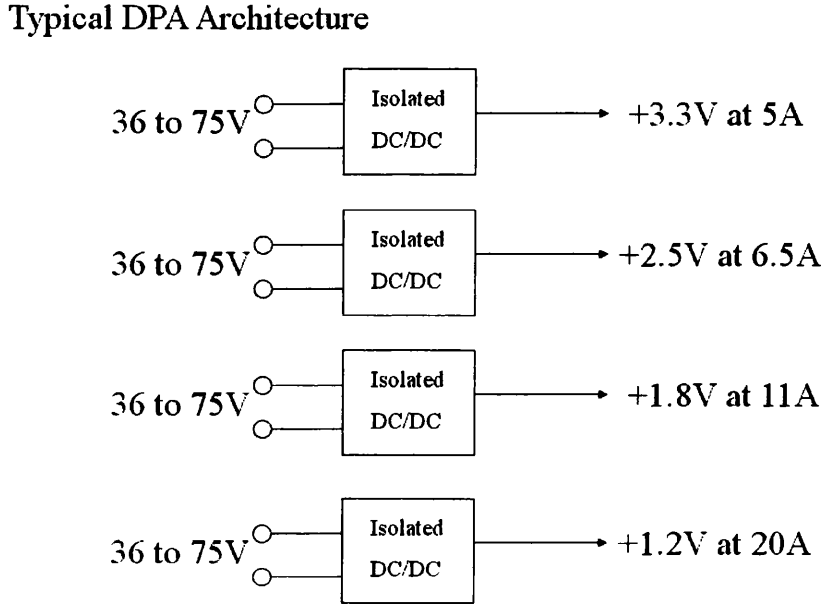


Fig 1.3 DPA Architecture

The DPA architecture works provided the number of supplies required by end equipment is limited but clearly the number of power modules is directly proportional to the supplies required with resulting cost and space requirement.

The alternative to this direct approach is to use an intermediate bus architecture (IBA) which uses a single isolated converter to generate an intermediate voltage followed by point of load (POL) non isolated buck converters to generate the required low voltage supplies. The various options to this approach is illustrated in fig 1.4.

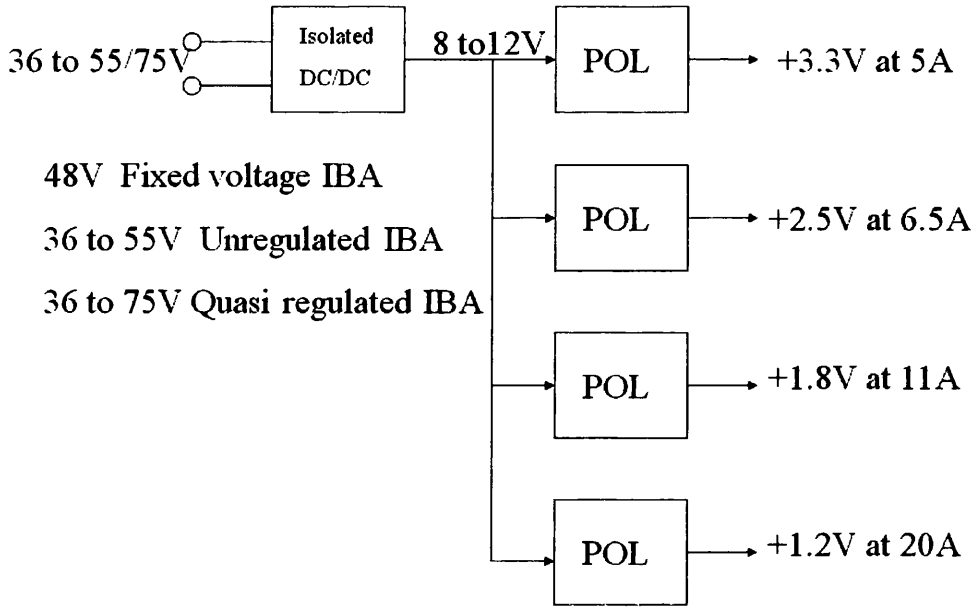


Fig 1.4 IBA Architecture

The fixed voltage IBA provides a fully regulated intermediate voltage of 9 or 12V, and compatible with the input voltage range of POL converters.

Alternatives to this approach include unregulated and quasi - regulated IBC's. The unregulated version operates at a fixed duty cycle and has advantages in regard to power efficiency but has a more limited input range due to the requirement to keep the POL converter inputs to less than 12V [5] [6]. A quasi regulated approach allows for the wider input range and will use feed forward [10] techniques to maintain the IBC output below 12V.

1.3 Isolated DC/DC Converter Topologies.

Isolated converter topologies include :-

1. Flyback
2. Forward
3. Push Pull
4. Two Switch Forward
5. Half Bridge
6. Full Bridge

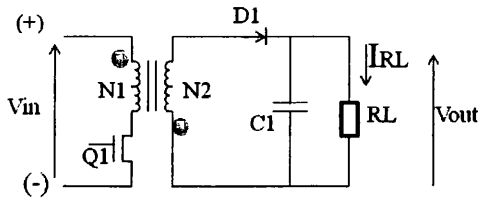
These topologies are illustrated below in figs 5 - 10 and extensively in [7] and a comparison of the relative advantages and disadvantages listed in [8]. The particular examples shown here do not represent the only options to each topology, use of the "current doubler" circuit on the secondary side of a half bridge circuit and complex magnetic design for synchronous rectifier drive is shown in [27]. A recent addition is the "Fly Forward" topology which as the name suggest combines the operation of a forward converter with that of a flyback converter via the design of the secondary side winding and rectifiers. This architecture was Patented in 2009 [49].

Significantly from the point of view of the controller required the flyback and forward converter topologies operate with one primary side switch, the Push Pull, Two Switch Forward and Half Bridge topologies operate with two primary side switches and the Full Bridge with four primary side switches.

From the viewpoint of the power Mosfets specification the half bridge and full bridge topologies subject the devices in the off state to the Line voltage and not to twice that as for some other topologies [9]. This reduced breakdown voltage requirement allows for improved Rds(on) performance. Further considerations on Mosfet selection in regard to breakdown voltage requirements and failure modes are outlined in [28].

Isolated Converter Topologies - Simple schematics

Flyback



Forward

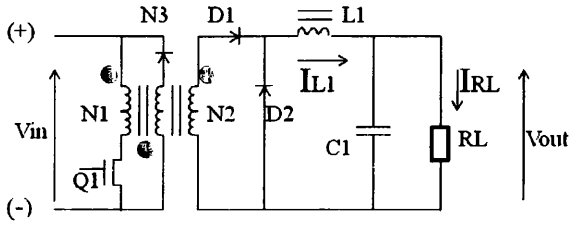
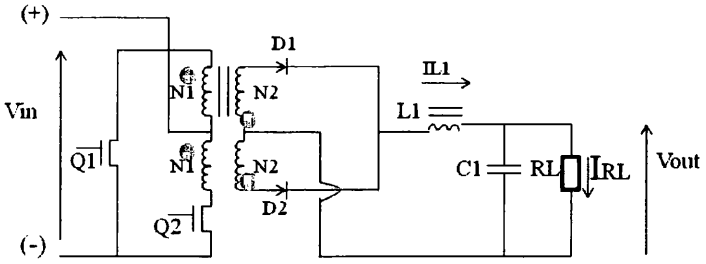


Fig 1.5 Fly back Topology

Fig 1.6 Forward Topology

Push - Pull



Two -Switch Forward

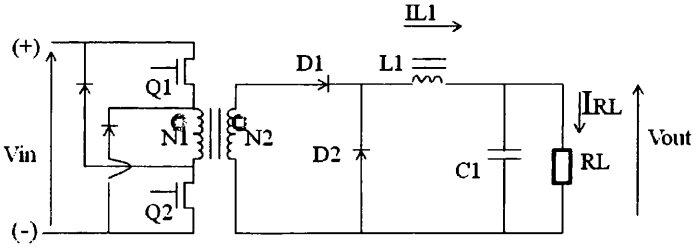


Fig 1.7 Push Pull Topology

Fig 1.8 Two Switch Forward Topology.

Half Bridge Converter - Simple schematic

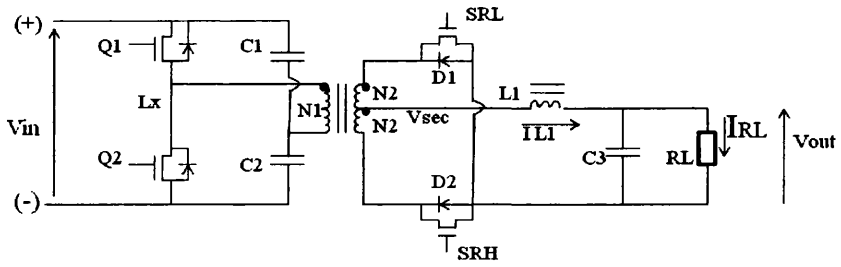


Fig 1.9 Half Bridge Topology

Full Bridge

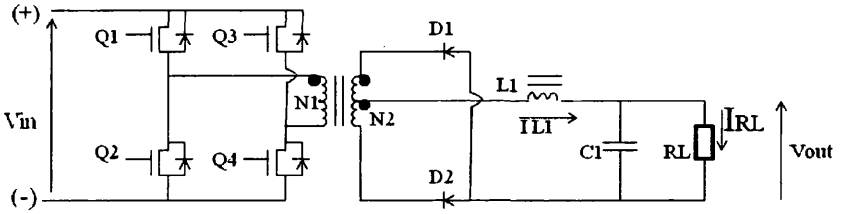


Fig 1.10 Full Bridge Topology

1.4 Control Methodologies

Voltage mode Control

The simplest example of this control method is illustrated below fig 1.11 and regulates the duty cycle (D) to achieve the required output voltage against load and line variation. The inclusion of a method of line voltage feed forward [10] offers significant advantages for the latter requirement. The principle of this feature and the various ways of implementation is illustrated in fig 1.12.

Fundamentally the feed forward technique involves the change in line voltage directly modulating the operating duty cycle D to offset the effect on output voltage without waiting for the voltage control loop to react.

The inclusion of output current into the feed forward path in the illustration can be considered as another example of this intrinsic property in current mode control to be discussed in the next section.

The steady state accuracy of the output voltage is dependent on that of the reference voltage across temperature and aging, and the dynamic range and performance of the PWM conversion [11].

Transient performance to a load step will be dependent on the control loop bandwidth in particular that of the opto isolator. A description of the requirements for stability is given in [11] and an extensive analysis of stability requirements and loop compensation of dc-dc converters is found in [12] with relevant extract included in Appendix D.

Voltage mode control

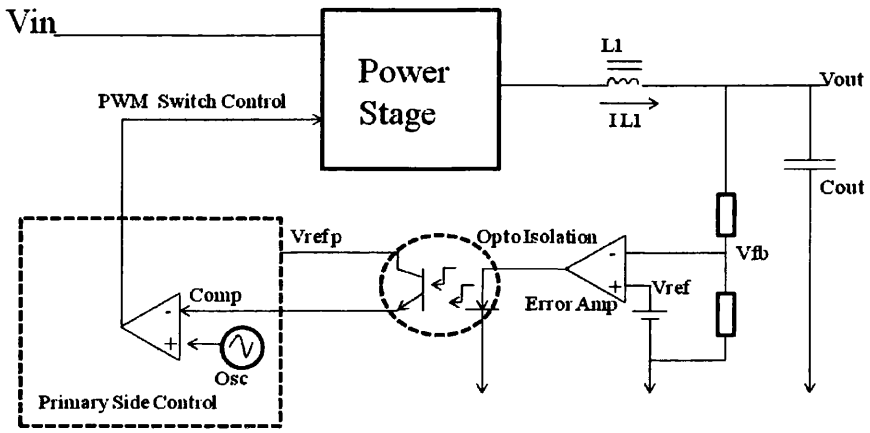


Fig 1.11 Voltage Mode Control

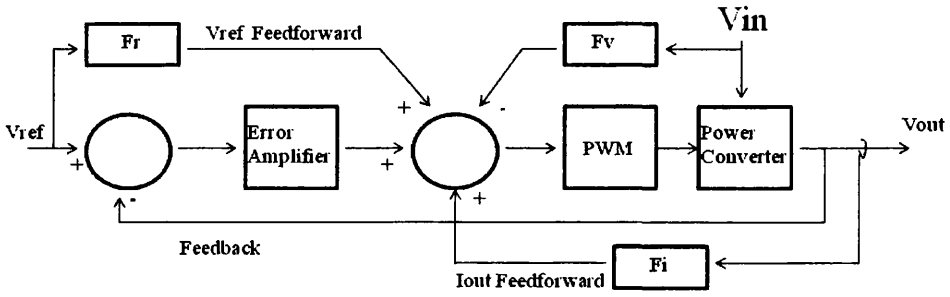


Fig 1.12 Feed Forward Techniques [10]

Current mode Control

Current mode control contains two feedback loops an outer loop, containing the output voltage sensing and an inner loop providing output current sensing. This method offers a number of advantages over pure voltage mode control including inherent line feed forward function as stated in the previous section. The method also provides for the avoidance of flux imbalance in two switch topologies and simpler feedback loop stabilisation due to the elimination of the output inductor in the small signal analysis [13].

Current Mode Control

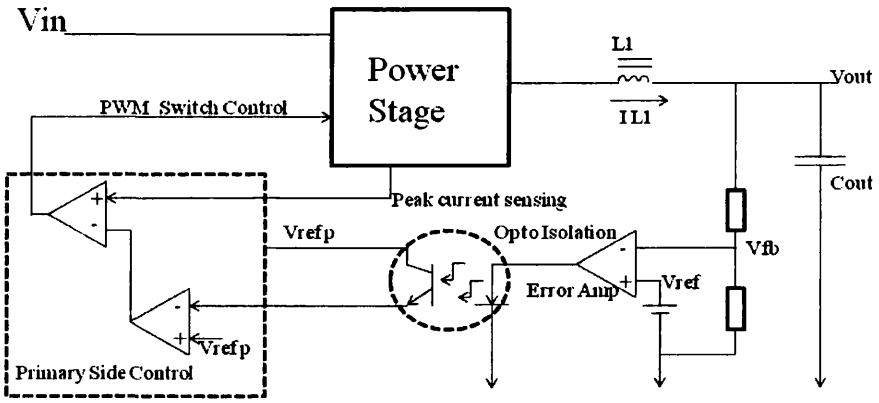


Fig 1.13 Current Mode Control

The application of peak current control does however present deficiencies as well as advantages notably the requirement to apply slope compensation to prevent sub harmonic oscillation during transient changes in the Vin voltage. This requirement is fundamentally due to the output voltage being proportional to the average inductor current and not the peak current. The technique of slope compensation is covered

extensively in [13] and involves the addition of a ramp signal with the sensed current signal. An example of the practical implementation is illustrated in [16].

The above description represents constant frequency "Peak" current mode control, other techniques exist including constant frequency "Valley" and "Average" current mode control. Examples of control methods involving frequency variation include "Constant On" and "Constant Off" time techniques.

1.5 System Partitioning

The above descriptions of control methods show the requirement of all regulated power supplies for feedback from the output to control the power stage and the need for isolation which means the inclusion of some form of AC coupling i.e. a power transformer in the power path and in the feedback path by the inclusion of an opto coupler device as illustrated in fig 1.11 and fig 1.13. These devices have limited bandwidth, poor accuracy and degrade with time and temperature.

It should be noted that whilst opto couplers have been the default signal isolation device, means other than the use of an opto coupler are available from products such as RF isolators [14], Micro transformers [15] and devices based on the GMR principle [50] which offer possible improvements but may have additional operational requirements and significantly increased cost.The use of pulse transformers for isolated gate drives and timing signals also presents performance and space issues making it desirable to minimise the number of isolation boundary crossings. Alternative means [29] are offered as for opto coupler replacement but with the same implications.

For isolated dc-dc converters there is therefore a requirement to cross the isolation boundary a minimum of two times. This however represents the simplest of systems and if control resides on the primary side further crossings of the isolation boundary may be necessary, one example being the provision of drive signals to secondary side synchronous rectifiers where used to replace rectifier diodes to improve efficiency e.g. D1,D2 Fig 1.9. Other requirements may include Overvoltage protection,

frequency synchronisation with load clocks, parallel output operation, and power sequencing among multiple supplies. Inclusion of these functions with the requirement for individual signals crossing the isolation boundary would represent an unacceptable burden of cost and area to a product such as that shown in Fig 1.2.

The question therefore is, can the control function be better located, the alternative being on the secondary side. An overriding reason for traditionally locating the control function on the primary side was that, other than in the special case of a residual output voltage to be discussed in chapter 2.2, there is initially no supply voltage available on the secondary side.

Power supplies such as these have to power up with the rising Vin supply and meet output voltage specifications within very short start up times. Without a supply voltage to the control function located on the secondary side it is difficult to see how this can be achieved.

There are however an increasing number of advantages [17] [30] to locating the control on the secondary side particularly where the power supply and its load are considered as a single system level element. From the nature of the load i.e. predominantly digital equipment containing memory it is reasonable to conceive of the load interacting with its power supply to adjust operation, at any time following successful power up and preferably through a standard digital interface.

A method of achieving secondary side control with the transfer of power always under the single control circuit is illustrated in Fig 1.14. It can be immediately seen that this approach requires a further crossing of the isolation barrier. The auxiliary power supply, whilst low power, still represents an isolated dc-dc converter in its own right and is clearly an undesirable overhead. A commercial example of this approach is shown in [16], [25].

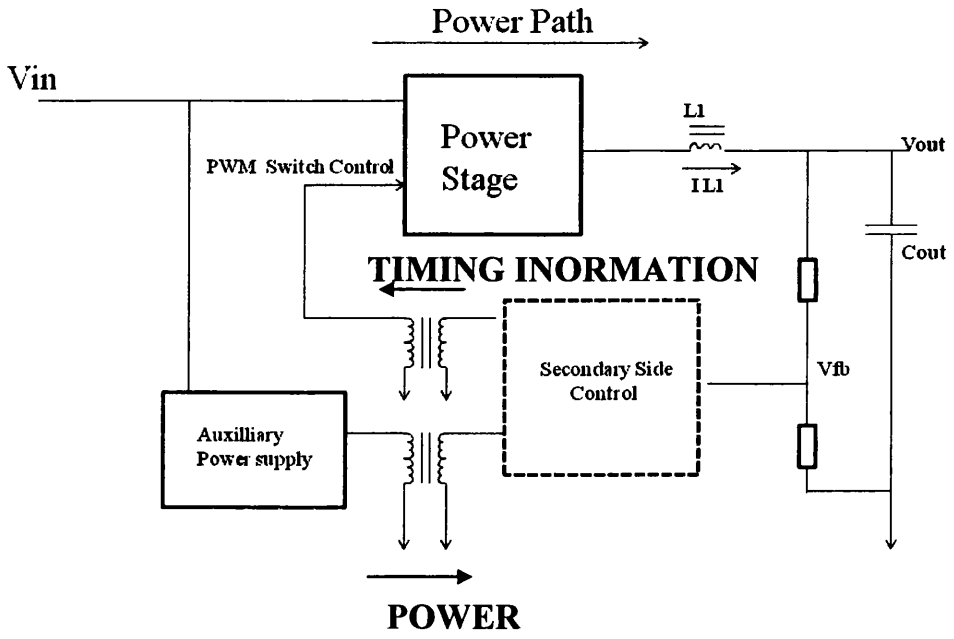


Fig 1.14 Auxiliary Power Supply – Secondary Side Control

The alternative to that shown in Fig 1.14 is to recognise that the fundamental function of the main power path is to transfer power from primary to secondary and if the primary side switching can be initiated under open loop control then there is the potential for the secondary side control to power up and assume complete control within the required ramp up period of the output voltage. Such a system is illustrated in Fig1.15. This illustration highlights three fundamentals the first being the minimum crossing of the isolation boundary, the second being the supply to the secondary side control from the main power path and thirdly the requirement for the soft start function on the primary side. The soft start function would be a feature of a primary side control design but has additional significance in this arrangement.

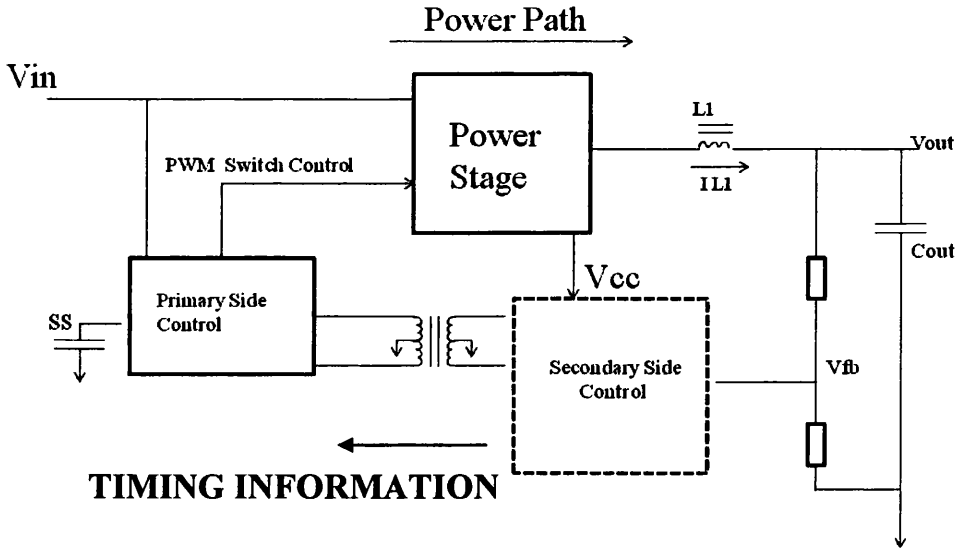


Fig 1.15 Secondary Side Control

As stated in the summary the objective of this work is to confirm the feasibility of this approach, to define the requirements for the primary and secondary side control circuits and confirm by device level circuit design.

As can be seen from Fig 1.15 the system consists of a primary side start up, slave driver device, one crossing of the isolation barrier for the control function and a secondary side master control device. The secondary side device may be implemented by a mixed signal analogue – digital control circuit or be a digital control circuit as represented by [18].

There is one proviso to the minimum crossing of the isolation barrier illustrated in fig1.15 and that is the requirement to turn off the pre regulator circuit associated with the primary side control device. This requirement generally amounts to an auxiliary winding on the output inductor and a diode. This is used to feed back a Vcc supply to the primary device as the output voltage increases and turns off the Vin to Vcc current path.

1.6 Digital or Analogue

The increasing use of digital control techniques from the claimed origin of research at PESC 1977 [19] to the current product offerings of companies such as Linear Technology, Primarion (Infineon), Texas Instruments and Zilker Labs among others represents the development of market acceptance although as reported in 2005 market penetration was still regarded as low in most applications [20].

The inherent ability to provide system communication is seen as a distinct advantage and driving force but cost parity is still required for general acceptance in the market along with efficiency improvement.

These products tend to be targeted at POL applications but not all. The Potentia PS-1005 and PS-1006 devices provided primary side status information communicated to a secondary side controller.

The Silicon Labs Si8250 digital power controller supports isolated and non isolated applications, its application to a half bridge converter is shown at [21]. The absolute maximum ratings for the device however represent a fundamental limitation in that the normal supply voltage range for the device is up to 4V. This limitation is driven by the Silicon process used for digital circuits and limits the gate drive voltage available to the synchronous rectifiers unless separate gate driver circuits are used adding to the area requirement and total system cost.

This limitation would not apply to a 12V BCD or SOI process used for an analogue mixed signal solution which would be capable of providing drivers able to meet the peak current requirements for efficient mosfet switching [22]. With this approach a two chip solution is possible and with the inclusion of the required communications capability particularly a PMBus [23] interface on the secondary side controller it is believed that the advantages of the digital controller can be matched.

2 Theory

2.1 Power Transfer

The half bridge topology shown in fig 1.9 has a number of advantages particularly in regard to the power mosfet breakdown voltage requirements and the utilisation of the magnetic core [30], it is therefore widely used in these applications. A controller design for this two switch topology would also provide the gate drive signals required for other two switch topologies. The fundamental relationship between the output voltage and the input voltage is given by

Eq (1) $$\frac{Vout}{Vin} = \frac{N2\ T(on)}{N1\ T(s)} = \frac{N2\ (D)}{N1}$$ Vin* = Vin/2 fig 1.9.

Where N2/N1 represents the transformer turns ratio and Ts is the period of the switching frequency. The output voltage is therefore stepped down from Vin by the transformer turns ratio and the ratio of the on time to the switching period. The peak drain currents of the power devices will be defined by

Eq (2) $$Id(max) = \frac{N2}{N1}\left(Irl + \frac{dIL1}{2}\right) + Imag$$

where Imag is the peak magnetizing current.The critical voltage and current waveforms for such a half bridge converter are illustrated in Fig 2.1.

The PWM function is illustrated in this instance by the oscillator ramp and the output of the error amplifier defining the on time of the low side (Q2) and high side (Q1) power Mosfets. This represents voltage mode control. Replacing the oscillator ramp with a ramp derived from the inductor current or the current in the primary side power devices would constitute current mode control.

The LX node i.e. the common point between the two power Mosfets switches between the Vin voltage during the Q1 on period and ground during the Q2 on period. During the off period this node is at Vmid defined by C1 and C2 across the Vin supply to ground. The voltage on the gate of Q1 is required to turn on the Nchannel MOS [22] device and therefore requires a gate voltage at least above the threshold voltage of the device. This is generally achieved by adding the Vcc supply to the Vin voltage by a technique known as bootstrapping [24].

The inductor current ramp up slope will be defined by

Eq (3) $$\frac{dI(L1)}{dT} = \frac{(Vsec - Vdiode - Vout)}{L1}$$

where dT is the power mosfet on period and Vdiode represents the forward diode voltage of either D1 or D2 as shown in fig 1.9 and in Apendix C. The average current will be defined by the output voltage divided by the load illustrated by RL.

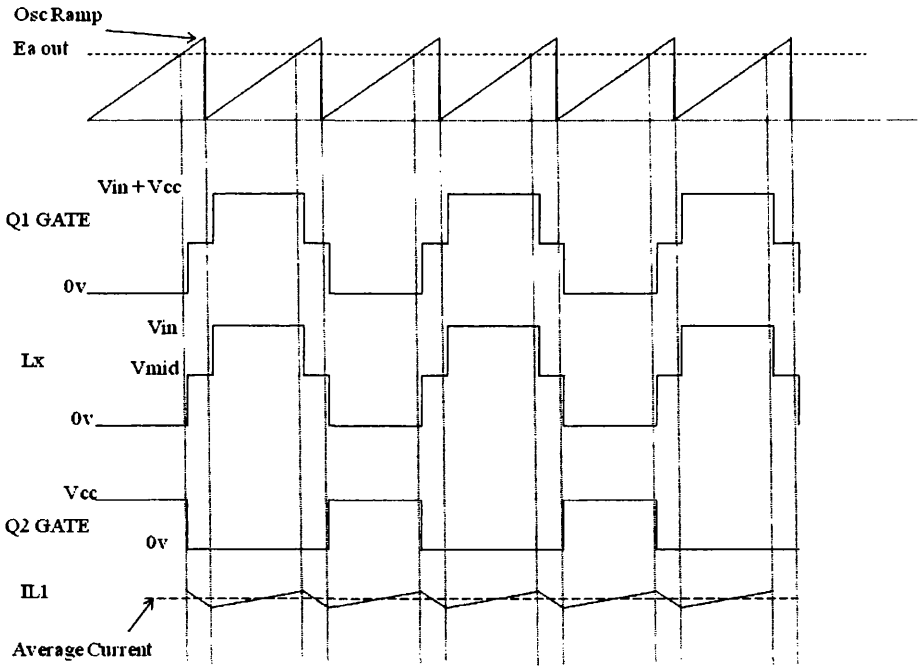


Fig 2.1 Half Bridge Converter Waveforms

The efficiency can be improved significantly if the diode rectifiers in the output circuit are replaced by synchronous rectifiers SRH and SRL. These power Mosfets with Rds(on) figures in the range of a few mOhms require the provision of control signals such that SRL is off for the Q1 on period and SRH is off for the Q2 on period. The inclusion of break before make time delays such that the synchronous rectifier is turned off before the respective primary side device is turned on and not turned back on again until that device is effectively switched off is best achieved by all signals being derived from one monolithic control circuit.

2.2 Start up Requirements

In order to meet the output voltage start up requirements the control circuits themselves have to power up sufficiently within the output voltage time frame to initiate and maintain power transfer through the power path continually under control such that the profile of the output voltage meets specification.

In order to meet the objective of a minimum parts count it is desirable that the primary side device is capable of powering directly off of the Vin supply to provide a stable Vcc voltage of the required level from which all primary side functions are powered including the gate driving of the primary side power Mosfets. To achieve this requirement a pre regulator circuit is required which provides the high voltage breakdown capability to connect directly to the Vin supply and a voltage breakdown path connected from the output side to ground. This breakdown path is used to regulate the Vin to Vcc charging path and is described in detail in fig 6.1.3.

Having successfully powered up the primary side control device this device has then to start switching the primary side power devices and transferring energy through the power path to the secondary side. An example of a start up sequence proposed in [17] is shown in fig 2.2 below.

This illustration shows the output voltage increasing under primary side soft start control during which time the supply to the secondary side controller has increased above its UVLO value and a secondary side soft start function is initiated. At this time

point control of primary side switching and therefore power transfer is assumed by the secondary side device using soft start control. The significant issue with this approach is that if two soft start functions are used in this way it is not possible to control the hand over point over process and temperature variations sufficiently to satisfy the requirement by the load for a monotonic rise in the output voltage. This issue is referred to in [17] and the droop considered acceptable if sufficiently early in the output voltage rise time. The illustration shows this occurring at 1v of a 3.3v final output voltage.

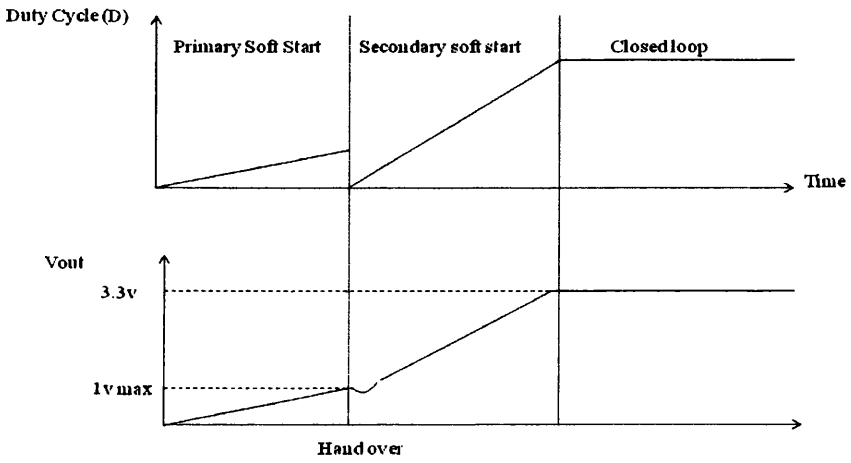


Fig 2.2 Start Up Sequence

The output voltage profile of fig 2.2 is however unacceptable to many load equipments, an example of an acceptable output voltage start up performance is shown in [26]. In order to achieve this performance it is considered necessary to dispense with the secondary side soft start period and for the control loop located on the secondary side to lock to the rising output voltage level and assume control for the remaining charge up period. A proviso to this statement is that it is considered necessary to include a soft start function on the secondary side device for the

provision of hiccup mode [48] over current protection, this requirement is fully explained in chapter 3.3.

Start up times from Vin connection to ninety percent of Vout are typically in the ten to twenty millisecond range. The implications being the primary side power up, soft start period, secondary side power up and control loop lock time need to be sufficiently within this time frame for the control loop to maintain monotonic rise in the output voltage to the final value.

2.3 Line Regulation Requirements

The output voltage of the converter having charged up to its final value is required to be maintained at this value to within the specified tolerance. The initial accuracy would typically be within plus or minus two percent and variation with line voltage less than this with typical figures of a few millivolts quoted representing 0.2 percent for an output voltage of 1.2v. In order to be able to achieve this the required adjustment of switching duty cycle has to come under feed forward control which is either provided from the primary side VIN voltage or from current monitoring in the secondary side. The bandwidth of the voltage control loop is not going to be set wide enough to provide a fast enough response and maintain stability.

2.4 Load Regulation Requirements

The ability to respond to a load step of potentially zero load to full load whilst maintaining tight control of the output voltage is a challenging requirement as illustrated in the specification shown in chapter 3. The voltage control loop in this instance has to provide control of the switching duty cycle. The resulting fall in output voltage has to be conveyed fast enough to increase the energy transfer sufficient to maintain the output voltage within specified tolerance, a task made easier if the control is on the secondary side of the isolation barrier.

3 Objective Specifications

3.1 Power System Specifications

An example of a supply module vendor's [26] data sheet specification is shown in table 3.1. This is for the 1.2V/25A version, the product family includes 1.5V, 1.8V at 25A, 2.5V,3.3v/15A and 5V/10A products.

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
Vi	Input Voltage range		36		75	V
Vioff	Turn off input voltage	Decreasing Vi Note 1	29	31	33	V
Vion	Turn on input voltage	Increasing Vi Note 1	32	33	34.5	V
Ci	Internal Input Capacitance			0.5		uF
Po	Output Power	Vout initial setting	0		30	W
n	Efficiency	50% max Io Max Io 50% max Io Vi=48v Max Io Vi=48v		83.5 82.5 84 83		%
Pd	Power dissipation	Max Io		6.3	10	W
Pli	Input idling power	Io=0A, Vi=53V		1.8		W
Prc	Input standby power	Vi=53V		0.13		W
Fs	Switching frequency	0-100% Imax	290	320	350	KHz
Voi	Output voltage initial setting and accuracy	Tref=25C Vi=53V	1.176	1.2	1.224	V
Vo	Output adjust range		1.0		1.32	V
	Vo tolerance band	0-100% Io	1.16		1.24	V
	Idling voltage	Io = 0A	1.18		1.22	V
	Line regulation	Max Io		5	12	mV
	Load regulation	0-100% Io		5	10	mV

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
Vtr	Load transient Voltage deviation	Vi=53V load step 25-75-25 % of max Io		+/- 160	+/-250	mV
Ttr	Load transient recovery time			25	50	uS
Tr	Ramp up time 10 to 90% Vo		5	6	7	mS
Ts	Start up time Vi connection to 90% Vo	0 to 100% of max Io	9	10	11	mS
Tf	Vi shut down fall time From Vi off to 10%Vo	Max Io Io = 10%	0.05 0.3	0.1 0.7	0.2 1.0	mS mS
Trc	RC start up time Rc off to 10% Vo	Max Io Io = 10%		0.5 0.5		mS mS
Io	Output current		0		25	A
Ilim	Current limit threshold	Tref < max	26	31	35	A
Isc	Short circuit current	Note 2		20		A
Voac	Output ripple, noise	Max Io, Vo		70	130	mVp-p
OVP	Over Voltage protection	Tref = 25C Vi=53V 0-100% max Io		1.55		V

Note 1 See information section Turn off input Voltage.

Note 2 RMS current in hiccup mode, Vo lower than 0.5v.

Table 3.1

The above data sheet table illustrates the performance achievable by such power supplies, of note is the efficiency achieved, the dynamic response times and deviation to load transients of fifty percent of full load in tens of micro seconds and the start up times from Vin connection of milliseconds. Implicit in this product specification are controller functions required e.g. the inclusion of over voltage protection and the method of over current protection i.e. in this product hiccup mode OCP is provided as stated in note 2. The accuracy of the output voltage is to within two percent which therefore sets the requirement for the reference voltage provided to the output voltage feedback on the secondary side and therefore by the proposed secondary side controller.

The input voltage range defines the breakdown voltage requirement of the primary side pre regulator circuit which along with the high side drive requirement of the half bridge topology defines the semiconductor process to be used.

The following proposed objective specifications therefore define the primary and secondary side integrated circuits required to control the operation of an isolated dc-dc converter as specified above.

3.2 Primary side Controller Objective Technical Specification

Description

The proposed integrated circuit is intended to provide the function set required for the primary side device of a two switch isolated DC-DC converter such as a half bridge circuit. The device is intended to power up from the Vin supply and provide a regulated Vcc supply and low temperature coefficient reference voltage for circuit operation. The device will initiate output switching under soft start control through driver circuits capable of directly driving both high and low side power Mosfet switches. At the end of the soft start period the device will operate at the set maximum duty cycle until switching control is assumed by a secondary side controller which may occur at any time during the soft start period.

The circuit will also provide a user definable oscillator, over temperature protection and two level over current protection to the primary side power components.

Absolute Maximum Ratings

PARAMETER	LIMIT	UNIT
Storage Temp	-65 to 150	deg C
Operating Junction temp	150	deg C
Power dissipation TSSOP 16	850	mW
Thermal Impedence	75	deg C/W
VIN	100	V
VCC	14.5	V
Vbst	114.5	V
VLX	100	V

Vbst - Vlx	14.5	V
Logic Inputs	-0.3 to Vcc+0.3	V
Analog Inputs	-0.3 to Vcc+0.3	V
Preg Input Current continuous	5	mA

Recommended Operating Range

PARAMETER	LIMIT	UNIT
VIN	36 to 75	V
VCC	10.5 TO 13.5V	V
CVcc	>4.7	uF
FOSC	200 TO 500	KHz
ROSC	40 to 200	KOhms
COSC	80 to 220	pF
Soft Start Capacitor	10 to 100	nF
Cref	0.1	uF
Cboost	0.1	uF
Analog Inputs	0 to Vcc - 2	V
Digital Inputs	0 to Vcc	V
Reference output current	0 to 5	mA

SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS Min Typ Max	UNIT
Pre Regulator				
Input voltage	Vin		36 to 75	V
Input Leakage current	Ilkg		10	uA
Input sourcing current	Istart		40	mA
Regulator bias current	Ireg		100	uA
Regulator output	Vreg		9.5	V
Vreg hysterysis			0.6	V
UVLO			8.9	V
UVLO hysterysis			0.6	V
Reference				
Output voltage	Vref		3.25 3.3 3.35	V
Short circuit current	Isat		40	mA
Load Regulation	dV/dI		-30	mV

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS Min Typ Max	UNIT
Oscillator				
Max Frequency	Fmax	Rosc = 40k	500	KHz
Accuracy		1% Rosc	+/- 5	%
Soft Start				
Current Output	Iss	Start up condition	20	uA
Completion Voltage			6.8	V
Discharge Current		Normal/hiccup	20/0.25	uA
Over Temperature Protection				
Activating Temperature	OTPon	Tj increasing	135	deg C
De-Activating Temperature	OTPoff	Tj decreasing	115	deg C
Over Current Protection				
Current limit	Moc		100	mV
Current limit	Soc		150	mV
Cs to DH,DL delay			100	nS
Leading edge blanking			50	nS
Primary Driver High Side				
Output high voltage		Sourcing 10mA	Vbst -0.3	V
Output low voltage		Sinking 10mA	Vlx +0.3	V
Rise time		Vcc = 10v cl=3nF	15	nS
Fall time		Vcc = 10v cl=3nF	15	nS
Peak source current			2	A
Peak sink current			2	A
Primary Driver Low Side				
Output high voltage		Sourcing 10mA	Vcc -0.3	V
Output low voltage		Sinking 10mA	Pgnd +0.3	V
Rise time		Vcc = 10v cl=3nF	15	nS
Fall time		Vcc = 10v cl=3nF	15	nS
Peak source current			2	A
Peak sink current			2	A

Pin Configuration

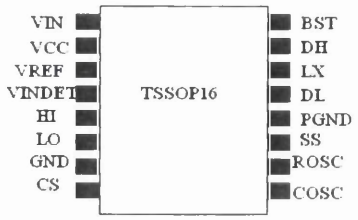


FIG 3.1 Primary Side Controller Pin Configuration

PIN DISCRIPTION		
1	VIN	Input supply voltage
2	VCC	Internal Supply voltage
3	VREF	Reference voltage
4	VINDET	VIN feed forward, Line UVLO, OVLO shutdown function
5	HI	Digital drive input high side
6	LO	Digital drive input low side
7	GND	Analogue ground
8	CS	Current limit input
9	COSC	Oscillator capacitor connection
10	ROSC	Oscillator resistor connection
11	SS	Soft Start control
12	PGND	Power ground
13	DL	Low side gate drive
14	LX	High side source and transformer connection
15	DH	High side gate drive
16	BST	Bootstrap voltage

Block Diagram

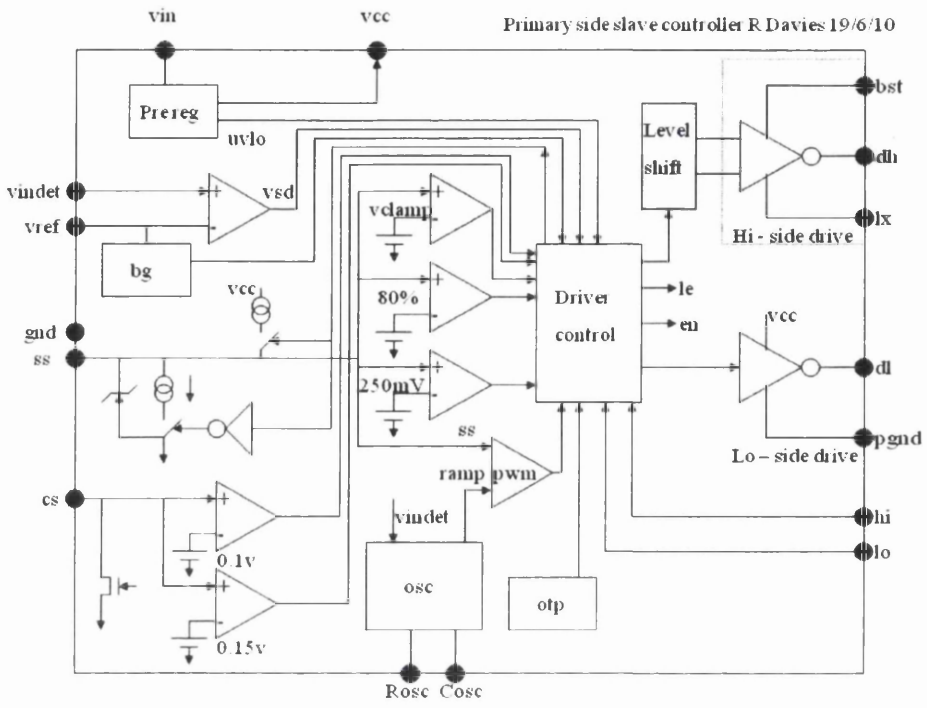


FIG 3.2 Primary Side Controller Block Diagram

Functional Description

Start Up

The device will charge the Vcc capacitor from the Vin pin until the Vcc supply has reached its completion voltage. On Vcc exceeding the upper UVLO voltage the device will enable its internal circuitry and allow operation of the band gap based reference voltage to begin to charge. Once the reference voltage has exceeded its internally defined reference ready level, operation of the oscillator is begun and charging of the soft start pin enabled. The pre regulator has potentially a 100v voltage drop from the Vin pin to the Vcc pin with a saturation current level of 40mA and therefore a power dissipation of 4W. Clearly the temperature rise at this power dissipation would be unacceptable and is avoided by voltage feedback from the power path to the Vcc pin to ensure the Vin to Vcc current path is turned off.

Reference Voltage

The Vref pin is charged to 3.3v and is intended to be trimmed at die sort to have an initial voltage within plus or minus 1.5% at room temperature. The reference is based on the principle of a band gap cell [44] to provide a high degree of temperature invariance.

Soft Start

The soft start function will control the duty cycle of the output switching during the period in which it is charging through the oscillator ramp range. The rate of change of the voltage on the SS pin is defined by the value of the external capacitor being charged by the internally defined charging current. The soft start function is also to be used to control the duty cycle under over current protection operation.

PWM Operation

Output switching will be defined by the oscillator frequency and the duty cycle by the slicing level of the oscillator ramp and the soft start voltage when the soft start voltage is within the oscillator ramp range. The period prior to the SS voltage entering the ramp range will have both outputs in the off state. Output switching will commence with the DL output switching high first so as to allow a charging cycle for the BST supply before the DH output is required to go on. Output switching will run at the dmax level once the SS pin has charged above the maximum ramp level and is held at its clamp level. The upper turning point of the ramp waveform will be defined by the voltage on the VINDET pin. This feature will provide a feedforward function during the soft start period extending the period for increased line voltage and therefore softening the soft start function. Control of output switching is taken over by the Hi and Lo inputs once either switches high.

Over Current Protection

The current in the primary circuit power devices is monitored on the low side by a sense resistor. Two level protection is provided, if the voltage seen at the CS pin exceeds the moderate over current level the protection circuitry will reduce the duty cycle by starting to discharge the SS pin. If this level continues once discharged past 80% of the ramp amplitude output switching is stopped and a dramatically reduced discharge rate on the SS pin will provide the hiccup ratio. Exceeding the higher level stops switching immediately and the SS pin is discharged at the 0.25uA rate.

Over Temperature Protection

The device will provide thermal protection disabling switching when the temperature exceeds the higher threshold and not enabling until below the lower threshold. Switching restarts under soft start control.

Output Drivers

The device will provide cmos driver outputs with a typical peak current charging capability of 2A for fast and efficient switching of the primary power Mosfets. The high side driver circuit will provide level shift capability up to a maximum of 100V on the LX pin.

3.3 Secondary side Controller Objective Specifications

Description

The proposed integrated circuit is intended to provide the control functions required to perform from the secondary side, current mode control of an isolated dc-dc converter. The device will provide a regulated Vcc voltage to power all functions including the capability to directly drive the gates of synchronous rectifier power Mosfets. The device will provide an oscillator, an error amplifier, and a reference voltage required for current mode PWM control of the dc-dc conversion. The device will offer two modes of operation one where the device is powered from an auxiliary supply derived from the primary side and where the device retains control of PWM switching of the power path at all times and a second mode of operation where the device is powered from the secondary side and takes over control from a slave primary side device.

In both operating modes the device will provide the dominant OCP and OTP functions once control has been assumed and will offer user adjustment of various parameters via a PMBus interface.

Absolute Maximum Ratings

PARAMETER	LIMIT	UNIT
Storage Temp	-65 to 150	deg C
Operating Junction temp	150	deg C
Power dissipation MLP55 24	850	mW
Thermal Impedence	29	deg C/W
VIN	14.5	V
VCC	14.5	V
Logic Inputs	-0.3 to Vcc 0.3	V
Analog Inputs	-0.3 to Vcc 0.3	V

Recommended Operating Range

VIN	14	V
VCC	9 to 12	V
CVcc	>4.7	uF
FOSC	200 TO 500	KHz
ROSC	40 to 200	KOhms
COSC	80 to 220	pF
Soft Start Capacitor	10 to 100	nF
Cref	0.1	uF
Analog Inputs	0 to Vcc - 2	V
Digital Inputs	0 to Vcc	V
Reference output Current	0 to 5	mA

SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS Min Typ Max	UNIT
Pre Regulator				
Input voltage	Vin		12 to 14	V
Input Leakage current	Ilkg		10	uA
Input sourcing current	Istart		40	mA
Regulator bias current	Ireg		100	uA
Regulator output	Vreg		9.5	V
Vreg hysterysis			0.6	V
UVLO			8.9	V
UVLO hysterysis			0.6	V

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS Min Typ Max	UNIT
Reference				
Output voltage	Vref		3.25 3.3 3.35	V
Short circuit current	Isat		40	mA
Load Regulation	dV/dI		-30	mV
Oscillator				
Max Frequency	Fmax	Rosc = 40k	500	KHz
Accuracy		1% Rosc	+/- 5	%
Soft Start				
Current Output	Iss	Start up condition	20	uA
Completion Voltage			6.8	V
Discharge Current		Normal/hiccup	20/0.25	uA
Over Temperature Protection				
Activating Temperature	OTPon	Tj increasing	135	deg C
De-Activating	OTPoff	Tj decreasing	115	deg C
Over Current Protection				
Current limit	Moc	OCP 0.1 to 1V	100 1000	mV
Current limit	Soc	OCP 0.15 to 1.5V	150 1500	mV
Cs to HI,LO delay			100	nS
Leading edge blanking			50	nS
Over Voltage Protection				
Activating Voltage	OVPon		1.47	V
De-Activating	OVPoff			V
Primary Driver				
Output high voltage		Sourcing 1mA	Vcc -0.3	V
Output low voltage		Sinking 1mA	gnd +0.3	V
Rise time		Vcc = 10v cl=0.3nF	15	nS
Fall time		Vcc = 10v cl=0.3nF	15	nS
Peak source current			200	mA
Peak sink current			200	mA
Secondary Drivers				
Output high voltage		Sourcing 10mA	Vcc -0.3	V
Output low voltage		Sinking 10mA	Pgnd +0.3	V
Rise time		Vcc = 10v cl=3nF	8	nS
Fall time		Vcc = 10v cl=3nF	8	nS
Peak source current			4	A
Peak sink current			4	A

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS Min Typ Max	UNIT
Break Before Make delays				
SRH to HI outputs	BBM1	Rbbm1 22k to 110K	10 to 50	nS
SRL to LO outputs	BBM2	Rbbm2 22k to 110K	10 to 50	nS
BBM adjustment	dBBM		10 to 20	%
Over Voltage Protection				
Over voltage trip point	OVP	+20 %	1.47	V
Over voltage adjustment	Ovp trim		+2 to +36	%
Dmax Limit				
SRL, SRH outputs	DMAX	Fosc = 250KHz	95	%
PMBus				
Input Voltage Low			0.8	V
Input Voltage high			2.2	V
Output Voltage Low		Vcc =10v I sink = 4mA	0.4	V
Pull Up Current			100 350	uA

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS Min Typ Max	UNIT
Serial Bus Timing				
Clock Frequency			400	KHz
Glitch Immunity			50	nS
Start Set up time			4.7	uS
Start hold time			4	uS
SCL low time	T_low		4.7	uS
SCL high time	T_high		4	uS
SCL,SDA rise time			1000	nS
SCL,SDA fall time			300	nS
Data set up time		250		nS
Data hold time		300		nS
Error Amplifier				
Input Offset voltage	Voffset		5 15	
Input Bias Current	Ib		0.5 2	uA
AVOL		1v <Ea_out<5v	60 90	dB
CMRR		2v <Ea_out<8v	65 95	dB
PSRR		2v <Ea_out<8v	65 95	dB
Output Sink Current	Isink	Ea_out = 1v	1 2.5	mA
Output Source Current	Isource	Ea_out = 5v	-1.5 -3	mA
Output Voltage High	Vouth	I Ea_out= - 0.5mA	8 10	V
Output Voltage low	Voutl	I Ea_out= 1.0mA	1 2	V
Unity Gain BW			7 10	MHz
Slew Rate	SL		5 10	V/uSec

Pin Configuration

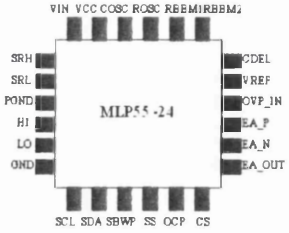


Fig 3.3 Secondary Side Controller Pin Configuration

PIN DISCRIPTION		
1	SRH	Synchronous Rectifier Gate drive
2	SRL	Synchronous Rectifier Gate drive
3	PGND	Power ground
4	HI	Digital drive output high side
5	LO	Digital drive output low side
6	GND	Analogue ground
7	SCL	Serial Bus Clock
8	SDA	Serial Bus data
9	SBWP	Serial Bus Write Protect
10	SS	Soft Start control
11	OCP	Over Current detection level
12	CS	Current limit input
13	EA_OUT	Error Amplifier Output
14	EA_N	Error Amplifier inverting input
15	EA_P	Error Amplifier non inverting input
16	OVP_IN	Over voltage protection input
17	VREF	Reference Voltage
18	CDEL	Synchronous rectifier delay capacitor connection
19	Rbbm2	Break before make timing resistor connection
20	Rbbm1	Break before make timing resistor connection
21	ROSC	Oscillator resistor connection
22	COSC	Oscillator capacitor connection
23	VCC	Internal Supply voltage
24	VIN	Input supply voltage

Block Diagram

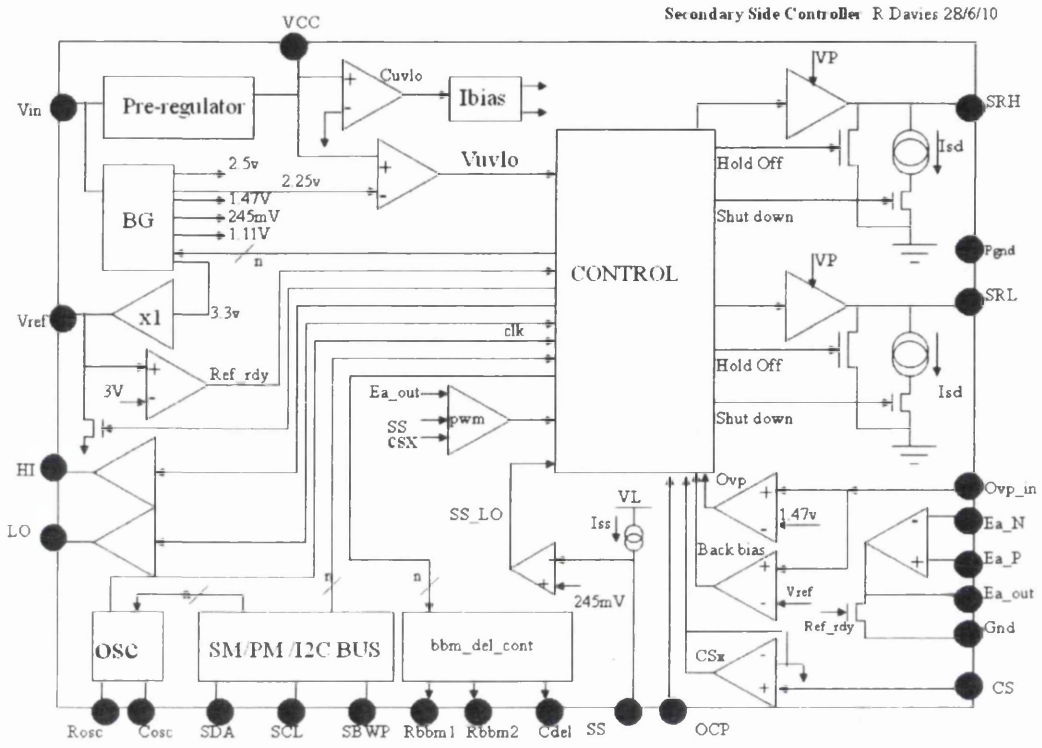


Fig 3.4 Secondary Side Controller Block Diagram

Functional Description

Start Up

The device will charge and regulate the voltage at the VCC pin from the VIN supply. The Pre regulator will operate as described for the primary side device with the exception that continuous operation is now possible as the voltage drop and therefore power dissipation are significantly reduced from that of the primary. Supplying the Vcc pin directly at a voltage above the Vreg level will disconnect the Vin to Vcc charge path.

Reference Voltage

The Vref pin is charged to the initial untrimmed value on Vcc exceeding the UVLO level. The reference voltage circuit is as for the primary side with the exception that trimming of the reference voltage is via the serial data bus from the secondary side.

Error Amplifier

The error amplifier input range will provide ground sensing capability and potentially provision for input offset trimming via the PMBus. Both inputs and output are pinned out allowing for application level gain and compensation setting.

Soft Start

The soft start function will control the duty cycle of the output switching during the period in which it is charging through the oscillator ramp range only if the device is configured for continuous secondary side control. The rate of change of the voltage on the SS pin is defined by the value of the external capacitor being charged by the internally defined charging current. The soft start function is also intended to be used to control the duty cycle under over current protection operation. For operation under primary side open loop power up the soft start circuit is initially disabled and enabled for OCP operation after the output voltage has reached final value.

PWM Operation

Output switching under secondary side control will be defined by the oscillator clock frequency and the duty cycle by the slicing level of the current sense ramp and the error amplifier feedback level. The dv/dt of the ramp waveform will be defined by the current in the power path components on the secondary side and the gain applied e.g. via the turns ratio of a current monitoring transformer. Current mode control will provide a feedforward function as described in [13].

Over Current Protection

The current in the secondary circuit power devices is monitored to provide current mode control and therefore provides the information for over current protection. Two level protection is provided, if the voltage seen at the CS pin exceeds the moderate over current level the protection circuitry will reduce the duty cycle by starting to discharge the SS pin. If this level continues once discharged past 80% of the dmax

amplitude output switching is stopped and a dramatically reduced discharge rate on the SS pin will provide the hiccup ratio. Exceeding the higher level stops switching immediately and the SS pin is discharged at the 0.25uA rate. For operation under open loop primary side power up the soft start function is disabled on entering the 0.25uA discharge rate and restart is via a primary side soft start with the secondary side soft start disabled.

Over Temperature Protection

The device will provide thermal protection disabling switching when the temperature exceeds the higher threshold and not enabling until below the lower threshold. Switching restarts under soft start control provided other operation qualifications are met e.g. UVLO requirements. As for OCP operation under open loop primary start up the soft start function is disabled and restart occurs under primary side soft start.

Output Drivers

The device will provide cmos driver outputs with a typical peak current charging capability of 4A for fast and efficient switching of the secondary power Mosfets. The drives to the primary side device primarily provide timing information via a pulse transformer into the primary side driver and therefore have a significantly lower peak current requirement.

Over Voltage Protection

A separate input pin is provided for over voltage protection of the output voltage. This provides protection of excess output voltage independent of the voltage control loop and therefore will remain operational in the event of failure in the primary voltage control mechanism. The trip level is set at 20% above the internal bang gap reference voltage level. The appropriate feedback ratio will allow the setting of the required OVP level at the application design level.

PMbus Operation

The PMbus interface comprising the SCL, SDA and SBWP pins provide the interface to allow for adjustment of parameter settings via serial data on the SDA pin clocked in via the SCL pin. The SBWP pin connected low inhibits writing of data into device registers.

4 Circuit Design

4.1 Half Bridge Converter Design

The schematic shown in Fig 4.1 (repeated in Appendix B) represents a complete half bridge dc-dc converter. It is important to point out that this design is a functional level design i.e. it makes use of ideal components such as the voltage controlled switches and the transformer models comprising the power train. It is used to confirm the operation of the proposed primary and secondary integrated control circuits which are themselves designed using functional models at this stage.

It should also be noted that there are other methods of achieving some of the design features illustrated available to the application level designer, an example would be the use of an external pass transistor with the primary side pre regulator to extend the power dissipation range and therefore extend the start up time available. The application level (OEM) designer may choose not to rely on the on chip OTP functions offered and use a discrete device which he can better locate next to critical power train components.

The point is that the design of the controlling integrated circuits makes available an optimum function set to the application designer and at the same time not commit their use to the converter design. Perhaps the most significant example of this approach is the inclusion of the soft start function on the secondary side control circuit. It is the contention of this work that use of a soft start function on both the primary and secondary is not viable for achieving monotonic rise in the output voltage, however from the perspective of the semiconductor vendor offering a product with more than one application use is desirable. The inclusion of the soft start function on the secondary side device allows for the device to be used with an auxiliary supply and in continuous control of the main power path.

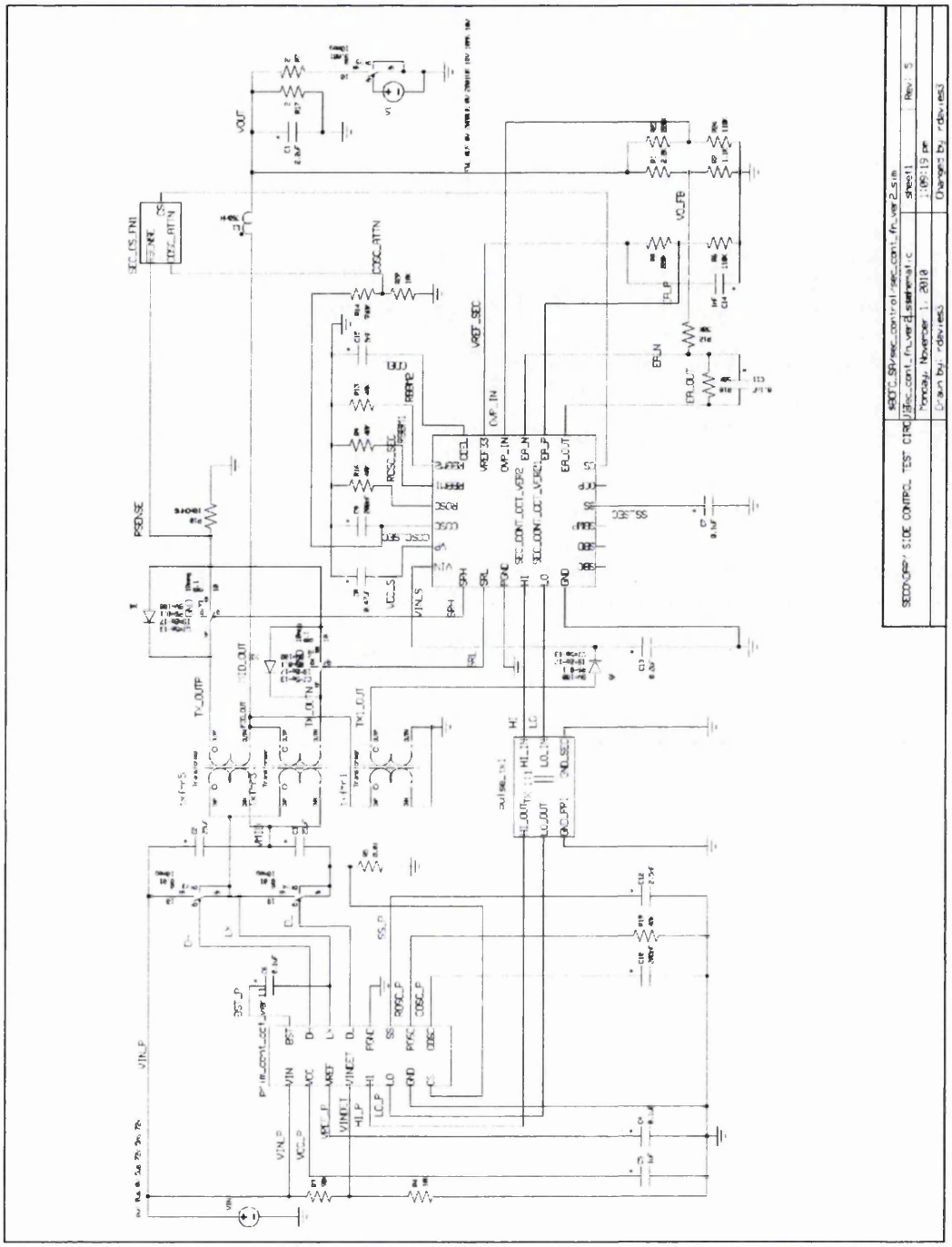


Fig 4.1 Half Bridge Topology Functional Circuit Simulation Diagram

4.2 Primary Side Controller Functional Circuit

The primary side control circuit "Prim_cont_cct_ver1" is shown in fig4.2 and contains the following function blocks

1. Pre-regulator
2. Reference Circuit
3. Oscillator
4. Vindet Control
5. Soft Start circuit
6. Pwm comparator
7. Over current protection circuit
8. High and low side driver circuits.
9. Control logic circuit

The following is a description of the functional level implementation of each of the above circuits.

Pre-Regulator

The pre-regulator schematic "pre_reg_fn" is shown in fig 4.2.1, the function is modelled by VCCS G1 connected between VIN and VP this function sources a current saturating at 36mA at VIN = 72V. This current will therefore charge the recommended 4.7uF external VP capacitance to 10v in 1.3mSeconds. The comparator "comp2" switches high at 10V, the reference to the comparator is switched to 9.8V providing 200mV of hysteresis. The input to G1 is connected to ground turning off the VP charging current. Load taken from the VP supply results in VP decaying to 9.8V at which point the charging current is switched back on recharging VP to 10v. This cycle repeats as a hysteretic regulator. The first crossing of the 9.6v reference level clocks the output UVLO_L high confirming the VP supply is operational. The latch dff2_bg1 is reset when the VP supply falls below the 8.8v reference, indicating an under voltage condition to the control block.

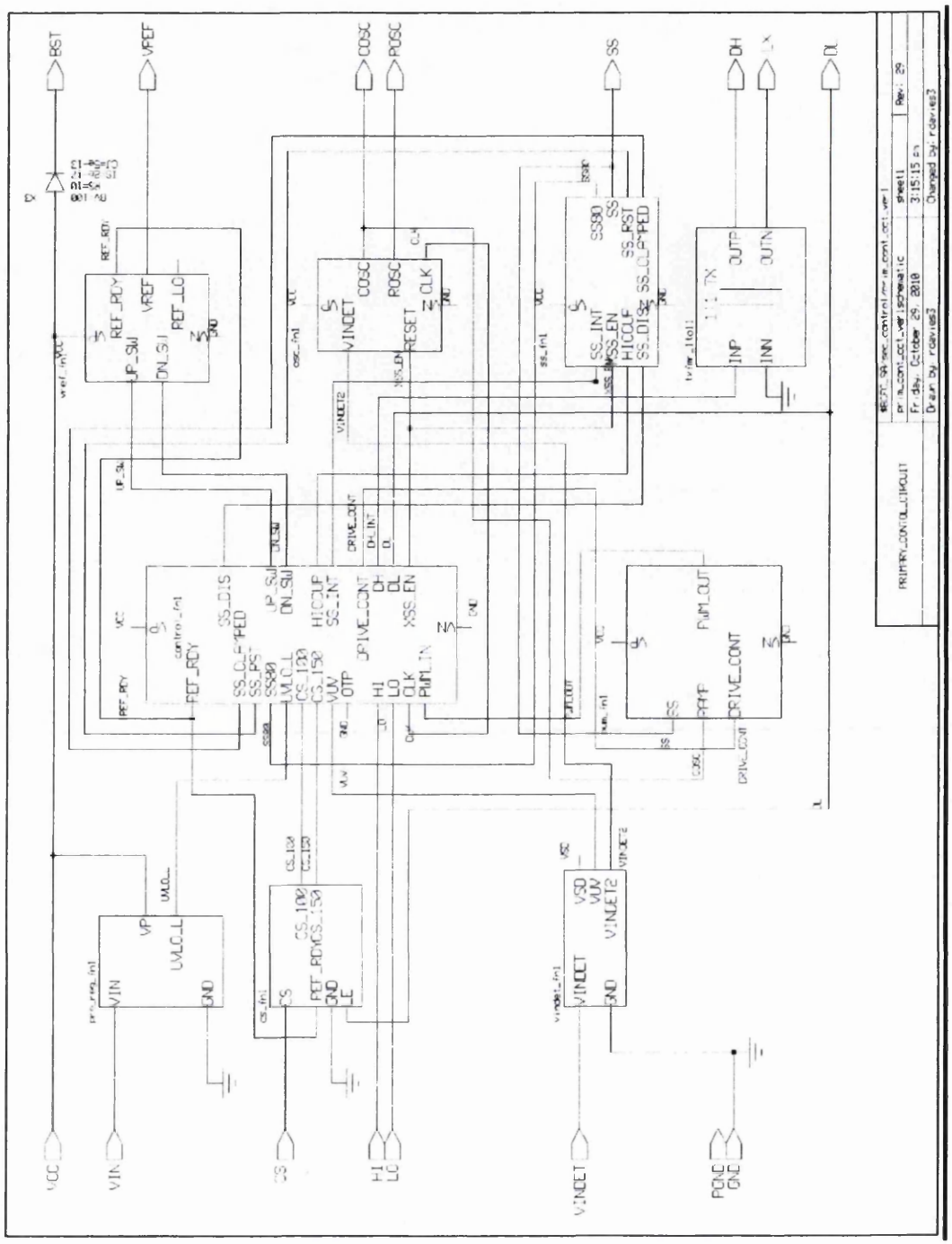


Fig 4.2 Primary Side Controller Functional Circuit

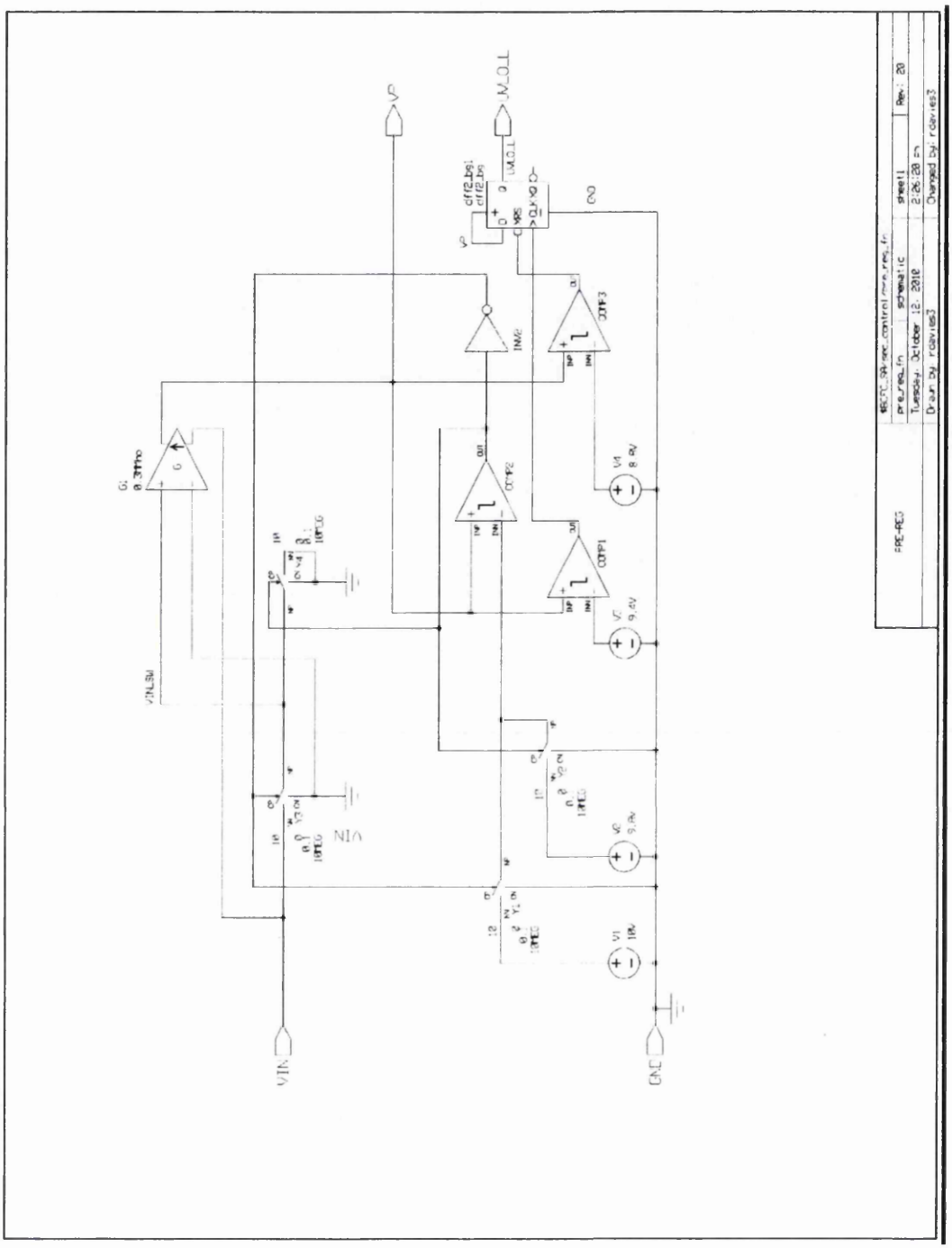


Fig 4.2.1 Pre Regulator Functional Circuit

Reference Circuit

The reference schematic "vref_fn is shown in fig4.2.2. The reference voltage is allowed to begin charging on the input UP_SW going high. This signal from the control block represents all qualifying conditions having been achieved. The VREF pin is charged via VCCS G1 until 3.3V is achieved at which point COMP2 switches turning off the latch, VREF can decay under load to 3.25V until COMP3 switches and clocks the latch on recharging VREF to 3.3v. The 50mV of hysteresis represents a tolerance of 1.5% on the reference voltage.

Oscillator

The oscillator circuit "osc_fn" is shown in fig 4.2.3. The charging current is defined by the input VINDET applied across the external resistor ROSC. The VINDET input is one tenth of the VIN voltage and therefore provides feed forward information to the oscillator. The upper turning point of the ramp generator is also defined by the vindet voltage therefore the ramp waveform at COSC increases with the line voltage but remains at the set frequency defined by

I = Vindet/Rosc, and Frequency = I/CdV assuming the discharge time is negligible.

Therefore to a first order Frequency = Vindet/ Rosc Cosc Dv where dV = Vindet Frequency = 1/Rosc Cosc and therefore as required independent of Line voltage. With this arrangement the amplitude of the oscillator ramp is linearly proportional to the line voltage and therefore for a constant slicing level from the voltage control loop the PWM time generation is inversely proportional to line voltage and reduces the duty cycle to maintain the volt second product constant.

The oscillator circuit contains function block "clk_fn" which generates the clock signal synchronous with the peak of the oscillator ramp waveform. The clock generation function is shown in fig 4.2.3.1.

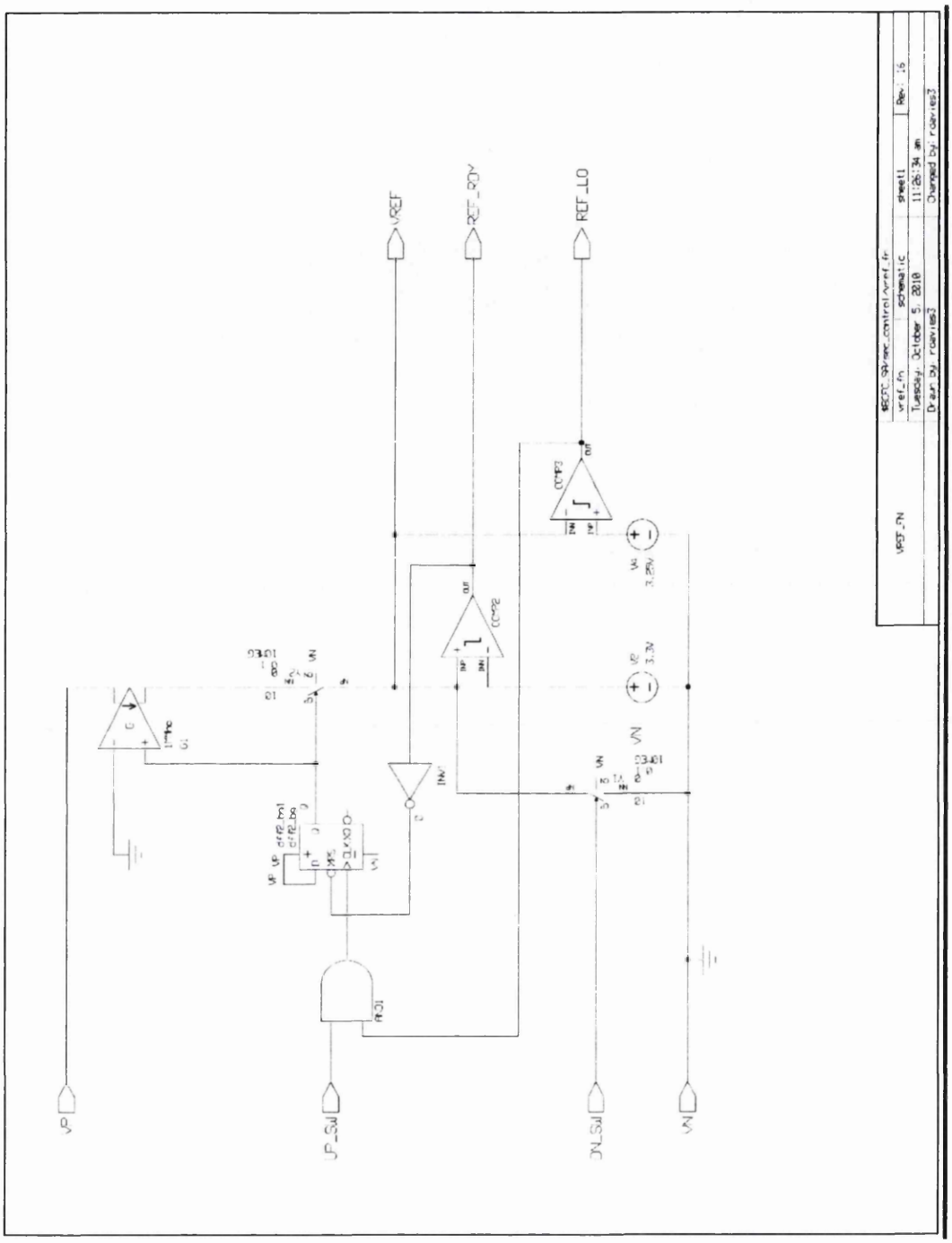


Fig 4.2.2 Reference Voltage Generator Functional Circuit

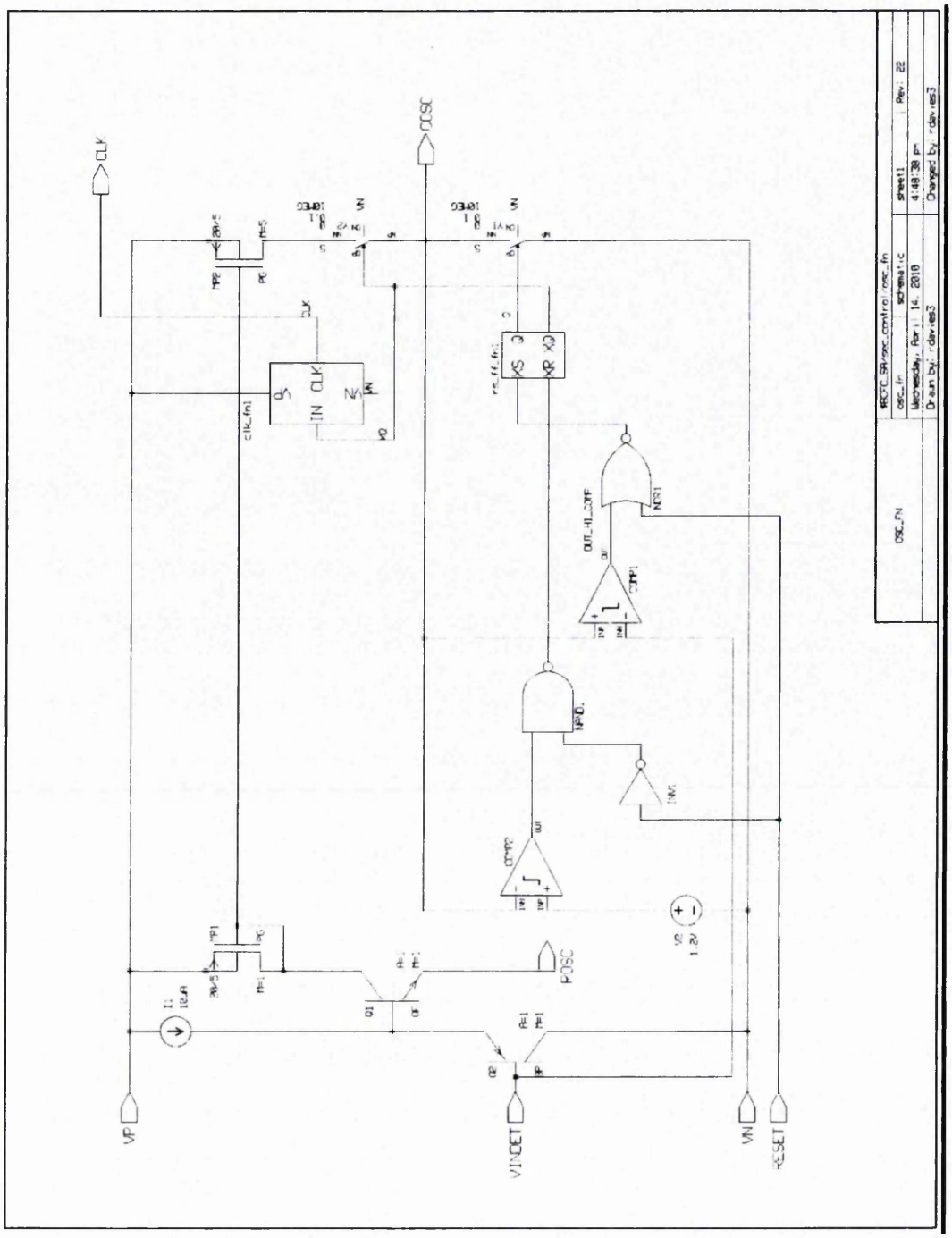


Fig 4.2.3 Oscillator Functional Circuit

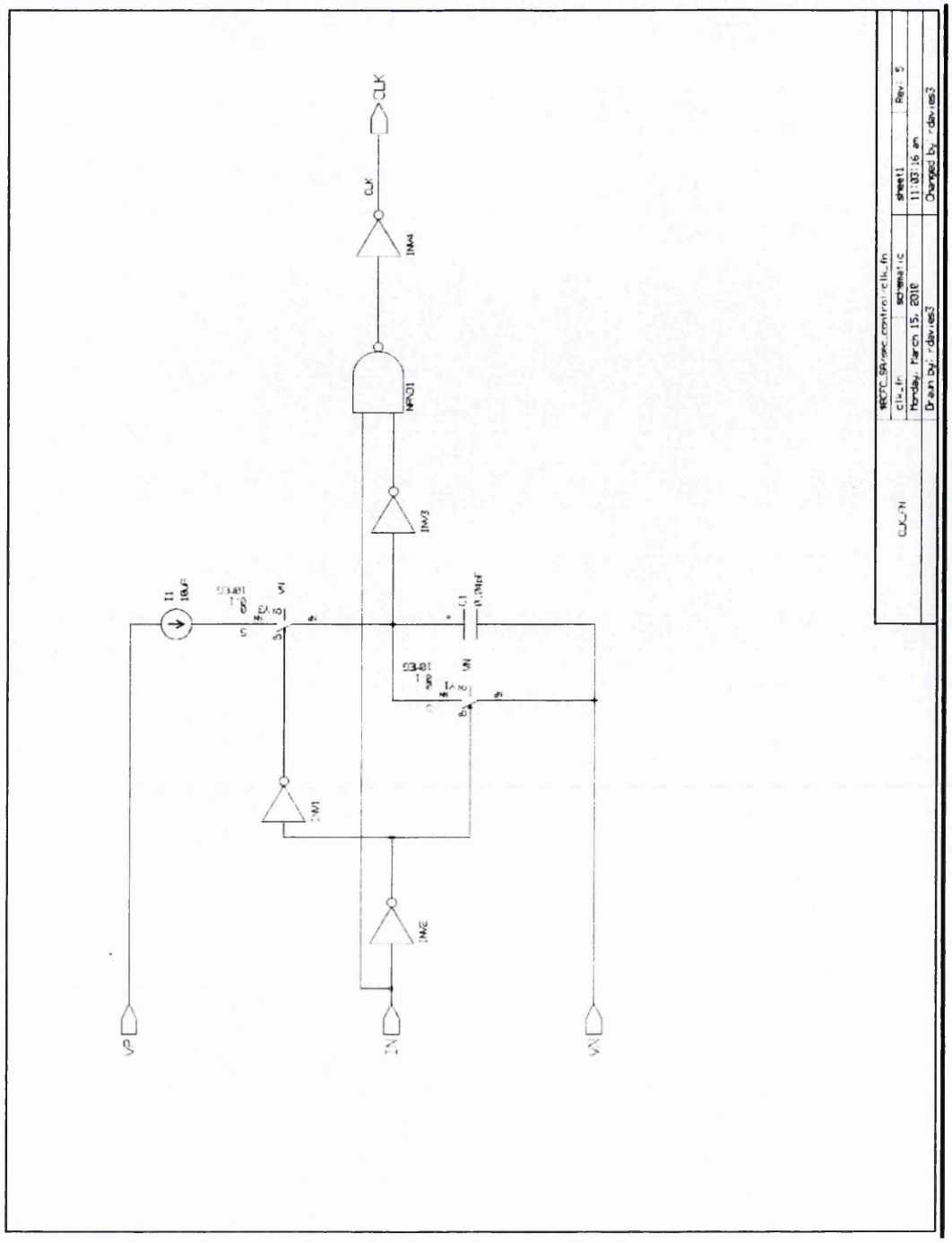


Fig 4.2.3.1 Clock Generator Functional Circuit

Vindet_control

The Vindet control circuit "vindet_fn" is shown in fig 4.2.4. This functional block defines control outputs VSD, VUV and VINDET2. The vindet input is buffered by Y1 the output of Y1 is compared to reference voltages V3 and V4 by comparators Comp1 and Comp2 respectively to provide outputs Vsd and Vuv.

The Vsd output offer a shut down function associated with the Vindet input. This function is not used in the functional level design but in a device level design would provide the capability to shut down the current demand of the circuit as stated in the objective specification.

The Vuv output provides a line uvlo function to inhibit operation below a line voltage of 33v assuming an external attenuation ratio of 10 to 1.

The line uvlo function is one of the required qualifiers to enable output switching and is shown connected into the control_fn circuit block.

The output of Y1 is also shown attenuated fifty per cent by R1,R2 to provide output Vindet2. This output is included to illustrate that for the device level design, issues of common mode range and supply headroom in circuit blocks such as the oscillator and pwm circuit may require some reduction in the vindet voltage used below that of the external 10:1 ratio.

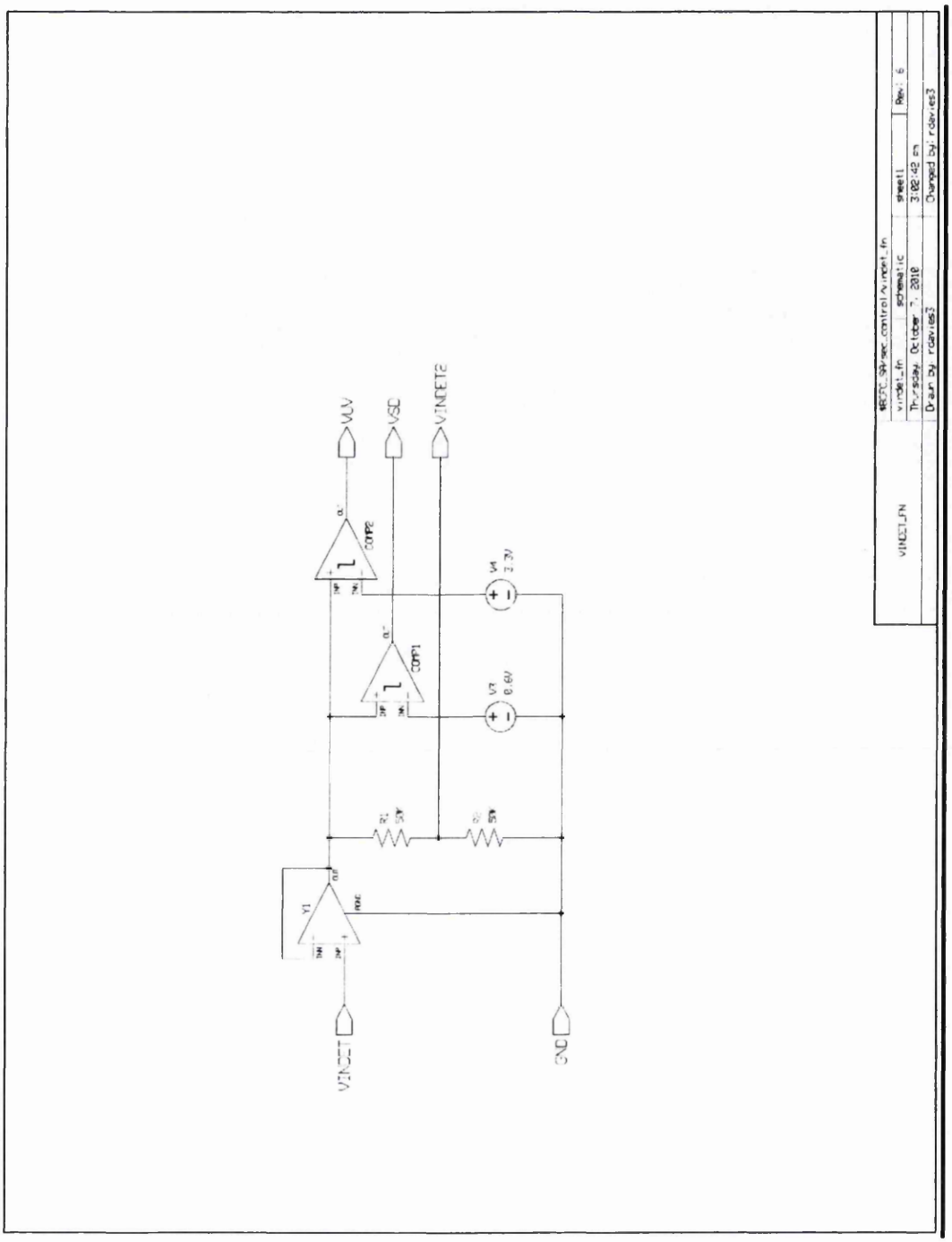


Fig 4.2.4 Vindet Functional Circuit

Soft Start Circuit

The soft start circuit "ss_fn" is shown in fig 4.2.5. This circuit provides the capability to slowly increase the pwm duty cycle provided by the controller at start up and therefore limiting initial inrush current into the discharged output capacitance of the converter. The circuit achieves this by control of the ramp rate seen at pin SS which provides the comparison level relative to the oscillator ramp input to the pwm circuit.

The SS pin is charged from current source I1 via voltage controlled switch Y3 once input XSS_EN has gone high. The SS pin voltage will increase at a rate proportionate to the fixed internal current source and inversely proportionate to the external capacitance connected from the SS pin to ground. The soft start period is therefore programmable at the application design level. The SS pin charges to the completion voltage of 6V provided by reference V2 and the Vbe voltage of Q1. At the completion voltage the SS pin will therefore be fixed at a convenient voltage to define a DMAX of 96 % of the maximum oscillator ramp waveform. On reaching this level output SS_CLAMPED switches high indicating the condition to the control block.

The soft start circuit can also be used to reduce the operating duty cycle in order to provide OCP capability. This function is provided in the soft start circuit in response to the dual level detection of the operating current in the power train. The lower detection level if exceeded during the ramp up period interrupts the soft start charging for the remaining period of that switching cycle. This is achieved by the input SS_INT going high and turning off vcsw Y3. This state is reset each alternate clock cycle thus maintaining the duty cycle constant between the high and low side on periods and therefore maintaining flux balance in the power transformer.

If the lower detection level is exceeded after the SS pin has reached its clamp level then from the control block input SS_DIS switches high and begins to discharge the SS pin via vcsw Y4. This results in the discharge of SS at the rate

defined by the on state resistance of Y4 until the SS pin has reached the 80% level with subsequent reduction in D. This state is indicated by output SS80 going

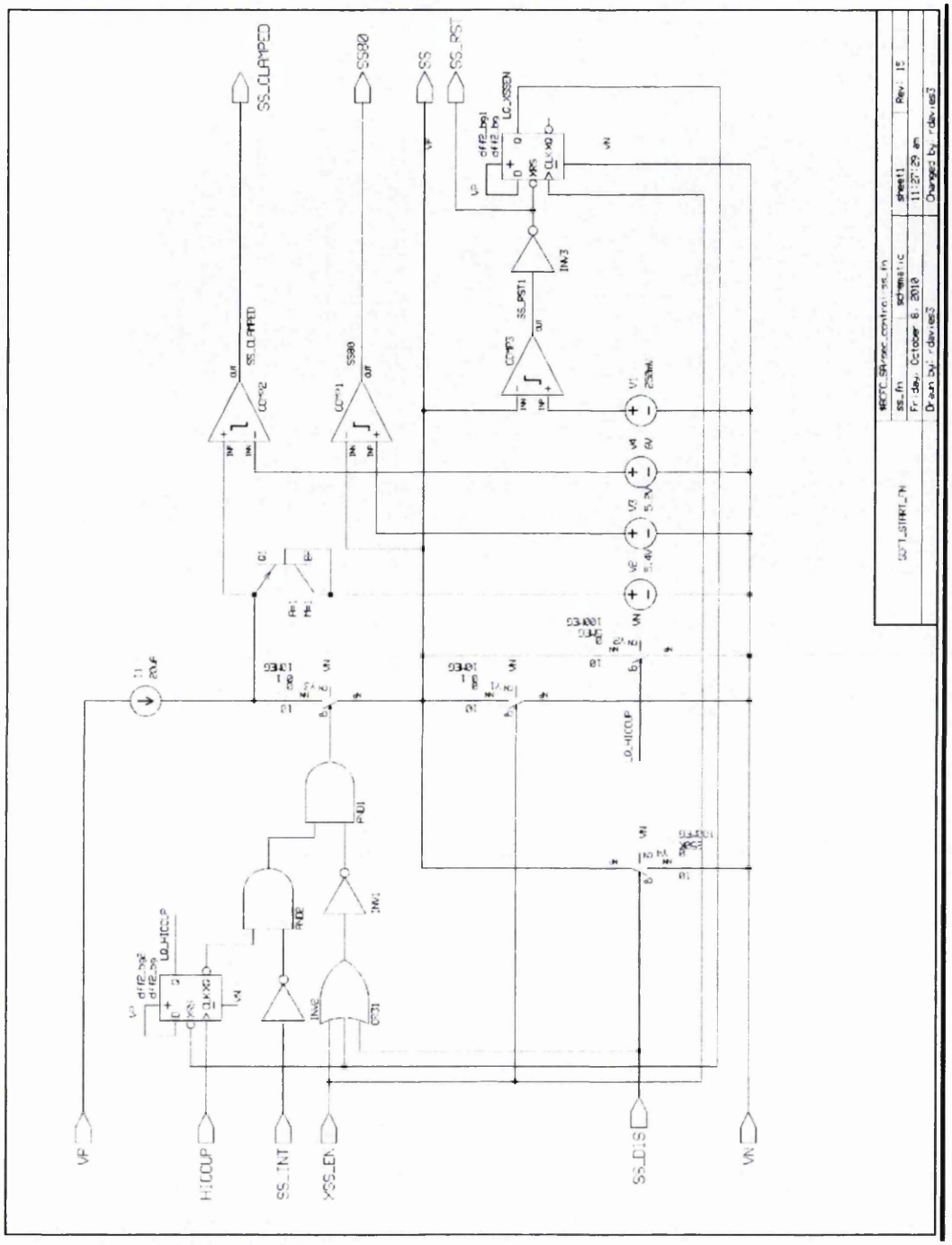


Fig 4.2.5 Soft Start Functional Circuit

high. The control circuit is designed such that after this event the output switching is disabled and the hiccup state entered. In the soft start circuit this results in the discharge rate of the SS pin reducing by a factor of twenty in order to achieve a suitable on to off ratio for the hiccup mode. The soft start circuit is designed to switch immediately into hiccup mode if the higher OCP detection level is exceeded. The input HICCUP clocks the latch turning off Y3 and turning on the discharge path Y2. This state is maintained until the SS pin has discharged to the 250mV level and comparator COMP3 switches and resets the hiccup latch via signal LQ_XSSEN.

PWM comparator

The pwm comparator circuit "pwm_fn" is shown in fig 4.2.6. This circuit converts the crossing point between the oscillator ramp input and the soft start input to a digital output via comparator COMP2. The input DRIVE_CONT inhibits output from PWM_OUT when primary side switching is stopped either from the primary side OCP or when control has been assumed by the secondary side control circuit.

Over Current Protection circuit

The OCP detection circuit "cs_fn" is shown in fig 4.2.7. This circuit represents the detection of the current in the primary side power components. This function is often achieved by using a ground referenced low value sense resistor. This method is the simplest but represents an efficiency loss hence the trade off of the low value and hence low detection voltage levels. The circuit shown provides dual level detection the 100mV level intended to represent the Imax level and to initiate a gradual response. The 150mV level therefore representing one and a half times Imax provides the immediate response. The input LE represents the inclusion of a leading edge blanking function to provide an internal rejection of the leading edge of the input signal to prevent false triggering of the OCP.

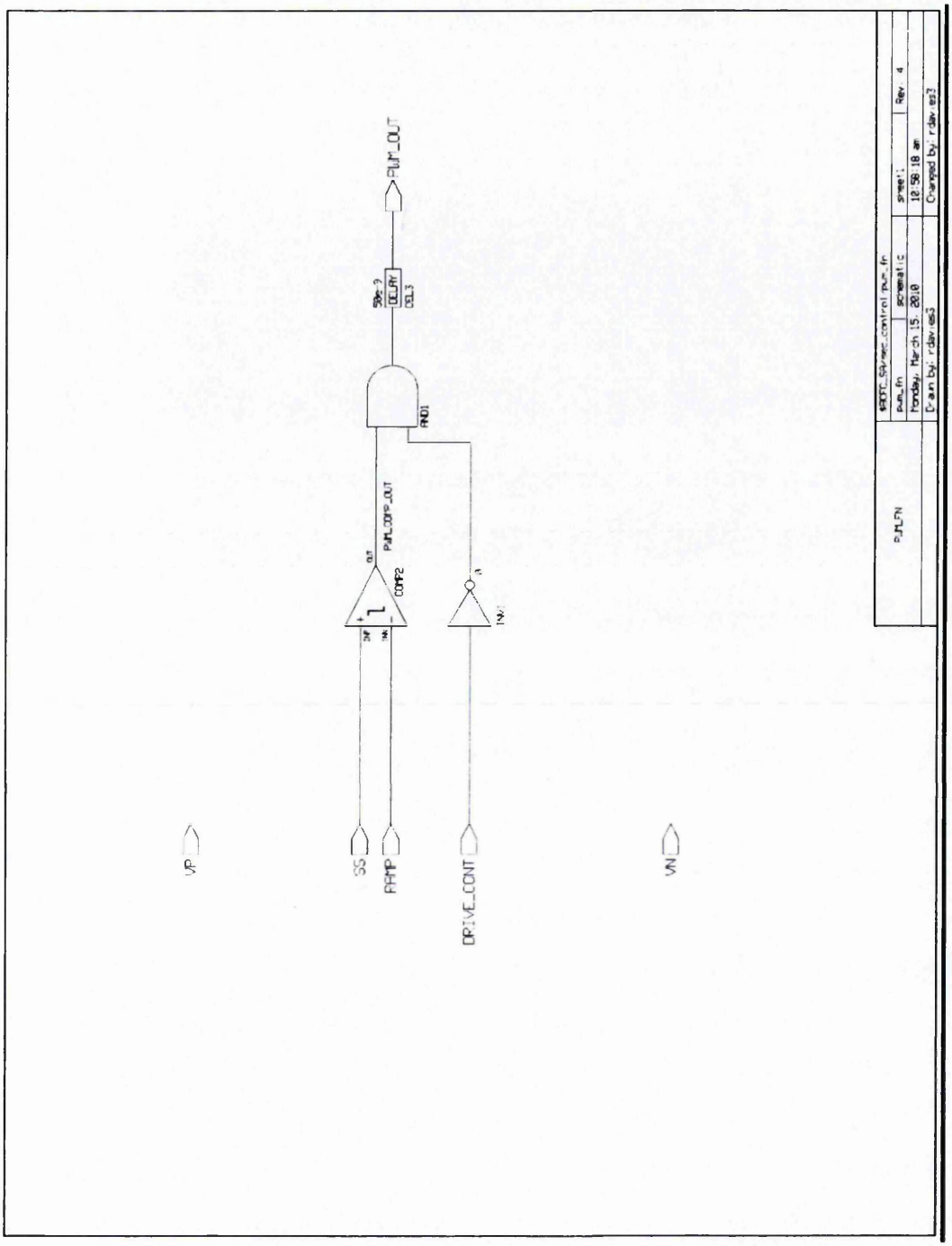


Fig 4.2.6 PWM Functional Circuit

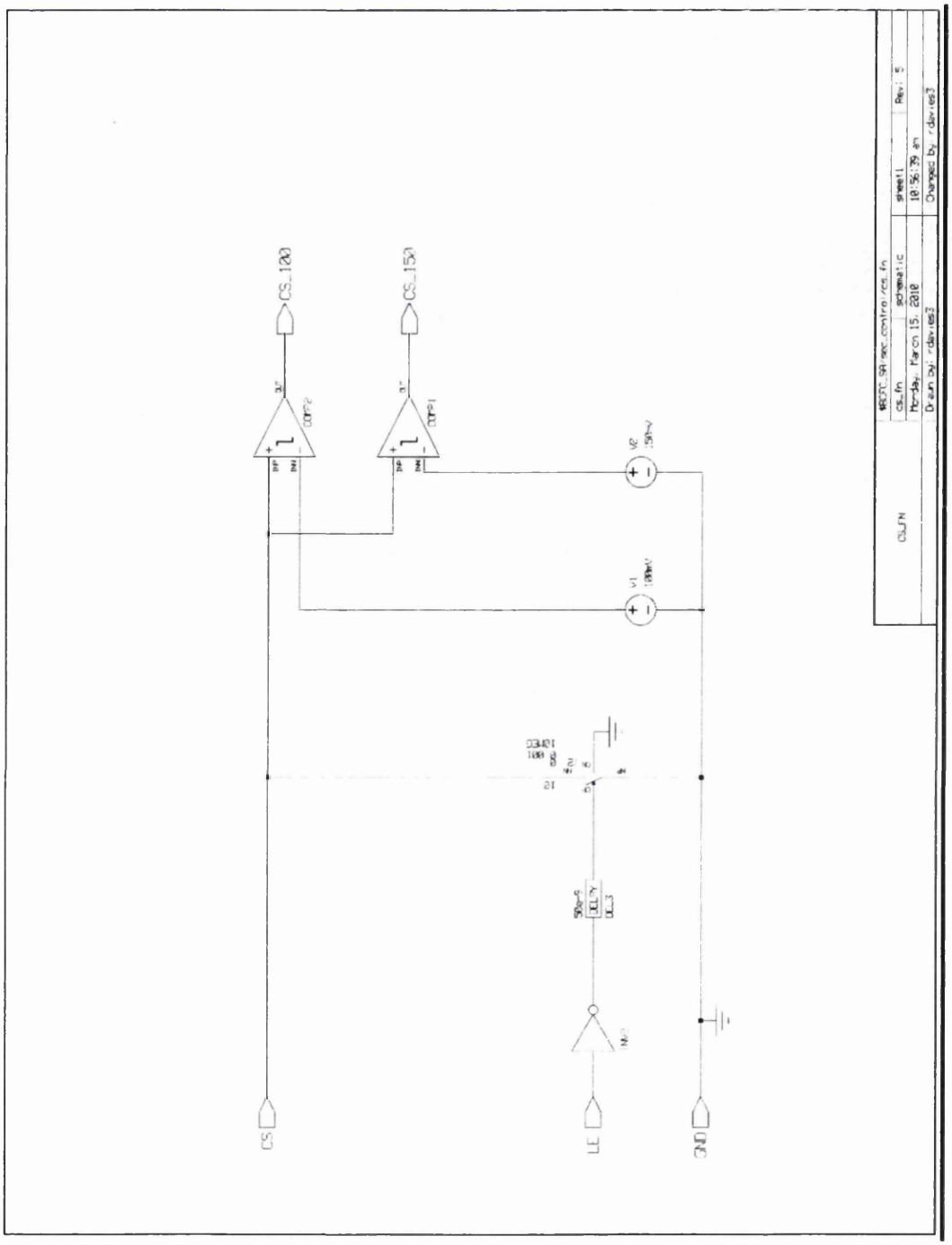


Fig 4.2.7 CS (OCP) Functional Circuit

High and low side driver circuits

The primary switch gate signals DL and DH do not require any specific drive capability due to the use of the ideal vcsw elements in the power train. The high side drive signal DH has a ground referenced input to the level shift transformer "tx_fn" . The output of this transformer is referenced to the LX node of the power transformer primary. The model for this function is shown in fig 4.2.8.

Control logic circuit

The control circuit block of the primary side "control_fn" is shown in fig 4.2.9. This circuit contains the logic design to implement the operation of the primary side device as outlined in the objective specification. The inputs UVLO_L, OTP and VUV represent the qualifying conditions for start up and when met result in gate and31 going high clocking dff2_bg2 output UP_SW high which starts the charging of the reference voltage VREF. When Vref has fully charged signal REF_RDY clocks dff2_bg3 latching the ref_rdy state high. The output of nand2 and signal DRIVE_CONT set output of or2, XSS_EN low. The drive_cont signal is initially reset low by the output of and31, this reset is released when the qualifying conditions are met allowing for dff2_bg4 to set drive_cont high on a rising edge of either input HI or LO via gate or1. The signal xss_en going low initiates the start of the soft start charging period and when signal SS enters the oscillator ramp rang input pulses begin on input PWM_IN. The PWM data is gated alternately to the low and high side drive outputs via the toggle circuit tff2_bg1. Signals tog_q and tog_xq gate the pwm input via an3_bg1 and an3_bg2. Activity on inputs HI and LO represent control of the primary side drive being taken over from the secondary side via the x_drive_control input to and9 going low and therefore isolating the DH,DL outputs from the pwm input. The drive to the DH,DL outputs then coming via and1, and2.The clock signal to tff2_bg1 is derived from the oscillator circuit and occurs at the peak of the oscillator ramp waveform. The clk input is also used to reset via nand5, dff2_bg8 and via and8 dff2_bg7. These latch circuits are therefore reset each oscillator cycle provided the other inputs to the and gates are met. The latch circuit dff2_bg8 sets output SS_INT high on the rising edge of input CS_100 the effect of ss_int in the soft start circuit is

to interrupt the charging of the SS pin for the remaining duration of the oscillator period and the next cycle. This action results in the interrupted duty cycle remaining constant between alternate high and low on periods and therefore avoiding introducing a volt second imbalance at the transformer. Note that for a half bridge the over current detection is on the low side only for ease of implementation therefore the information obtained has to be carried over to the next high side period to maintain flux balance in the transformer. The effect of this interrupt function is to reduce the charge rate of the soft start capacitor for the duration of the over current and therefore to help the converter to start into a fully discharged output capacitance without damage to the power train components.

The input SS_CLAMPED on switching high is latched by dff2_bg6. This state is held by the latch until reset by input SS_RST. An input high on SS_100 will now via and6 clock dff2_bg7 switching output SS_DIS high. This signal to the soft start circuit switches in the discharge path vcsw Y4 reducing the pwm D via the voltage on the SS pin. This function is reset each alternate cycle as for the interrupt function and if repeated continuously such that the SS pin is discharged below the SS80 level then input SS80 will clock dff2_bg9. The output of this latch clocks dff2_bg5 setting output HICCUP high. The hiccup signal being high will immediately stop output switching via gate and9, and in the soft start circuit will switch the discharge of the SS pin to the reduced rate defined by vcsw Y2 and maintain this state until fully discharged and reset by the signal LO_XSSEN as described in the soft start circuit description. Hiccup operation starts immediately input CS_150 goes high and repeated charge and discharge of the SS pin occurs for the duration of over current detection.

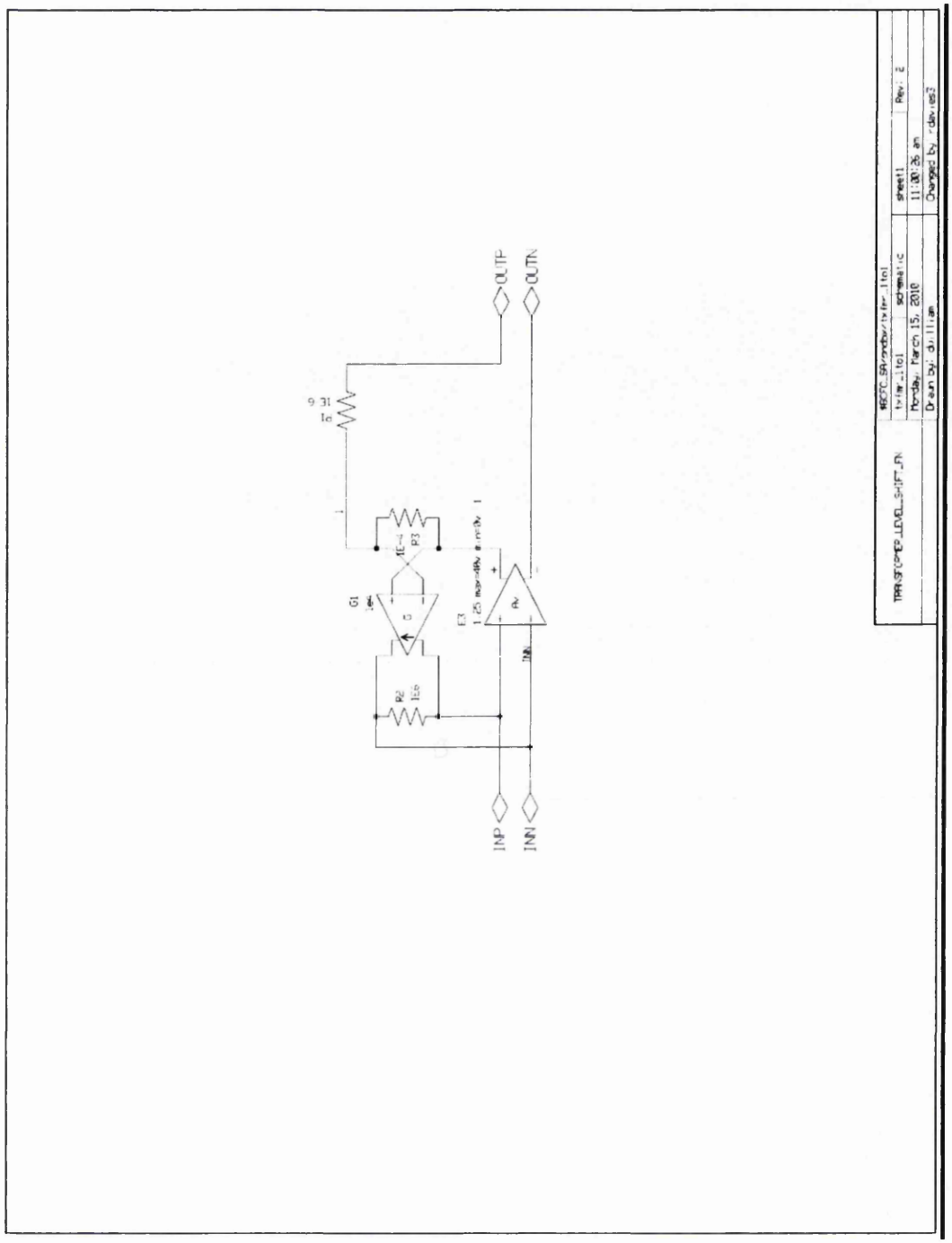


Fig 4.2.8 Transformer Functional Circuit

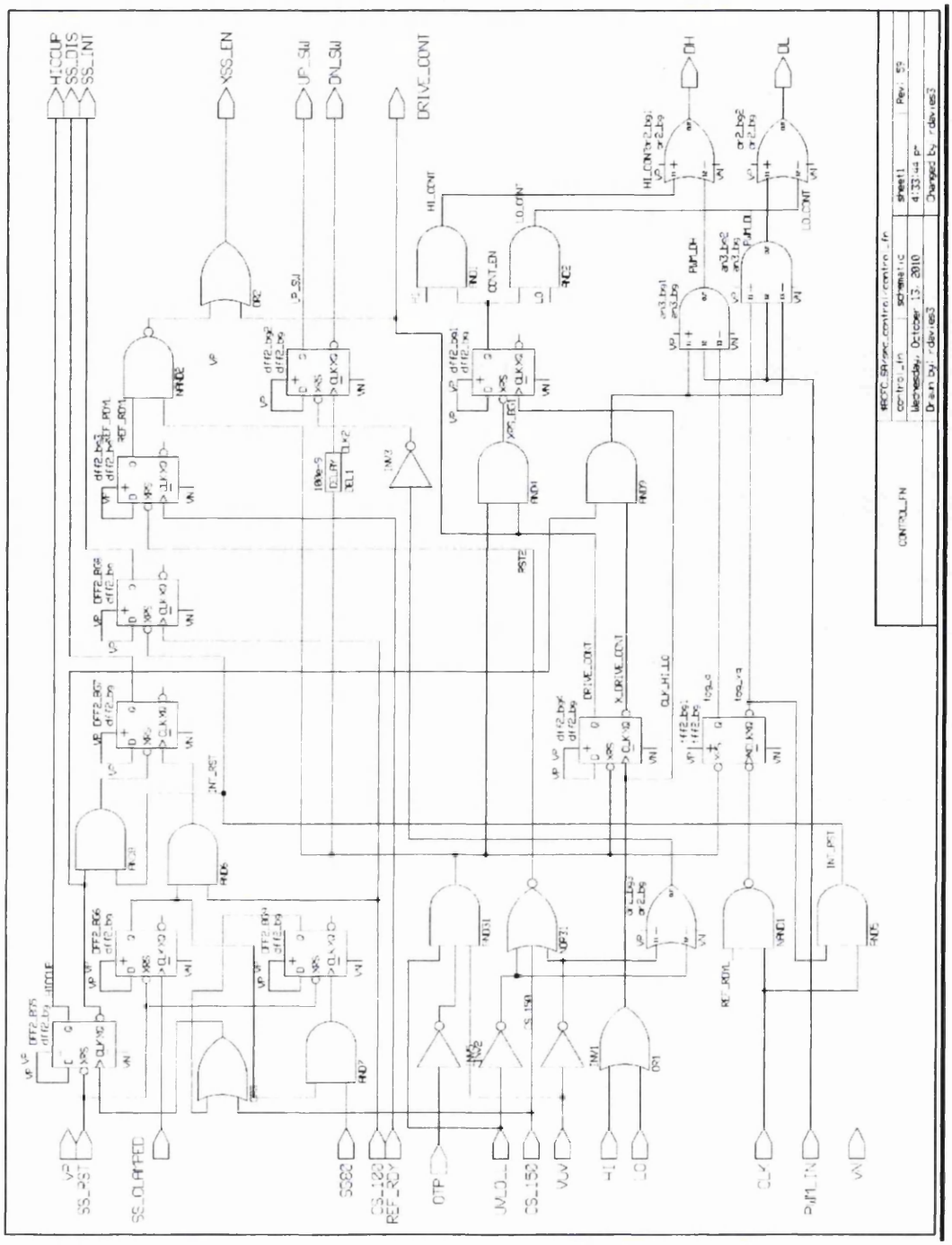


Fig 4.2.9 Control Functional Circuit

4.3 Secondary Side Controller Functional Circuit

The secondary side control circuit "sec_cont_cct_ver2" is shown in fig 4.3 and contains the following function blocks.

1. Pre regulator
2. Reference circuit
3. Oscillator
4. Soft start circuit
5. Pwm Comparator circuit
6. Over current protection circuit
7. Secondary Over Current control circuit
8. Primary side drive circuit
9. Synchronous rectifier drive circuit
10. Pwm Generator circuit
11. Serial Bus Interface
12. Over voltage protection circuit
13. Delay generator circuit.

A major consideration in integrated circuit design is the ability to re use known good circuit design including where possible the physical layout of such circuits. The starting point for achieving this design efficiency is if possible effective system partitioning i.e. if the function requirements of the system allow for the location of circuits with compatible supply voltage ranges such that circuit requirements can be achieved on a common silicon process. In the context of this design, the primary side device requires high voltage devices available for the pre regulator function and the high side drive circuit, other than that the circuitry is effectively twelve volt ground referenced. In this context a significant number of primary side circuit blocks will be compatible between the primary side controller and the secondary side. These circuit blocks include:-

1. Pre-regulator circuit
2. Reference circuit
3. Oscillator
4. Soft start circuit
5. Over current protection circuit

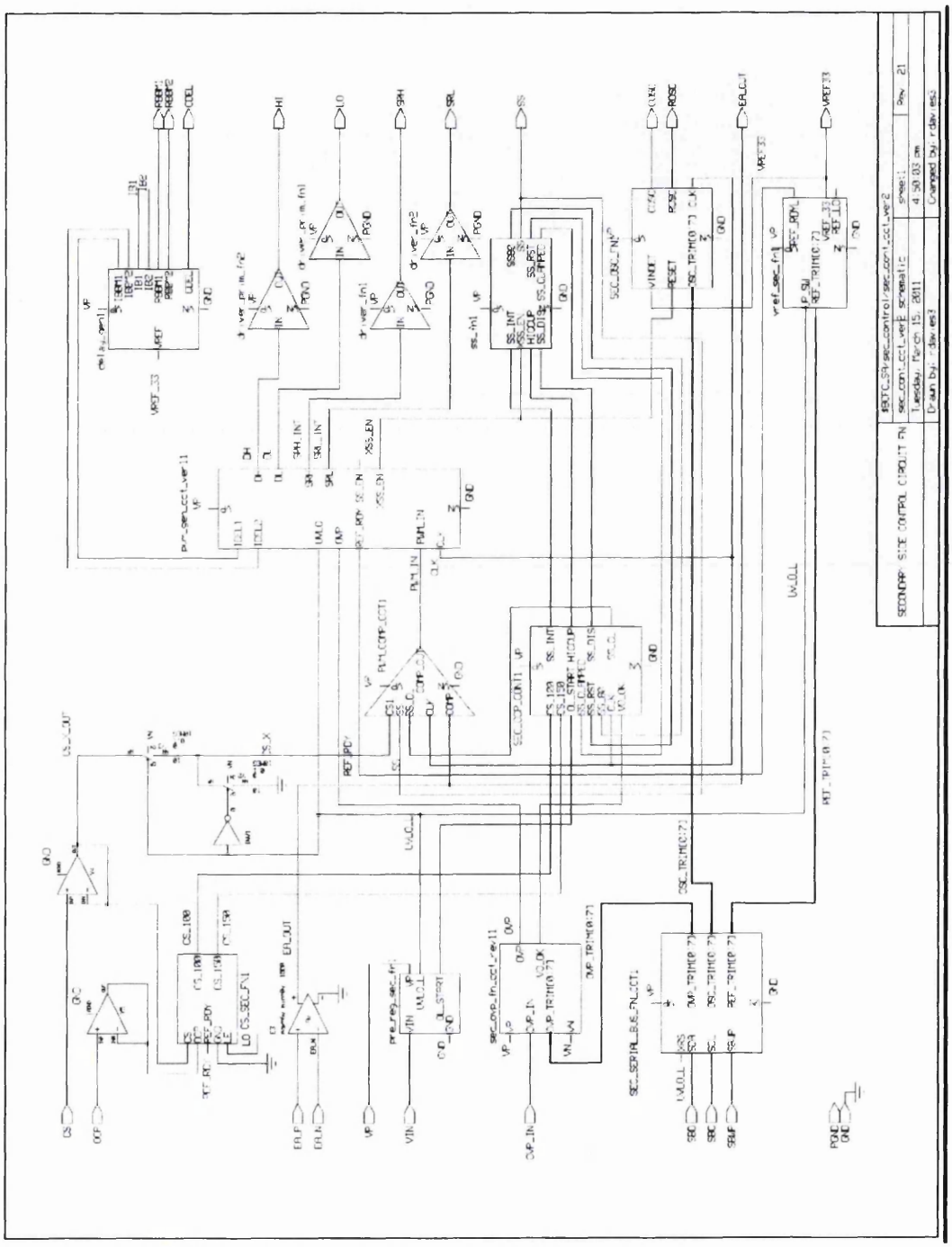


Fig 4.3 Secondary Side Controller Functional Circuit

Particularly at the functional level these circuits are as for the primary side controller and descriptions of operation are therefore not repeated here other than to explain the provision for parameter trimming via the serial PMbus these include the oscillator and reference circuit shown in Figs 4.3.1, Fig 4.3.2, Fig 4.3.2a and initial control of the soft start circuit via the pre regulator and the OCP circuit Fig 4.3.3, Fig 4.3.4, Fig 4.3.5 respectively.

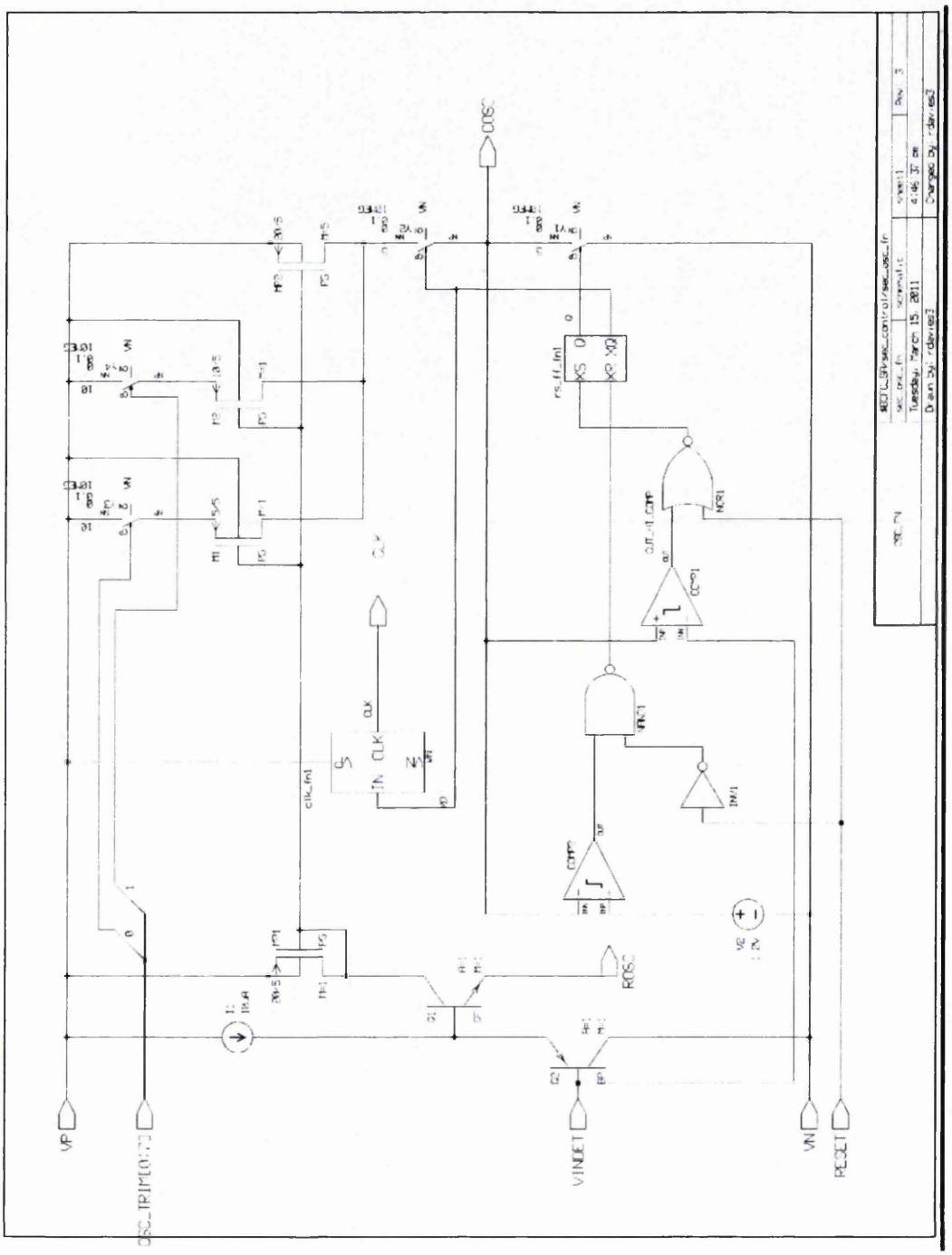


Fig 4.3.1 Secondary Side Oscillator Functional Circuit

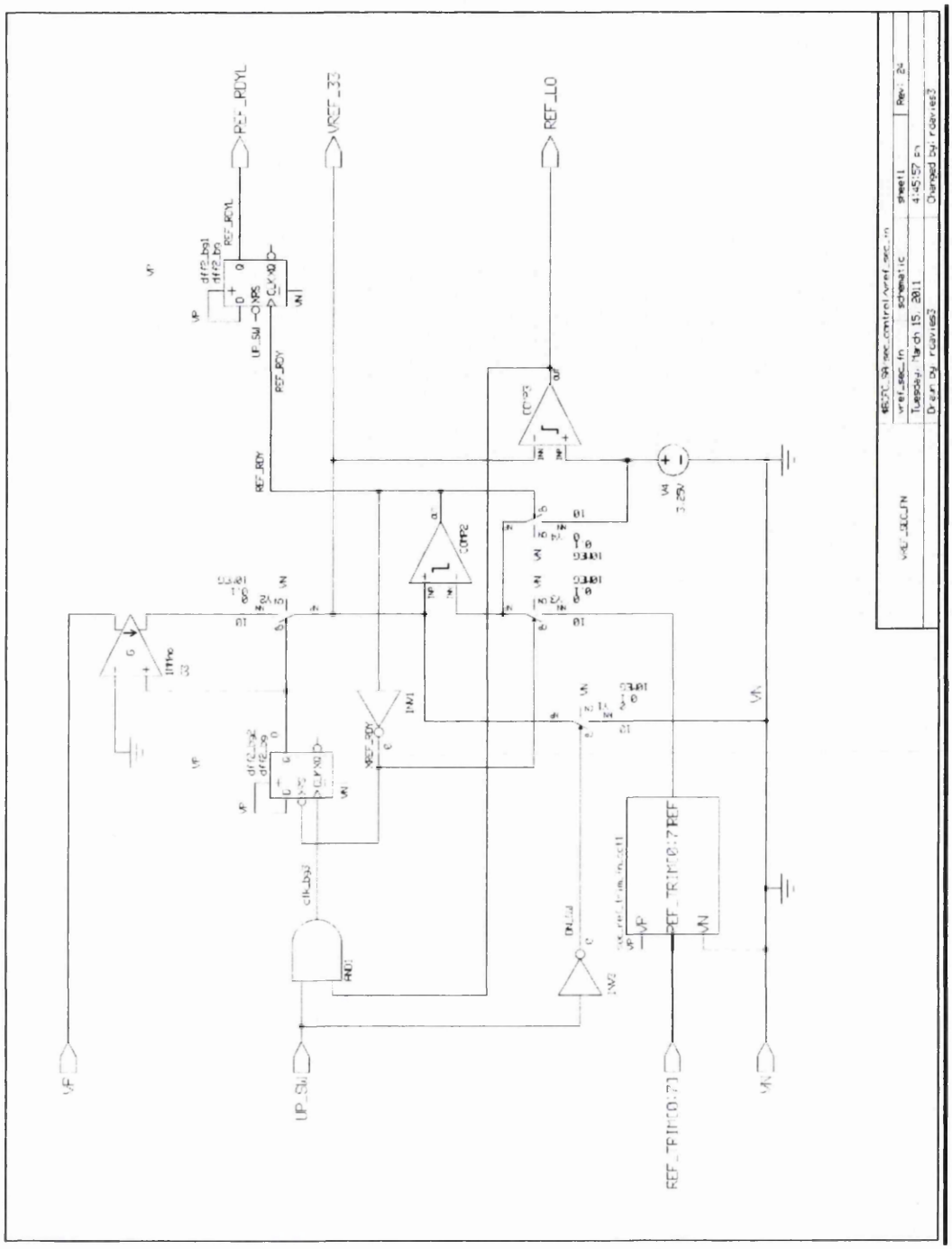


Fig 4.3.2 Secondary Side Reference Voltage Function

In the functional schematic of Fig 4.3.2 the reference trimming capability is via bus "ref_trim[0:7]" and changes the reference voltage for comparator "comp2" in circuit block "sec_ref_trim_fn_cct" Fig4.3.2a by digital decoding of four trim bits used and

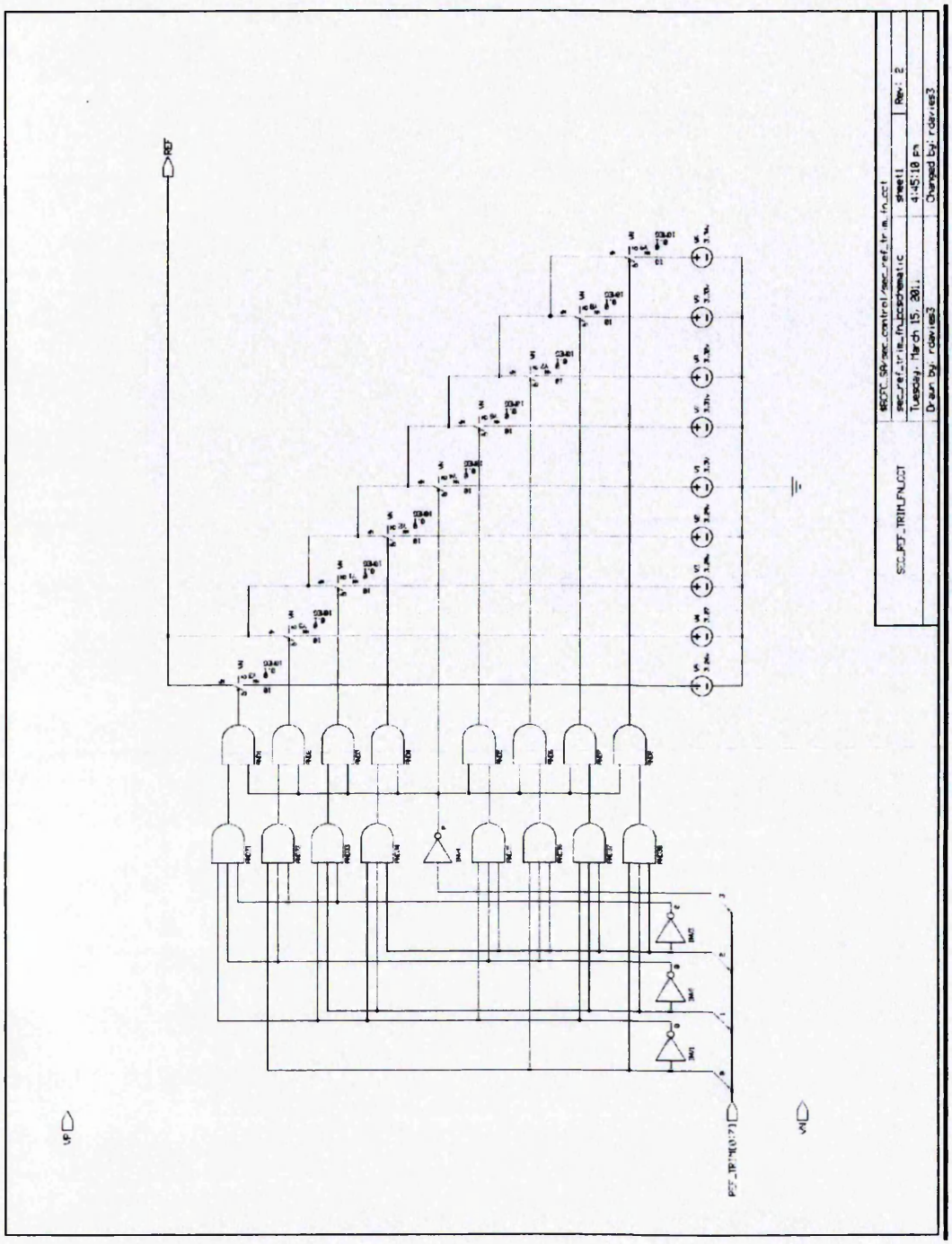


Fig 4.3.2.1 Secondary Side Reference Trim Circuit

selection of the programmed reference voltage. In the device level design this would be achieved by the use of analogue switch circuits to short sections of a matched resistor array to adjust the resistance in the band gap cell and also change the feedback gain in the output amplifier stage of the reference voltage block.

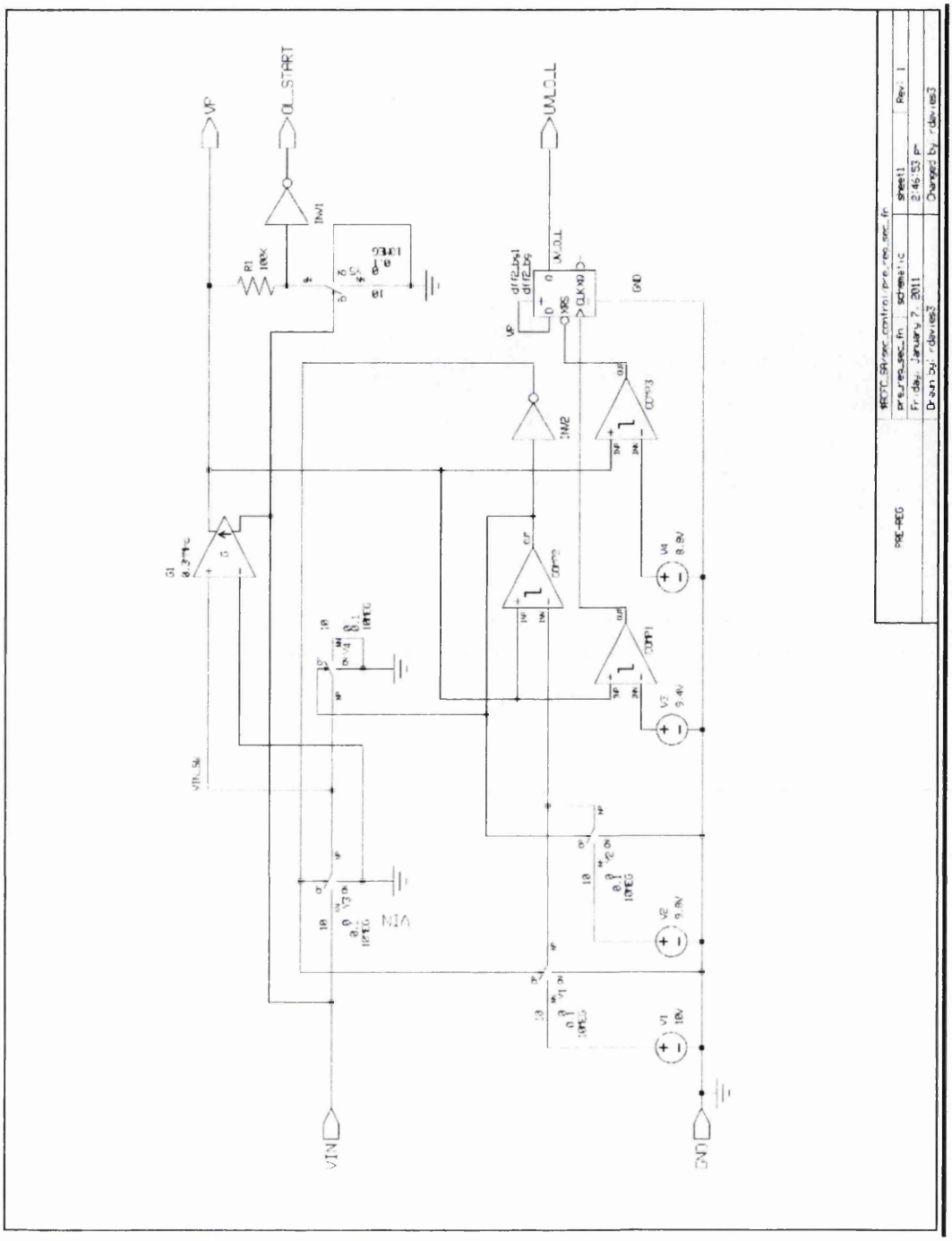


Fig 4.3.3 Secondary Side Pre Regulator Function

The pre regulator circuit has the additional provision for VIN voltage detection. This function provides the information to the soft start circuit to define open loop start up as indicated by output "OL_START" and therefore initially disabling soft start operation via the "SS_CL" signal out of the "sec_ocp_cont" block. The absence of a

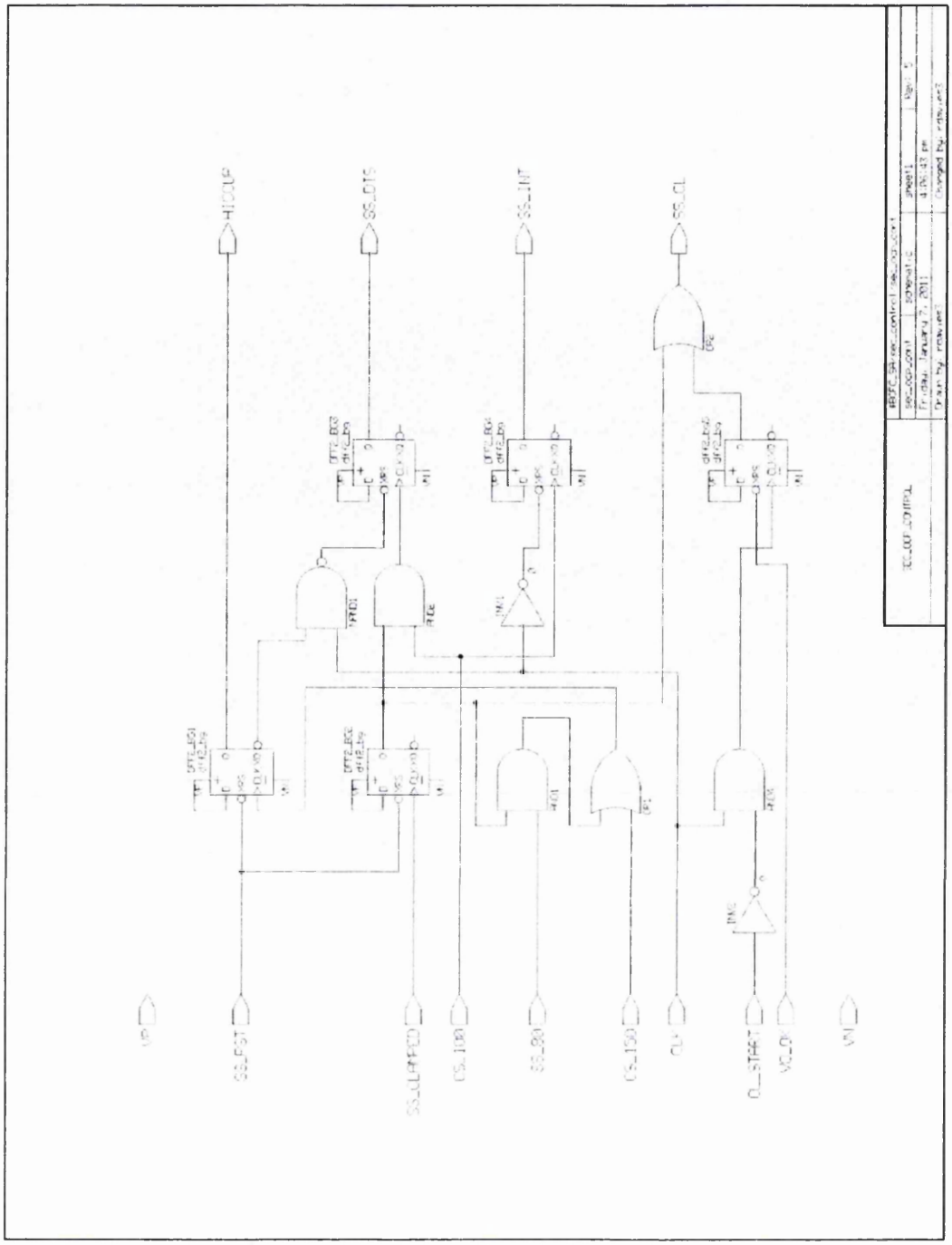


Fig 4.3.4 Secondary Side OCP Control Circuit

voltage on the Vin pin will therefore imply start up via an auxiliary supply to the VP pin and enable the soft start function immediately. Logic control of this function is located in circuit "sec_ocp_cont" Fig 4.3.4. The function is reset by input "VO_OK" when converter output voltage is detected to be approaching its final value, signal "SS_CL" is then under over current protection control only.

The remaining functional circuit block operation specific to the secondary side requirements are described in the following schematics and text.

Secondary Over Current Control Circuit

The circuit "sec_ocp_cont" is shown in Fig 4.3.4.This circuit block contains logic functions associated with the dual level over current protection. If the over current detection threshold is exceeded input "CS_100" can clock dff2_bg4 output "SS_INT" high. This signal interrupts the soft start charge during the remaining oscillator period and is reset on the leading edge of the next "CLK"pulse. This action has the effect of softening the soft start period. The input "SS_CLAMPED" clocks ddff2_bg2 high when the soft start function has reached its final value, this enables via "and2" input "CS_100" and via "and1" input "SS_80". If the over current detection threshold is exceeded input "CS_100" goes high clocking dff2_bg3 output "SS_DIS". This signal causes the discharge of the soft start pin for the remainder of the oscillator period, repeated action results in the soft start pin being discharged below the "SS_80" level. When this occurs any further input on "SS_100" triggers a "HICCUP" cycle via and1, or1 and dff2_bg1. The hiccup function is not reset until the soft start pin has been discharged to its lower threshold and input "SS_RST" has gone low resetting dff2_bg1. The hiccup function is enabled at any time for an over current of 1.5times the OCP threshold via input "CS_150". The output "SS_CL" is associated with the soft start clamped state and preventing the initial operation of the soft start function for primary side start up.

Pwm Comparator Circuit

The circuit "pwm_comp_cct" is shown in Fig 4.3.5. This circuit illustrates the requirements of a PWM comparator for current mode control over that of the simpler function required on the primary side. The comparator reference level COMP_P is defined by whichever of inputs "SS" or "COMP" is at the lowest voltage via the wire OR connection of Q2 and Q6. Bias currents are simply set by R2 and MP2 – MP6.

The input "SS" is initially switched to VP via vcsw y1 and y2 if there is pre regulator detection of primary side start up leaving input "COMP" only to determine

the comparator reference level. For secondary side start up the "SS" input has duty cycle control until the soft start pin has reached the clamp voltage indicated by signal "SS_CLAMP". The "SS" input is again switched to VP via vcsw y1 and y2 .
The CS1 input represents the current ramp in the converter power path and drives the input COMP_N via Q4. On exceeding the COMP_P voltage level the comparator output COMP_OUT switches low ending the PWM on period and clocks dff2_bg1 via OR1 output XQ switches input CS1 to VP via MP8 and MN2 ensuring that a reversal of the comparator switching cannot occur until the leading edge of the CLK input when the latch is reset via INV1.This action releases input "CS1" for the next cycle. Output "COMP_OUT" is therefore a square wave into "pwm_gen_cct_ver1".

Pwm Generator Circuit

The circuit "pwm_gen_cct_ver1" is shown in Fig 4.3.6 and provides the remaining functions required for start up, BBM and PWM control. Output switching is inhibited until all qualifiers are met to allow for successful operation. These include "UVLO", "OVP" and "REF_RDY". The reference voltage generator is released to power up once the under voltage lock out level has been exceeded by the VP voltage. Once the reference voltage is close to its' final value the oscillator is enabled by signal "XSS_EN" to generate a sawtooth waveform [43] on pin "COSC" and a positive clock pulses on input "CLK". With the qualifiers met the output of and31 is high enabling nand1, dff2_bg4 is reset on the rising edge of "CLK" setting "BBM_ST" high and "XBBM_ST" low via inv7. The first "CLK" signal following the output of and31 going high has clocked dff2_bg1 setting "TOG_XRS" high releasing the toggle function tff2_bg1 to toggle outputs "TOG_Q" and "TOG_XQ" on each positive edge of "CLK" via inv10, inv11, and inv9. The BBM delay circuit "bbm_blk1", Fig 4.3.7 switches output "CAP1" low without delay resulting in a low output at "COMP1" clocking dff2_bg2 via inv8. Signal "SS_LO" enables and2 and and1, the complimentary output of dff2_bg going low enables gates nor1 and nor2. The output of tff2_bg1 is reset until the second clock pulse and therefore selects drive path and1, nand4, nand10. The output "SRL" is turned off without delay, output "DL" turns on after the delay at node "CAP2". Output "SRH" is on as the complimentary output of dff2_bg2 and the output of nand1 are low due to "TOG_Q" low. Output "DH" is high via nand2 and inv1.

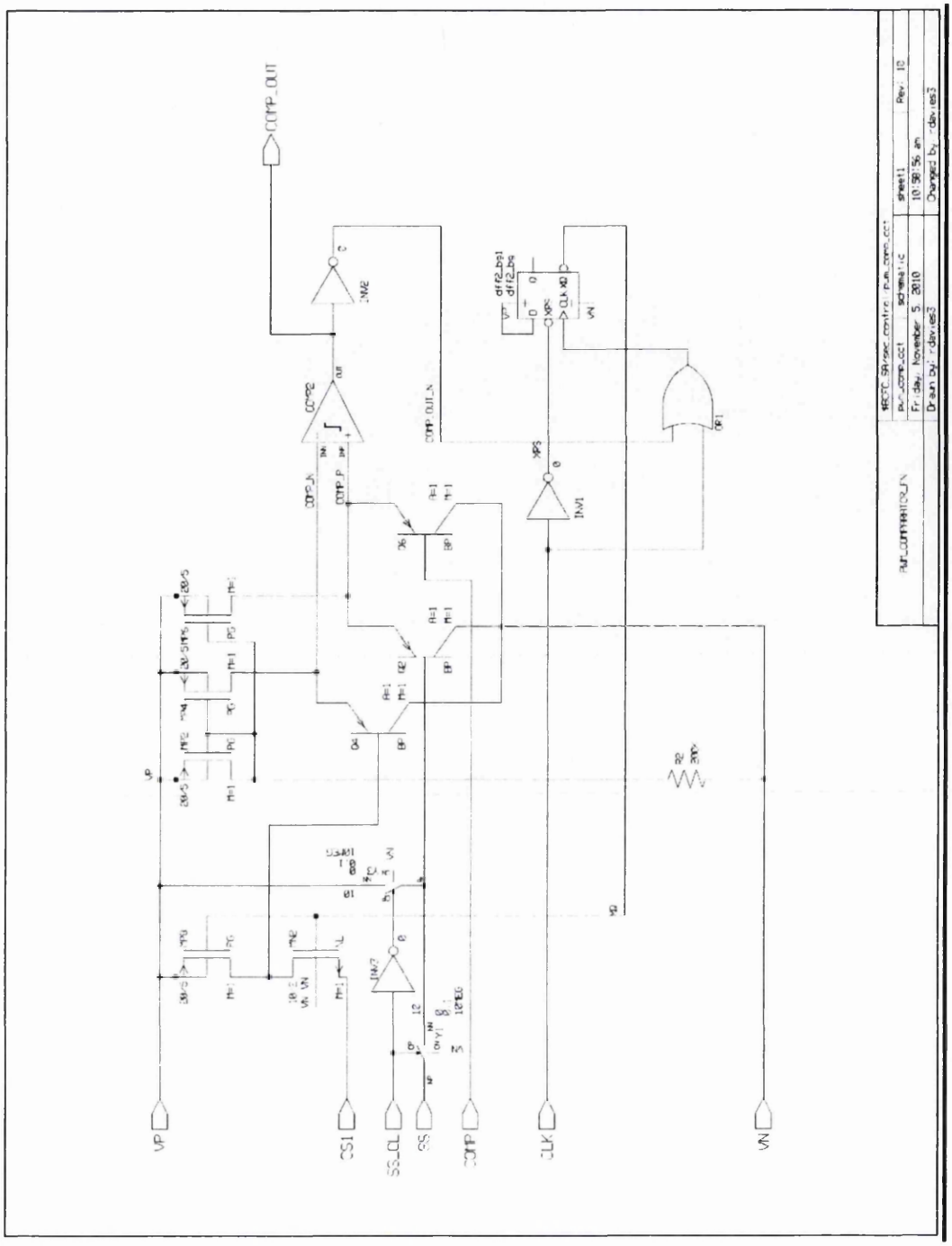


Fig 4.3.5 Secondary Side PWM Comparator Circuit

The falling edge of "PWM_IN" clocks dff2_bg4 setting "BBM_ST" low, "XBBM_ST" high resulting in a fast turn off of "CAP2" and a slow charge of "CAP1" turning "DL" off and "SRL" on after the defined delay.0The next "CLK" input resets dff2_bg4 on the positive going edge and therefore sets "BBM_ST" high "XBBM_ST" low and toggles dff2_bg1 selecting the "DH", "SLH" outputs.

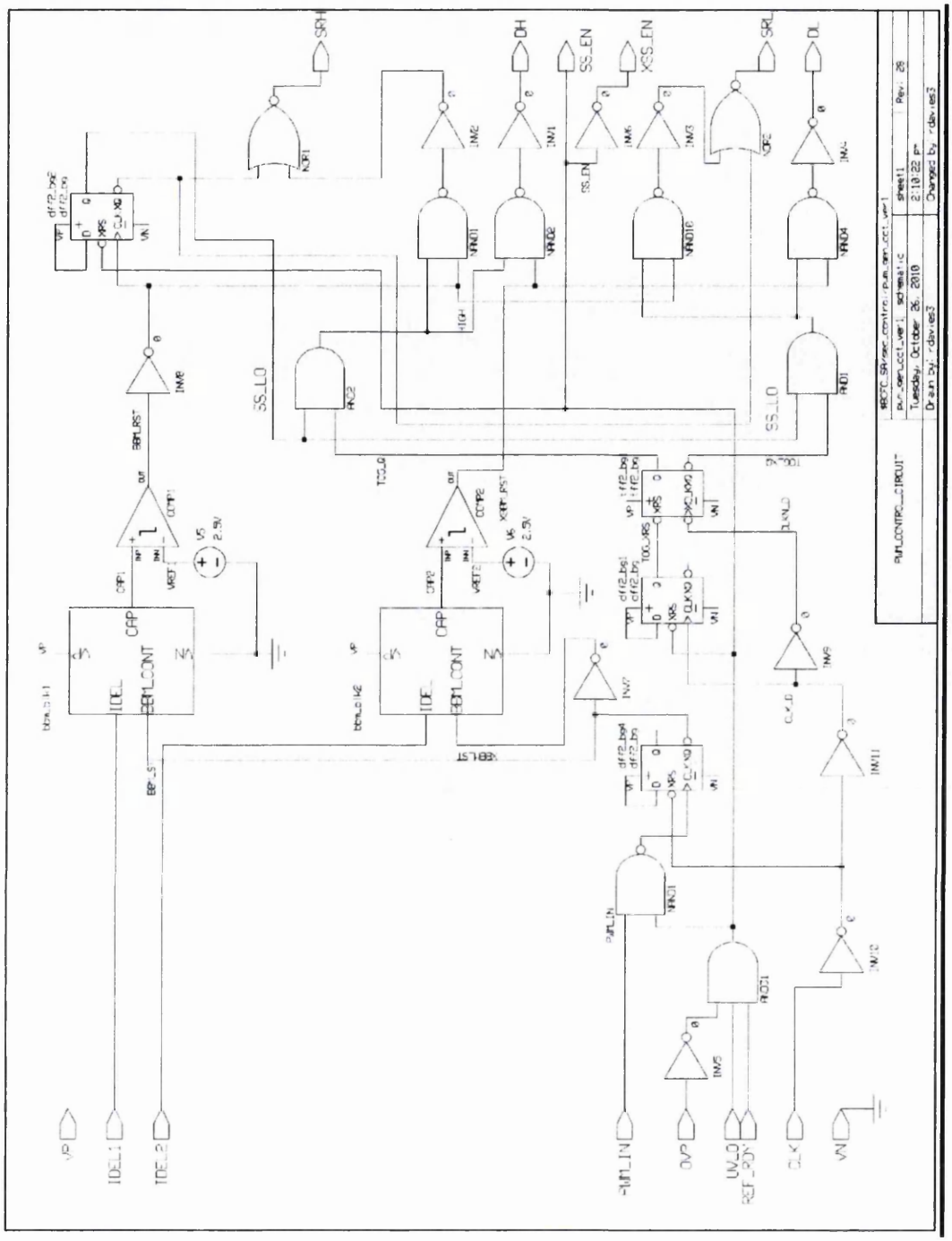


Fig 4.3.6 Secondary Side PWM Control Circuit

The delay times are defined in the "bbm_blk" circuits by the charging currents, the capacitance on the charge node and the comparator reference voltage. The charging currents are defined by the reference voltage and external resistors in "delay_gen".

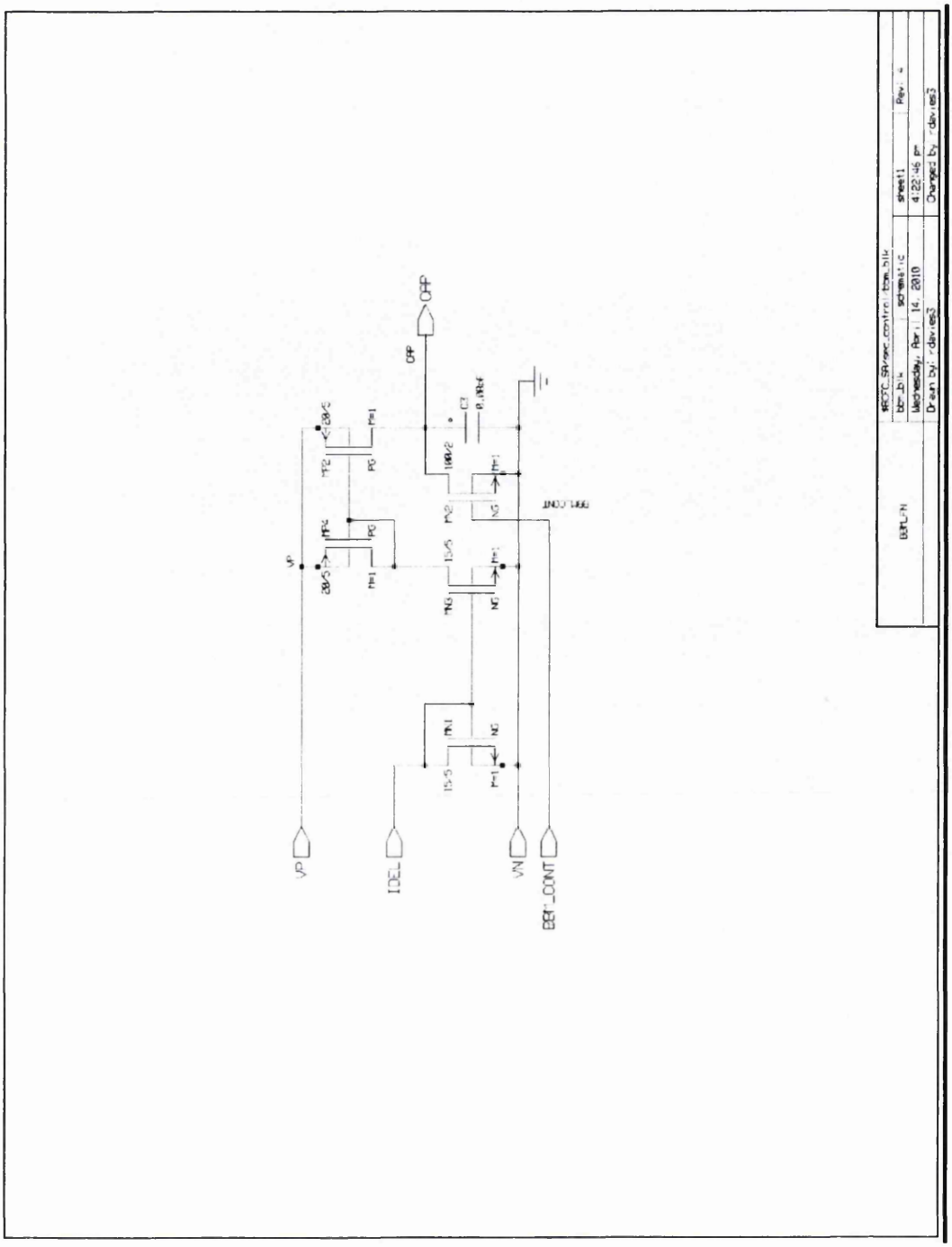


Fig 4.3.7 Secondary Side BBM Delay Circuit

Delay Generator Circuit

The circuit "delay_generator_circuit" is shown in Fig 3.4.8. The output current "IBBM1" defines the delay to the ongoing edge of the primary drives "DH", "DL". The current defined from "VREF" via Q7,Q8,Q5,Q6 applied to an external resistance

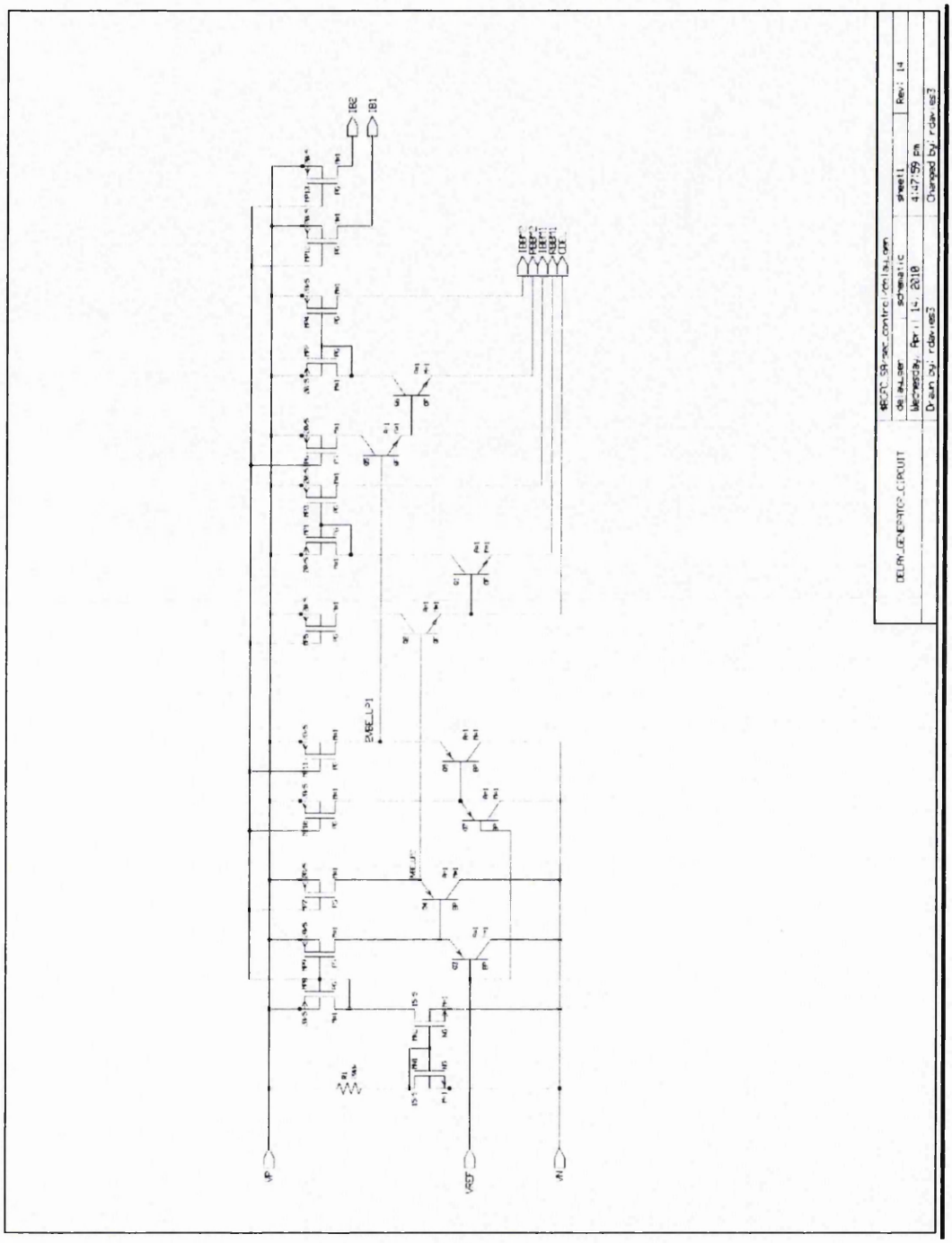


Fig 4.3.8 Secondary Side BBM Delay Current Generator Circuit

connected at pin "RBBM1"and is mirrored via mp2 to mp4 [45]. The delay to the ongoing edge of the secondary drives is defined by current sourced from output "IBBM2". This Current is defined from "VREF" via Q3,Q4, Q2,Q1 applied to an external resistance connected at pin "RBBM2". In this instance an external capacitance connected at pin "CDEL" results in a slow rise to the voltage applied at "RBBM2" due to the limited charge rate to "CDEL" from current source MP5. This has the effect of having the delay to the ongoing edge of the secondary drives extend out beyond the oscillator period and to slowly reduce providing a soft start to the secondary side synchronous rectifier drives.

Primary and Secondary Side Drive Circuits

The driver circuit is shown in Fig 4.3.9. At the functional level the difference between the primary and secondary driver circuits amounts to only the value of resistance included in the output stage. In the case of a secondary side controller the secondary side synchronous rectifier drives SRH, SRL require greater current drive capability than that of the primary outputs DH, DL which essentially only convey timing information. The drivers are non inverting with the drive paths cross connected to ensure no operational overlap of the pull up and pull down drives occurs. At device level design this is essential as the current capability of the output stages is specified in amps and if this level of current is allowed to "shoot through" device damage is likely.

Over Voltage Protection Circuit

The circuit "Sec_Ovp_Fn" is shown in Fig 4.3.10. The circuit contains comparators "COMP1" and "COMP2" . The comparator "COMP1" has its reference voltage selected via serial bus "OVP_TRIM" illustrating an application of the PMbus where the load equipment is able to interface with its power supply operation and in this instance adjust the threshold of overvoltage protection applied to its supply. The secondary side control device is specified with a separate "OVP" pin as this separation eliminates the possibility of losing overvoltage protection of the output voltage with loss of voltage control loop operation. As for the reference voltage trimming at device level design trimming of the threshold for OVP operation would be achieved by switching in or out matched resistors [46] or arrays of resistors to

achieve the required threshold value. The comparator "COMP2" is included in this circuit block to provide the knowledge of the converter output voltage approaching final value for use by the OCP function in defining required OCP response.

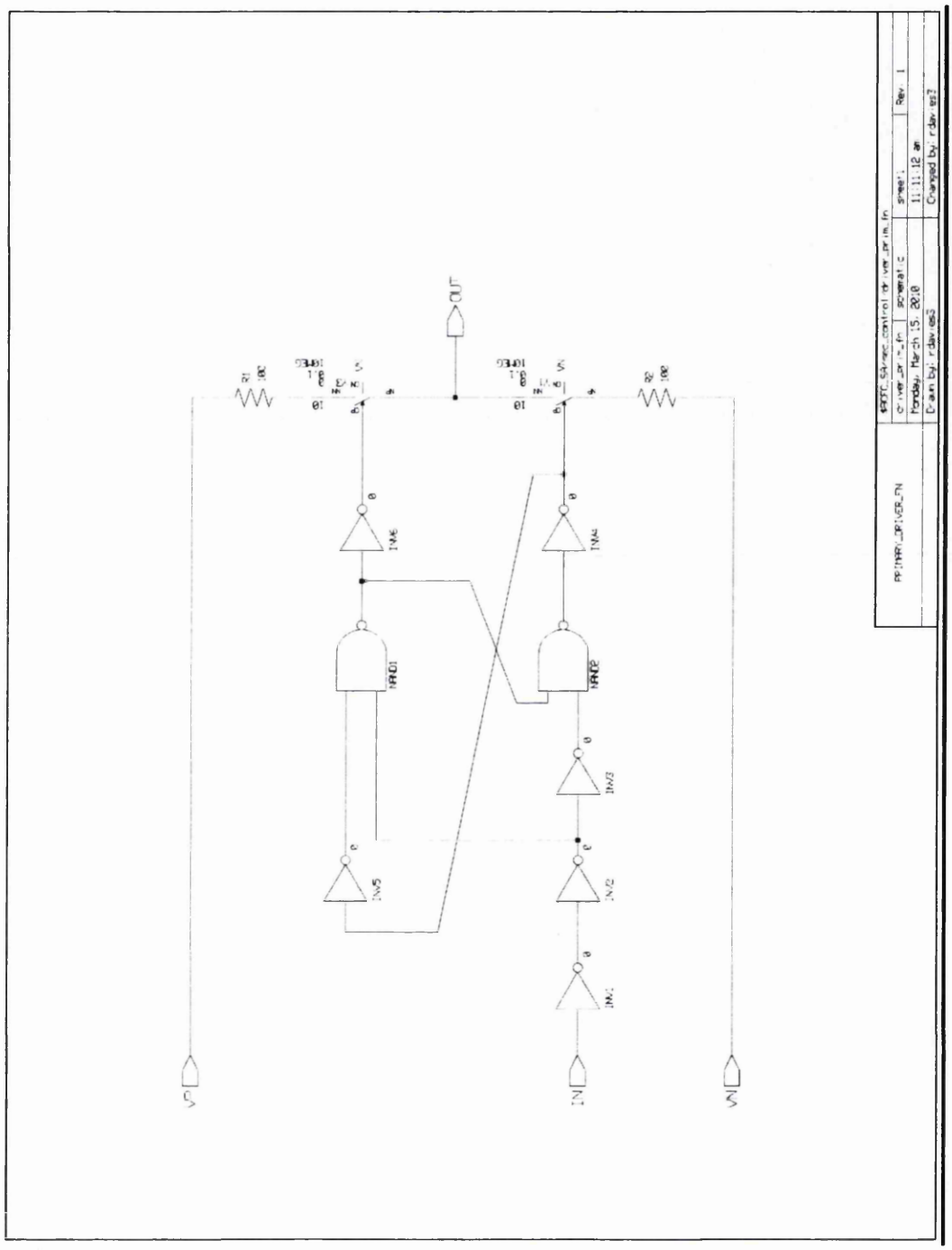


Fig 4.3.9 Secondary Side Primary Driver Functional Circuit

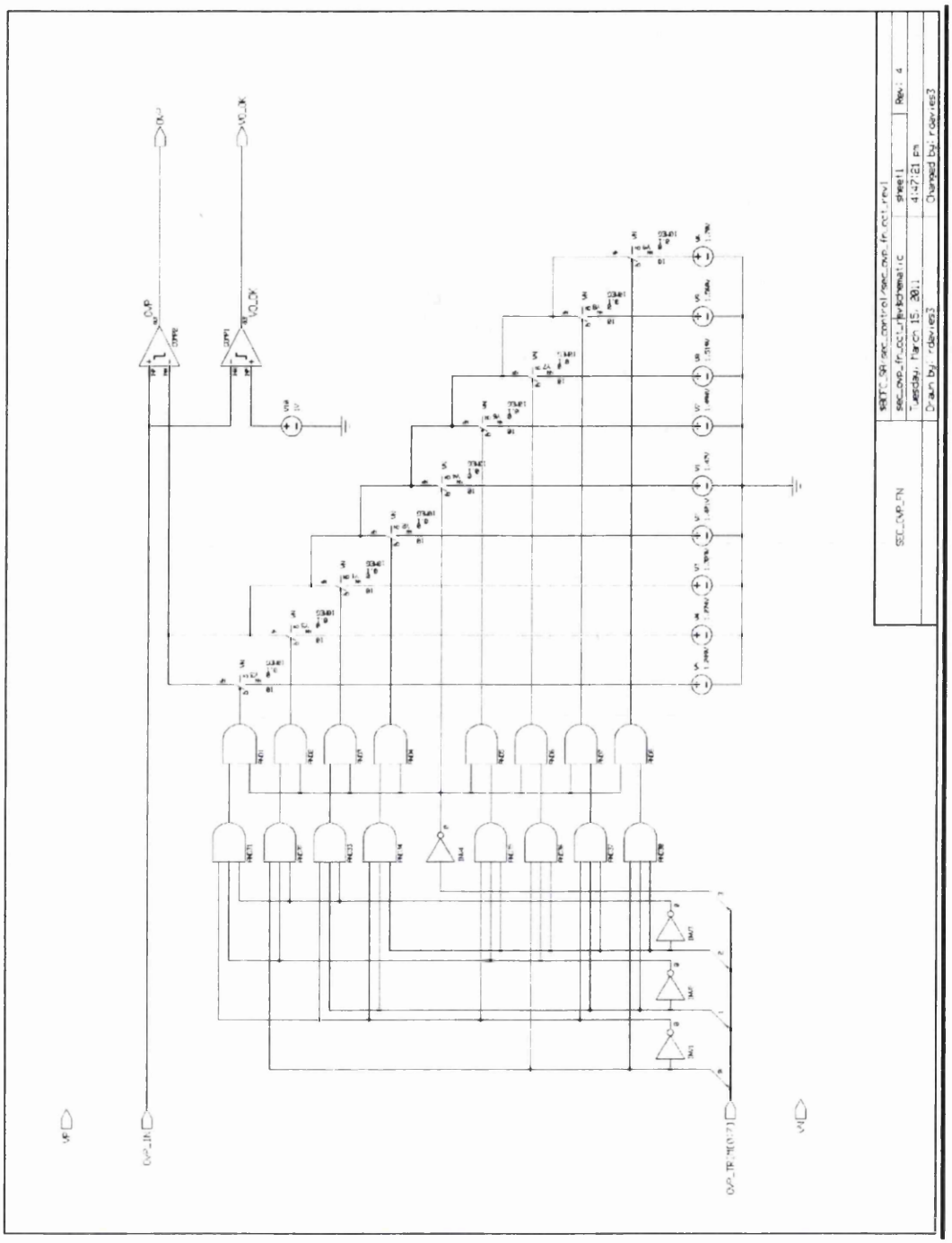


Fig 4.3.10 Secondary Side OVP Functional Circuit

PMbus

The PMBus interface is represented at functional level by "sec_serial_bus_fn_cct" and is shown in Fig 4.3.11 and Fig 4.3.12. This interface is a "slave receiver" in that it only allows the system to send serial data to adjust operating parameters as described previously. The system proposed for this secondary side controller is also that for a single device i.e. physical address pins as proposed in [47] are not included as this would compromise the pin count – package size requirement for minimising the component foot print. The trim data is therefore required to be downloaded by the system and will remain valid for as long as the secondary side controller has a power supply above UVLO level. The functional circuit implementation therefore comprises a three byte size SIPO shift registers. The data is latched to the parallel registers on completion of the clock count. In a device level implementation account would have to be taken of the packet structure proposed on page 30 of reference [47] to ignore address and command byte data or to implement a means of address programming as suggested on page 32 of reference [47]. A bidirectional bus implementation is also a possibility for system interrogation of the power supply setting. The degree of implementation of these functions will be dominated by the cost to value calculations for inclusion of these functions on Silicon. The operation of the functional circuits shown is simply to clock in data from the SDA input and to count clock cycles in circuit "bit_count_fn_cct" Fig 4.3.13, latching the data to the respective output bus for all three shift registers on reaching the twenty fourth clock count. Using this method change to trim data would therefore have to be entirely reloaded each time a change to any parameter was required.

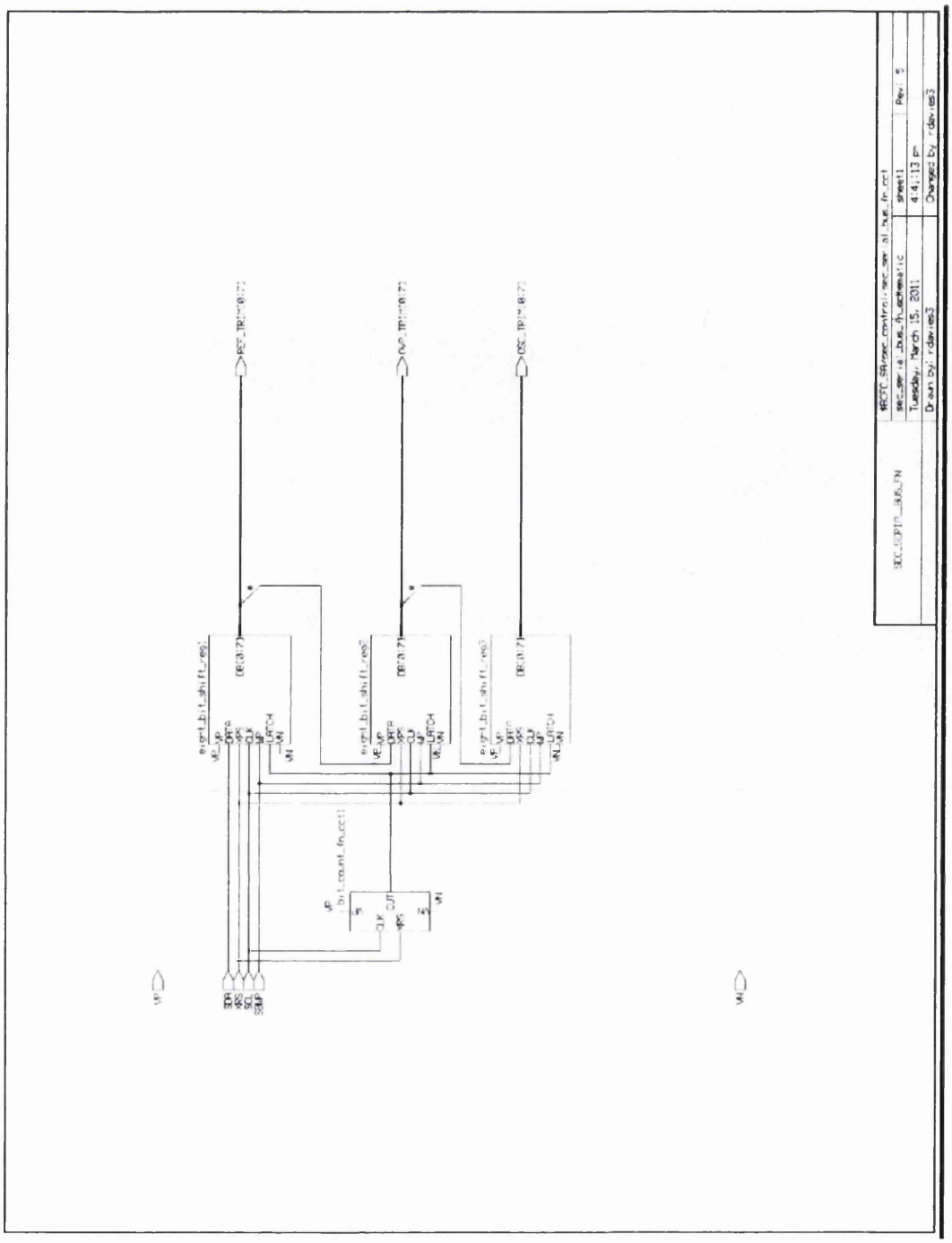


Fig 4.3.11 Secondary Side PM Bus Functional Schematic

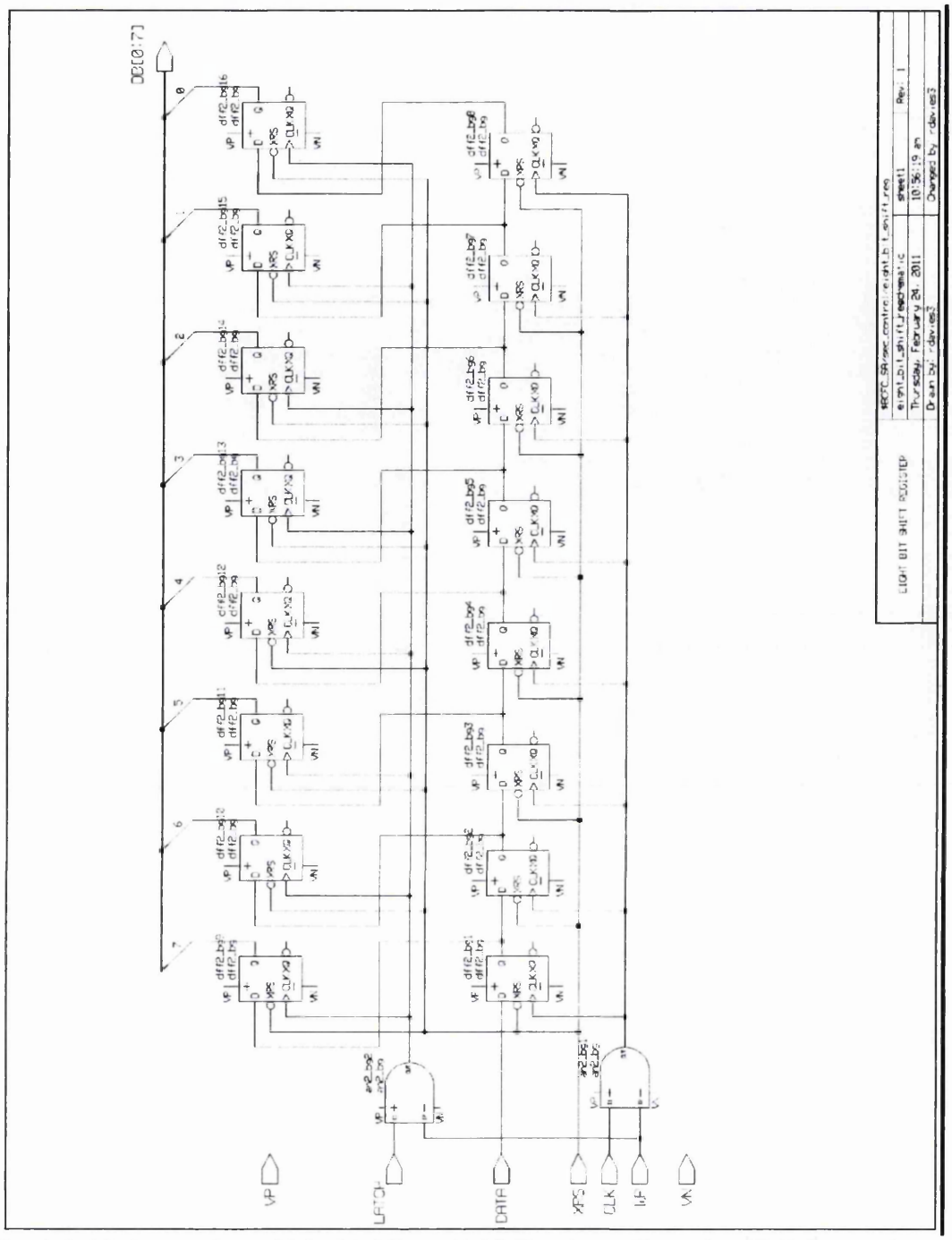


Fig 4.3.12 Secondary Side PM Bus Shift Register Functional Schematic

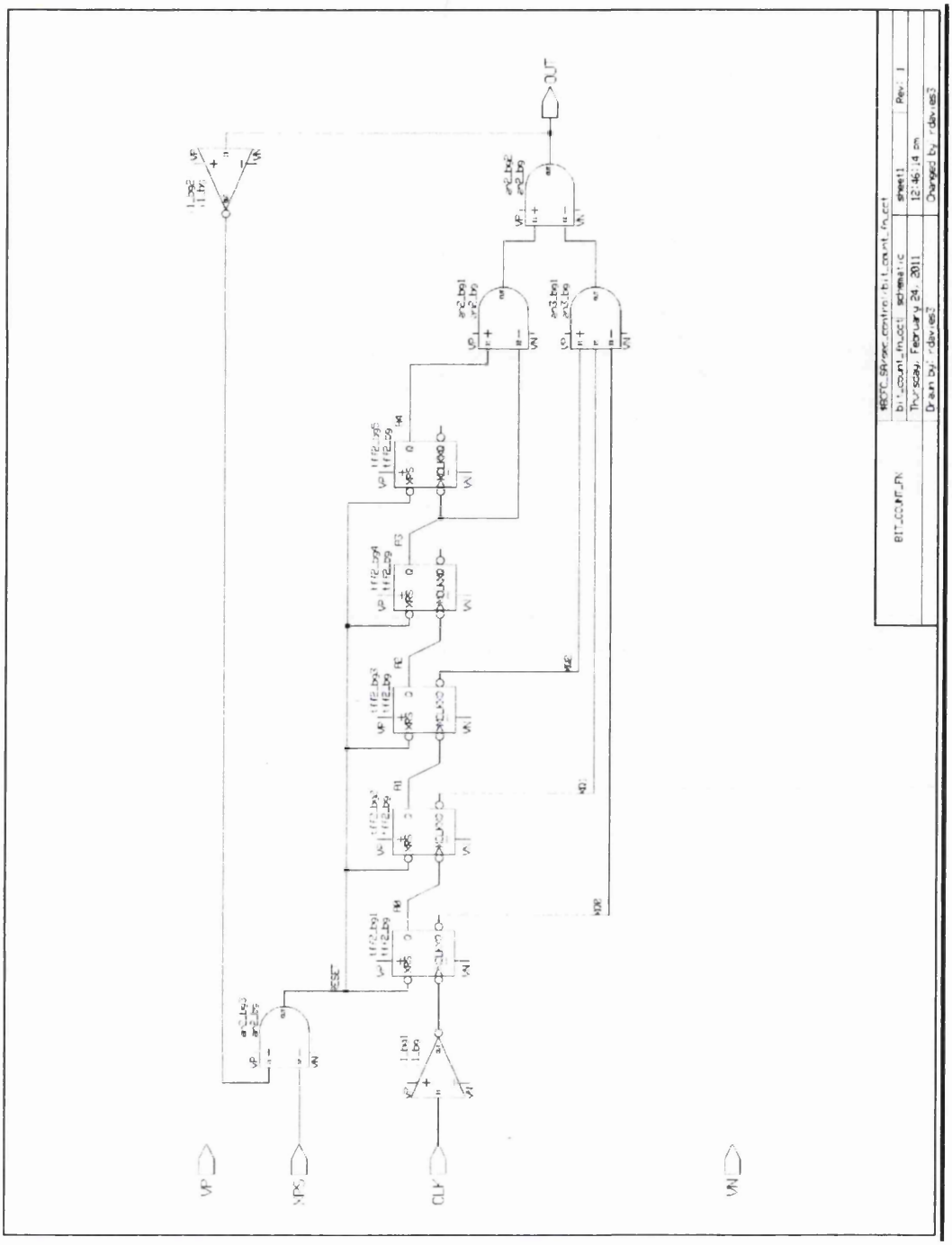


Fig 4.3.13 Secondary Side PM Bus Bit Counter Functional Schematic

5 Design Simulation

5.1 Primary Side Start up.

Firstly it is made clear that the time constants illustrated here for simulation time efficiency are of significantly shorter duration than may be necessary or preferable for hardware operation. The sequence of events will however remain the same but likely to occur over ms as opposed to us durations. The rising voltage on the VIN supply causes the Vcc supply to be charged through the pre-regulator circuit. The depletion mode DMOS device in this circuit as described previously acts as a current source between the Vin and Vcc pins charging the Vcc capacitor C5 to its final regulated value. The rate of rise of the Vcc_P voltage up to the UVLO voltage will be a function of the saturation current of the DMOS device the value of the external capacitance and any load current drawn by pre enabled circuit blocks. It can be seen from the simulation plot shown in Fig 5.1 that the primary side reference voltage is not released to charge up until the Vcc_P supply is above its UVLO level at the 190us point. At device level design bias currents to the majority of circuit blocks will be based on the bandgap circuit derived reference voltage and are therefore held off until Vref_P has reached its final value. This can be seen in Fig5.1 as oscillator operation COSC_P is not started until VREF_P has completed its charge up at 230us. The primary side device has at this point successfully self powered off the line voltage, all the qualifiers have been met as described in section 4.2 and the oscillator is running at the designed frequency.

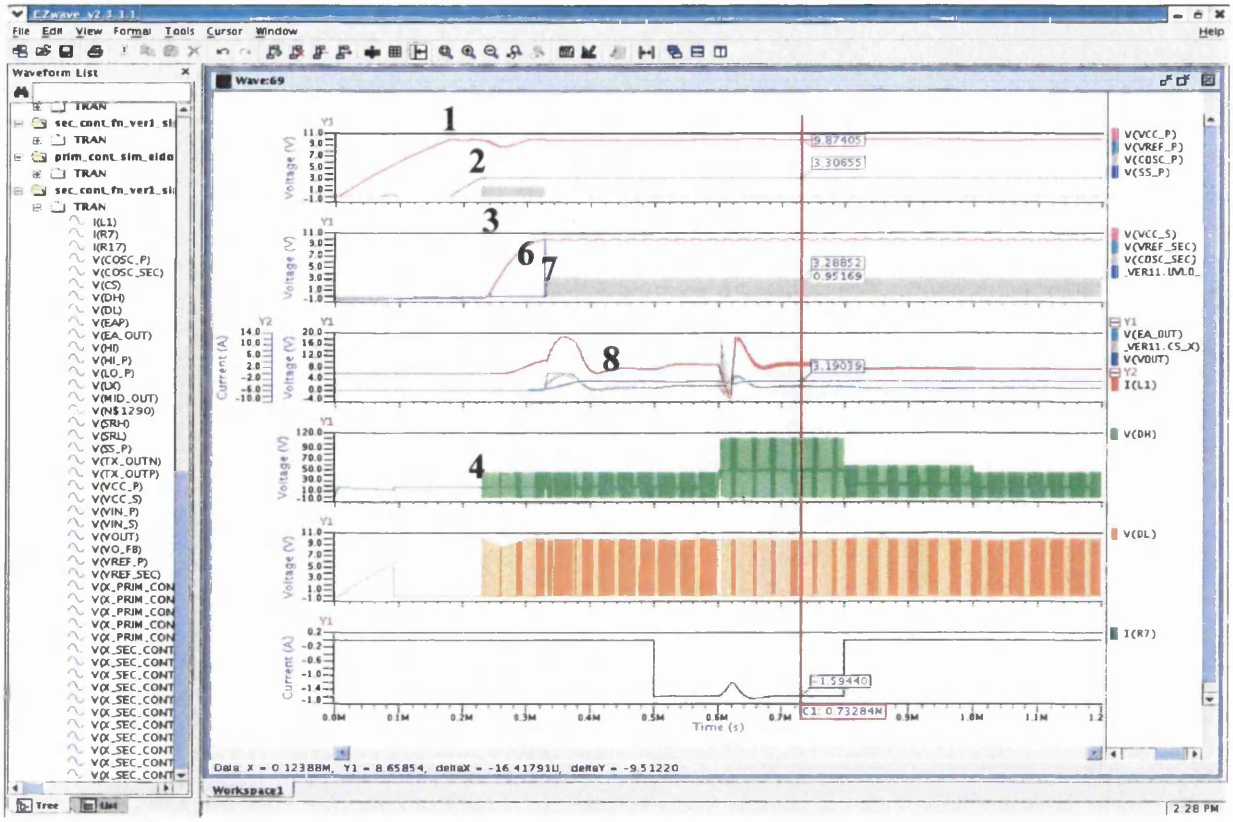


Fig 5.1 Secondary Side Control Functional Simulation Plot

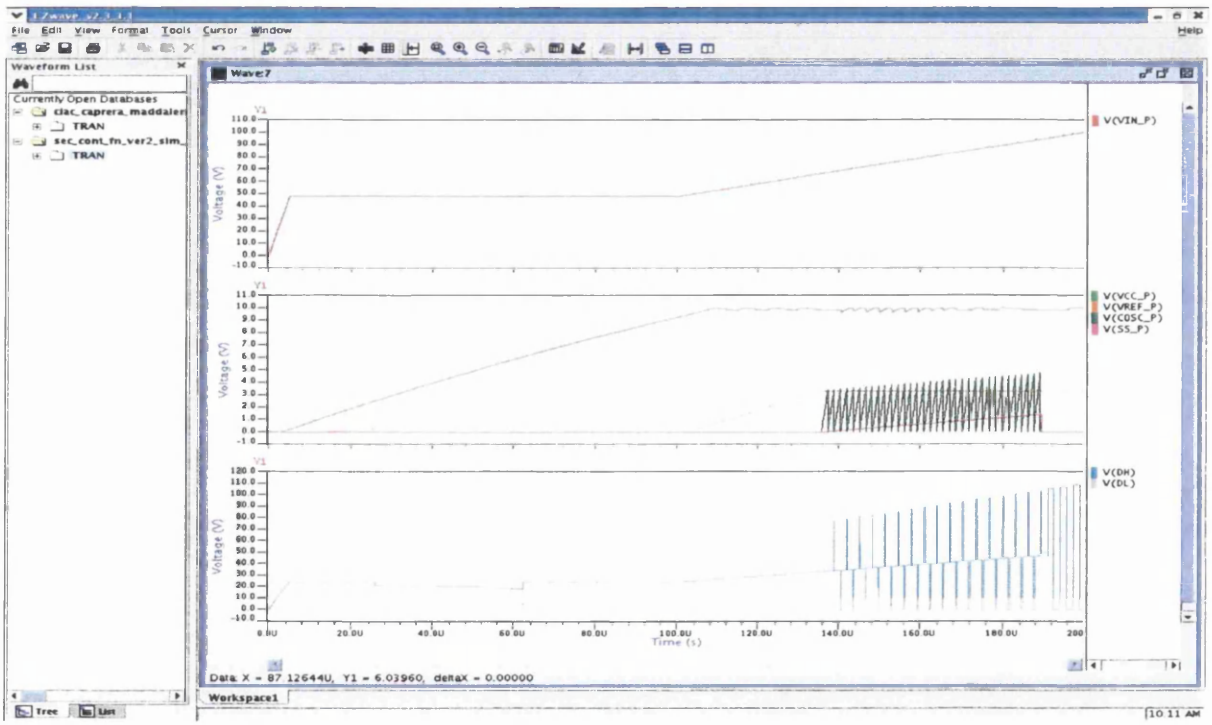


Fig 5.2 Secondary Side Control Soft Start and Feed Forward Simulation

5.1.2 Soft Start

With the oscillator running on the primary side device the soft start function is released. As the soft start voltage enters the oscillator ramp range PWM pulses begin to drive the primary outputs. This is shown in detail in Fig 5.2.along with the feed forward function associated with the VINDET input resulting in the proportionate increase in the oscillator amplitude. The soft start function continues to charge through the ramp range increasing the PWM duty cycle linearly until it reaches its DMAX clamp level or is terminated early. Fig 5.2 shows the soft start pin "SS_P" not reaching that level. The feed forward function is increasing the oscillator ramp range in this instance but "SS_P" would with more time reach the clamp level. The reason for "SS_P" being discharged and "COSC_P" terminating at this point is that hand over to the secondary side controller has occurred and these functions are no longer required and therefore turned off or reset to be ready for any further primary side start up cycle. This event is also shown in Fig 5.1 at the 325us time point. The primary side device has successfully completed its soft start up function and is now driven from the secondary side. Note that synchronous rectifier outputs are provided from the secondary side controller and therefore do not run during the primary side start up period.

5.1.3 Feed Forward Control

As has been previously referred to the primary side device provides for feed forward control of the duty cycle. This function reduces the duty cycle with increasing line voltage to linearly maintain the required volt second on time with increase in line voltage and conversely increases duty cycle with reduced line voltage. This function is open loop and therefore fast, its operation is shown in Fig 5.2 for the period in which the primary side device has control of the start up period. In Fig 5.3 where at the 600us time point a step from 48v to 100v in the line voltage has occurred a feed forward response under current mode control can be seen. The duty cycle of both the DH and DL drives can be seen to have dramatically reduced due to the sharp spikes in signal CS_X. The response can be seen to be immediate preventing an overshot in the output voltage. During the period 600 to 630us the control loop responds with the

error amplifier output "EA_OUT" increasing due to the fall in Vout and the current mode feedback responding to regain its lock position with the error amplifier. The output inductor current "IL1" can be seen to fall from its steady state level and then over shoot to return VOUT to its required value.

5.1.4 Level shift and Boost Voltage

Fig 5.2 is an early simulation of start up operation and illustrates a requirement of the control circuit for optimum operation. The DH output is required to switch to a "BST" voltage above the VIN line voltage in order to effectively turn on the enhancement mode Nmos power switch. The BST voltage is achieved by charging the BST pin from the Vcc supply on the low side DL cycle, at this time the LX pin is shorted to ground by the low side power mosfet driven by DL. Capacitor "BST_P" is shown connected between BST and LX in Fig 4.1 and is used to retain this high side gate drive voltage through the DH on period. The low side switching period is therefore required to occur first if the high side drive is to effectively turn on the high side power Mosfet. For a half bridge converter termination of the low side on period results in the LX node returning to the mid point of the Vin supply. When turned on the DH output switches to the BST voltage which turns on the high side power Mosfet represented by Y3 in Fig 4.1, pulling the LX node to the VIN supply. The DH output then sits at VIN+VCC as can be seen in Fig5.2.The DH output via vcsw Y3 is holding the LX node of the power transformer at VIN with the other side of the primary winding at the mid point voltage VMID, established by C1 and C2 Fig4.1. The BST capacitor must be sized relative to the power Mosfet gate capacitance such that the Vgs droop is insignificant within the Dmax on period, effectively the oscillator period. The BST voltage is recharged on each low side on period.

5.1.5 Primary Side Over Current Protection

The primary side device is required to protect the primary side power train components. An over current on the secondary (load) side of the converter can be better protected from that side but a fault on the primary side may possibly not be detectable from the secondary side. The "CS" pin on the primary side controller

provides the over current response shown in Fig 5.5. The MOC level "100ref" has been exceeded but not the SOC level "150ref" resulting in the discharge of the soft start pin. As the soft start pin enters the oscillator ramp range it will reduce the operating duty cycle and due to the continuous over current detection finally terminate output switching. The discharge rate of the soft start pin can be seen to immediately reduce at that point to provide an extended hiccup period. A hiccup cycle will effectively look like a start up to the secondary side device with the exception that the VCC_S and VREF_SEC supplies may not be fully discharged. It can be seen that in this instance Fig 5.5, the oscillator is left running as hand over to the secondary side has not occurred. For protection of the primary side components after hand over it would be necessary to restart the primary side oscillator once an over current was detected and to allow for a SOC response only. By this method a secondary side overload would be handled by the secondary side controller and not allowed to reach SOC level.

5.2 Primary to Secondary side Handover

It is shown in Fig 5.1 that during the period 240 to 328us the "VCC_S" supply can be seen to charge up, the secondary side UVLO signal switching high at 328us with "VREF_SEC" fully charged by 334us resulting in the start up of "COSC_SEC" and enabling of all other functions . This is illustrated in more detail in Fig 5.4. The converter output "VOUT" has begun to charge but is well below the final value, as a result the error amplifier output "EA_OUT" increases rapidly with the resulting increase in duty cycle observable on DH and DL. The increased duty cycle and resulting increased current in the secondary circuit shown in trace "IL1" is reflected in the increase in the current mode feedback signal "CS_X" which increases to the EA_OUT level. During this period the increased current has accelerated the increase in output voltage and as VOUT approaches its final value the error amplifier begins to reduce EA_OUT with a resulting fall in duty cycle in the 380us region. The secondary side current mode control continues in operation over load and line voltage steps as shown in Fig 5.1. A load step is applied at 500us by switching in R7, Fig4.1 doubling the load on VOUT and resulting in the transient drop in output voltage and increase in "IL1" observable in the period to 550us.

5.2.1 Pre Bias Protection

The nature of the load equipment supplied by such power supplies does not allow for a non monotonic rise in output voltage, as highlighted in section 2.2. A non monotonic rise in output voltage can be considered to occur where an existing output voltage sometimes known as a pre bias exists and which is discharged at the start up of converter operation prior to subsequent power up. It is shown in Fig 4.1 that outputs SRL and SRH drive voltage controlled switches which short rectifier diodes X3 and X4 respectively. The normal operating condition for the synchronous rectifiers is normally on as illustrated in Fig 5.6 at the end of the CDEL charge up period. This operating condition provides a discharge path from the output to ground when the current in the output inductor is insufficient to prevent the current going to zero and reversing driven by the output voltage within the oscillator period as could occur at the start of a soft start cycle where the duty cycle is very low. The synchronous rectifiers improve efficiency by removing power loss of the forward voltage drop of the rectifier diodes times output current with the significantly reduced power loss of the Rds(on) of the power Mosfets times the output current. The issue of initial discharge can be addressed by monitoring of current direction or can be solved by the simpler method of recognising that if the synchronous rectifier drive is inhibited well beyond the designed start up time for the output voltage then the synchronous rectifier drive can be started and "phased in" without significant loss of efficiency. This capability is provided for with the CDEL pin on the secondary side controller. The capacitance connected to this pin results in an application level definable variable delay to the BBM2 time which initially holds off the synchronous rectifiers and gradually phases in the on time with the increase in voltage on the CDEL pin. The phase in feature is important in that it avoids the sudden removal of the diode drop from the output circuit of the power path with resulting change in output voltage.

5.2.2 Monotonic Rise of Output Voltage

The simulation plot of Fig 5.1 shows the output voltage to increase continuously during the start up the hand over period and on to final value. The crucial factor here is the relative time constant of the output voltage and the power up and lock time of the error amp and current mode control of the secondary side. As stated at the start of section 5.1 for simulation efficiency the time constant of the soft start period and the output voltage have been reduced significantly, yet the output voltage rise is monotonic. The power up times for the controller circuits are realistic and therefore show the capability for power up and hand over within required power up times for the converter output voltage. In order to achieve the monotonic rise in Vout the compensation of the error amplifier has to be correct or oscillation in the output voltage as shown in Fig 5.7 will result both at initial handover and Vin and load transient conditions. The 48 to 100v step in the VIN voltage at the 600us point can clearly be seen to have resulted in a reduction in the output voltage due to too rapid a response from the error amplifier.

5.2.3 Secondary Side Current Mode Control

The secondary side device operates current mode control as described in "PWM Comparator Circuit" fig 4.3.5. This is confirmed in fig Fig5.3 and Fig 5.4 where the current defined ramp waveform can be seen to interact with the error amplifier output level to define the duty cycle at the primary to secondary hand over and at the line voltage step response respectively. The immediate reduction in duty cycle to the step in VIN voltage at the 600us time point, Fig 5.3, prior to the reaction of the error amplifier output is evidence of the feed forward function provided by current mode control. The CS input includes slope compensation, this is applied at the application level not within the secondary side controller and is therefore under the control of the application level designer.

5.2.4 Synchronous Rectifier Drive

The drive to the synchronous rectifiers is shown theoretically in Fig 5.6, the diagram illustrates the relationship between the primary drives DH, DL and the synchronous rectifier drives SRH, SRL. As shown the SRH output is required to turn off the synchronous rectifier associated with the high side on phase and the SRL output to turn off the synchronous rectifier associated with the low side on phase. The CDEL pin is also shown charging with the resulting Phase in of the synchronous rectifier on time ending in the synchronous rectifiers normally on and selectively off with appropriate break before make time set by the Rbbm1,2 values. The simulation plot Fig 5.8, illustrates the circuit design achieving this objective with the synchronous rectifier drives locked to the respective phase and duty cycle of the primary drives. Fig 5.8 does not include the phase in operating in order to illustrate the potential to discharge the output voltage if the synchronous rectifiers are enabled too early. The phase in capability is shown in Fig 5.9 and Fig 5.9a, it can be seen that the trailing edge of the SRH, SRL outputs has been delayed beyond the oscillator period and is reduced with the increase in the voltage on the CDEL pin gradually introducing synchronous rectifier operation in the secondary side power circuit.

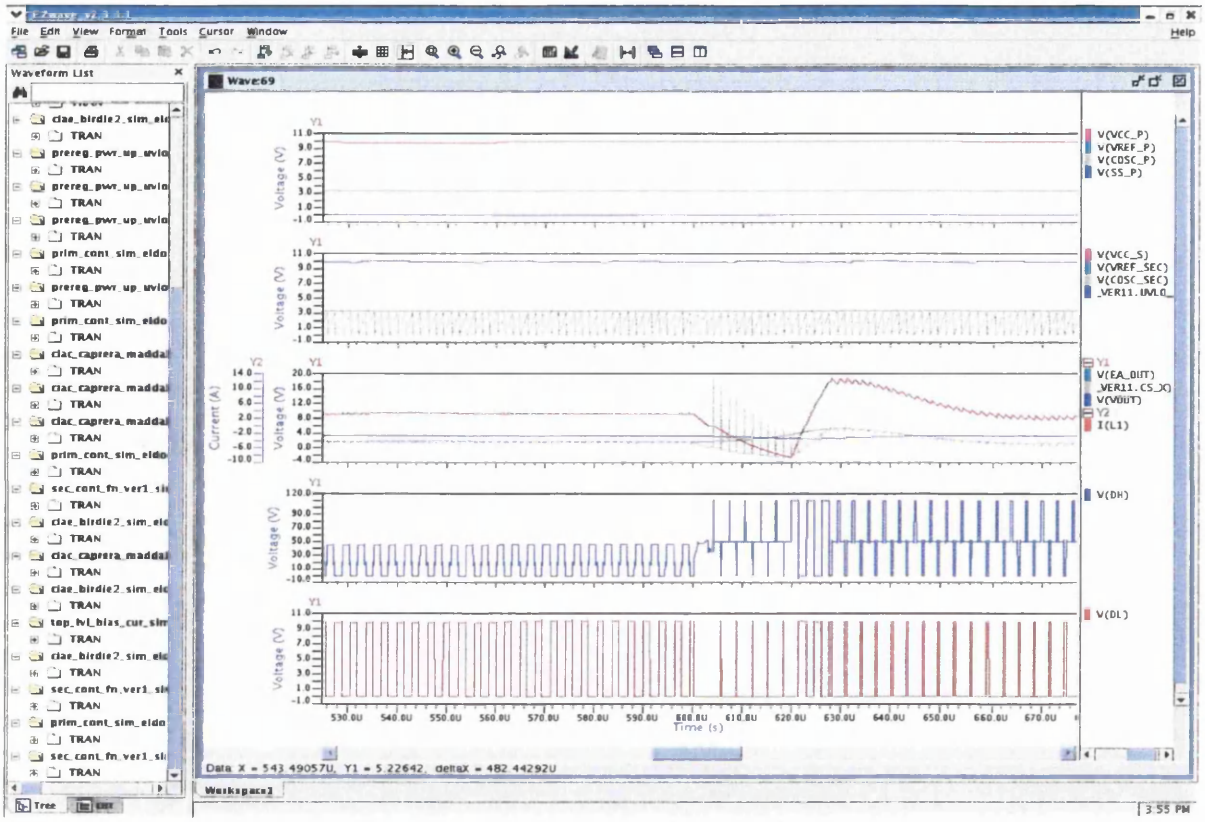


Fig 5.3 Secondary Side Control Line Voltage Step Response Simulation

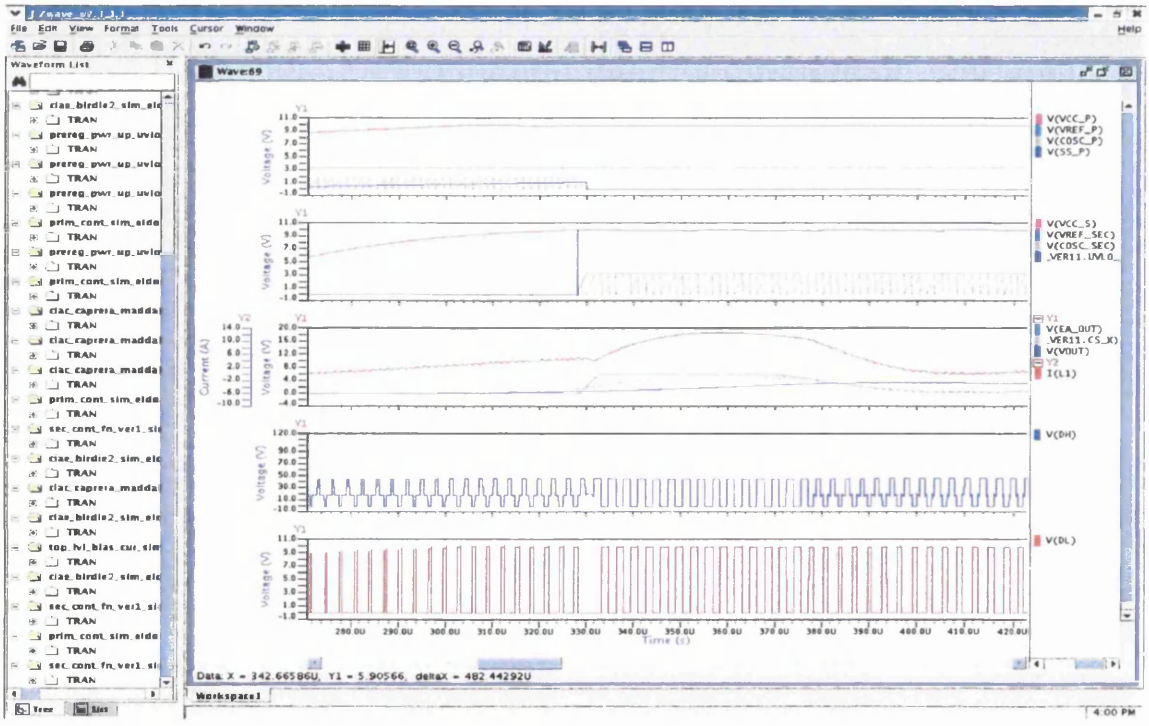


Fig 5.4 Secondary Side Control Hand Over Simulation

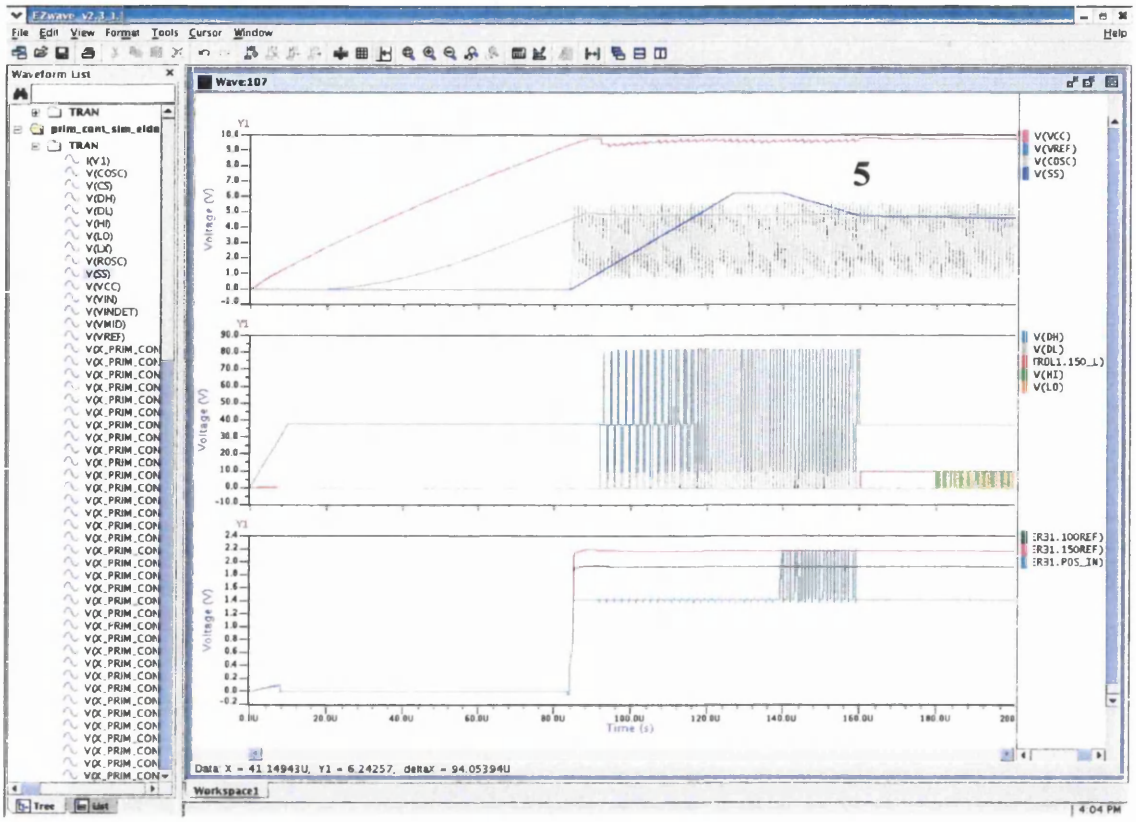


Fig 5.5 Primary Side OCP Response Simulation

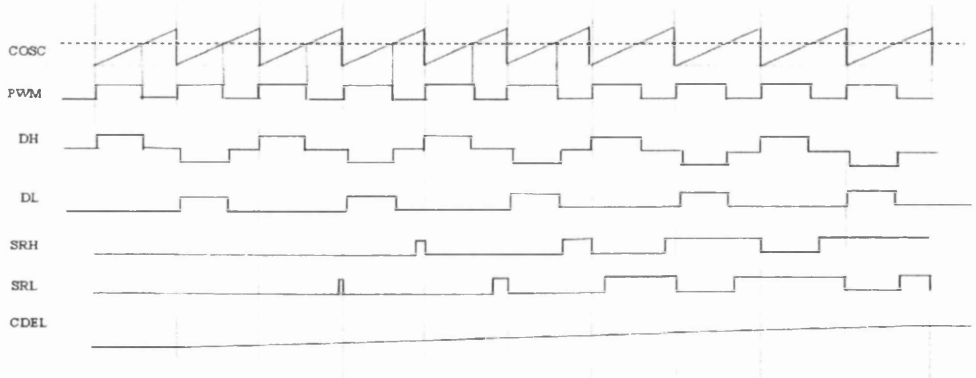


FIG 5.6 Synchronous Rectifier Timing Diagram

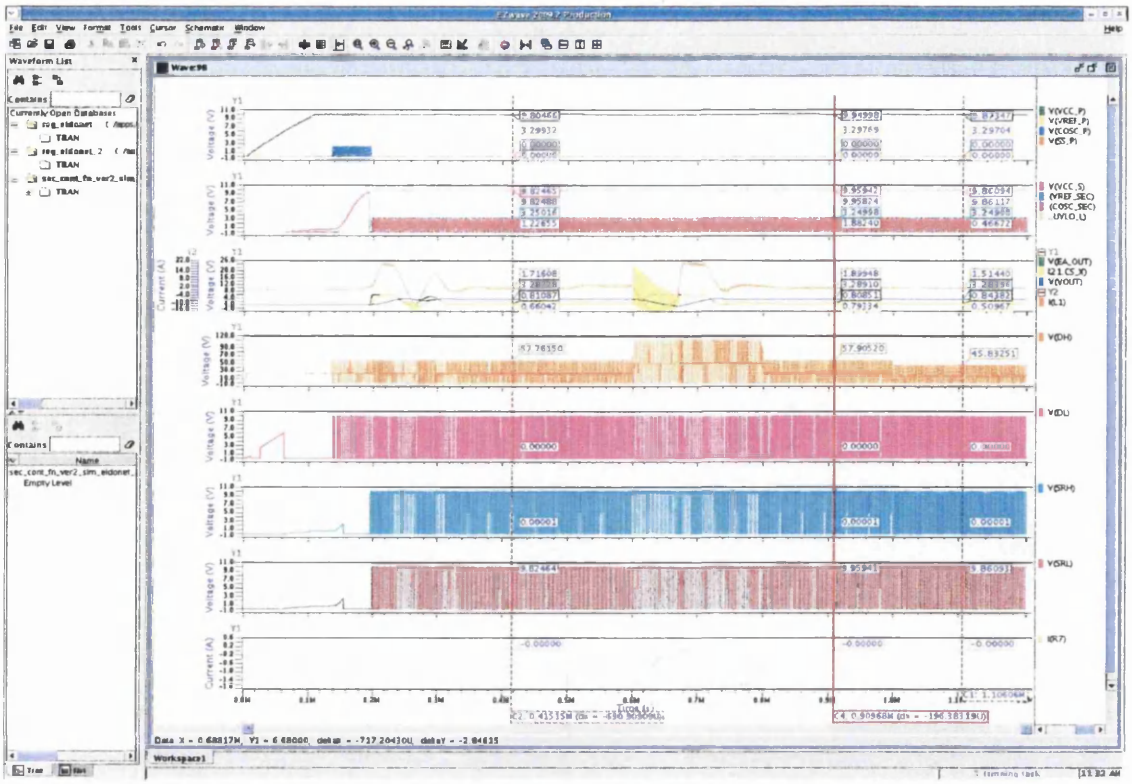


Fig 5.7 Secondary Side Control Function Simulation Plot 2

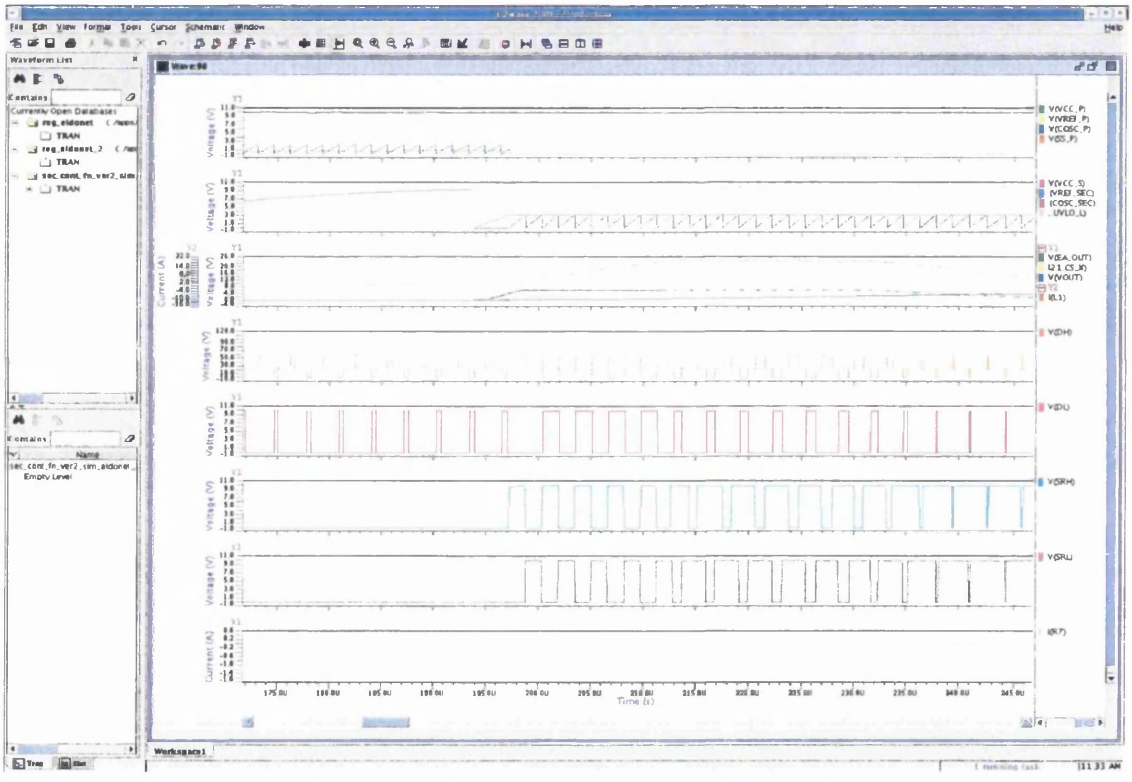


Fig 5.8 Synchronous Rectifier Timing

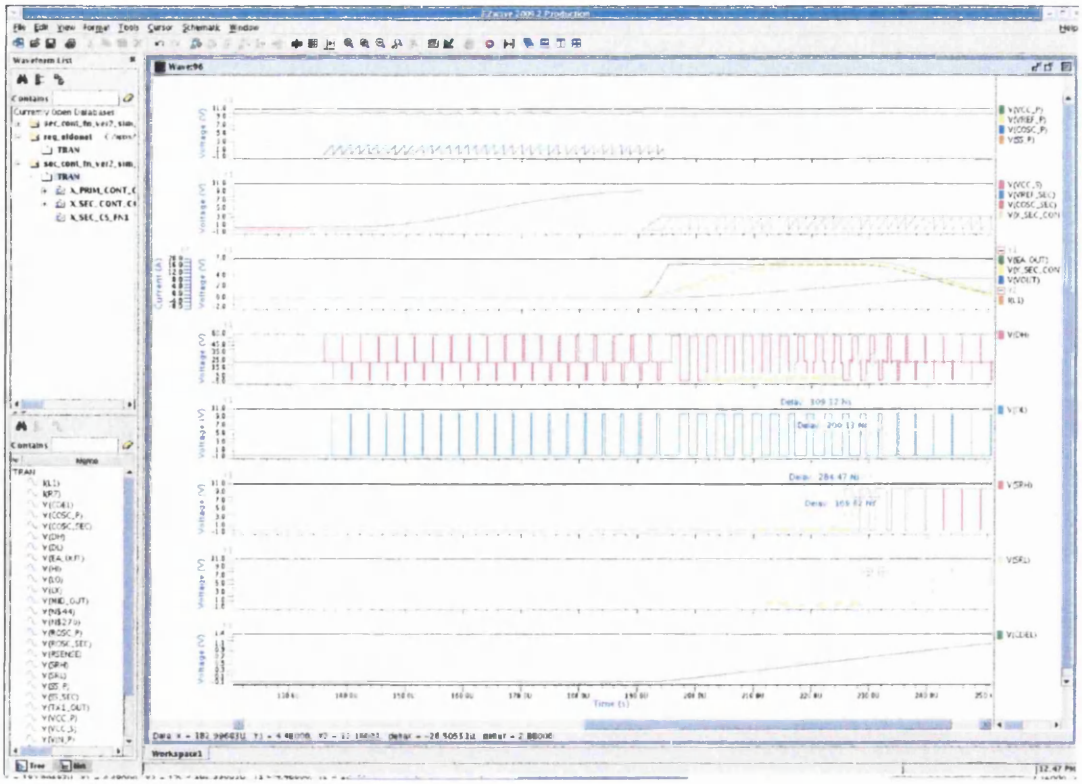


Fig 5.9 Synchronous Rectifier Phase In

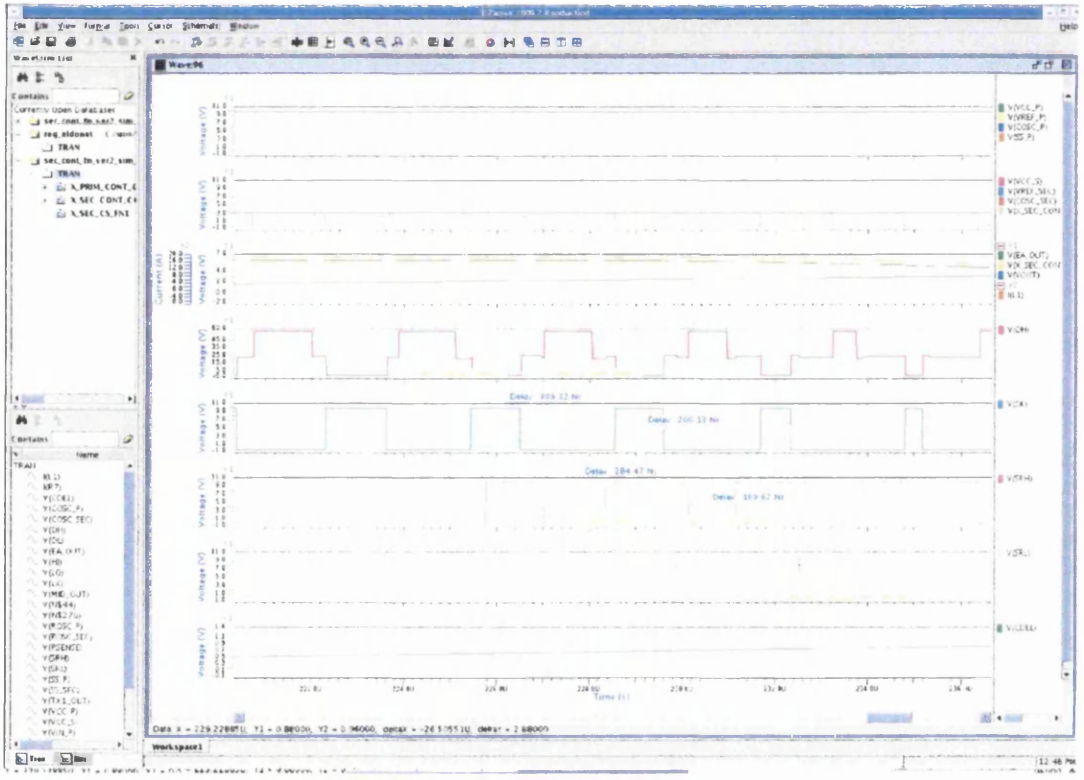


Fig5.9a Synchronous Rectifier Phase In - Zoom In

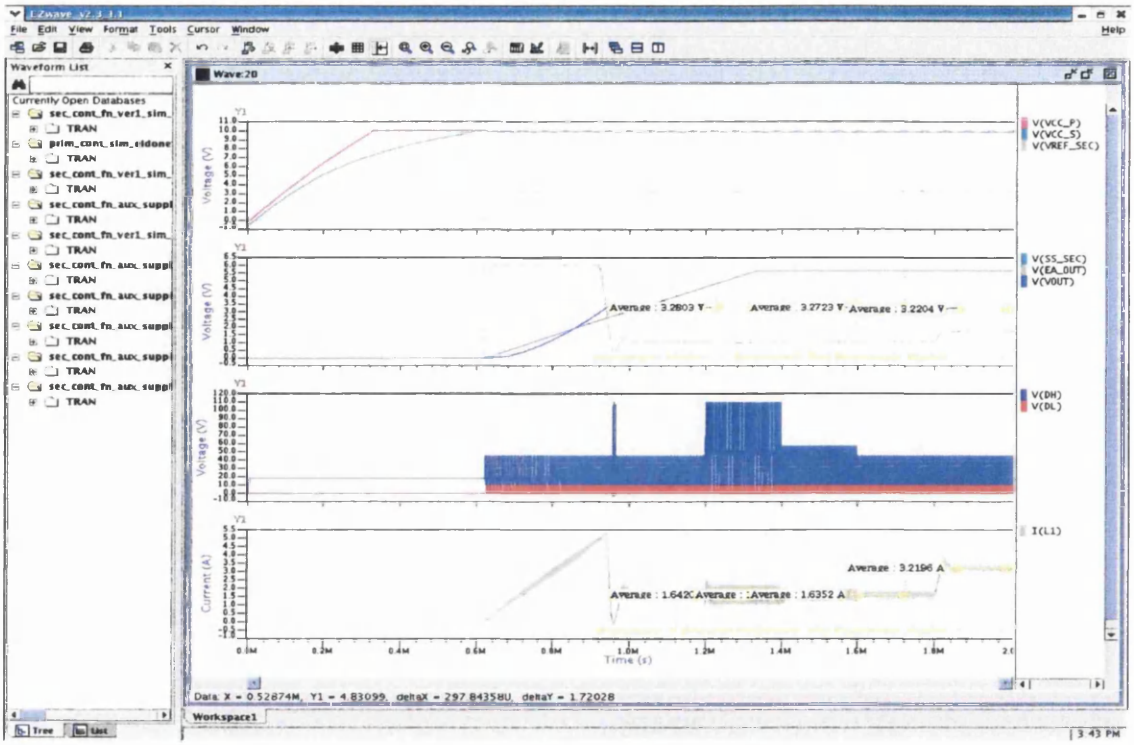


Fig 5.10 Auxiliary Circuit Architecture – Simulation Plot

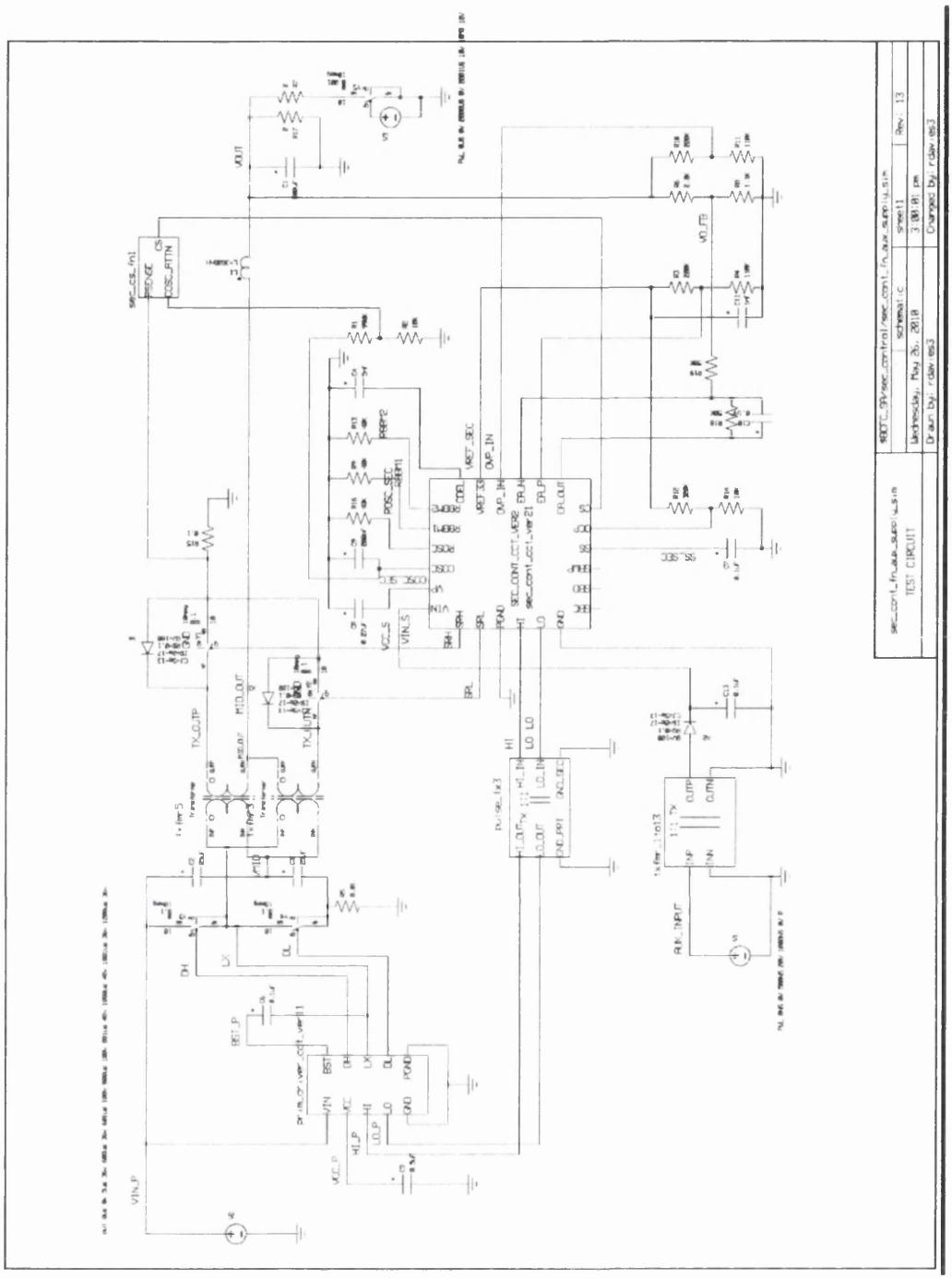


Fig 5.11 Auxiliary Circuit Architecture Simulation Schematic

6 Device level Design

6.1 Silicon Design Methodologies

The requirements to be able to successfully create mixed signal circuits on monolithic Silicon processes include the availability of the process providing an appropriate voltage range and device arsenal with SPICE [32] level models developed from accurate characterisation data. A device level simulation tool using the SPICE models is required and extensive simulation of DC, Transient and AC analysis to verify the circuit design performance is required to achieve the objective specification. Simulation methodologies specific to Switch Mode power supplies is covered by Sandler [33] with examples of modelling of magnetic components as used in the transformer functional description shown at [34]. An example of the dc analysis of the pre regulator design is shown in Fig6.1 obtained using the ELDO simulator from Mentor Graphics [35], transient performance for a Vcc capacitance value of 0.47uF is shown in Fig 6.1.2.The device level schematic is shown in Fig 6.1.3.

The availability of a standard cell library containing common digital functions is usual along with design rules for the physical design of the captured schematics. A common requirement early in the project is for a die size estimate where ever possible based on known areas for analogue functions previously designed on the process and a standard cell count estimate. A profile of the estimated die size and bond pad locations is then used to produce a bonding diagram for the selected package confirming that the final integrated circuit can be assembled. Following completion of the circuit layout design verification of the result requires the running of DRC and LVS checks to verify firstly that the process layout rules have been complied with and secondly that the layout is a true representation of the captured schematics. Checks to verify adherence to SOA rules are also available though not always.

The above design procedure will have some flexibility in the schedule if an in house process of the semiconductor vendor is used. If a Silicon foundry route is taken then

the tape out date of the captured layout is fixed anchoring one corner of the cost, time, quality triangle [38] with resulting pressures on cost and risk to quality. This approach is however increasingly common driven by cost competition of Silicon foundry vendors and the perceived discipline of the fixed tape out schedule. The alternative perspective however is that this methodology can result in a greater number of iterations due to increased error rate of engineers working under excessive time pressure.

The circuit design will have taken into consideration testing requirements and where ever possible means of facilitating testing to confirm that function and parameters meet the objective specification are included. This may include additional circuitry to provide a "test mode" and additional bonding pads to provide trimming capability to e.g. reference voltages, amplifier gain setting or compensation. Trimming capability via poly fuse blowing is expensive in area in the "pad ring" and may impact on the die size if the total pad count dimension pushes the die size to become "pad limited". The trim range shown in Fig 6.1.4 is the result of up trimming via the PMBus interface to TR0 – TR4 to the secondary side band gap reference voltage. The Y axis indicates the cumulative increase in mV of the reference voltage. The down trim capability via TR5,6 is shown in the Fig 6.1.5, the top plot indicating the initial output voltage with the "typical" value highlighted. The lower graphs show the result of down trim from that voltage.

The fabrication of the Silicon provides a period for completion of a "test plan" and "test programme" ready for the receipt of the completed Silicon wafers from the foundry. The design will usually be evaluated initially by the design engineer responsible and if functional will move to product engineering who are responsible for ensuring that the design can be manufactured in volume and will meet all objective specification across temperature and process variation and the yield requirement. The product would then be released to the market accompanied by promotional and design in support material.

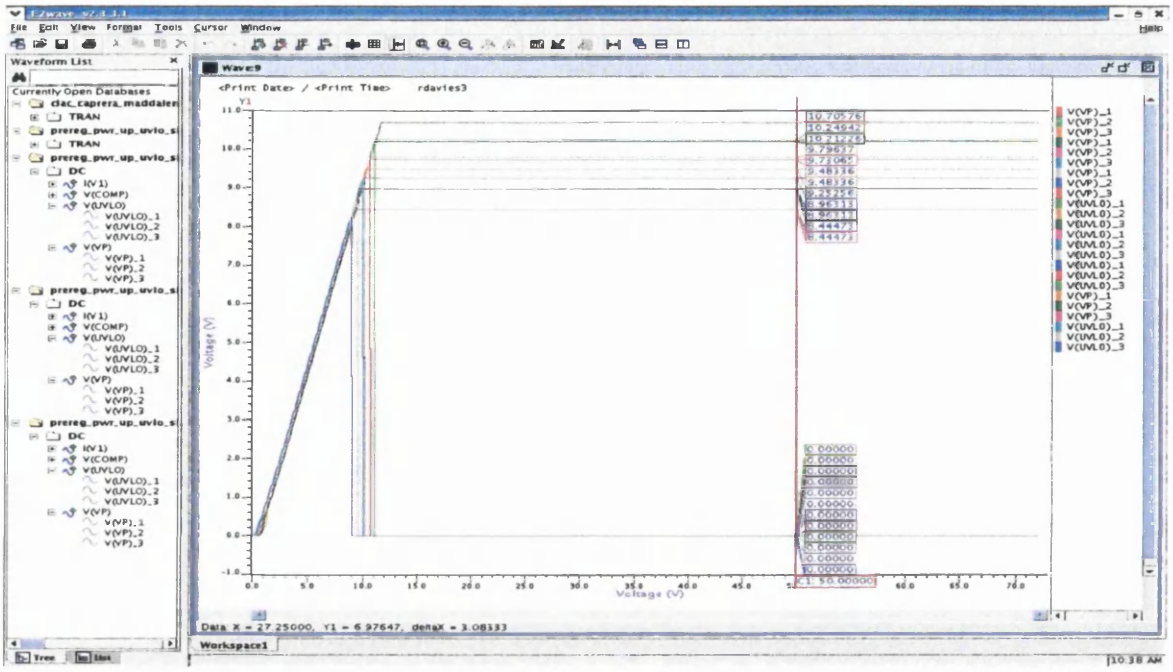


Fig 6.1 Device Level Pre Regulator Circuit DC Analysis Simulation Plot

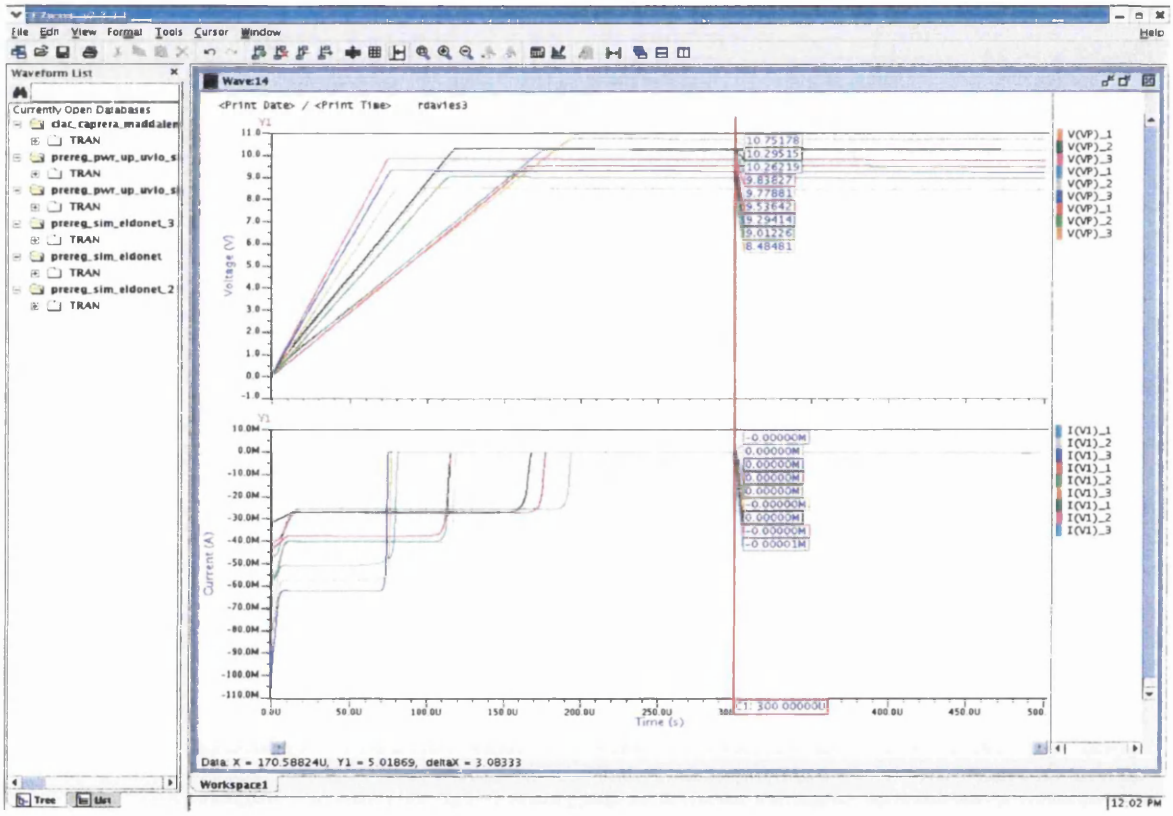


Fig 6.1.2
Device Level Pre Regulator Circuit Transient Analysis Simulation Plot

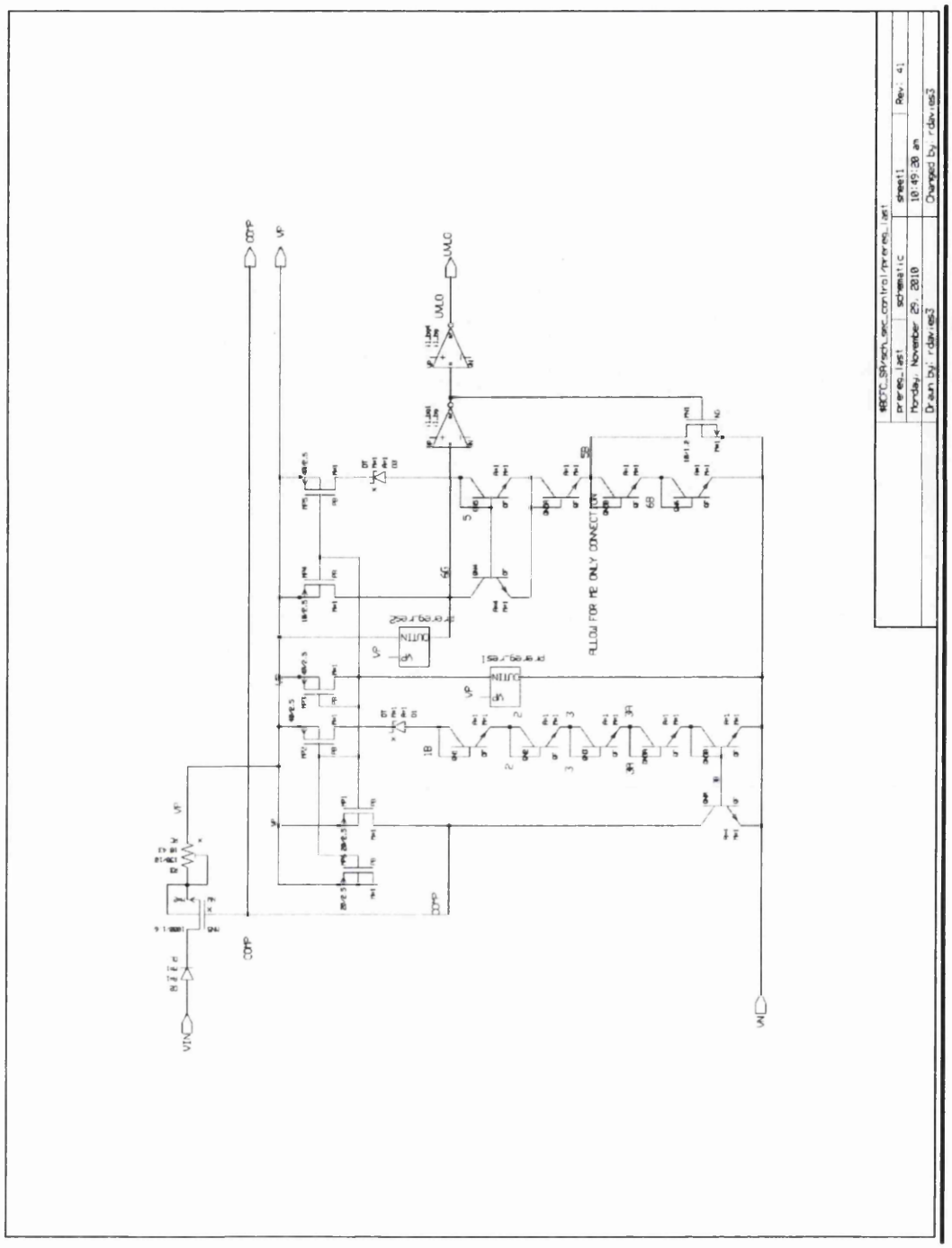


Fig 6.1.3 Device Level Pre Regulator Circuit Schematic

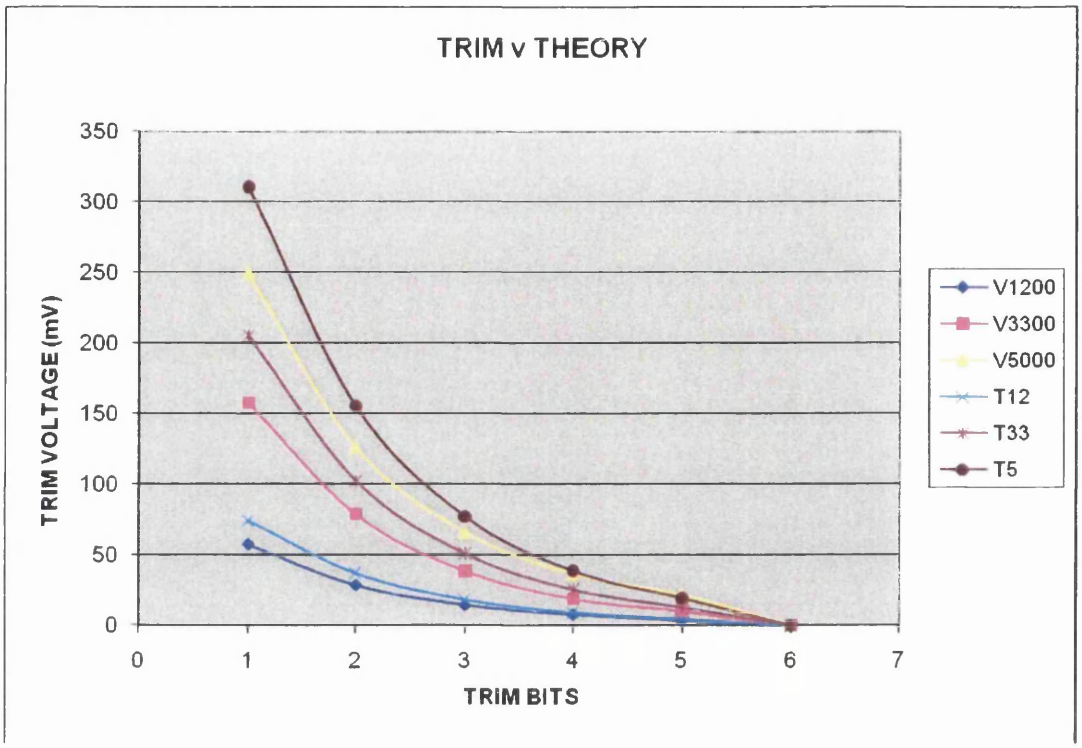


Fig 6.1.4 Device Level Vref Trim Theory versus Simulation

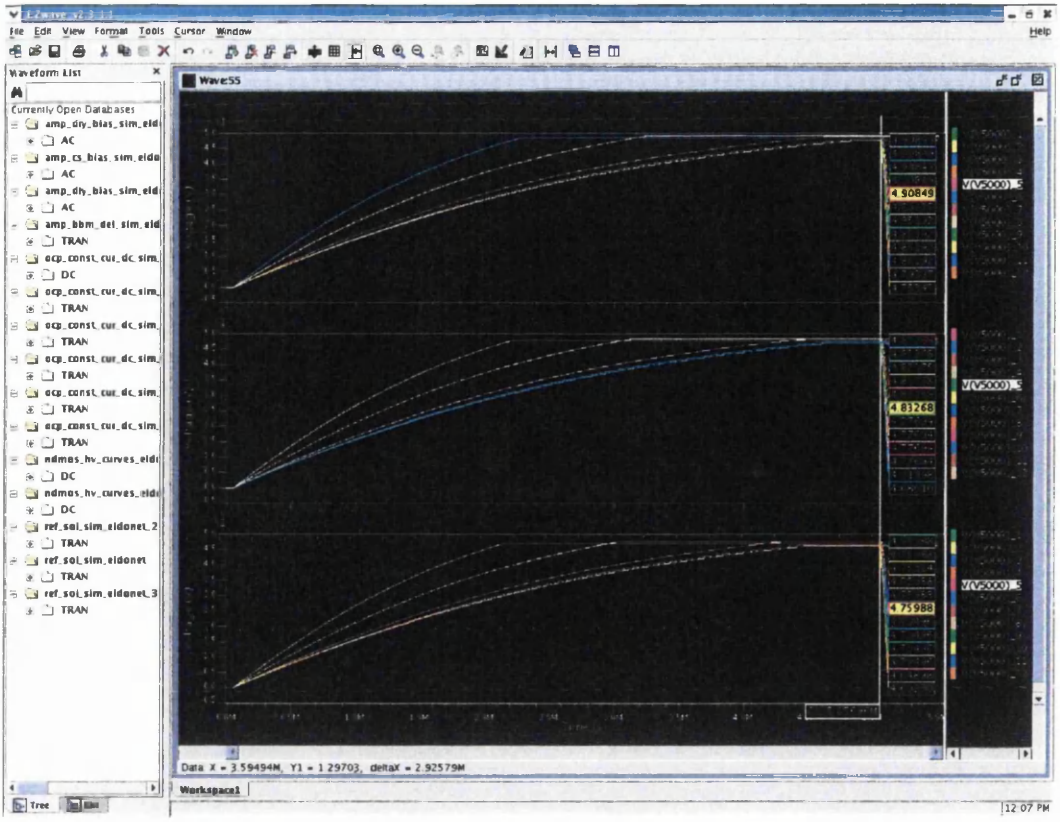


Fig 6.1.5 Device Level Transient Analysis Simulation Plot

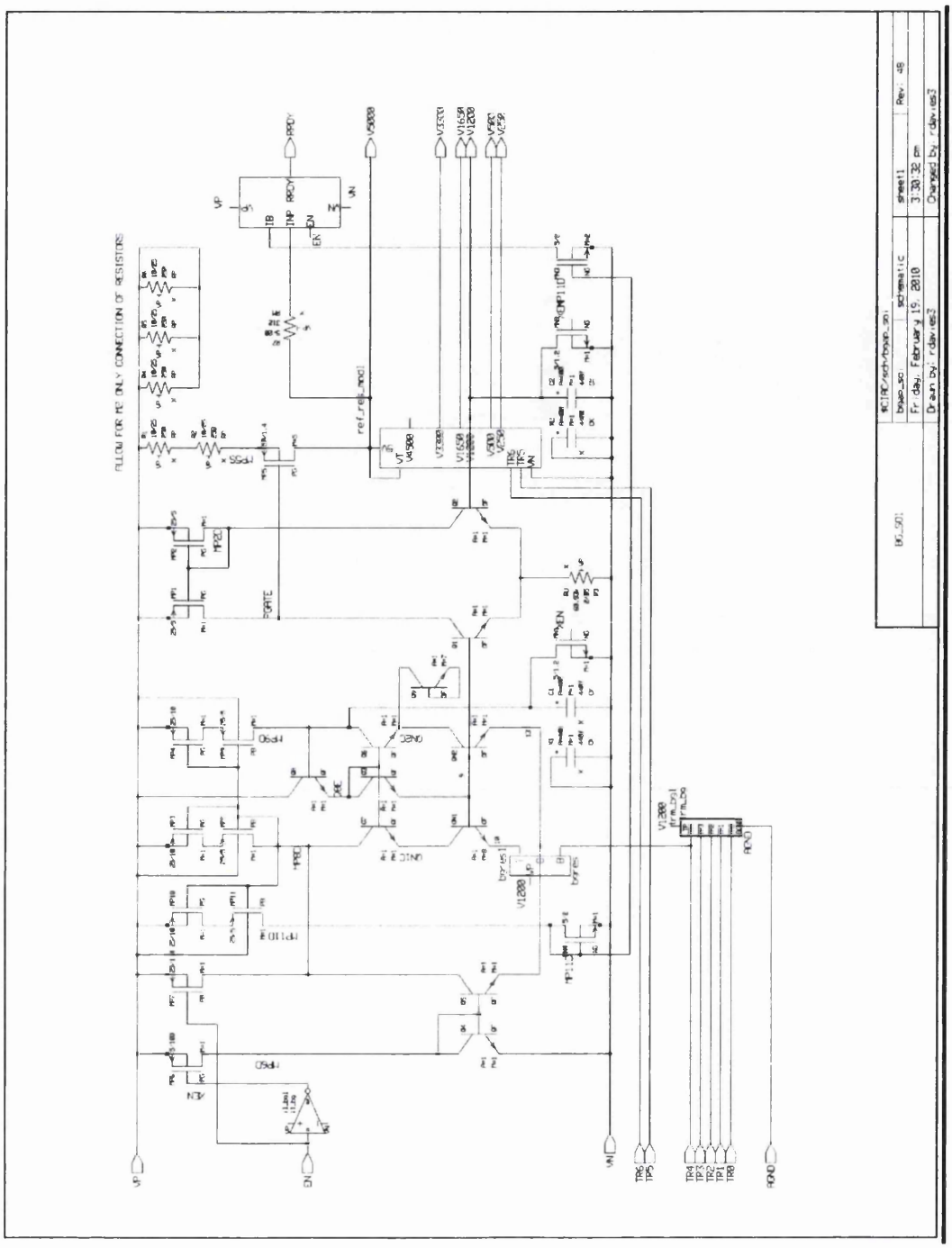


Fig 6.1.6 Device Level Bandgap Reference Schematic

6.2 Silicon Process Requirements for Primary Side Controller

To be able to provide the self start up and high side drive capability the process used for the primary side device would have to have available high voltage isolation both to the substrate and to the BVdss parameter. Both these capabilities have been available above 100V on BCD [39] bulk silicon processes. Increasing voltage capability is however generally associated with increased dimensions in junction isolated devices resulting in increased die size.

This issue is significantly improved with the availability of an SOI [40] process with die size reduction of 50% common. A comparison of the cross sections of BCD and SOI processes is shown in Fig 6.2. An illustration of an SOI process flow is shown in Fig 6.2.1 and Fig 6.2.2. Modelling for this process would be based on BSIMSOI device models [36].The relationship between HV LDMOS device BVdss on the SOI process and field distance is illustrated in Fig 6.2.3 and Fig 6.2.4.

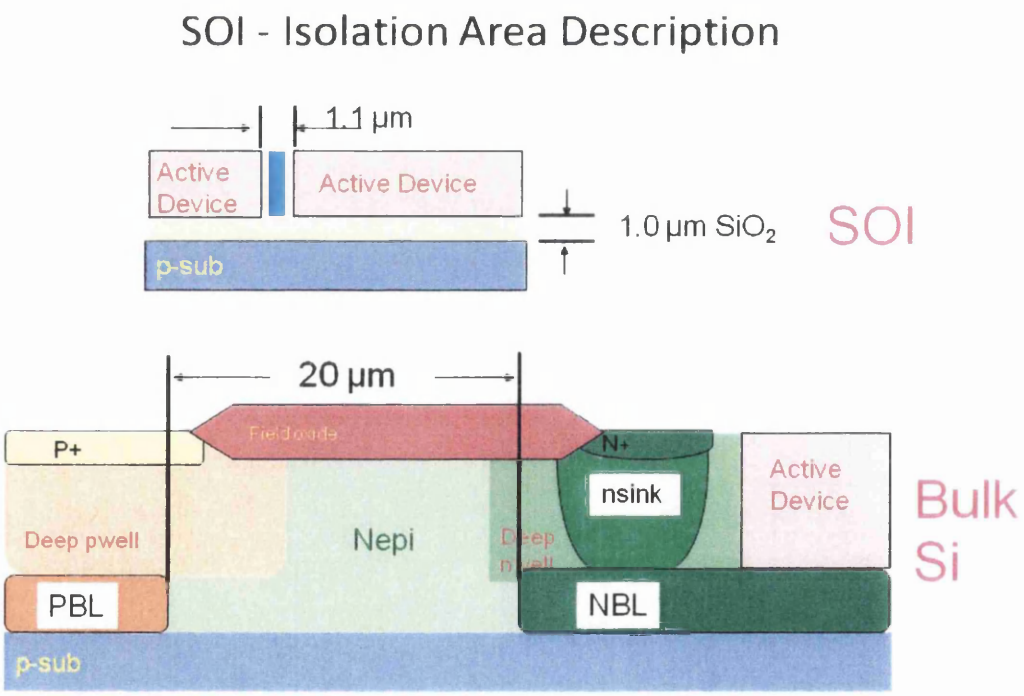


Fig 6.2 BCD versus SOI Process Isolation Distance Comparison

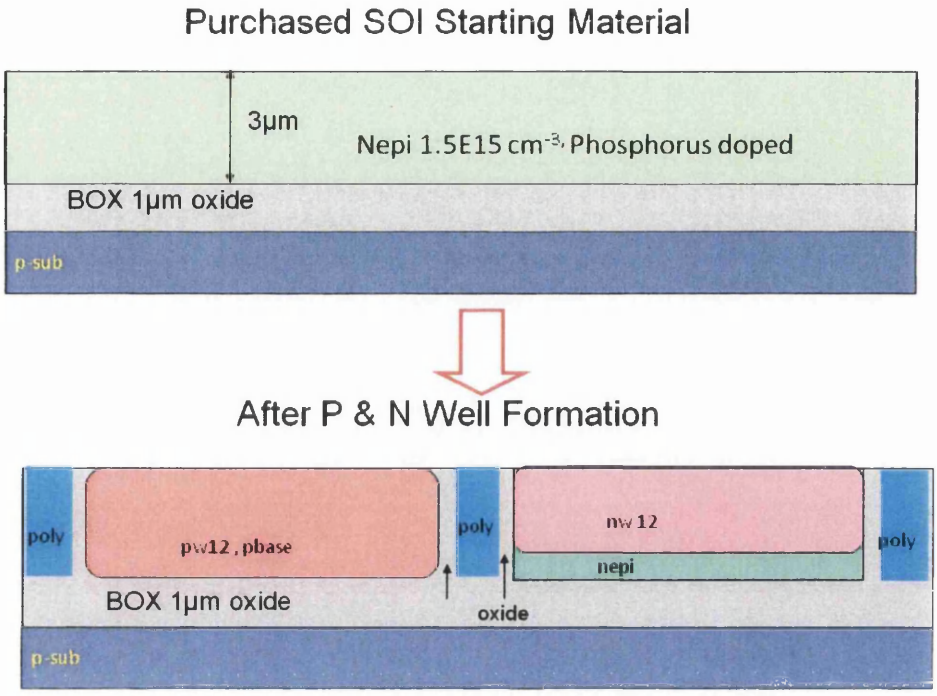


Fig 6.2.1 Initial SOI Process Flow Steps

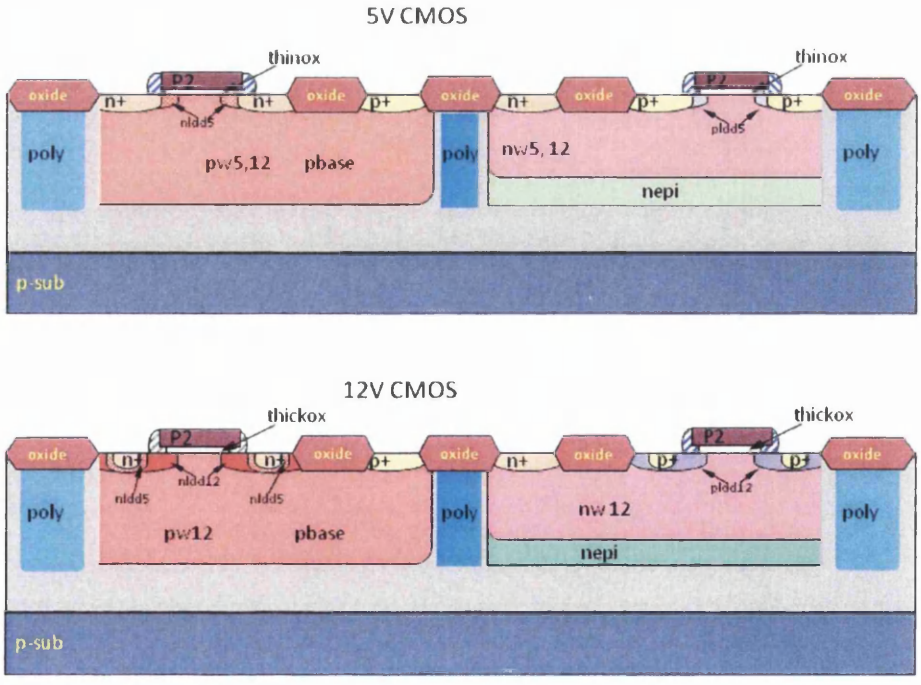


Fig 6.2.2 SOI 5v and 12V CMOS Device Cross Section

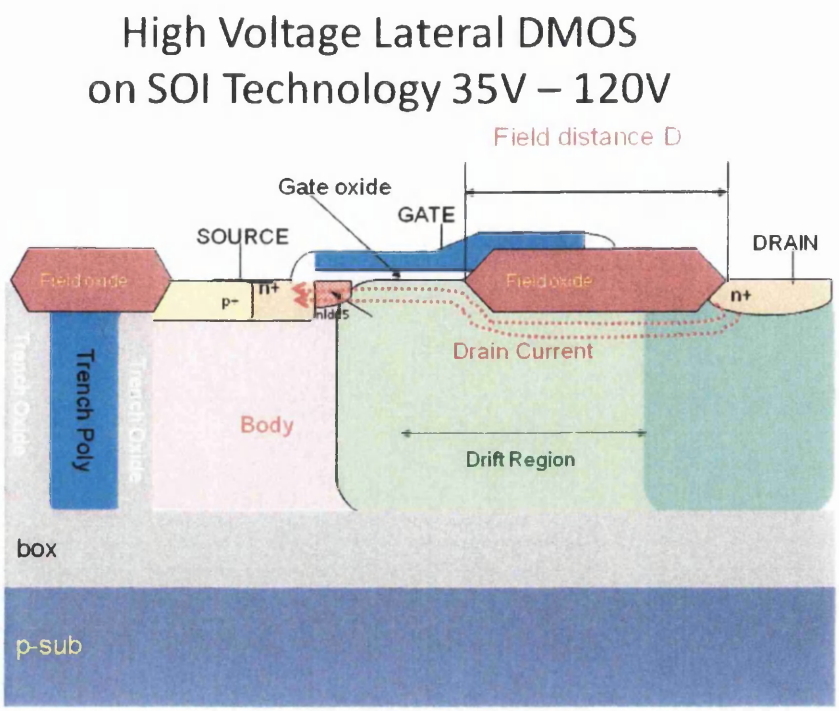


Fig 6.2.3 SOI 100V Lateral Dmos Structure

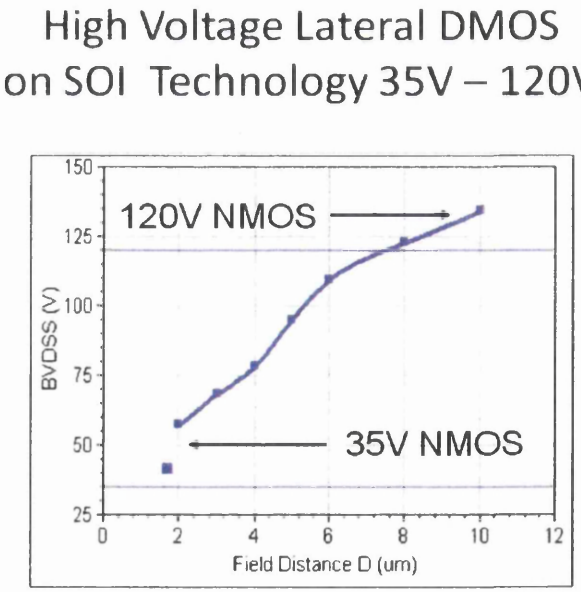


Fig 6.2.4 HV Lateral Dmos BVdss versus Field Distance

As shown for greater than 120V capability required for reliable 100V operation the field distance is 10uM despite the effective gate length being sub micron. When one considers that this dimension applies across the width of the device. For a saturation current of tens of mA as required for the pre regulator the gate width is of the order of a few thousand microns, the field distance dimension therefore expands the area of high voltage devices considerably. These devices are therefore used only when necessary. In the case of this design the requirement would be for the pre regulator pass transistor between the Vin and Vcc pins and as cascode [41] devices in the high voltage level shift circuit.

6.3 Silicon Process Requirements for Secondary Side Controller

The secondary side device is essentially a 12V circuit and the 12V CMOS device arsenal offered by the SOI process illustrated in Fig 6.2.2 plus the bipolar transistors and passive devices available e.g. poly-poly capacitors and high resistivity poly resistors would suffice to create the design. The SOI process has been shown to offer area saving in respect of a BCD process but that does not rule out the possibility of a 12v junction isolated process offering greater die size advantage. However, the common functions identified between the primary and secondary side devices would tend to make it advantageous to use the same process for both designs.

6.4 Device Level Circuit Examples

Fig 6.2.5 "prim_cont_top" illustrates the top level schematic for the primary side controller designed on the SOI process described in section 6.2. This schematic shows essentially the pin out for the device, the ESD structures required for each pin, trimming resistors for the reference voltage and the "core" of the device. Fig 6.2.6 "prim_cont_cct" is the schematic for the "core". The circuit blocks illustrated in the objective specification block diagram and in Fig 4.2 are identifiable in more detail in

this schematic. Detailed device level schematics confirmed functional by simulation exist for the design.

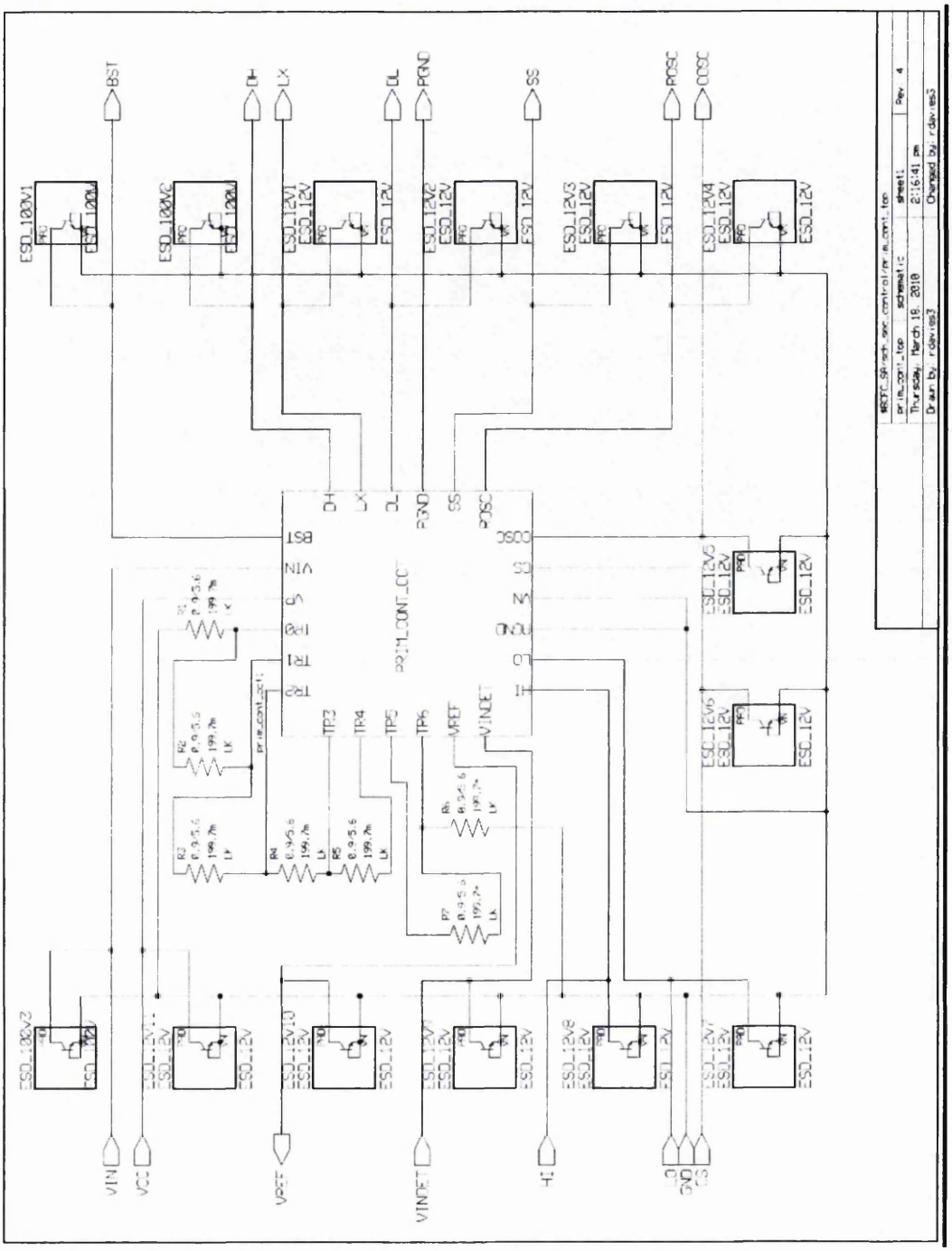


Fig 6.2.5 Device Level Primary Side Controller ESD Schematic

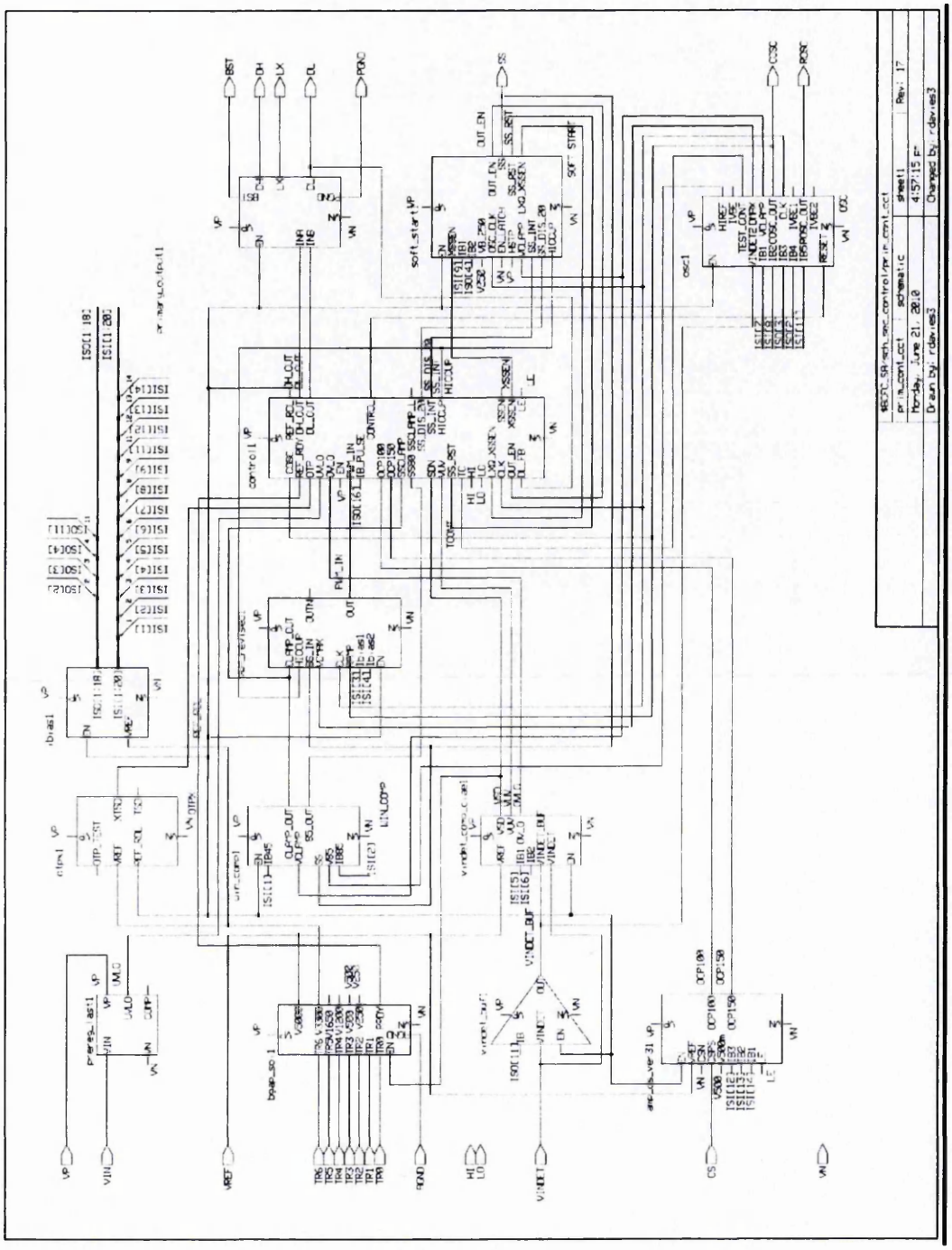


Fig 6.2.6 Device Level Primary Side Controller "Core" Schematic

Fig 6.2.7 "sec_cont_top" illustrates the top level schematic for the secondary side controller designed on the SOI process described in section 6.2. This schematic shows essentially the pin out for the device, the ESD structures required for each pin.

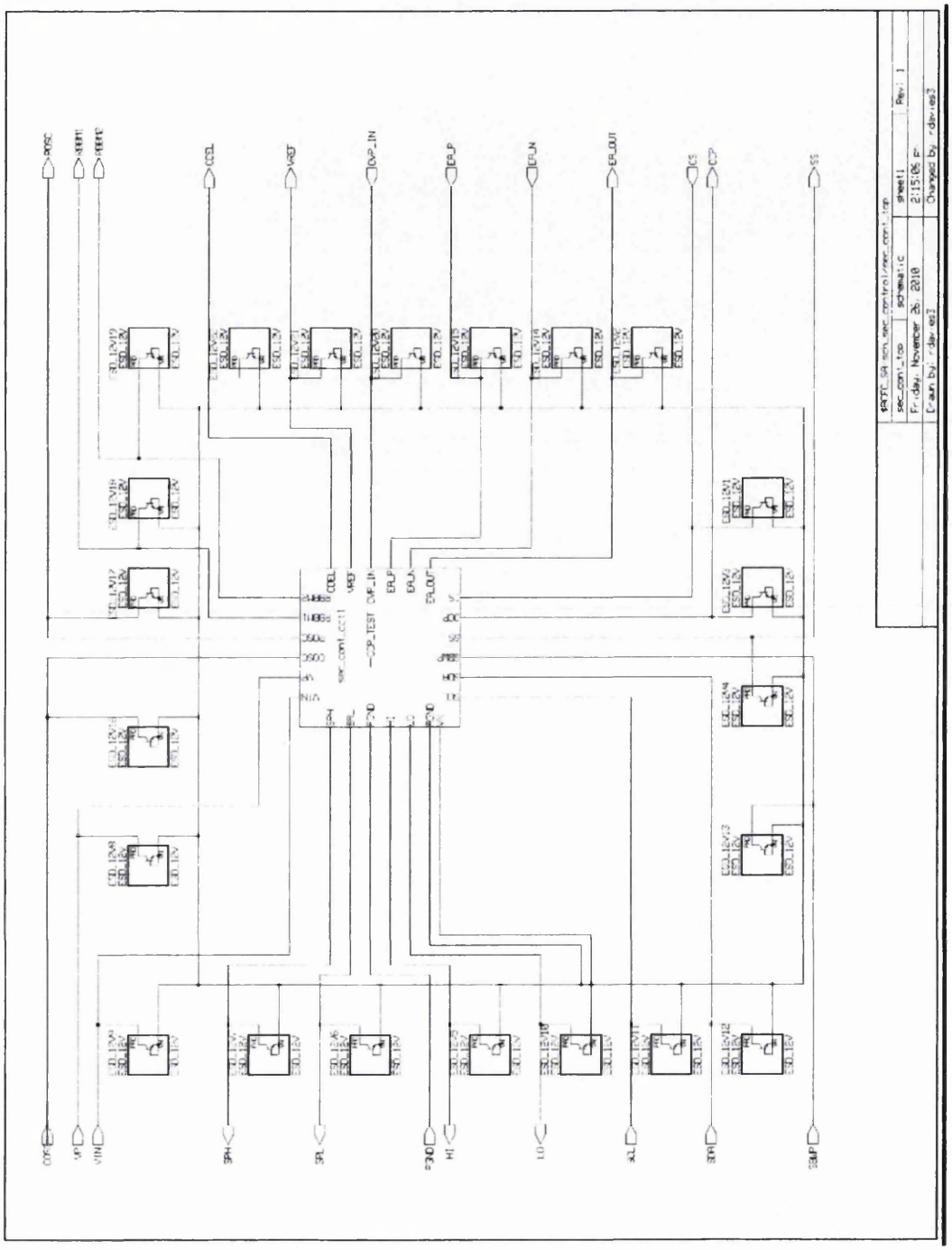


Fig 6.2.7 Device Level Secondary Side Controller ESD Schematic

The absence of trim resistors at this level is a direct result of the PMbus interface included in the design. Fig 6.2.8 "sec_cont_cct" shows the circuit schematic immediately below the ESD level again with identifiable circuit block to the OTS.

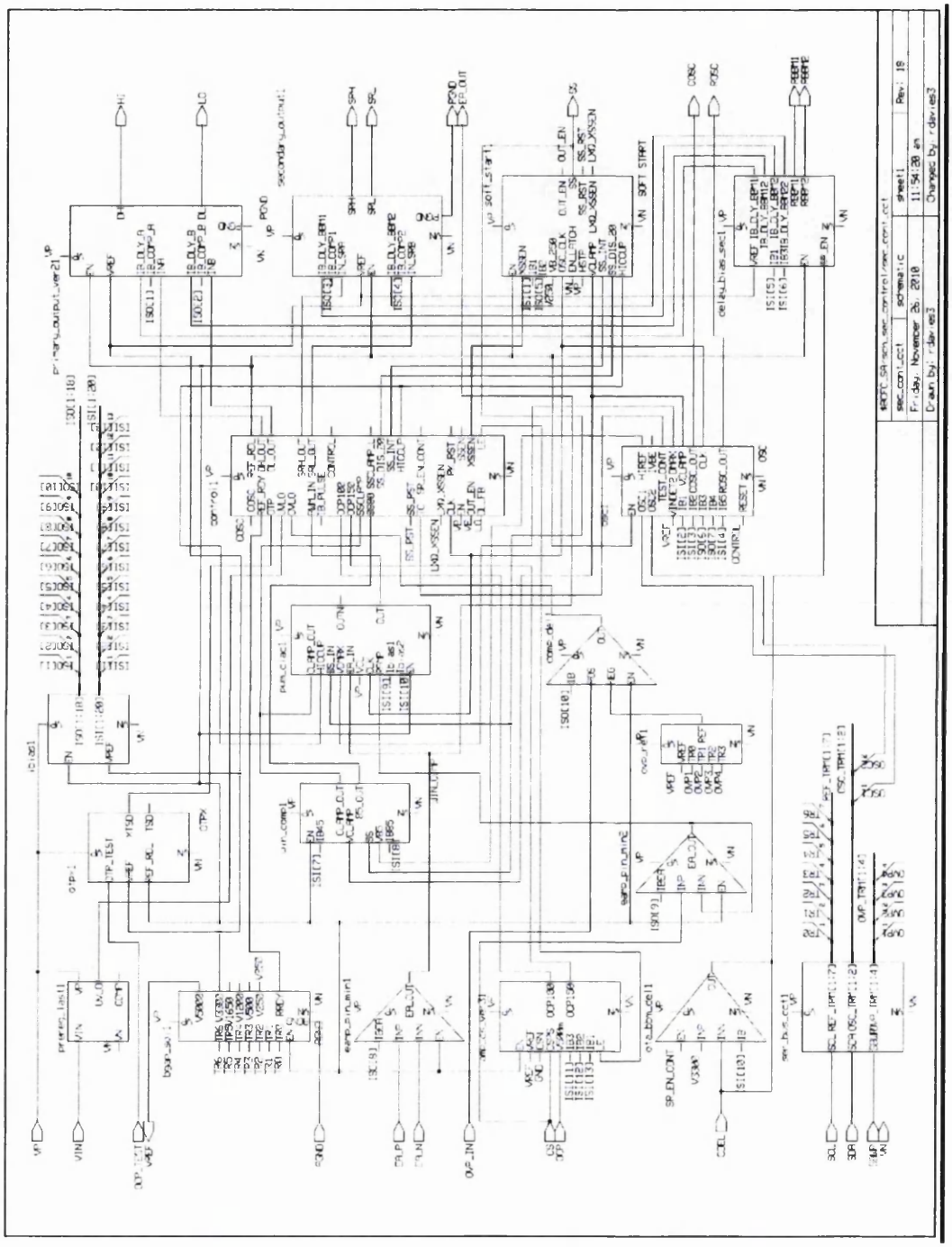


Fig 6.2.8 Device Level Secondary Side Controller "Core" Schematic

7 Conclusions and Future Work

The above design study has demonstrated the feasibility of dispensing with the auxiliary isolated power supply strategy to power a secondary side control device in isolated DC-DC converters. The objective specifications are to be presented for market testing with a view to completion of device level physical design and fabrication.

A primary objective of this work has been the definition and design of an optimum specification for isolated DC-DC converter control circuits. It is understood that across the design community engaged on application level design in this area no single consensus would exist as to the "optimum" arrangement for the design of these power converters and the resulting controller integrated circuit requirements. The further objective has therefore been to provide integrated circuit control devices which do not constrain the application level design engineer to a specific strategy but to offer alternative approaches from the same device with selection defined by external pin connections as opposed to different device offerings based on metal mask variations which imposes increased part number inventories on OEM manufacturers.

The use of current mode control has been assumed on the secondary side controller due to the advantages of inherent feed forward capability and volt second balanced drive to the power transformer. The external connection of the oscillator ramp waveform at the Cosc pin to the CS pin would provide a voltage mode controller should the application level designer so choose but at the cost of the loss of feed forward capability.

In order to offer state of the art converter products such as those referred to in [3] [4] and [26] significant in house design knowledge of power electronics, planer magnetic design, multilayer PCB board design and layout specific to these products is required and is represented by the performance and reliability achieved.

The simulation circuits representing a half bridge converter shown in Fig4.1 and Fig 5.11 are used to demonstrate operation of the controlling integrated circuits and are at no time presented as representing state of the art converter design. This is self evident not only in the use of ideal switches instead of power Mosfets but also in the time constants set to reduce simulation time. The operation of these simulation circuits would be as shown if realistic time constants of tens of mili seconds were used instead of hundreds of micro seconds but would extend the simulation time and memory requirements significantly.

The objective specifications and device level design of the integrated circuits for both the primary and secondary side devices as illustrated in Fig6.2.5 to Fig6.2.7 are presented as viable alternative options in the devices available to the market.

References

[1] Zaki Mooussaoui, Greg Miller "Digital Power Control Highlights" Intersil technical brief WP0589 2003.

[2] Underwriters Laboratories UL60950 "Safety of Information Technology Equipment" ISBN 0-7629-0470-4.

[3] Ericsson Power modules selection guide April 2010 PKM/B/U series. www.ericsson.com/ourportfolio/products/powermodules.

[4] "Ericsson's highly efficient 1/16th brick module provides 1/8th brick performance for upgrades and downsizing". www.ericsson.com/news/archive/2009/090212

[5] B.C.Narveson, A Harris, "Power management solutions for telecom systems improves performance cost and size" Texas Instruments analog applications journal 3q 2007.

[6] "Selection of Architecture for Systems using Bus Converters and POL converters" Ericsson power modules design note 023.

[7] Lee " Computer Aided Analysis and Design of Switch Mode power Supplies" chapter 4. ISBN 0824788036.

[8]] Lee " Computer Aided Analysis and Design of Switch Mode power Supplies" pp 129-130. ISBN 0824788036.

[9] Abraham.I.Pressman "Switching Power Supply Design" pp chapters 2 and 3. ISBN 0-07-052236-7.

[10] Richard Redl "Feedforward Control of Switching Regulators" APEC 09 seminar 1.

[11] Abraham.I.Pressman "Switching Power Supply Design" pp chapter 12. ISBN 0-07-052236-7

[12] Christopher Basso, ON Semiconductor "Stability Analysis and Loop Control in Switching Power Supplies"APEC 09 seminar 13.

[13] Abraham.I.Pressman "Switching Power Supply Design" pp chapter 5.5 ISBN 0-07-052236-7

[14] Silicon Labs Inc Austin Tx "When to use a digital isolator Vs an Optocoupler".

[15] Analog Devices Inc ADuM5242 data sheet.

[16] Intersil ISL6742 data sheet FN9183.2 October 2008 p15 fig 14.

[17] Bob Mammano " Isolated Power Conversion : Making the case for Secondary Side Control" Texas Instruments Inc, EDN Magazine June 7th 2001. www.ednmag.com.

[18] Ericsson Power Modules AB "Implications of Digital Control and Management for High Performance Isolated DC-DC Converter" March 2007 MPM-07:000199 Uen Rev A.

[19]] Ericsson Power Modules AB " Is Digital Power Moving Forward" Technical Paper PCIM China 2008.

[20] EDN Power Technology "Digital Power Management Market Crossing the Threshold" Linnea C Brush August 2005.

[21] Silicon Labs Si8250/1/2 data sheet Fig 7 page 17
www.silabs.com/support documents/technicalDocs/si8250.pdf

[22] Mospower Applications, Siliconix Ltd pp chapter 3.2 "Switching Characteristics". ISBN 0-930519-00-0.

[23] "Introduction to the PMBus" Robert V White, Artysyn Technologies System Management Interface Forum 2005 www.powerSIG.org

[24] Edward S Oxner " Power FETS and Their Applications" p 151 Prentice Hall ISBN 0-13-686923-8.

[25] Analog Devices ADM1041 data sheet "Secondary Side Controller with Current Share and Houskeeping"

[26] Ericsson Power Modules AB PKU400 series data sheet. EN/LZT 146 308 R4B July 2008.

[27] "Design and Performance Evaluation of Low voltage High Current DC/DC on board modules" Yuri Panov, Milan M.Jovanovic, IEEE Transactions on Power Electronics vol 16 No.1 January 2001.
[28] "Unclamped Inductive Switching Rugged Mosfets For Rugged Environments" AN601 Vishay Siliconix document number 70572.

[29] Bob Bell, Don Alfano National Semiconductor "Digital Isolators: A Space Saving Alternative to Gate Drive Transformers in DC-DC Converters". How2Power March 2010 issue.

[30] P.Alou, A.Soto,J.A.Cobus, M Rascon "Dual Voltage Quarter Brick DC-DC Converter with Control in Secondary Side" IEEE 2005 transactions 0-7803-8975-1.

[31] PICOR PI3101 data sheet http:\\cdn.vicorpower.com/documents/datasheets/Picor/ds_pi3101.pdf.

[32] http://en.wikipedia.org/wiki/SPICE

[33] Steven M Sandler "SMPS Simulation with Spice 3" McGraw-Hill isbn 0-07-913227-8.

[34] Steven M Sandler "SMPS Simulation with Spice 3" McGraw-Hill isbn 0-07-913227-8. Chapter 2 fig 2.5.

[35] http://www.mentor.com/uk/

[36] http://www-device.eecs.berkeley.edu/~bsimsoi

[37] George Young, Gerry Tomlins Commergy Ltd "Improving Power Conversion Efficiencies" Digital Power Forum 06 Richardson TX.

[38] Carl Chatfield Timothy Johnson "A Short Course in Project Management" http://office.microsoft.com/en-us/project-help/a-short-course-in-project-management-HA010235482.aspx.

[39] B Murari, F Bertotti, G.A.Vignola (Eds.) "Smart Power ICs Technology and Applications" Chapter 1.4. Springer isbn 3-540-60332-8.

[40] B Murari, F Bertotti, G.A.Vignola (Eds.) "Smart Power ICs Technology and Applications"Chapter 2.2.2 Springer
ISBN 3-540-60332-8

[41] R Jacob Baker, Harry W.Li, David E.Boyce "CMOS Circuit Design, Layout And Simulation". Chapter 22.2.1, IEEE Press Series ISBN 0-7803-3416-7
[42] B Murari, F Bertotti, G.A.Vignola (Eds.) "Smart Power ICs Technology and Applications"Chapter 8.6.2 Springer ISBN 3-540-60332-8

[43] http://en.wikipedia.org/wiki/Sawtooth_wave

[44] Grey, Hurst, Lewis, Meyer "Analysis and Design of Analog Integrated Circuits" p323 Wiley ISBN 0-471-32168-0.

[45] Phillip E Allen, Douglas R Holberg "CMOS Analog Circuit Design" p227 ISBM0-19-510720-9.

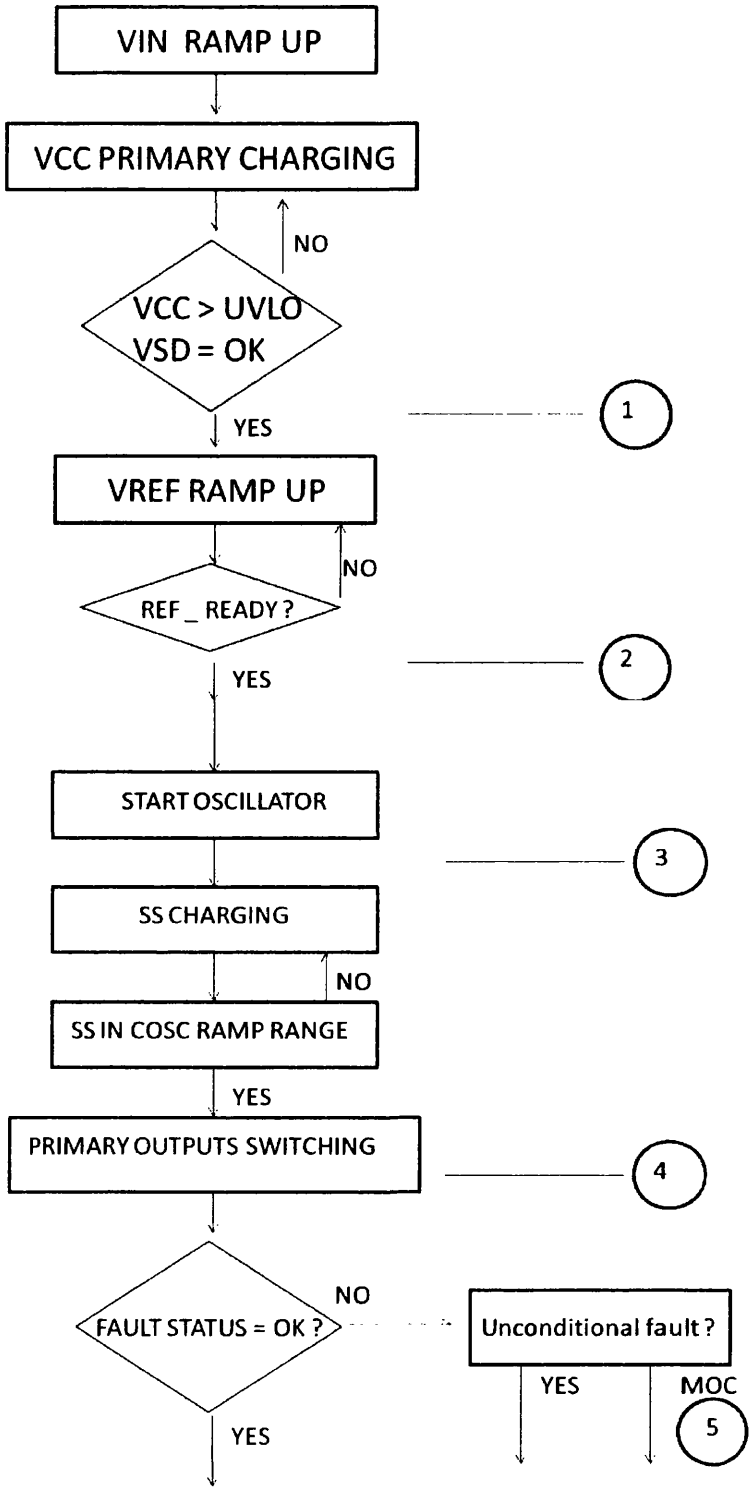
[46] R Jacob Baker, Harry W Li, David E Boyce "CMOS Circuit Design and Simulation" chapter 7.2.1 IEEE series microelectronic systems ISBN 0-7803-3416-7.

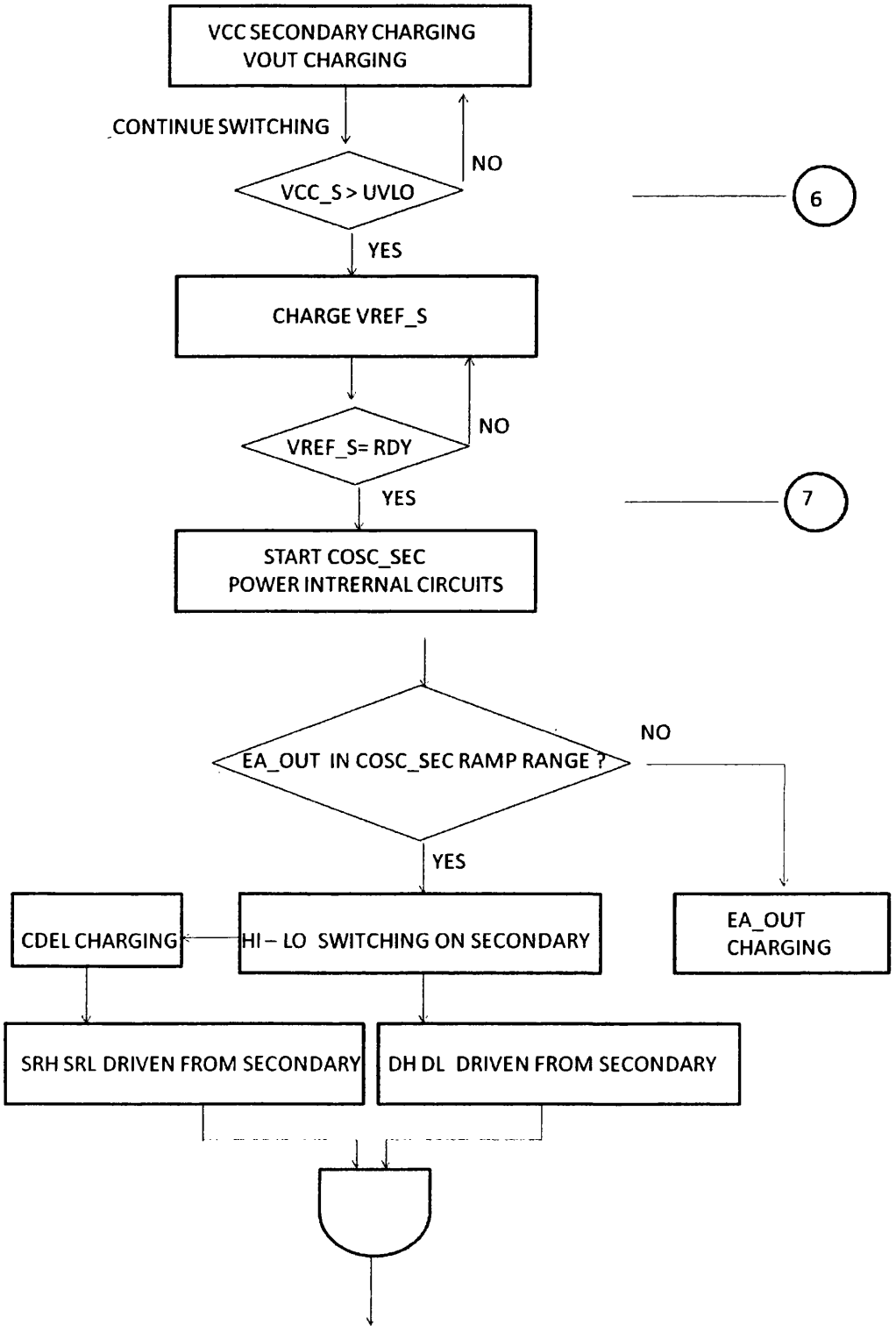
[47] "Introduction to the PMBus" Robert V White, Artysyn Technologies System Management Interface Forum 2005 pages 22 – 32 www.powerSIG.org.

[48] B Murari, F Bertotti, G.A.Vignola (Eds.) "Smart Power ICs Technology and Applications" Chapter 7.5.8 page 331. Springer ISBN 3-540-60332-8

[49] US Patent 2009/0196075 "Fly Forward Converter Power Supply" Douglas Paul Arduini.

[50] NVE Corporation Application Bulletin "AB-7" "GMR in Isolation" March 2008.


VIN RAMP UP
VCC PRIMARY CHARGING
NO
VCC > UVLO
VSD = OK
YES
1
VREF RAMP UP
NO
REF _ READY ?
YES
2
START OSCILLATOR
3
SS CHARGING
NO
SS IN COSC RAMP RANGE
YES
PRIMARY OUTPUTS SWITCHING
4
NO
FAULT STATUS = OK ?
Unconditional fault ?
YES
MOC
5
YES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VOUT CHARGING
CONTINUE SWITCHING
NO
VCC_S > UVLO
6
YES
CHARGE VREF_S
NO
VREF_S= RDY
YES
7
START COSC_SEC
POWER INTRERNAL CIRCUITS
NO
EA_OUT IN COSC_SEC RAMP RANGE ?
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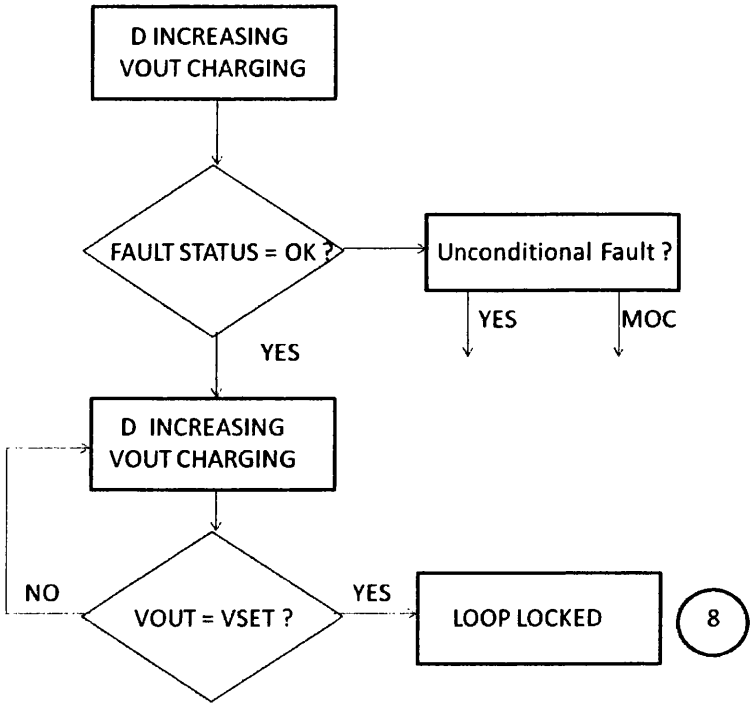
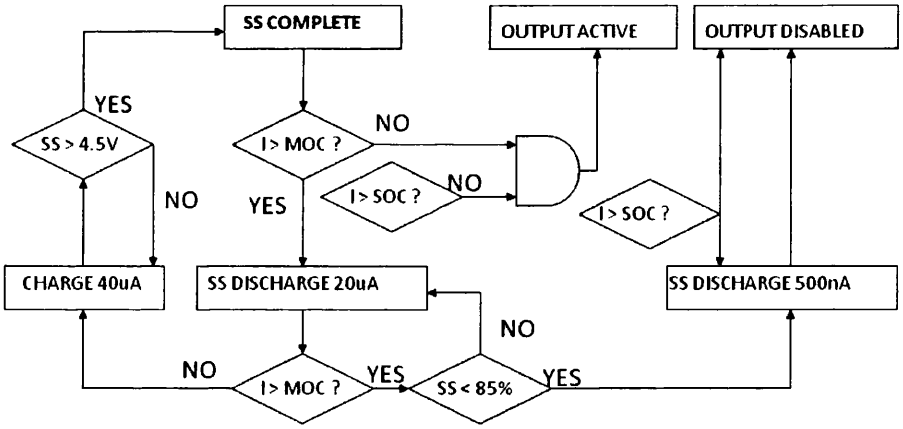
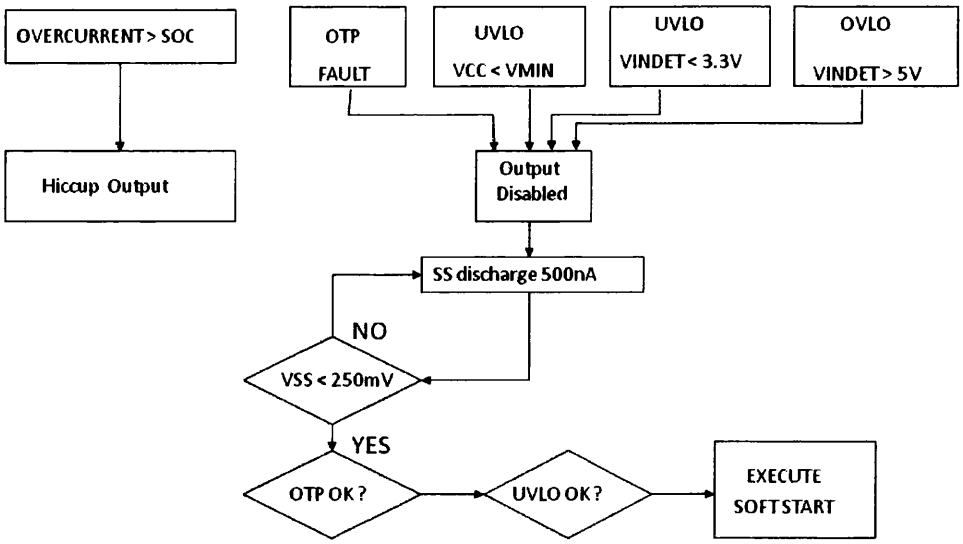
CDEL CHARGING
HI – LO SWITCHING ON SECONDARY
EA_OUT
CHARGING
SRH SRL DRIVEN FROM SECONDARY
DH DL DRIVEN FROM SECONDARY

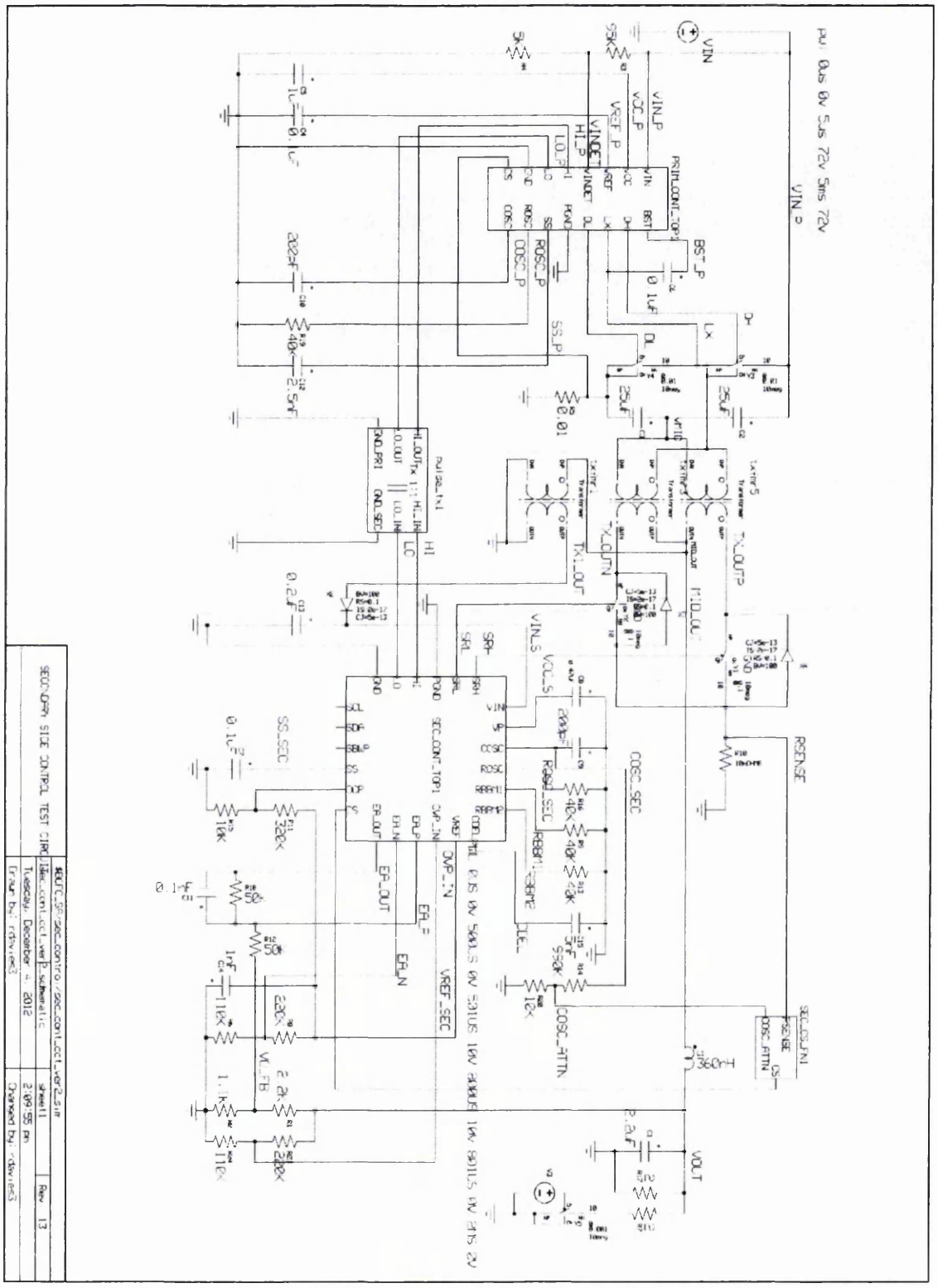


State Diagram – Moderate Over Current



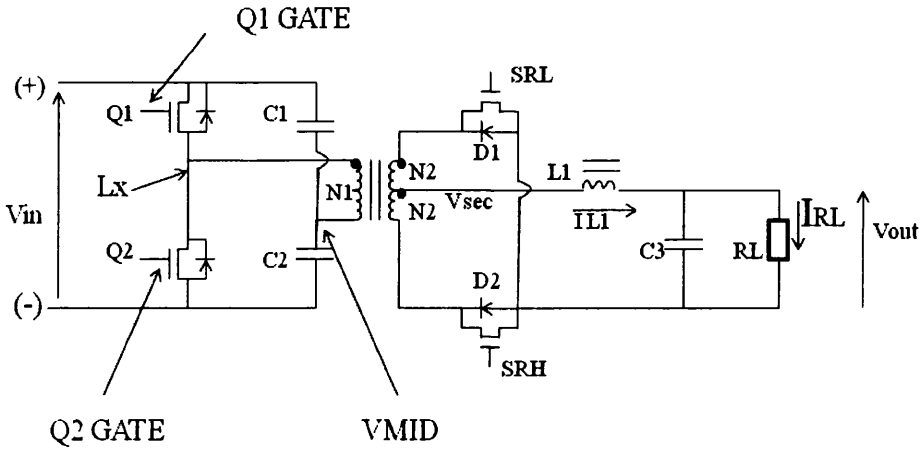
State Diagram – Unconditional Faults





APPENDIX C

Half Bridge Converter - Simple schematic



APPENDIX D

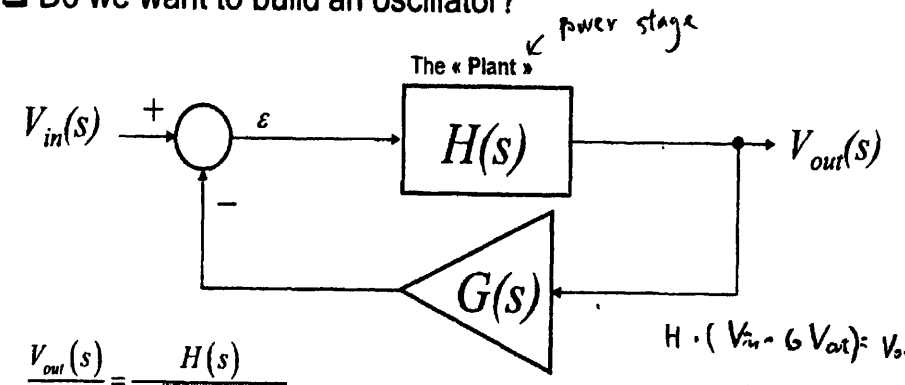
Extract from [12]

What do we expect from a DC-DC Converter ?

1. A stable output voltage, whatever loading, input, temperature and aging conditions.
2. A fast reaction to an incoming perturbation such as a load transient or an input voltage change.
3. A quick settling time when starting up or recovering from a transient state

Positive or negative feedback?

- Do we want to build an oscillator?



$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{H(s)}{1+H(s)G(s)}$$ → Open-loop gain $T(s)$.

$H \cdot (V_{in} - G V_{out}) = V_{out}$

$H V_{in} = (1 + HG) V_{out}$

$$V_{out}(s) = \lim_{V_{in}(s)\to 0}\left[\frac{H(s)}{1+G(s)H(s)}V_{in}(s)\right]$$

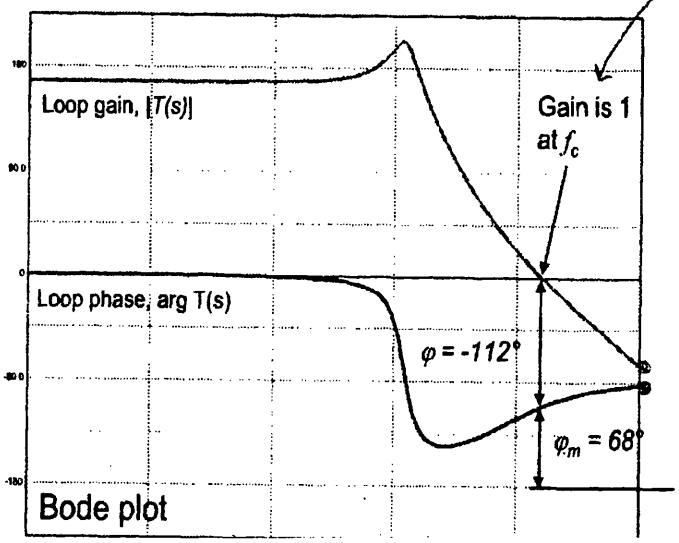
To sustain self-oscillations, as $V_{in}(s)$ goes to zero, quotient must go infinite

$\to 20\log 1 = 20 \cdot 0 = 0$ dB

$$1+G(s)H(s)=0 \longrightarrow \begin{cases} |G(s)H(s)|=1 \\ \angle G(s)H(s)=-180° \end{cases} \longrightarrow \text{Nyquist: } -1, j0$$

Conditions for steady-state stability

- We do not want to create an oscillator!
- Conditions for non-permanent oscillations are:
  - total phase rotation less than -360° at the crossover point



Total phase delay at f_c:

-112° $H(s)$ power stage
-180° $G(s)$ opamp

total = -292°

Stable!