Charge writing on nanocrystalline tin dioxide nanoparticles.

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Charge Writing on Nanocrystalline Tin Dioxide Nanoparticles

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Submitted to the University of Wales in the fulfilment of the requirements for the degree of Doctor of Philosophy

2007

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ACKNOWLEDGEMENT

I would first like to express my deepest gratitude to my supervisor Prof. Steve Wilks for giving me the opportunity to undertake this research at Swansea University. The course of research has enhanced not only the knowledge of the subject but also the attributes that would equip me for my future path. Also I owe a sincere debt to Dr. Thierry Maffeïs, who initially discovered the charge writing phenomena. Without his constant assistance and the number of hours invested in me, this work would not have been possible. His depth of knowledge and analytical techniques has never ceased to amaze me. I would also like to thank Dr. Vincent Teng for all his knowledge imparted and support during the course of the study.

Additionally I would like to thank Dr. Mark Penny for his practical help in the lab whilst I became familiar with the UHV system. He is the joyful person, who has been more than helpful whenever I encountered a barrier in the research or doubts in my research, till the last part of challenge in dissertation. Also, special thanks to Dr Richard Cobley for his precious time in assistance for my dissertation.

None of this would have been possible without the constant support of my family, Jasmin Liu and friends. Without a shadow of a doubt I would not have got this far without their limitless confidence in me. Their patience and encouragement during the time of disappointment, despair and frustration brings out a new surge of energy in me to carry on. I know how extremely blessed I am to have such a supportive family and friends, which things would be so much harder without them.

Also, to thank Overseas Research Student (ORS) Scholarship (reference number: 2003048004), for none of this would have happen without the financial support.

Most importantly, I want to thank God for His everlasting love and spiritual support throughout the challenging years during research. *'It is God who arms me with strength and makes my way perfect' (Psalm 18: 31-32)*

ABSTRACT

Nanotechnology is an emerging field that shows the potential to bring the development in the various aspects of research to a new level. However, this evolution relies on the advancement in fabricating and locating material on surfaces with nanoscale precision. Self assembly is believed to be the solution to overcome the challenges and is presently being pursued in various guises, one of which is nanopatterning.

Nanocrystalline tin dioxide is an n-type wide band gap semiconductor, which is commonly used for gas sensing applications. In Swansea University, the research on gas sensors had led to the discovery that by applying negative voltage pulses from a Scanning Tunnelling Microscope (STM) tip, it is possible to pattern the 8nm nanocrystalline tin dioxide grains. This results in features that are of average size of about 5nm in height and 17nm in width. Further research reveals that close to 100% success rate can be obtained with -6.0V tip voltage for 100μs, and the features patterned could be erased by scanning with a positive tip voltage. Moreover, the apparent height of the features on STM scans is dependent on the scanning tip voltage; and the grid Scanning Tunnelling Spectroscopy (STS) revealed a higher current flow into the patterned features. These experiments are in agreement and suggest that the patterned features are electronic in nature, as opposed to topographic.

This thesis investigates the nanopatterning phenomena exhibited by tin dioxide grains at high temperature using the techniques of STM/STS, and with the aid of oxidising and reducing gases. At elevated temperature, nanopatterning on tin dioxide reveals a "charge spreading" effect, resulting in bigger feature size and lower current flowing through the patterned features. The studies also demonstrated the possibility to trigger the charge writing mechanism whilst scanning with a higher magnitude of tip voltage, charging large areas of the surface. The research on gas exposures with oxygen (oxidising) and carbon monoxide (reducing) gas favours the proposal that patterned features are electronic in nature; as well as acting as a feasibility study for the possibility of using the patterns for molecular docking applications. The

investigation on the erasing process showed that a high magnitude voltage will result in removal of individual charged tin dioxide grains from the surface instead of extraction of electrons. Suggestions for future work that could be explored based on the findings presented in this study are presented in the last section of the thesis.

CHAPTER 1 INTRODUCTION

Since the evolution of solid state devices, which brought along the development of microelectronic industry, our daily life has never been the same again. The technology advancement has greatly facilitated and brought comfort and convenience to our everyday life. The necessary daily task such as banking, telecommunication, even shopping has never been so advanced. This great development has improved the entertainment industry significantly such that the visual and audio aspects have stunned the world year after year. All the continuous breakthroughs and improvements are highly attributed to the rapid growth in the research of solid state electronic devices. However, all the common electrical appliances such as digitised microwave ovens, flat screen televisions, laptop personal computers, handphones and many more were nothing but a dream few decades ago.

In 1959, the famous talk "There's plenty of room at the bottom" by Richard P. Feynman[1] presented a whole new evolution to the world, from electronics to biochemistry, he presented visions and ideas that awed the audience, as shown by these bold statements:

> *"What would our librarian at Caltech say..... if I tell her that, ten years from now, all the information that she is struggling to keep track of – 120000 volumes..... can be kept on just one library card!"*
>
> *"If we wanted to make a computer that had all these marvellous extra qualitative abilities, we would have to make it, perhaps, the size of the Pentagon..... But there is plenty of room to make them smaller"*
>
> *"You put the mechanical surgeon inside the blood vessel and it goes into the heart and 'looks' around....."*

In just the time frame of less than 50 years, some of these visions have been fulfilled with great achievements and brought great benefits to the world in all areas of

research. Quoting from Neil Armstrong, what Richard P. Feynman said in 1959 was definitely "*One small step for man, one giant leap for mankind*".

After Richard Feynman mentioned about '*plenty room to make them smaller*', it became a direction where the development was heading for the next few decades. Among the many researchers, Gordon E. Moore, the Intel co-founder shared this same vision. In 1965, he supported the miniaturisation of transistor count per chip that predicted the number of transistor on a chip doubles about every two years. This exponential growth of transistor counts per chip is commonly known as Moore's law[2] (Figure 1-1).

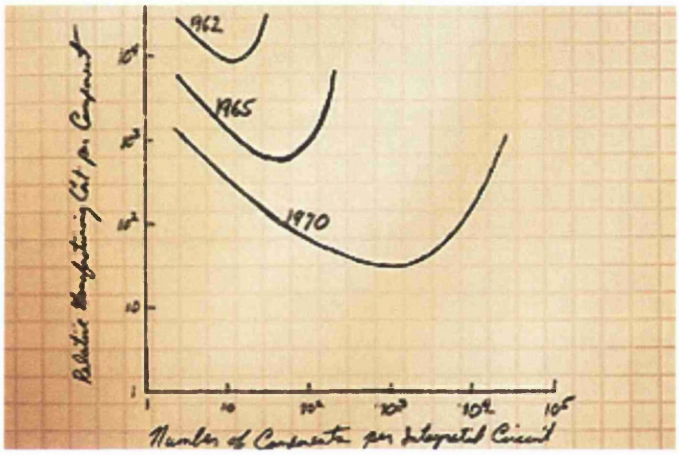

Figure 1-1 Moore's Law

His report focused on cramming more components onto semiconductor integrated circuits, which had demonstrated high reliability and improved performance, greatly simplified design and reduced cost. He reported that the cost per component is nearly inversely proportional to the number of components required for circuit on the semiconductor integrated circuits, which are the reasons for the boom in sales in the semiconductor market[11].

Intel has indeed achieved this vision (Figure 1-2). The number of transistors present on the computer processor had increased exponentially over the years, which had brought great convenience and speed to the present computing world.

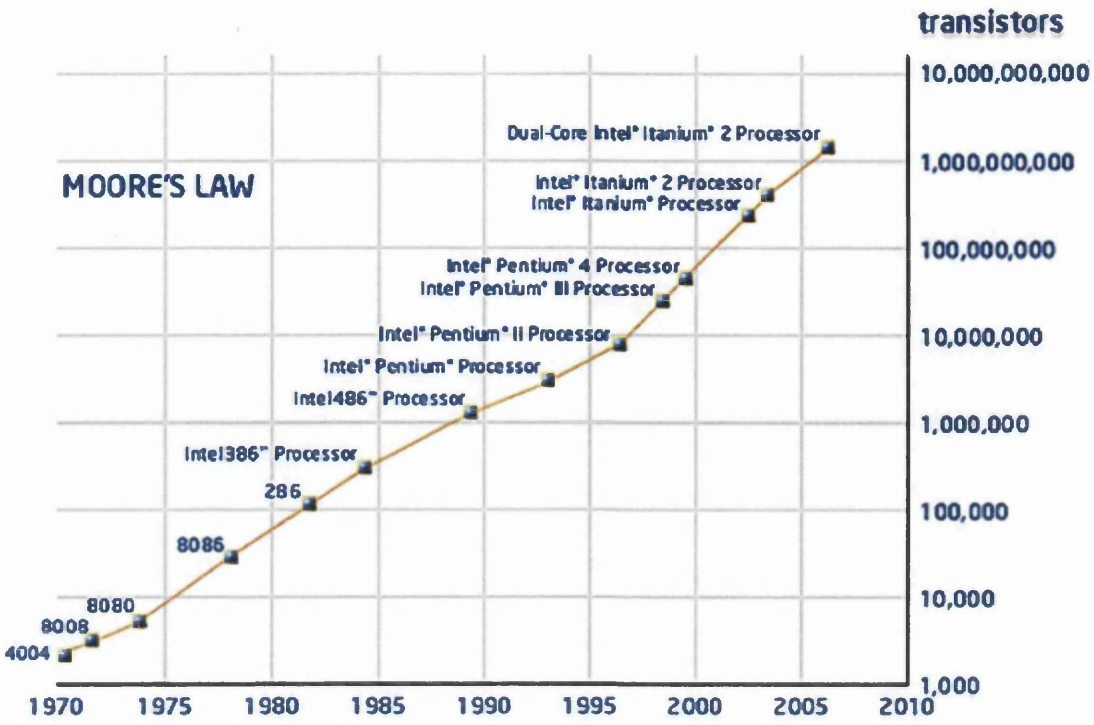

Figure 1-2 Moore's Law Vision Achieved at Intel

However, in a recent presentation by Gordon E. Moore, he admitted that Moore's law will meet its limit[3]. The power leakage is one of the major challenges for Moore's Law (Figure 1-3). The power loss as heat given off per cm^2 has been increasing and heat generated by many chips is too much for the cooling surface. Furthermore, as the size of the transistor reduced, the thickness between gates is getting smaller, which the thin insulating layers can breakdown due to electrons tunnelling through.

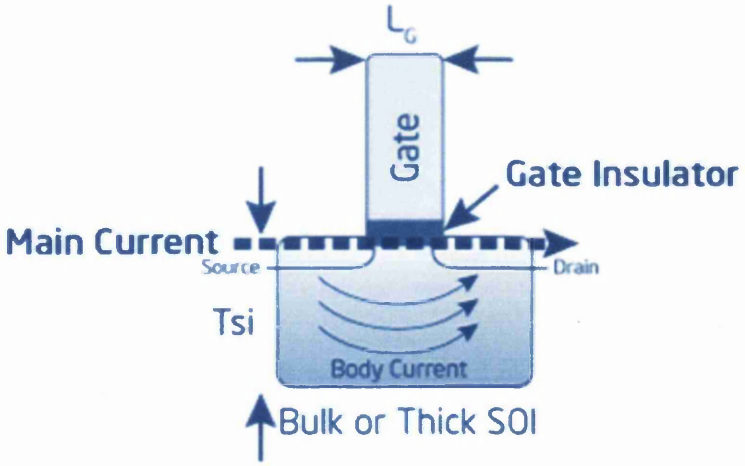

Figure 1-3 Power Leakage on a Planar Transistor

Therefore, Intel is presently looking into the Tri-Gate transistor structure (Figure 1-4), which is fabricated either on Silicon on insulator (SOI) substrate or standard bulk-silicon substrate. It has a gate electrode on the top and two gate electrodes on the sides of the silicon body. This transistor architecture can significantly improve the electrostatics and short-channel performance, thus provide the room for further scaling down of the device, hence making room for more transistors within the same area. With this idea, Gordon Moore ended the presentation with the statement: *'No exponential is forever but we can delay "forever"'.*

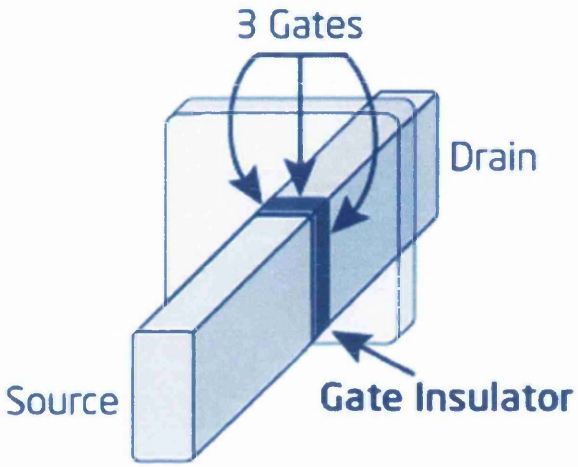

Figure 1-4 Tri-Gate Transistor Structure

While Gordon Moore is facing the challenge to lengthen the time scale to the limitation on Moore's law, Tze-chiang Chen from IBM research has posted a question in a recent presentation in New Delhi, India. "*Is nanotechnology the solution to limitation in device scaling?*"[4]. The word "Nanotechnology" was first introduced in 1974 by Norio Taniguchi of the University in Tokyo, Japan[5], which used it to refer to the ability to engineer materials precisely at nanoscale. The prefix nano in the word nanotechnology means a billionth ($1x10^{-9}$), meaning nanotechnology involves the manipulation and control of various structures of matter having dimensions of the order of a billionth of a meter.

It is not clear when humans first came into contact with nanosized material, but it is known that in the 4th century A.D. Roman glassmakers had been fabricating glasses containing nanosized metals[6]. Figure 1-5 shows an artefact called the Lycurgus cup from that period, which is made from soda lime glass containing gold and silver nanoparticles of size about 70nm and in the ratio 1:14[7]. At the nanoscale, the optical properties of the material are different from their macroscale counterparts, where the absorption wavelength in visible light shifts to shorter wavelength with respect to the size of the material[8]. Hence when a light source is placed inside the Lycurgus cup, the selective absorption of light by the nanoparticles will change the cup to red colour but looks green when the light is reflected off it.

Figure 1-5 Lycurgus Cup

At the IBM research centre, several nanotechnology research projects have been conducted throughout the past decade. The centre focuses on nanomaterials, trying to manipulate and control the unique properties so as to bring forth the potential in nanotechnology to the world.

To improve on the security in communication, IBM research centre's quantum cryptography project[9] aims to provide security on communications over insecure channels. The idea is to encode the information in the quantum states of individual optical photons and transmit them to the receiving end, which would sort the photons according to their states and send them to detectors capable of registering the arrival of single photons with high efficiency and low noise. This guarantees the security by the fundamental quantum properties of light rather than by computational complexity or physical barriers to interception. This development depends critically on the quality of the light detector, which needs to have both high efficiency for detecting single photons and very low dark-count probability (the probability that a noise count occurs in the absence of any photons). The light detector was successfully built and the technology was licensed in October, 2005.

Another successful research project has been made in 2002, where IBM scientists built the world's smallest operating computing circuits by creating a precise pattern of carbon monoxide molecules on a copper surface[10]. These tiny structures were designed to demonstrate the fundamental digital-logic OR and AND functions (Figure 1-6), data storage and retrieval, and the "wiring" necessary to connect them into functioning computing circuitry. By moving a single molecule, it initiates a cascade of molecule motions, just as topping a single domino and ended up with a pattern that fall into place in sequence. This research idea is mentioned as data propagation function by Richard Turton[11] when showing the possible contribution from quantum dots.

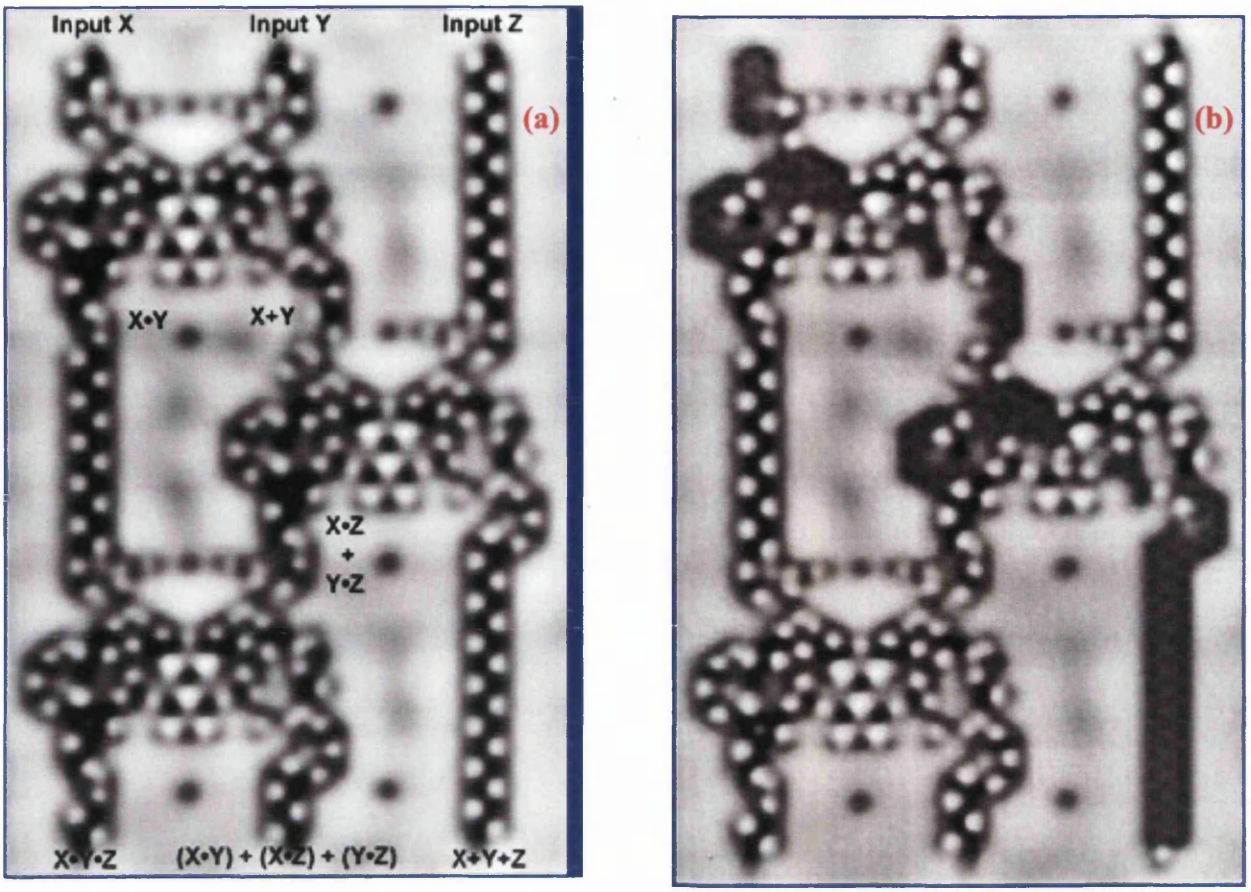

Figure 1-6 (a) Logic 3-input sorter in the initial configuration. Overlayed symbols (+ for OR, dot for AND) show the logic operation of the sorter in stages. The 3-input sorter comprises three 2-input sorters. This device computes the logic AND, the logic OR, and the logic MAJORITY simultaneously. (b) Logic 3-input sorter after Input X was triggered and has propagated to the OR output on the right

Development continues on the size scaling on the logic gates. Another research project aims at achieving quantum logic with Barium ions was initiated based on the idea from Richard Feynman that quantum mechanics might lead to a qualitatively new kind of computer that is far more powerful than any classical devices[12] (Figure 1-7). At the moment, this project is directed at understanding what processes limit the superposition state lifetime (decoherence), which is the most important limiting factor in quantum computation.

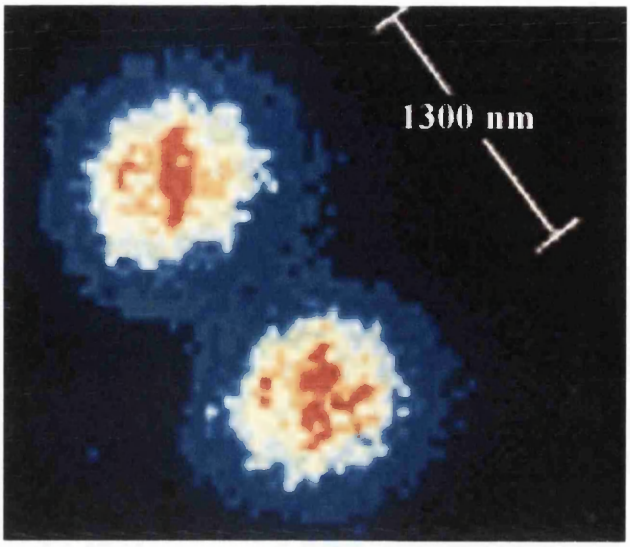

Figure 1-7 Two Barium Ions in a Trap

Abhilash Sugunan[7] mentioned that '*Without stone cutting tools, stones would not have been very helpful to man*'. Similarly, in order to manufacture devices from nanomaterials, it is vital to have new fabrication technique and equipment that is able to provide understanding of the properties of these materials. The rapid growth in the research on nanomaterials for the past decade was highly facilitated by the development of Scanning Probe Microscopy (SPM). Techniques such as Scanning Tunnelling Microscopy (STM), Atomic Force Microscopy (AFM), Scanning Near-Field Optical Microscopy (SNOM) provides the information on the physical, chemical, electronic and optical properties of the nanomaterials.

This thesis presents another aspect of research, charge writing, using one of the state-of-art techniques mentioned above, STM. In recent years, due to the many possible applications across a wide range of disciplines, the manipulation and control of the size and shape as well as composition of submicrometre particles and large molecules attracts more scientific and commercial interests. In this aspect, self assembly is gaining the attention for fabricating devices at the nanoscale. However, it is very difficult to hold molecules onto a flat substrate[13] and it is a challenge to provide solutions for all variety of research and development programs, hence this put forth the idea of 'writing' a charge pattern onto a substrate[14].

Even though charge writing provides the selectivity of patterning the surface chemically, structurally or electronically on a nanometer scale, there is still a significant challenge in understanding the mechanism behind this controlled assembly[15]. This thesis presents a study of the charge writing phenomenon on tin dioxide nanoparticles that offers very competitive feature size. Also, the long charge retention time observed could provide the solution to some problems which occur in other charge writing research. If the nanopatterning performed on the material has indeed induced the charge confinement within the grain of the material, it could offer remarkable applications in nanoscale catalysis, molecular docking, ultra-high density data storage and even quantum logic gates.

This thesis is aimed to further the understanding of the possible mechanisms behind nanoscale patterning of tin dioxide nanocrystalline surfaces and is structured as follows:

Chapter 2 – Literature review

Chapter 3 – Theoretical appreciation for Scanning Tunnelling Microscopy (STM) and Scanning Tunnelling Spectroscopy (STS)

Chapter 4 – Experimental procedures employed over the course of this project, from sample preparation to electrochemical etching of STM tips.

Chapter 5 – Result 1 - Nanopatterning

Chapter 6 – Result 2 – Gas Exposure and Possibility of Grain Removal

Chapter 7 – Conclusion and Future Work

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CHAPTER 2 LITERATURE REVIEW

As mentioned in the previous chapter, the birth of Scanning Probe Microscopy (SPM) has brought forth a new era into nanotechnology research. The progress of the research depends on the ability to fabricate and locate the particles/molecules on surfaces with nanoscale precision. This explains the reason for the great interest in self-assembly[1,2] of structures, which is believed to be the way in achieving these targets. Several methods provide physical surface modification through damage, deposition of materials from the STM tip, or diffusion of surface atoms towards the STM tip that show nanoscale lithography. This chapter provides the theoretical foundations that are related to the project, as well as work by other institutions in similar research areas.

2.1 TIN DIOXIDE PROPERTIES

Tin dioxide (SnO_2) is an n-type, wide band-gap (E_g = 3.6eV) semiconductor with the rutile structure. Figure 2-1 shows the ball model illustration of a nearly perfect (ideal) tin dioxide (110) surface[3], where the green particles represent Sn^{4+} cations, while the blue ones represent the O^{2-} anions. The arrangement of the unit cell are $[(O^{2-}) (2Sn^{4+}+2O^{2-}) (O^{2-})]$. It was mentioned in the studies that the oxygen vacancies on the (110) surface actually increases the conductivity on the surface by more than two orders of magnitude with respect to the bulk conductivity. And this conclusion matches the research where the oxygen vacancies act as donors[4], hence resulting in the electrical conductivity of the material[5].

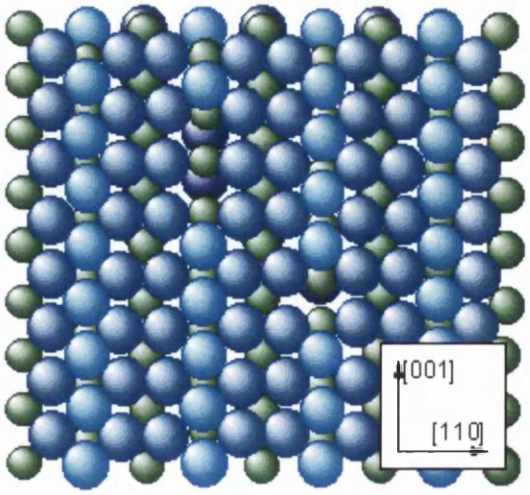

Figure 2-1 Structure of a near ideal tin dioxide (110) surface

2.2 GAS SENSING APPLICATION

In a review article[6], it is mentioned that solid state sensors[7] can be classified under two categories, the catalytic Pellistor sensors which depend on small temperature rises resulting from exothermic reactions and thus produce very small resistance changes in wire filaments, as well as the semiconductor sensors that are characterised by very large changes in resistance. Among the latter, tin dioxide is widely recognised to be the most commonly used material and of much higher sensitivity than catalytic Pellistor sensors. The long life span of tin dioxide sensors and low cost also contribute to their popularity.

In the field of gas sensing, tin dioxide is mostly used in its polycrystalline form, where layers of tin dioxide grains are deposited on a pair of electrodes on an alumina substrate (Figure 2-2(a)), which would allow the measurement of the change in resistance of the film. A platinum heater is usually found below the substrate (Figure 2-2(b)), to heat the sensor to operating temperature and to remove adsorbents and reactivate the sensor during operation.

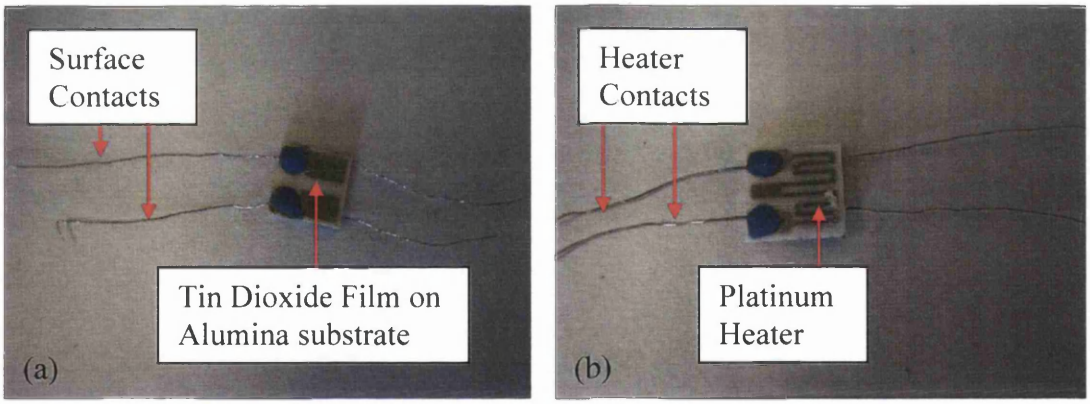

Figure 2-2(a) Top view of a gas sensor substrate (b) Bottom view of a gas sensor substrate

The sensitivity of the sensor depends greatly on the thickness of the tin dioxide layer, number of surface states, doping of elements that direct the sensitivity of the sensor to certain gases, grain size and the barrier height between grains.

2.3 GAS SENSING MECHANISM

Knowledge of the gas sensing mechanism provides insight into how the electrons behave in polycrystalline SnO_2. When oxygen species come into contact with the surface, they are absorbed onto the material surface and the electrons in the material surface are transferred to these chemisorbed oxygen species and create a depletion region within the tin dioxide grains. This increases the surface potential barrier which the electrons need to overcome for electric current to flow (Figure 2-3). This plays an important part in the gas sensing, for it determines the overall resistance[8] of the sensor by controlling the electron transfer between the nanoparticles.

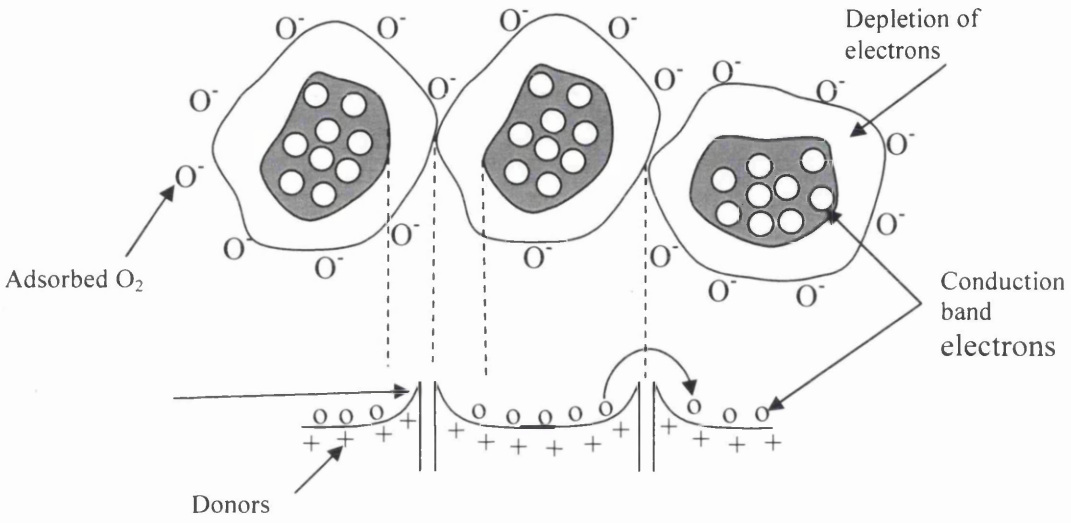

Figure 2-3 Grain of semiconductor showing the intergranular potential barrier

During the process of sensor fabrication, the tin dioxide film is annealed in a furnace, which results in sintering between the nanoparticles. This creates "sinter-necks" (narrow linkage path between adjacent grains at the grain-boundaries) between the grains (Figure 2-4) and these sinter-necks provide better control of the current flow between grains and improve the overall conductivity and sensitivity[9,10].

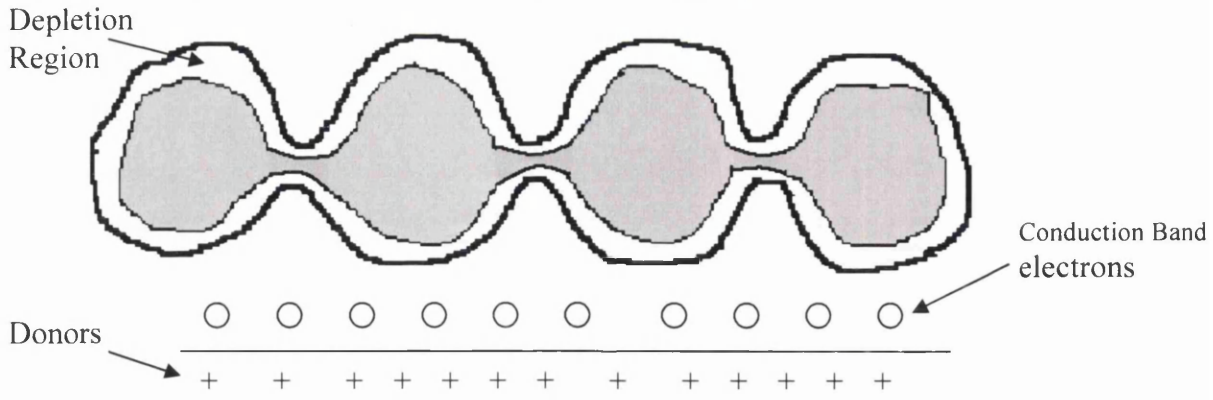

Figure 2-4 Illustration of intergranular relationship between sintered grains

The sinter-neck provides an easier path for the electrons to travel between grains, lowering the overall resistance of the sensing film. However, the narrow routes between the grains will change during gas sensing process. Looking at the grains joined by sinter-necks shown in Figure 2-5, when the sensor is exposed to oxidising gas such as oxygen gas (O_2), the depletion region is expanded due to more electrons taken by the adsorbed oxygen species. If sufficient oxygen came in contact with the surface, more electrons will be removed and the depletion region would grow to the extent that the narrow sinter-neck might be fully depleted, hence isolating the grain from its adjacent neighbour electronically. This 'pinch-off' effect leads to a dramatic decrease in current flow from grain to grain, therefore resulting in an extremely high resistance measured across the sensor.

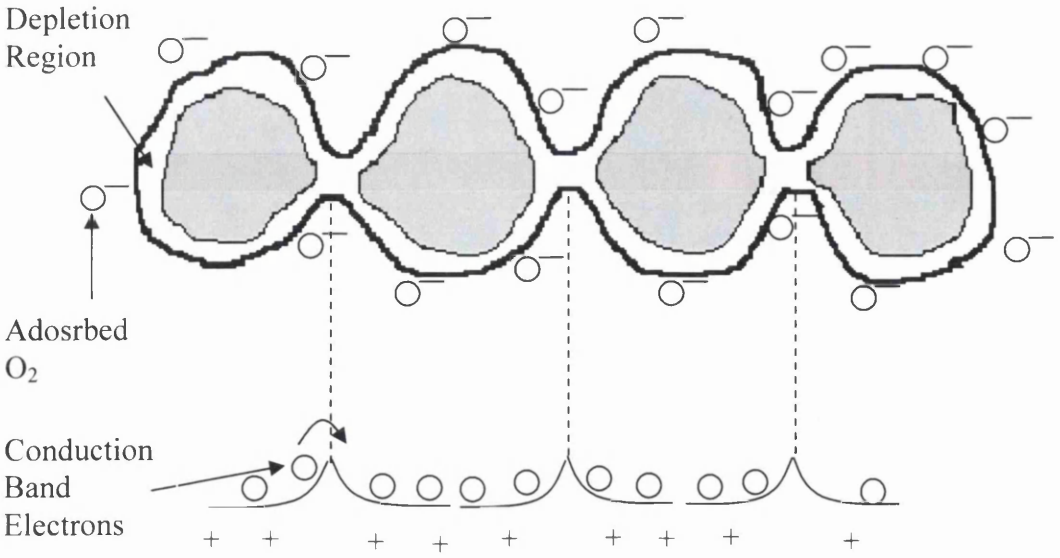

Figure 2-5 Illustration of Sintered Grains exposed to oxidising gas

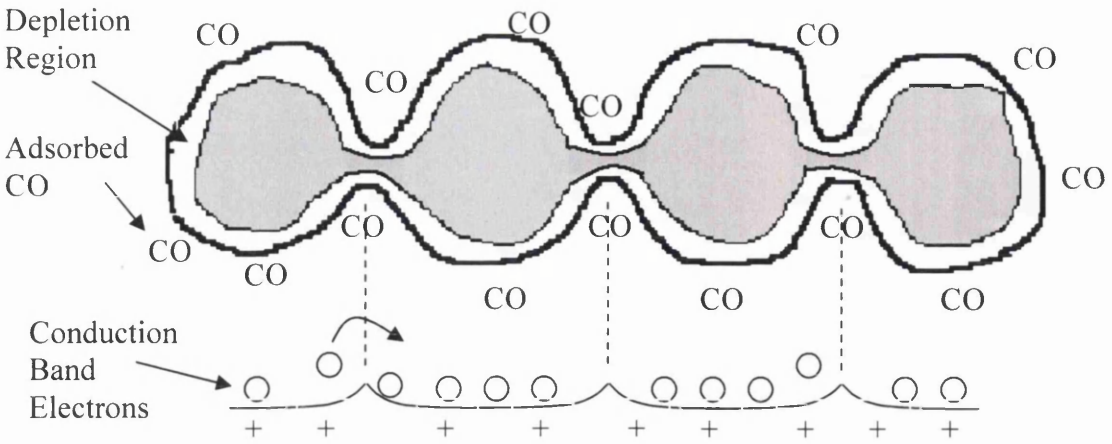

Figure 2-6 Illustration of Sintered Grains exposed to Reducing Gas

Conversely, when the gas sensor came into contact with a 'reducing gas', such as carbon monoxide (CO), the density of the negatively charged oxygen species that was chemisorbed on the surface decreases (Figure 2-6). This is because the reducing gas will also be adsorbed onto the surface, and combine with the oxygen species[6], hence releasing the electrons back to the material, increasing the free electrons at the conduction band and reducing the barrier height in the grain boundary for touching grains and reopening the conduction channel for sintered grains. This will decrease the resistance of the sensor tremendously.

The gas sensing mechanism is related to ionosorption, which is the process when an adsorbed gas acts as a surface state on the sensor surface, capturing electrons that are held to the surface by an electrostatic potential and therefore changing the surface's electrical characteristic. This type of bonding is of particular interest for gas sensing application because this will "activate" the adsorbing species, making it more receptive for a desired reaction. Oxygen can be ionosorbed in several forms namely, O_2^-, O^- and O^{2-}. O^-, which is most reactive species among the three, is believed to affect the surface charge and can lead to the high resistance exhibited by n-type semiconductors as the oxygen molecules capture electrons from the surface[11].

The rate of removal of these different oxygen species from the sensor surface is dependent on the reactivity and activation energy of the sensor. The activation energy refers to the amount of energy required by a system before a reaction can happen, which is commonly supplied by thermal energy or a photon. For an n-type

semiconductor, the reaction between reducing agents and the oxygen adsorbed onto the surface would replenish the conduction band with electrons and lower the resistance whereas the oxidising agent would do just the opposite.

2.4 NANOPATTERNING

Nanopatterning manipulates the material surface either physically or electronically, hence forming a pattern on the surface as desired by the user. This is of increasing scientific and commercial interest due to the wide range of possible applications across various disciplines.

2.4.1 Atomic Manipulation

Atom manipulation, as reported by Eigler[12] in IBM research centre, demonstrates nanopatterning using individual xenon atoms on a single-crystal nickel surface (Figure 2-7(a)). This technique can be described as a "sliding" process, which involves moving xenon atoms around the nickel surface via a lateral force between STM tip and xenon atom, yet having the ability not to alter the position of xenon atom during the imaging process. One of the main factors in achieving this is to choose materials with surface corrugation sufficiently large for imaging, but small enough for the "sliding" process. Another factor to take note of is the condition of the STM tip, which is crucial for this technique, which also requires a UHV environment, and liquid helium temperatures (4K).

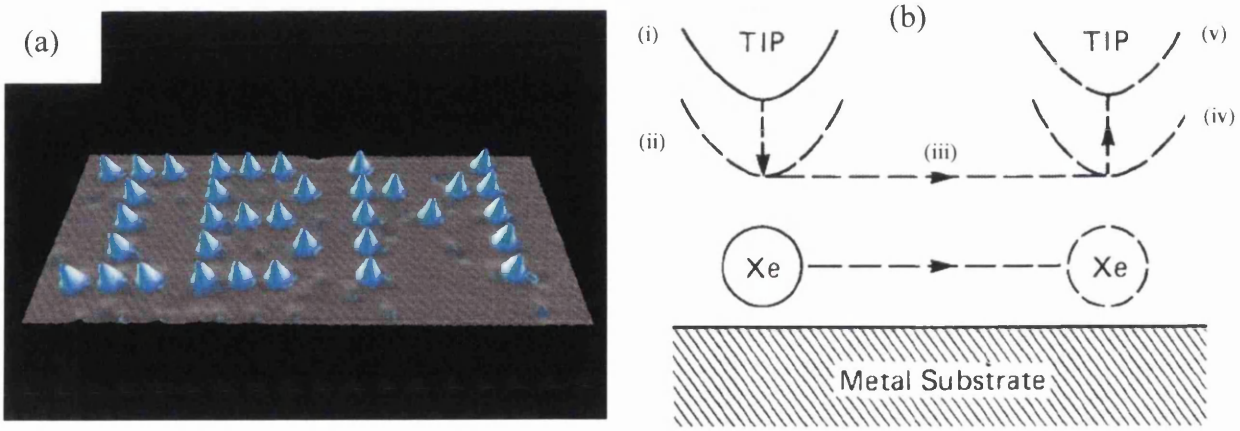

Figure 2-7 **(a) Xenon atom on Nickel surface** **(b) Illustration of "sliding" process**

The "sliding" process is illustrated as Figure 2-7(b). During scanning, the STM tip will maintain its height at (i) while locating the position of the xenon atom through normal STM scanning. When a desired xenon atom is detected, the tip will be lowered to position (ii), the height at which the atom-tip attractive force is sufficient to keep the atom locked under the tip. Maintaining this height, the tip will "slide" along path (iii) and stop at the desired position (iv), with the xenon atom following the path due to the attractive force. Then the tip is lifted to position (v), where the atom-tip force interaction is negligible, thus leaving the xenon atom at its new destination.

2.4.2 SPM Techniques

Apart from atom manipulation, many research groups are using voltage pulses to locally deposit material from the SPM tip. A recent review article by Wright and Chetwynd[13] suggested that in the area of nanomanipulation, many challenges such as holding organic molecules onto a flat surface[14], could be overcome by "writing" a pattern on a surface, in order to encourage site-specific adsorption.

Even though different types of SPM techniques are employed to pattern surfaces via deposition of material from the tip, the precise mechanism for the formation of the patterned features is not well understood, most of them could be classified under the two dominant theories, namely field evaporation or point contact.

Field Evaporation:

The field evaporation process is illustrated on Figure 2-8[15]. The tip before experiencing a high voltage pulse is shown as Figure 2-8(a). When a high negative voltage pulse is applied across the tip, the field emitted electrons flowing through the tip will heat up the sharp end of the tip (Figure 2-8(b)), which induces a field-gradient-promoted diffusion and hence flow of atoms from the shank to the apex of the tip, resulting in material transfer from the tip to the sample. However, when a high positive pulse is applied in the same way (Figure 2-8(c)), the tip will not experience the heating process because the field electrons from the sample will be hitting a larger area of the tip.

Nevertheless, for some cases reported[15,19], field evaporation was achieved with reversed tip voltage polarity to theory explained above.

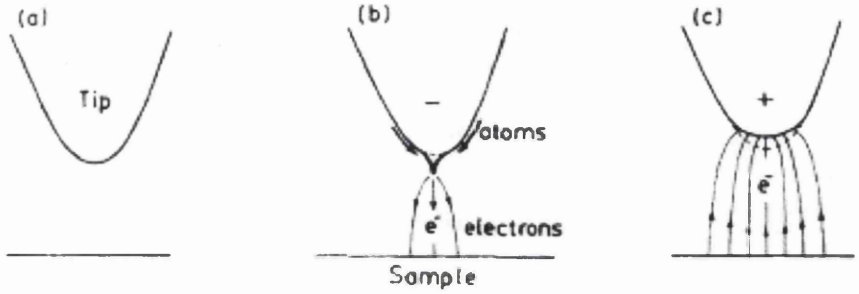

Figure 2-8 Demonstration of Field Evaporation Theory

Even though the tip will be gaining heat as a result of experiencing a negative voltage pulse, the temperature of the sample is unlikely to be affected by this field emission current flow from the tip[16]. However, the shape of the tip will be altered through the process, which would affect the field at the tip and the field current emitted. Therefore in order to deposit the material on the surface reproducibly, there has to be a continuous supply of atoms to the apex of the tip so that the tip can keep up with the consumption of atoms, else the consecutive voltage pulses can result in tip instabilities and make subsequent scanning impossible.

However, in the cases where the sample has an insulating layer, such as silicon oxide, the thickness of this insulating layer has a substantial effect on the success rate of field emission process. This therefore results in the variation of the magnitude of the voltage pulses with respect to the oxide thickness[17,18] during patterning. Table 2-1 summarises the parameters for field emission nanopatterning reported in previous articles.

Tip	Substrate	Parameters	Feature size
Gold[19,15]	Gold	+3.6V for 300ns	100-200Å wide 10-20Å high
Aluminium coated Tungsten[20]	Silicon	+6.5V for 1ms	5-20nm wide 0.4-2nm high
Tungsten[21]	Silicon	-7V for 1-60ns	10nmwide 3nm high
Gold coated STM tip[18]	Silicon oxide on Silicon	2-11V for 10ms	3-10nm wide 0.40nm high
Platinum[22]	n-type Silicon	-5.0V for 50μs	40nm wide
Gold[23]	Gold Film on Mica	+3.0V for 1.5ms	0.66 nm high

Table 2-1 **Parameters for Field Evaporation Technique**

Point Contact:

The other dominant theory of material deposition on surfaces, point contact, is demonstrated in Figure 2-9. The series of diagrams shows that the voltage pulse results in a small bridge between the tip and the sample. This formed contact will result in a sudden surge in current flowing from the tip to sample. As the feedback control loop of the SPM system is kept on, the sudden increase in current will cause the feedback loop to retract the tip from the surface. In the course of tip retraction, the tip draws the material deposited on the surface with it (like a meniscus with water) until the connection breaks. When the tip finally breaks from the connection, it will move towards the surface again to achieve current tunnelling set-point again.

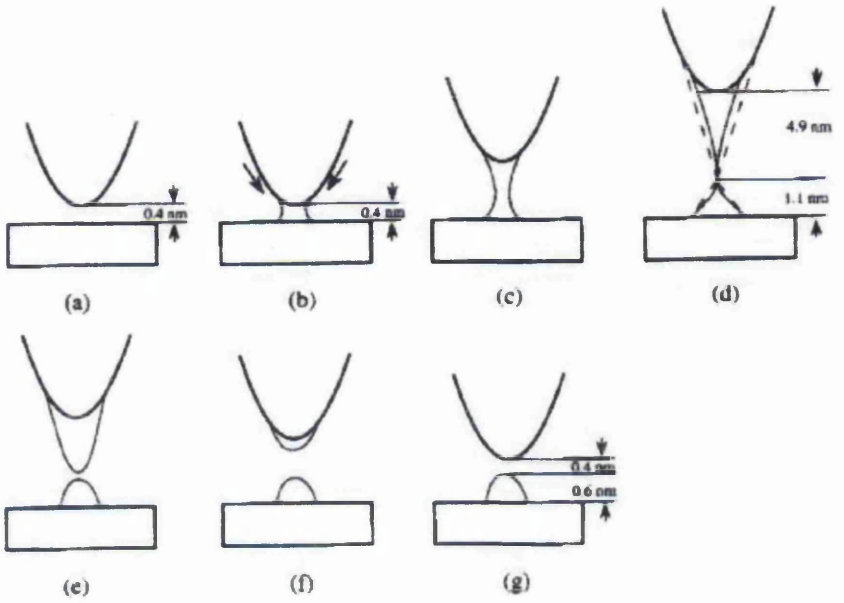

Figure 2-9 Demonstration of "Point Contact" Theory

The reason behind the formation of the bridge is not well understood. There are suggestions such as high temperature at the apex of the tip caused by field evaporation results in the contact formation; other explanation points to the mechanical deformation caused by the attractive electrostatic forces between the tip and sample. A study done by D. H. Huang[24] shows that platinum nanodots could be deposited on silicon regardless of the polarity of the tip, seems to be supporting the latter. Table 2-2 summarises the parameters used for nanopatterning with the point contact technique.

Tip	Substrate	Parameters	Feature size
Gold[25]	Gold	-6V for 14μs	38nm wide 3nm high
Platinum[24]	Silicon	±2.0V for 5ms	1.5nm wide
Aluminium coated Tungsten[20]	Silicon	+6.5V for 1ms	5-20nm wide 0.4-2nm high
Gold[23]	Gold film on Mica	-3.8V for 1.5ms	500nm wide 1nm high

Table 2-2 Parameters used for Point Contact Nanopatterning.

2.5 POTENTIAL APPLICATION OF NANOPATTERNING

To date, the various techniques are mostly still at the experimental stage. However, the prospect of the research is so rewarding that studies in this area are continuing, with several milestones achieved.

2.5.1 Data Storage

In 1959 at Caltech, Richard Feynman estimated that if we could represent the information content in a code of dots and dashes, "*all the information that man has carefully accumulated in all the books in the world can be written..... in a cube of material one two-hundredth of an inch wide*", where he uses 5 x 5 x 5 = 125 atoms to store one bit, which is comparable to DNA where 32 atoms are used to store 1 bit[26]. This gave a glimpse of how much room there is for data storage when going down to the atomic level.

Atom Manipulation

Data storage application refers to the capability of locally altering the state of a material in such a way that digital logic "0" and "1" can be differentiated. One successful example was conducted on the silicon surface, where each data bit was stored by the presence or absence of one silicon atom[27]. The writing process involves the transfer of silicon atoms to the tip of a scanning tunnelling microscope, in another word removing silicon atoms from a nearly filled lattice at the surface (Figure 2-10). The data can be read through the peak registered for the silicon atoms that protrude well beyond the noise level (Figure 2-11).

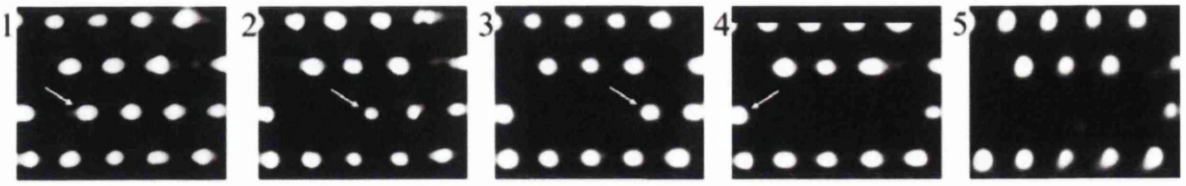

Figure 2-10 Process of Removing Silicon atoms from surface

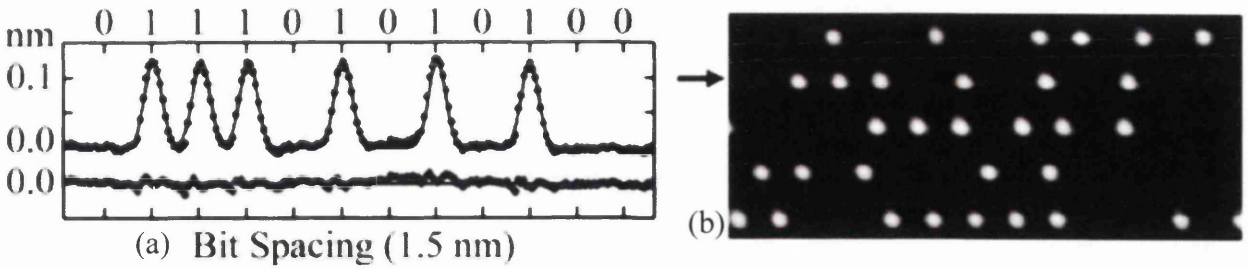

Figure 2-11 **(a) Line Profile on line indicated by arrow on (b) (b) Image of the Data Written**

When comparing the atomic memory to the memory storage on a CD-ROM, it shows a reduction from μm scale to nm, which leads to a 10^6 times higher density.

SPM Technique

Apart from atomic manipulation, another group has reported a technique that provides flexibility in controlling the size of the dots written, regardless of the polarity of the tip bias. The writing process in this technique uses Electrostatic Force Microscopy (EFM) on a $CeO_2/Si/CeO_2/Si(111)$ heterostructure[28].

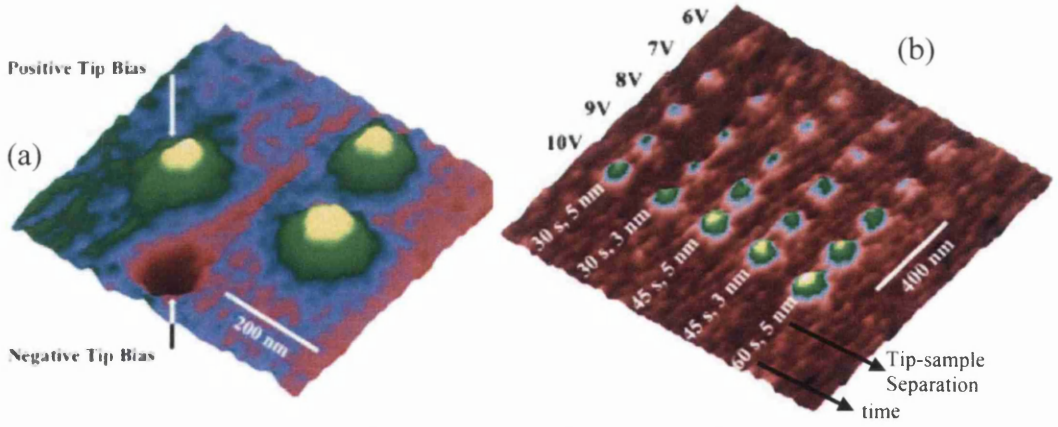

Figure 2-12 **(a) Dots written with different polarity (b) EFM image of dots array written at different writing voltages, tip sample separations and writing times as labelled.**

The writing process was performed by reducing the tip sample separation and applied a large charging bias to the EFM tips, where dots of both positive and negative charge can be written as shown in Figure 2-12(a). The written features can be controlled as the feature size scales linearly with the same

slope in relation to the various writing parameters of tip biases, tip to sample separation and write time (Figure 2-12(b)).

EFM became more popular in the research on data storage due to its ability to show a reverse in image contrast when scanning an electronic feature with different polarity. A simple system was presented by R. Dianoux[29], where a feature was patterned on SiO_2 by moving the EFM tip in close contact to the surface and applying a -10V pulse for a few seconds (Figure 2-13(a)). The cantilever is then retracted to the height where it is no longer affected by the Van der Waals forces, but sensitive enough to detect the electrostatic forces. When scanning the feature at this height, the tip bias was reversed at mid point and the image shows a contrast inversion on the phase image of the feature (Figure 2-13(b)), showing that the patterned feature is electronic in nature.

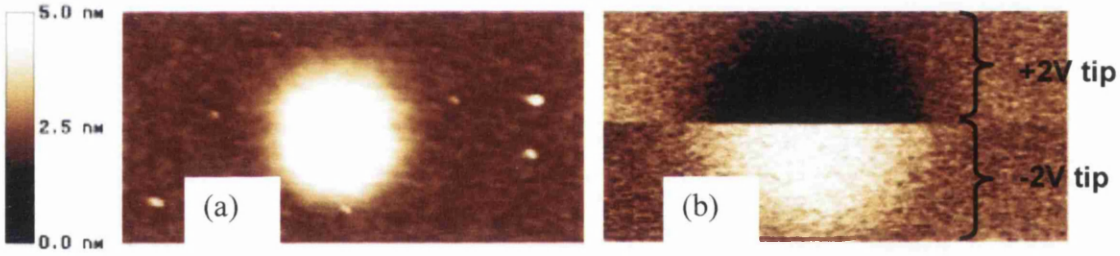

Figure 2-13 (a) Image reference to Apparent Height (b) Image reference to Phase

However, to date, only a few articles have reported the erasing of the written data, such as the high density erasable charge memory in an oxide-nitride-oxide-silicon (ONOS) system[30] reported in 1996. The writing process involved applying a voltage pulse between the tip and the silicon substrate in contact AFM mode, while the reading process could be performed by detecting the change of the surface potential or the capacitive force without contacting the ONOS media using SMM (Figure 2-14). The erasing of the data was done by a reverse polarity pulse on the tip on the location where data was stored.

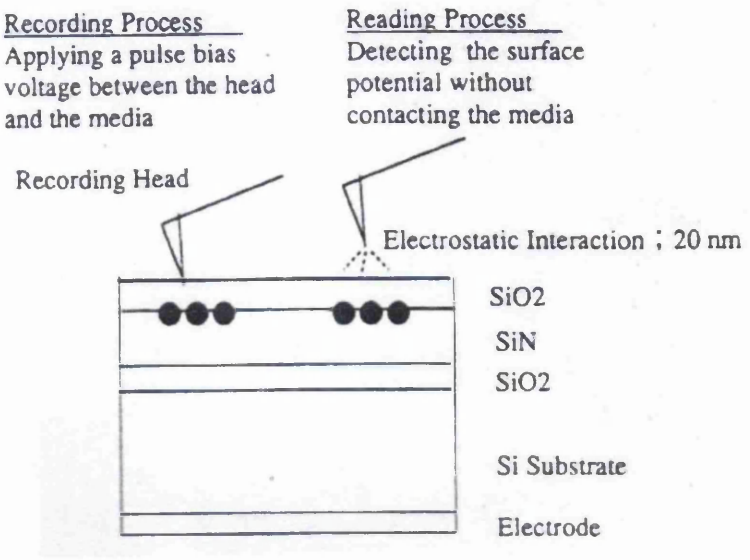

Figure 2-14 Reading and Writing process on ONOS system with Conducting AFM tip

2.5.2 Single Electron Tunnelling

As mentioned before, power loss and heat dissipation are the main challenges that need to be overcome for the miniaturisation and integration of conventional transistors to continue. Recently, quantum dot transistors are quoted to have the potential to provide an alternative way to solve the problem. Quantum dot transistors operate on the theory of single electron tunnelling (SET). SET main characteristics are the suppression of the tunnelling current around zero bias, so called coulomb blockade, and step-like behaviour of the current voltage (I-V) characteristic at higher voltages, namely, the coulomb staircase[31,32].

When 2 electrodes are placed close together (schematic shown as Figure 2-15 (a)), and an electron tunnels from the left electrode to the right, the transfer of this extra electron will produce a negative charge of $-e$ on the right electrode, hence leaving behind a net positive charge, $+e$ on the left electrode. However, the difference in charge between the junctions is now $2e$, meaning that the tunnelling of this electron across the junction has increased the energy of the system, which is forbidden as the overall charge difference between the junctions needs to be the same before and after any electron movement. This restriction on tunnelling is called Coulomb blockade. The effect of Coulomb blockade can be referred as the restriction on electron tunnelling that would

raise the energy of the system. To lift the blockade, the situation shown in Figure 2-15 (a) needs to be met, where there is a charge of half an electron on each side. If an electron now tunnels across from left to right under such condition, it transfers a charge of $-e$, resulting in a total charge of $-\frac{e}{2}$ on the right and $+\frac{e}{2}$ on the left. Since the difference in charge in each case is equal to e, the energy is the same both before and after the event, making it now favourable for an electron to tunnel across the junction.

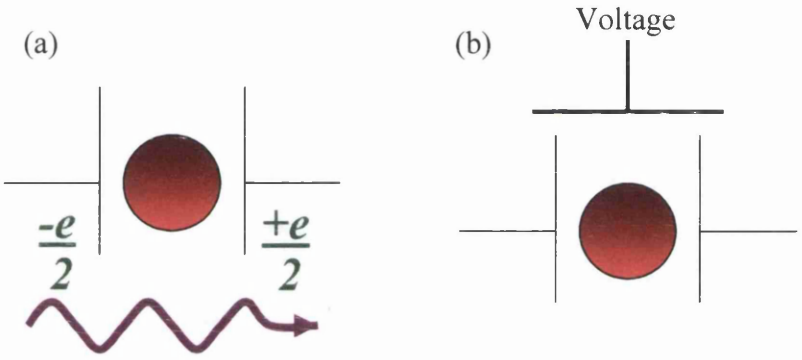

Figure 2-15 (a) Lift of Coulomb Blockade (b) Schematic representing a SET

If a third small electrode is placed centrally between the other two and makes an electrical contact to the thin layer of insulator above this electrode (Figure 2-15 (b)), then by altering the voltage applied to the contact, the charge contained on the central electrode could be varied. This refined structure is known as the single electron transistor.

The single electron transistor is a continuation of the miniaturisation of the conventional transistor or MOSFET, and exhibits great speeds as well as reliability[33]. Several groups are presently looking into this area of potential contribution to the world of nano-chips, such as the single electron transistor that is fabricated through a nano-oxidation process, where the formation of narrow oxidised titanium (TiO_x) trapped an island on the surface of Titanium metal film on α-Al_2O_3 substrate[34].

2.5.3 Molecular Docking

Another more immediate application of charge writing is molecular docking, which refers to the ability to pattern docking sites with localised charge and attract certain particles to park at the sites with precision. This means a new fabrication technique that immobilises the particles while "self-assembling" on the surface, which is crucial to the development of nano-scale devices [35,36].

Even though this technique will assist in opening a new chapter in nanotechnological research, the obstacle on charge retention and spatial localisation have limited its progress. Nevertheless, a successful case[37] had been reported that uses charge writing on PTFE-like fluorocarbon layers, and attracted silica nanoparticles to dock at the patterned region.

Figure 2-16 shows the process of the experiment. The patterns were written by applying voltage pulses through a conductive AFM tip (a), where the substrate is then dipped into a suspension of small charged particles (b). Due to the electrostatic attraction force from the charged pattern, the nanoparticles will attach themselves on to these charged sites (c) and the results are shown as (d).

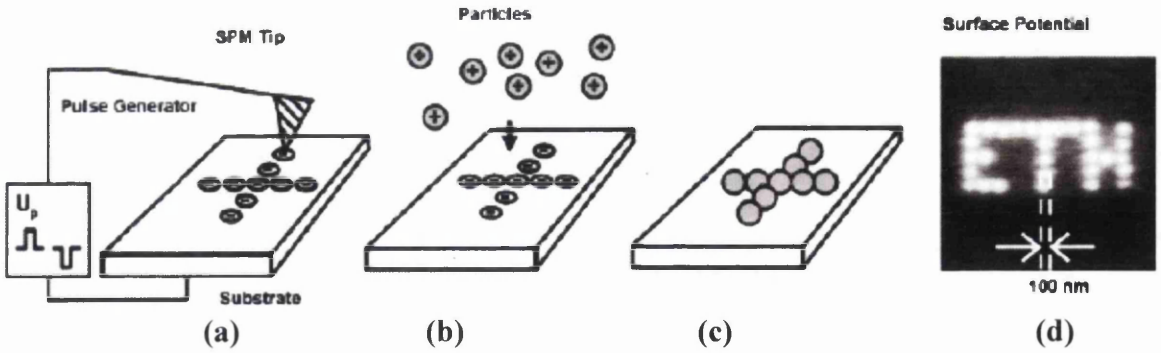

Figure 2-16 Example of Molecular Docking Application

Another case where a similar technique has been used to bind proteins to polystyrene[38] except the pattern is written using an electron beam. To make this technique suitable for nanoscale research, the size of the patterned features will need to be reduced from the hundreds of nm reported in both cases mentioned to less than 10nm, and localised high charge concentration

should be retained for substantial periods of time for sufficiently high resolution adsorption.

2.5.4 Logic Gates Application

It was pointed out by Richard Turton[31] that *"the limitation on the speed at which devices on a chip can be operated may ultimately be determined by the long interconnects which are necessary in any conventional chip layout, meaning that the delay times associated with these interconnects are likely to far exceed the switching times of the individual devices. In another word, scientists have gone to great lengths to make a quantum dot transistor, only to discover that the tremendous capabilities of the quantum dot cannot be fully appreciated when incorporated into an integrated circuit".*

Therefore to utilize fully the potential of quantum dots, radical changes in the design and philosophy of integrated circuits are required. An example of such a system has been proposed by a group at the University of Notre Dame, Indiana. The basic unit of the construct is a cell consisting of five quantum dots, the number of electrons is controlled so that there are precisely two in each cell (Figure 2-17)

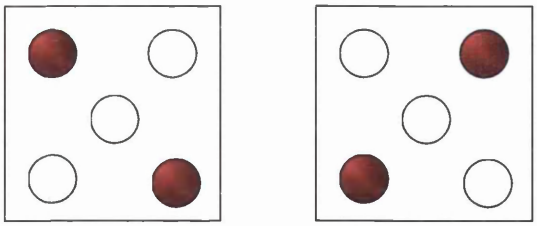

Figure 2-17 Possible configuration of quantum cell

The configurations are labelled as "0" and "1", which can be used to represent the basis of a binary system. The neighbouring cells interact with each other as the distribution of electrons in one cell tends to induce a similar distribution in the next. Due to this unique characteristic, if these quantum dot cells are arranged in row and the value of the cell at the left hand end is set to the state of "1", the will cause the next cell to adopt the same state, and the signal will propagate along the row until every cell shows the same state. With a multi-dimensional array of cells, it is possible to create a more

complex interaction, which could potentially behave as a single device and perform a highly complex function.

Scientists at IBM adopted the idea and managed to build structures that demonstrate the fundamental digital logic OR and AND function (Figure 1-6 in Chapter 1). The circuit was created using a precise pattern of carbon monoxide molecules on a copper surface[39], which shows the potential of introducing a new technique in circuit fabrication, hence providing an alternative to the limitation to device minimisation.

2.6 STUDIES AT SWANSEA UNIVERSITY

In the world of gas sensing, high sensitivity, selectivity, small size and low production costs are some of the advantages that made chemically sensitive solid state devices a popular choice.

Swansea University conducted research on gas sensors fabricated with tin dioxide nanoparticles. Research on the topic had laid the foundation for the understanding of the properties of this material, and it was also the first step to the discovery of the nanopatterning phenomenon reported in this thesis.

Technical Ambiguity

Even though scanning probe techniques had been developed over the years, it is almost impossible to accurately know and control the state of the tip apex[40]. This is especially true when scanning complex, non–atomically clean surfaces such as nanocrystalline SnO_2, where contaminants can be routinely picked up by the tip and dropped off on the surface. Researchers have developed their own "secret recipes" over years of experience so as to revive a suspected "crashed" tip and rectify the scan. Suggestions such as "soft crash" which involved intentionally pushing the tip into the surface in a controlled manner or scanning at high speed (usually >10 times the scan range) across step edges were some common practices. Performing spectroscopy could assist in cleaning the tip as the process often deposits contaminants, which the tip might have picked up from the surface. High voltage

pulses (>5V) and reversing tip polarity during scanning may achieve the same goal as well.

At Swansea University, the tip condition was very hard to predict during the gas sensor experiments, which resulted in difficulty whilst scanning. One of the approaches to try and combat this involved increasing the scanning voltage temporarily for few seconds. Unexpectedly the next scan revealed a higher intensity line on the image, which coincided with the area where the scanning voltage was increased (Figure 2-18(a)). The line profile graph (b) shows that the feature is about 8nm higher than the background surface. This opened the first chapter to nanopatterning research in the centre.

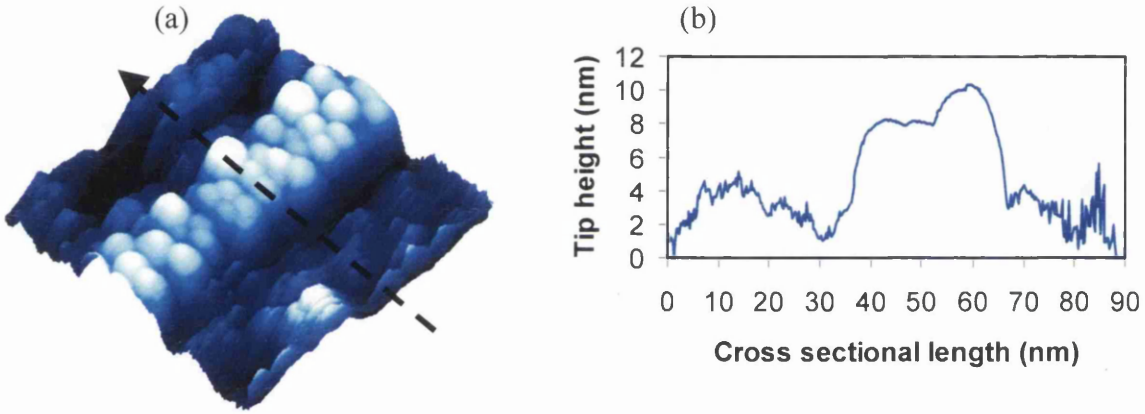

Figure 2-18 **(a) Image of the line feature of 30nm wide**
(b) Line Profile of the line feature

Due to this uncertain phenomena of whether the feature was electronic in nature or due to the deposition of contaminants from the tip, the procedure that resulted in the feature was repeated several times, and exhibited high reproducibility. Realising that the tip voltage pulses had such an effect on the material, the research moved from line to dot nanopatterning. After several attempts, a voltage pulse of -6V tip voltage for 100μs resulted in a dot feature that is of higher apparent height than the background (Figure 2-19). The dot size is very competitive when compared to other nanopatterning techniques, with an apparent height of 5nm and width of 14nm.

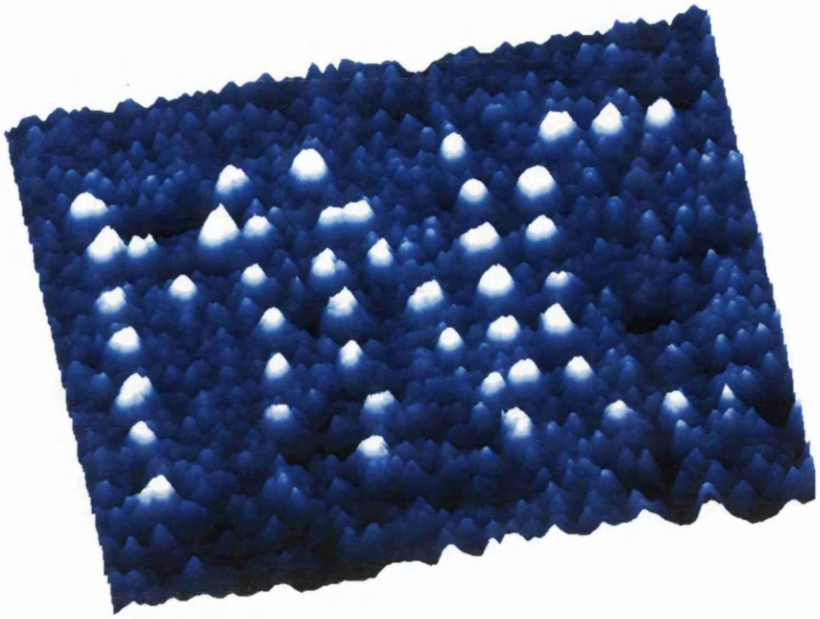

Figure 2-19 450 by 300nm^2 area patterned with voltage pulses[41]

To further understand the characteristic of nanopatterning, more experiments were carried out on these patterned dots.

Nanopatterning

To identify if the patterned features were due to electronic effects or a result of deposition of material from the tip, a dot feature was initially patterned on a flat surface. Afterwards two dots were attempted in the next scan, one of which directly on top of the first dot and the second at a new location. The subsequent scan revealed that the location where the first dot was patterned had no change in height (after receiving the second pulse) while a new feature appeared on the second location. The line profiles verified that the height measured on the first dot remains the same after the second attempt whereas a new feature of similar height appeared on the new location. This eliminates the possibility of point contact deposition of tungsten material from the tip, suggesting that the origin of the nanopatterning was electronic.

Charge Retention

To understand if the features created through nanopatterning are permanent, a study of the length of time that the feature can remain on the surface was conducted. A pattern was written on the surface, and was scanned repeatedly over a period of three days. During this time, the features remained unchanged. Line profiles from the pattern reveal that some of the features had disappeared after 74 hours, but the conclusion was that most of the written features could remain intact and stable under a UHV environment for up to 8 days.

Erasing Process

Since it was believed that a negative tip voltage was responsible for the appearance of the features, a positive biased tip could in theory reverse the process, that is, remove the features from the material surface. This experiment had to be conducted at 130°C because that is the only way to achieve a stable scan with a positive tip. The "erasing process" was carried out with a +3.0V tip voltage scanning across the area where nanopatterning took place and the result reveals that the height of the dots are gradually reduced scan after scan, as if the dots are slowly "blended" into the background surface. However, it was noted that the area scanned while performing the erasing process has a higher apparent height than the area not being part of the experiment. This suggested the possibility of "charge spreading", where the injected charge was being spread across the neighbouring particles when scanning with a positive tip voltage.

Oxygen Gas Exposure

To explore into the possibility of using the technique for molecular docking, a pattern was written on a surface and exposed to oxygen. This serves as both an experiment for molecular docking application as well as a verification of the electronic nature of the written features. The resulting images showed that some of the written features started to become broader after 25 minutes and after about 1 hour, some of the features vanished from the surface whereas the remaining ones were very broad in size. It is intriguing to note that the unwritten background remained unaltered and clearly defined throughout the whole experiment. This shows that the oxygen gas introduced has a greater effect on the written features than the

background surface, which indicates that the patterned features were very likely electronic and also shows the potential of this technique for molecular docking applications.

Nanopatterning Parameters

It is vital to understand the reason of how -6.0V tip voltage and 100μs provide the ability to successfully create a feature on the sample surface. As such, the magnitude of the voltage pulse and pulse width were varied to understand how important they were and how they affected the resulting features. The result shows that the pulse width only affects the success rate of nanopatterning when it is lower than 100μs, there is no effect when it is higher than that. As for the magnitude of the tip voltage, nanopatterning is only successful when it is higher than the critical threshold of -5.1V tip voltage but with very low success rate. To have nanopatterning repeatable, the tip voltage needed to be around -6.0V.

Voltage Dependent Scanning

As STM images the electrons density of the material scanned, variations in tip voltage while scanning electronic features should affect the tip height and therefore the contrast on the image. A line was written on the surface and scanned through a range of tip voltage, and the result showed that the apparent height of the line reduces as the scanning tip voltage increases, which suggests that the line is electronic in nature.

STS Studies

To further verify the electronic nature of the patterned features, a "MNC" pattern was written on the surface, and STS curves were acquired from the pattern and un-patterned background. The result shows that the patterned features provide an easier path for electron tunnelling, resulting in a higher current flow when compared to the un-patterned background. Further to that, the average IV curves chosen both from the patterned regions and the background shows that the conductivity of the patterned surface is ten times higher than the background for both spectroscopy voltage polarities. This means that the density of states is larger in the patterned dots, again suggesting that the nanopatterning is electronic in nature.

Electronic Force Microscopy Studies

As mentioned earlier, EFM would be the most suitable technique to confirm the electronic nature of the surface. However, as the "two-pass" technique of EFM is not really possible in the UHV system, a similar technique that could be described as "conducting non-contact AFM" was employed on a patterned surface. A line was written on the surface using an EFM cantilever in STM mode using the normal nanopatterning technique, then scanning was performed in non contact AFM mode with 2V and -2V applied on the tip . The results show a contrast inversion on the images when the polarity of the tip voltage was flipped. This again indicated the presence of electronic features but the inability to perform the two-pass EFM technique meant that the interpretation of the AFM data was not totally conclusive.

Charge Writing Mechanism

It is believed that the features created during the nanopatterning research at Swansea University are electronic in nature. Figure 2-20 shows a schematic diagram representing the normal STM scanning of tin dioxide, where the electrons can easily flow from grain to grain by tunnelling through the very thin barriers (2nm) present at grain boundaries.

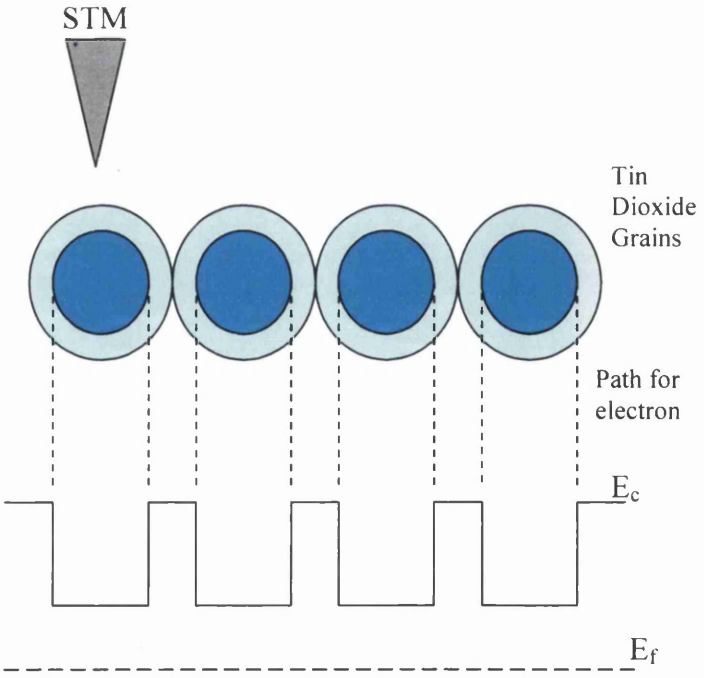

Figure 2-20 Illustration of normal scanning on tin dioxide nanoparticles

However, when nanopatterning is performed on one of the grains (demonstrated as Figure 2-21), the large current density caused by high tip voltage will alter the electron flow, so that the rate of electrons entering the nanoparticles is larger than the rate at which the electrons tunnel out of grains; hence resulting in localised band-bending. This modification caused by band-bending in the vicinity of the patterned grain will cause the conduction band edge of the patterned grain to decrease significantly when comparing to the neighbouring grains, therefore causes the entrapment of electrons. It is believed that the area of trapped electrons (Figure 2-21) would rise when the number of electrons captured increases. As such, during STM scanning with constant current mode over the patterned grain with a higher electron concentration, the feedback loop of the system would move the tip away from the grain so as to maintain the current set-point, hence forming a brighter spot on the STM image.

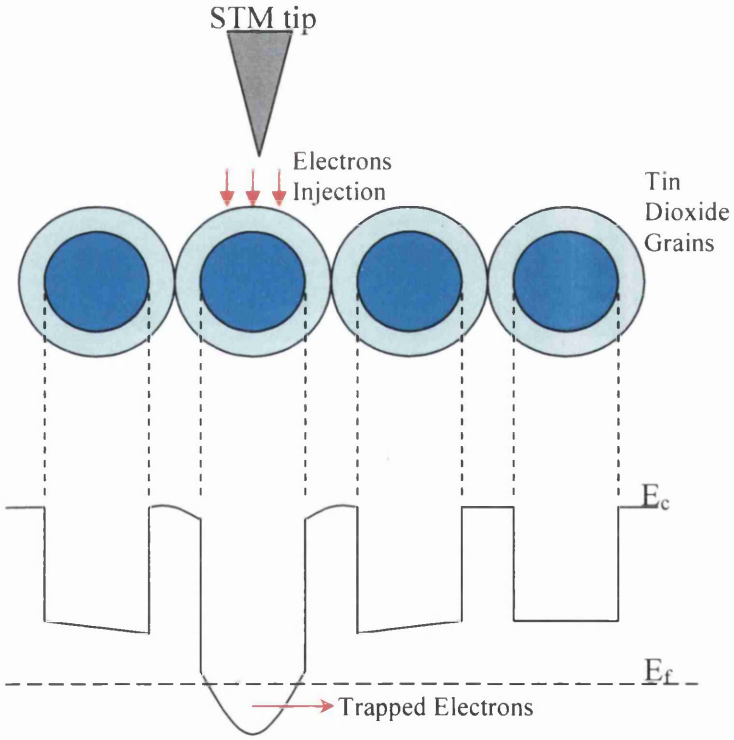

Figure 2-21 Illustration of effect of nanopatterning performed on a grain

The above hypothesis was simulated by solving Poisson equation and Schrödinger's equation[42]. The effect of charge injection into the patterned grain is performed by increasing the electron charge density uniformly within the patterned well by an amount equivalent to that of a single electron. The results show increasing band

bending with increased electron injection, which eventually saturates, in good agreement with the experimental results.

2.7 SUMMARY

The Multidisciplinary Nanotechnology Centre at Swansea University is the only research group looking into the nanopatterning of nanocrystalline tin dioxide particles with STM. According to the previous work done in the laboratory, the nanopatterning mechanism appears to be electronic in nature.

All the possible applications presented in the chapter shows the potential development opportunities and applications for nanopatterning research at Swansea University, and the advantage of low cost and potentially huge data density would make tin dioxide a very promising material to work with.

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CHAPTER 3 SCANNING TUNNELLING MICROSCOPY (STM) AND SCANNING TUNNELLING SPECTROSCOPY (STS)

Scanning Tunnelling Microscopy (STM) was first invented in the 1980s by Binning and Rohrer[1], which started a new era for surface and interface science. This technique was first invented for topographic imaging of surfaces on an atomic scale. However, with improvement and further development of the technique, it evolved to be capable of providing more information from the tunnelling process during operation. Simultaneously, the system is able to provide topographic information, as well as spectroscopic measurements. This spectroscopic measurement method is known as Scanning Tunnelling Spectroscopy (STS)[2,3], which provides information on the local electronic structure at the surface. This is widely used to study Fermi level pinning and probe the density of states of semiconductor surfaces[4].

This chapter focuses on the basic operating principles and theory for STM and STS. Applications of the technique will be presented to illustrate the information that could be obtained through both STM and STS. The understanding of the techniques facilitates the interpretation of the results comprehensively.

3.1 QUANTUM TUNNELLING

The basic principle of STM is based on the tunnelling current that originates through the quantum mechanical tunnelling effect, due to the wavelike properties of electrons in quantum mechanics [5].

Electrons are represented as a wavefunction in a conducting material. When it encounters a vacuum barrier, which has a potential energy that is larger than the kinetic energy of the electron, there is a possibility that it may break through the forbidden region and reappear on the other side of the barrier (as indicated as the leak-out electron wavefunction in Figure 3-1.

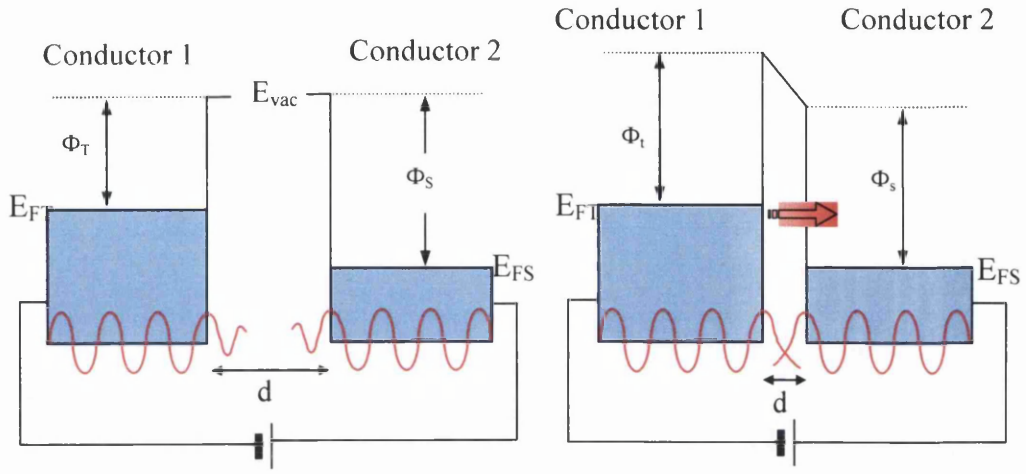

Figure 3-1 Illustration of Quantum Tunnelling Effect

When two electrically conducting materials are placed very close to one another, with a small voltage V applied between the materials, the wavefunctions may overlap and permit quantum mechanical tunnelling. This results in a flow of current, I, across the vacuum gap. This current is directly affected by the distance between the two materials as

$$I \propto \exp(-2kd) \qquad (3.1)$$

where k is the waveform vector, which is a function of energy, and applied voltage while d refers to the distance between both materials. In the case of STM, the two conducting materials are referred to as the tip and the sample.

3.2 PRINCIPLE OF OPERATION

As explained earlier, the basic principle of STM is based on quantum tunnelling phenomena, which involves a sharp tip being placed very close to a conducting sample surface. Then current would result when the electrons tunnel through the vacuum barrier between the tip and the sample surface.

The sharp tip is mounted on a piezoelectric tube, which controls the movement of the tip accurately, in all three dimensions. During operation, the STM system would control the tip position such that the tunnelling current or tip-surface distance is kept constant, according to the selection of the mode of operation (to be explained later). At the same time, scanning would be carried out over a small area of the sample surface where the movement of the piezoelectric tube would be recorded and displayed as an image of surface topography (Figure 3-2)

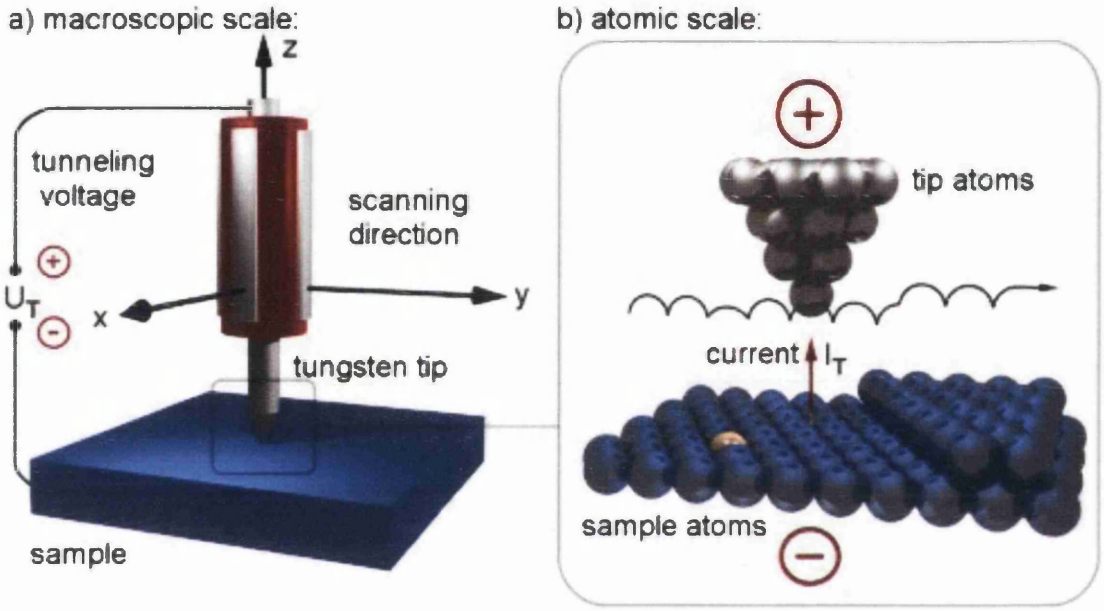

Figure 3-2 Schematic Illustration of STM Operating Principle

It is important to note that STM does not probe the position of the material nuclei; instead, it is a probe of the electron density, depending on the density of states on the surface of the sample.

3.3 THEORY OF STM

As mentioned, under classical physics, an electron cannot penetrate through a potential barrier that has a higher potential energy compared to its own. However, with quantum mechanical tunnelling, there is a possibility that an electron will appear on the other side of the barrier. The transmission coefficient for this to happen between a tip and sample is fairly complicated to calculate[6,7]. Fortunately, the coupling between tip and sample is weak when STM is in operation, as such, the

tunnelling current can be explained with the first-order perturbation theory suggested by Tersoff and Hamman[8].

Based on Bardeen's tunnelling current formalism[9],

$$I = \frac{2\pi e}{\hbar} \sum_{TS} f(E_T)[1 - f(E_s + eV)] |M_{TS}|^2 .\delta(E_T - E_s) \qquad (3.2)$$

where $f(E_T)$ is the Fermi function, V is the applied voltage, M_{TS} is the tunnelling matrix between ψ_T, the tip wavefunction and ψ_S, the surface wavefunction, and E_T and E_S representing the energies of states in the absence of tunnelling. In this case, the involvement of reverse tunnelling was neglected due to the higher temperature effect. The matrix element M_{TS} is expressed as:

$$M_{TS} = \frac{\hbar^2}{2m} \int dS.(\psi_T^* \nabla \psi_S - \psi_S \nabla \psi_T^*) \qquad (3.3)$$

where m is the free electron mass, the integral is taken from any surface ds lying entirely within the barrier region between tip and sample[10].

Substituting both the tip and sample wavefunctions into this tunnelling matrix element, and then further substituting into the tunnelling current model provides the result[11],

$$I \propto \sum_S |\psi_V(r_t)|^2 \, \delta(E_S - E_F) \equiv \rho(r_t.E_F) \qquad (3.4)$$

where r_t represents the position of calculated point source of current for an ideal STM tip.

As such, the ideal STM system would probe into $\rho(r_t.E_F)$ for measurement, which reflects the quantity known as local density of states (LDOS) at E_F, in other words, the charge density from states at the Fermi level.

3.4 LOCAL DENSITY OF STATES

The density of states (DOS) is the amount of electrons that exists at specific level of energy. The tunnelling conductance, σ (or I/V) is proportional to the LDOS.

$$\sigma \propto \rho(r_O, E) \qquad (3.5)$$

where $\rho(r_O, E)$ is the LDOS of the sample.

For STS, the tip-sample separation is kept constant, and the current measured with respect to the bias voltage giving the LDOS of the sample. Further to that, the polarity of the bias voltage on a STM system can show the occupied and unoccupied states of the sample.

The tunnelling process between the tip and sample across a vacuum barrier is demonstrated in Figure 3-3. The left side shows the STM tip, which is considered as metallic with a constant density of states at the Fermi level. The right section of the figure shows the semiconducting sample, with a surface state structure as illustrated in the diagram.

Referring to Figure 3-3(a), the tip and the sample demonstrate an electrical equilibrium when they are placed closed to one another. The difference in work functions results in an electric field in the vacuum region. As the Fermi levels are the same for both tip and sample, there is no tunnelling current present because the flow in both directions is equal.

However, the situation would change when a voltage, V, is applied to the sample. This is because the energy level of the sample will shift either upward or downward, by an amount |eV|, with respect to ground. When positively biased (Figure 3-3(b)), the energy level of the sample moves downwards, which results in electrons tunnelling from occupied states of the tip to the unoccupied state of the sample. At negative sample bias, the Fermi level of sample shifts upwards, causing the electrons to tunnel from the occupied states of the sample to the unoccupied state of the tip, shown as Figure 3-3(c).

The exponential dependence on the tunnel current with distance requires a large change in the tip displacement to maintain the tunnelling current when the DOS of the sample changes. It is this exponential dependence which makes STM so powerful.

This capability is especially useful for imaging III-V semiconductor surfaces, consisting of unoccupied states related to group III element and occupied states associated with group V element, (for instance, Gallium Arsenide (GaAs))

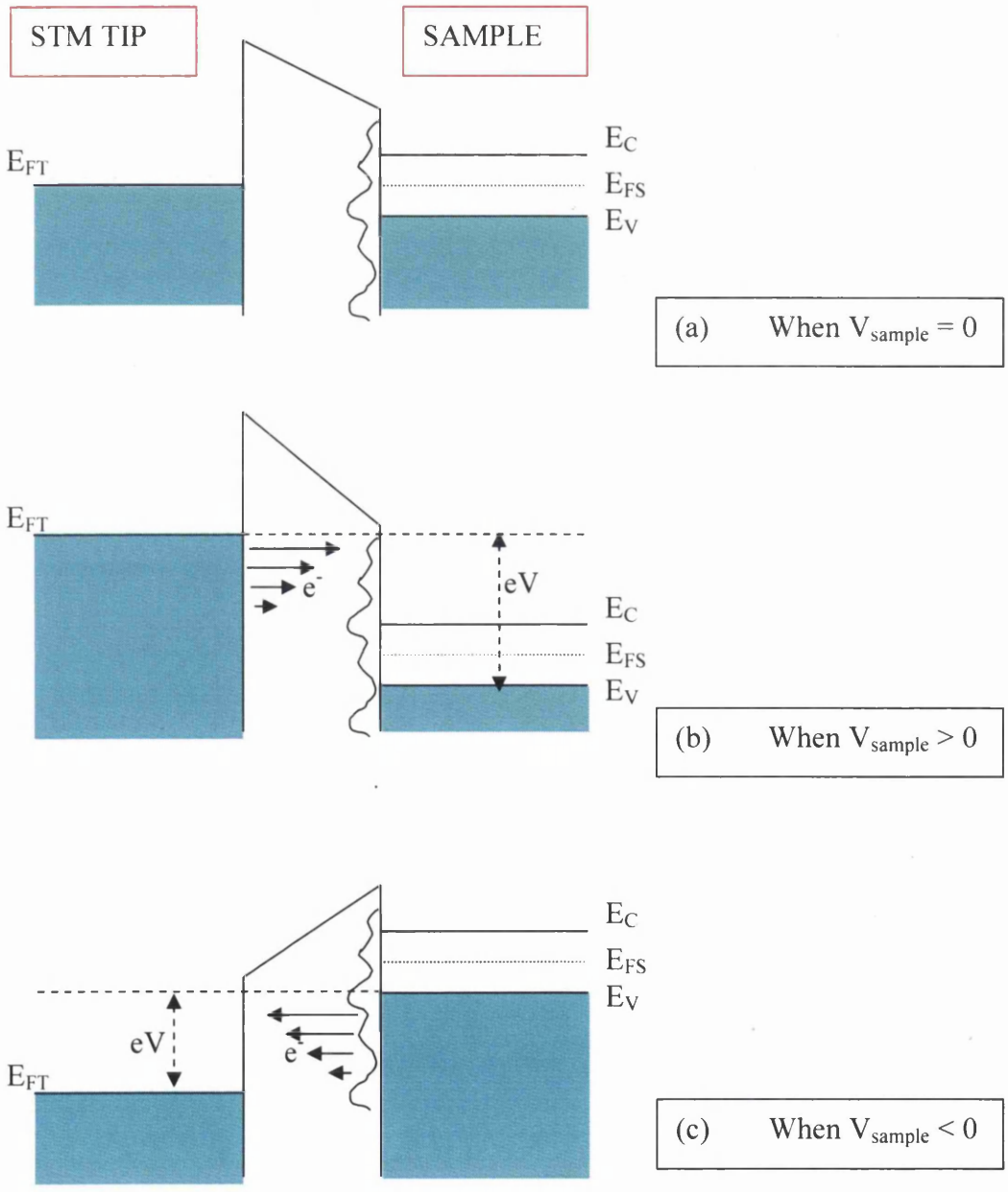

Figure 3-3 Schematic Illustration of Tunnelling Process Between Tip and Sample

3.5 MODE OF OPERATION

An STM system can be operated under two basic modes, namely constant height mode[1,12,13,14] and constant current mode[15]. The mode of operation commonly used is constant current mode, which was also the first operational mode introduced when Binnig and Rohrer[1] presented the STM system.

3.5.1 Constant Current Mode

During this mode, the tunnelling current is constantly checked against a desired tunnelling current value defined by the user, by means of a feedback loop function (Figure 3-5). The difference between the measured and required height (error signal) is used to determine if the piezoelectric driver needs to adjust the position of the probe tip, so as to keep the tunnelling current flowing between the tip and the sample surface constant. The variation of the applied voltage on the piezoelectric driver can be used to produce the topographical image of the STM; this is comparable to the record of height of tip from surface as a function of tip position (Figure 3-4)

Due to the variation in the height of the tip, this mode of operation is suitable for surfaces that are not atomically flat, or in another words, samples with steps and protrusions. The downside of the constant current mode is the time response for execution of the feedback loop, which slows down the scanning speed of STM.

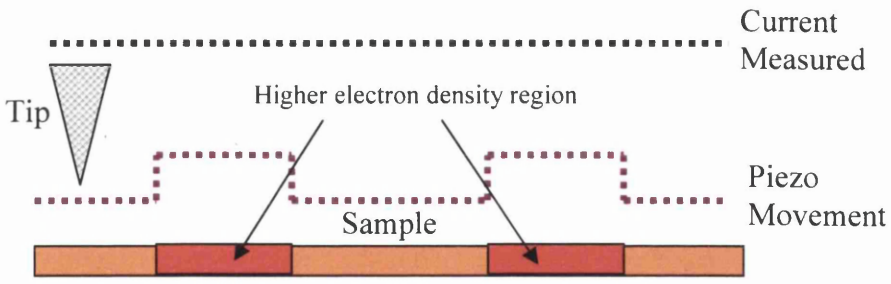

Figure 3-4 Schematic Illustration of Constant Current Mode

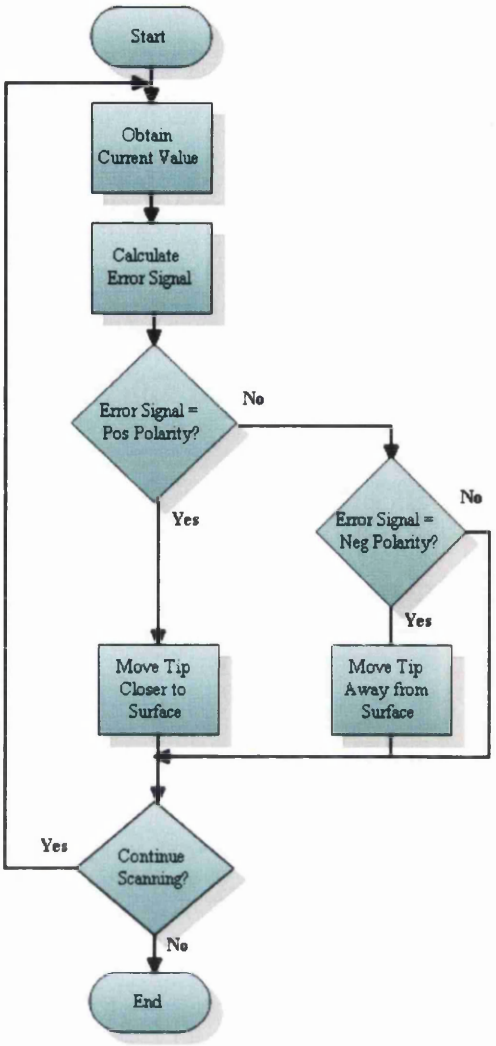

Figure 3-5 Operation Principle of STM Feedback Loop

Another point to note for this feedback loop is the factor called "gain". A simple explanation of the term is the sensitivity of the feedback loop in responding to the error correction. It is important that this parameter is set correctly due to the significant impact on the image scanned.

If the gain value selected is too large and the tip encounters a feature on the surface of the sample, the tip would respond too rapidly with possible overshoot. If the change in direction is downward, then this poses a risk that the tip might crash in to the surface. Even if not, the image obtained will consists of "spike-like" features from the overshoot.

In contrast, if the gain value is too little, the tip will respond very slowly to the change in tunnelling current. This could result in blurry images, in which the features could be elongated, showing a "tail-like" feature instead of clear images. The tip may also not be able to retract away from protrusions in time and crash on them.

For the Omicron system used in the course of this research, the optimum gain value can be gauged by comparison of the forward and backward line scan, which makes up the STM topographic image. These two scans should be near-identical to one another with none of the conditions mentioned above.

3.5.2 Constant Height

When STM is operating under this mode, the feedback loop is turned off completely, with the tip allowed to scan across the surface of the sample at a high speed, with a pre-determined height from the surface(Figure 3-6). Since the tip-sample separation is maintained, the tunnelling current recorded by the system would vary according to the different material conductance as a function of tip position, which in turn provides the information for producing the topographical images of the STM. Due to the feedback loop being turned off, this mode of operation is not affected by the response time required in the feedback loop, thus grants a higher scanning rate. This would improve the image distortion that was caused by thermal drifts and piezoelectric hysteresis. However, the drawback of this mode is the requirement of atomically flat sample surfaces, which are required for the tip not to have a possibility of crashing into surface protrusions.

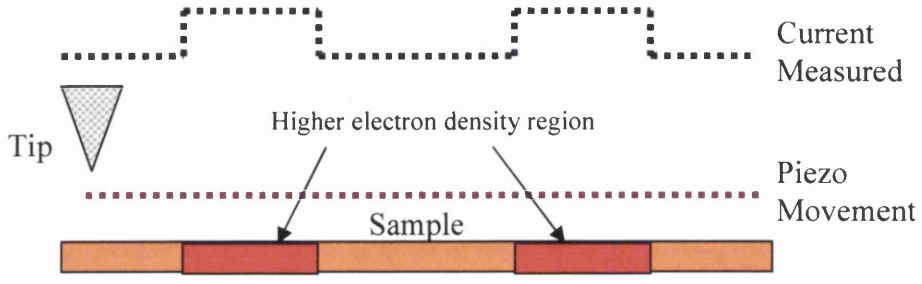

Figure 3-6 Schematic Illustration of Constant Height Mode

3.6 VOLTAGE-DEPENDENT IMAGING

As mentioned previously in this chapter, the STM topographic images were produced by means of either variation of the tunnelling current or the adjustment on the piezoelectric motor in positioning the tip, depending on the mode of operation selected. However, the bias voltage across the tip and sample determines which electronic states are accessed during tunnelling as well as the direction of the tunnelling current (either into or out of sample).

A good illustration is the Silicon (111) surface. Silicon is a very common material in the semiconductor industry. The Silicon (111) (7x7) reconstruction was first observed by Schlier & Farnsworth[16] using low energy electron diffraction (LEED) in 1959. Since then, many models were developed to hypothesize the structure of this surface, but none of these could be confirmed, until the intervention of STM. The acquisition of atomically-resolved STM images of the surface structure by Binning and Rohrer[17] evolved a widely-accepted dimer-adatom-stacking (DAS) fault model[18], which explained the Si(111) 7x7 reconstruction.

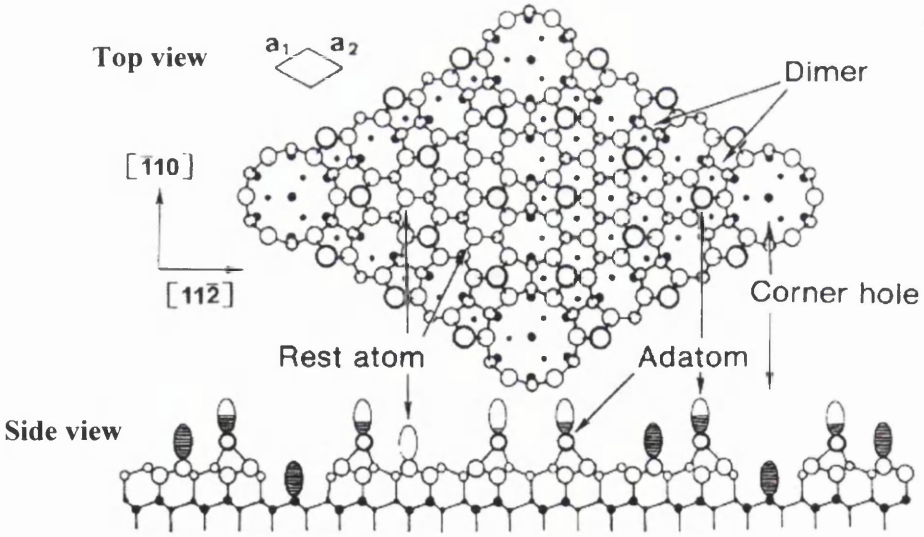

Figure 3-7 Dimer-Adatom-Stacking fault (DAS) Model of Si(111) 7x7 reconstruction

Referring to the schematic of the dimer-adatom-stacking (DAS) fault model (Figure 3-7) proposed by Takayanagi[18]. The Si (111) surface consists of repetitions of the above pattern, which can be recognised through the 4 deep corner "holes" marking the pattern.

The further networking of these deep "holes" connects the corners of the 7 by 7 mesh. Within the marked region are the twelve protrusions within the 7 by 7 mesh, known as the adatoms. And each adatom is bonded to three atoms (also known as rest atoms) in the second atomic layer.

Breaking the symmetry of the 7 by 7 along the short diagonal, it is noted that the left half of the model has a stacking fault in the third and fourth atomic layers, hence referred to as "the faulted half", while the right half is known as "the unfaulted half". There are 19 dangling bonds in each unit cell, 12 at the adatoms, 6 at the rest atoms and 1 at the centre atom deep in the corner hole. Each dangling bond can exhibit different energy levels as illustrated in the DAS model (Figure 3-7).

It has been mentioned that STM operates by interactions between the electron states of the sample and the tip (refer to section 3.2), therefore it is theoretically possible to visualise the relative spatial relationship between various electronic states, and hence map the electronic structure of a surface with atomic resolution. With the technique of current imaging tunnelling spectroscopy (CITS), Hamers[4.19] has successfully shown the localisation of various surface states on Si (111) 7x7. CITS is a spectroscopic mode which enables spatial mapping of differences in conductance (I/V), producing images of various electronic states at particular voltages, in another word, a voltage dependent imaging method.

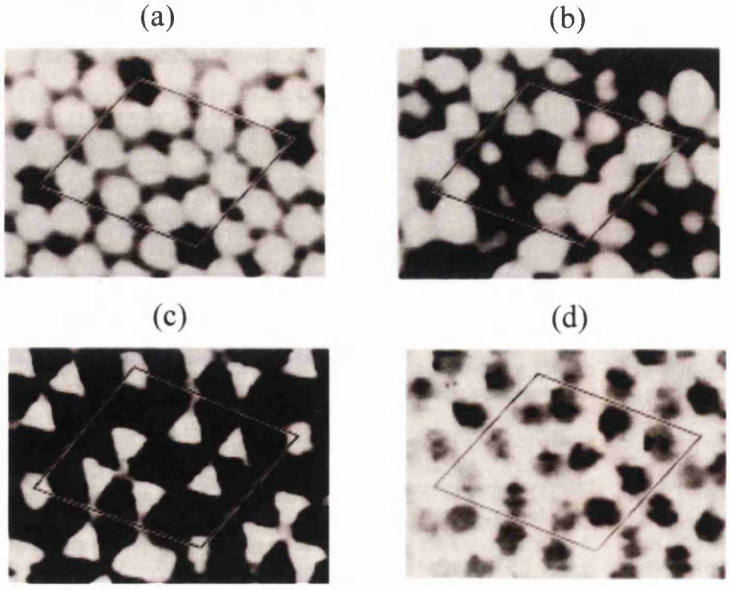

Figure 3-8 **STM images of Si(111) 7 by 7 surface. (a) Topographic image at +2.0V. Images of CITS Analysis between (b) -0.15V and 0.65V (c) -1.0V and -0.6V (d) -2.0V and -1.6V**

Figure 3-8 (a) image shows the surface of Si (111) (7x7) surface, with the right regions showing the 12 protrusions (adatoms) within the mesh being marked by the 4 deep "holes" at each corner, as a diamond shape structure. (b) to (d) shows the result of the CITS imaging technique on the Si(111) surface with respect to the variation in voltage.

The difference in the images between -0.15 and -0.65V (Figure 3-8 (b)) shows that the tunnelling current from the 12 adatoms were somewhat different across the (7x7) mesh. The currents flowing across the adatoms in the faulted half is higher compared to the unfaulted half. Also in general, more current comes from the adatoms adjacent to a corner hole when compared to the adatoms located towards the interior of the mesh.

Figure 3-8 (c) shows a differential current image acquired with voltages between -1.0 and -0.6V, which pointed out the position of the six dangling bonds associated with the rest atoms. The last image (d) is obtained with a bias voltage between -2.0 and -1.6V, showing the occupied states on the surface. It reveals the region of higher current density corresponding to Si-Si backbonds and bright spots at the corner holes.

As demonstrated, studies on different electronic states at the surface can be conducted with the aid of images obtained at different bias voltages, as well as investigation of CITS images taken at different voltage ranges.

Apart from the demonstration, voltage dependent imaging techniques can be used to determine if a feature scanned by STM on the surface is of electronic effect or physical topography[20]. Since images produced by STM come from a measurement of LDOS at the surface, the variation in voltage would reveal a difference in assessment of states, hence an image of different brightness that shows an electronic effect. Physical topographic features show no response to the variation in scanning voltage.

3.7 SCANNING TUNNELLING SPECTROSCOPY

As mentioned earlier, the evolution of STM throughout the years has developed more capability than just providing topographic information. The sample bias voltage which determines the electronic states that contribute to tunnelling current forms the foundation of Scanning Tunnelling Spectroscopy (STS). By varying the potential difference, a spectroscopic investigation can be carried out, allowing the study of the local surface phenomena.

3.7.1 Theory of STS

STS shows the relationship between the tunnelling current and the surface electronic states by variation of the voltage between the tip and surface sample. The local electronic states are represented by the following approximation, assuming that the LDOS of the tip has no variation throughout the course of measurement:

$$I \propto \int_0^{eV} \rho_S(E)\rho_T(-eV+E)dE \qquad (3.6)$$

where this approximation has taken into account the voltage dependence of the surface wave function.

Looking at an example of STS spectra for clean-cleaved n+ GaAs (110) shown in Figure 3-9, during the variation of voltage, electrons would tunnel from the full states of the sample into the empty states of the tip with negative sample bias, until the Fermi levels of tip meets the valence band of GaAs (≈-1.4V). As the voltage approaches 0V, the Fermi level of tip gets higher than the conduction band of the sample, which results in electrons tunnelling from the full states of the tip into the empty states of the sample.

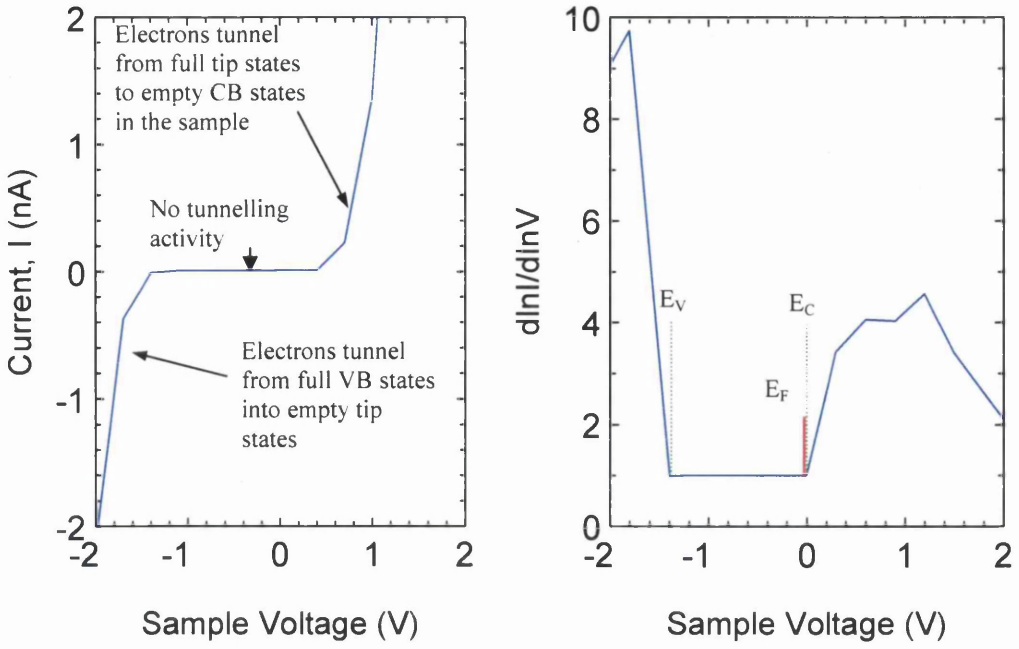

Figure 3-9 STS spectra for clean cleaved n+ GaAs (110)

Since the LDOS of the tip is assumed to remain constant, the first derivative dI/dV is proportional to the LDOS of the sample[21]:

$$\frac{dI}{dV} \propto \rho_S(E_F - eV) \qquad (3.7)$$

The above equation can be calculated by differentiation of equation (3.6). Even though the above equation relates to the surface LDOS, there is still no simple relationship to the density of states $\rho(-eV + E)$. Feenstra[21] proposed a normalisation of the differential conductance $\frac{dI}{dV}$ to the total static conductance $\frac{I}{V}$ to achieve such a relationship, which is as follows:

$$\frac{(\frac{dI}{dV})}{(\frac{I}{V})} = \frac{d\ln I}{d\ln V} \qquad (3.8)$$

This is a reasonable representation of the quantity measured using the STS method demonstrated above.

3.7.2 SPECTROSCOPIC MEASUREMENT

STS operation involves holding the STM tip over the surface at a fixed height, and measuring the tunnelling current as a function of the applied voltage, which increases in small steps over the predefined range (covers both negative and positive potential difference). This method is often referred to as 'sample-and-hold', achieved by Hamers[19] in 1986.

During operation, the feedback loop of the STM is temporarily disabled, so as to maintain a fixed tip-sample separation throughout. The tip needs to be held at a fixed height within 0.01Å because any variation of the tip height will change the tunnelling current much more than most surface features, both topographically and electronically, and thus affect the measurement. In this way, the I-V measurement performed at every pixel on the topography image would provide the localised spectroscopic information on the surface.

3.8 TIP AND SAMPLE INTERACTION

Several times in this chapter the high resolution that can be obtained using STM has been mentioned. However, this achievement is governed by the interaction between tip and sample, particularly the sharpness of the tip. Throughout this chapter, it was assumed in all situations that the STM tip used was atomically sharp, in other words, with only a single atom at its apex. However, in reality, the sharpness of the tip could be compromised either through not being etched to ideal sharpness or through degradation during a long scan.

Figure 3-10 demonstrates the importance of having an atomically sharp tip on an STM image. Looking at (a), where an ideal STM tip was used to scan across the sample, an ideal topography can be obtained. If a slightly blunt tip is being used for scanning, it still manages to produce quite a clear image but the sharpness of the image would be of compromised (b).

Figure 3-10(c) shows the situation when a tip had been crashed during scanning, where the tip is so blunt that the apex is larger than the surface feature. If this tip is used to perform scanning, the tip would be imaged by the feature instead of the tip

imaging the feature. This results in difficulty in interpretation of the STM images obtained as they represent the state of the tip instead of the state of the sample.

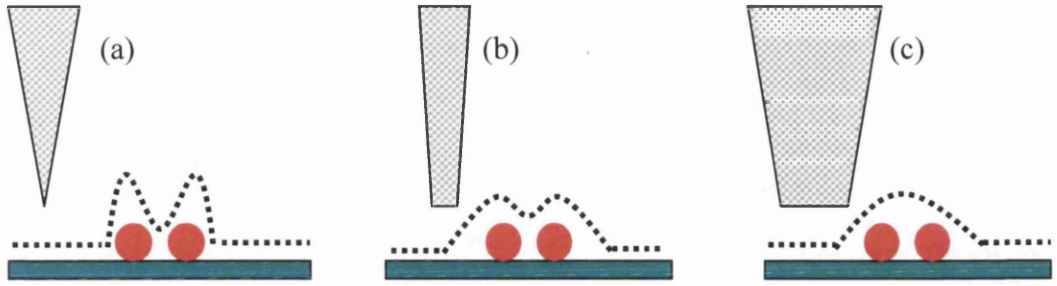

Figure 3-10 Scanning with (a) Atomically sharp tip (b) Acceptable Tip (c) Blunt Tip

Apart from the probe tip, the sample surface is as equally important a factor which could alter the STM image. To obtain atomically sharp images, it is crucial that the sample surface should be atomically flat and free of contaminants.

Lastly, a factor that needs to be taken note of during STM imaging is the effect of tip-induced band bending[22]. It is believed to restrict the accuracy of STS measurements. The effect has proven to be a function of sample doping concentration and the radius of curvature of the probe tip. Normally, this effect can be neglected or minimised when using samples with large doping concentration, e.g. higher than 10^{19} cm^{-3}

3.9 STM IMAGES

As STM continues to evolve, it is no longer restricted to just scanning or spectroscopic functions. The development over the past 10 years has been an exciting journey. Some examples of what the modern STM is capable of are shown below. Figure 3-11 (a) and (b) shows the deposition of one material on top of another using the STM tip[23], (c) and (d) shows moving the atoms around a surface with the STM tip to form a circular corral[24] as well as the corral collage[25], (e) shows the capability of STM in analysing two materials[26] and (f) data storage with the aid of electron deposition method[27].

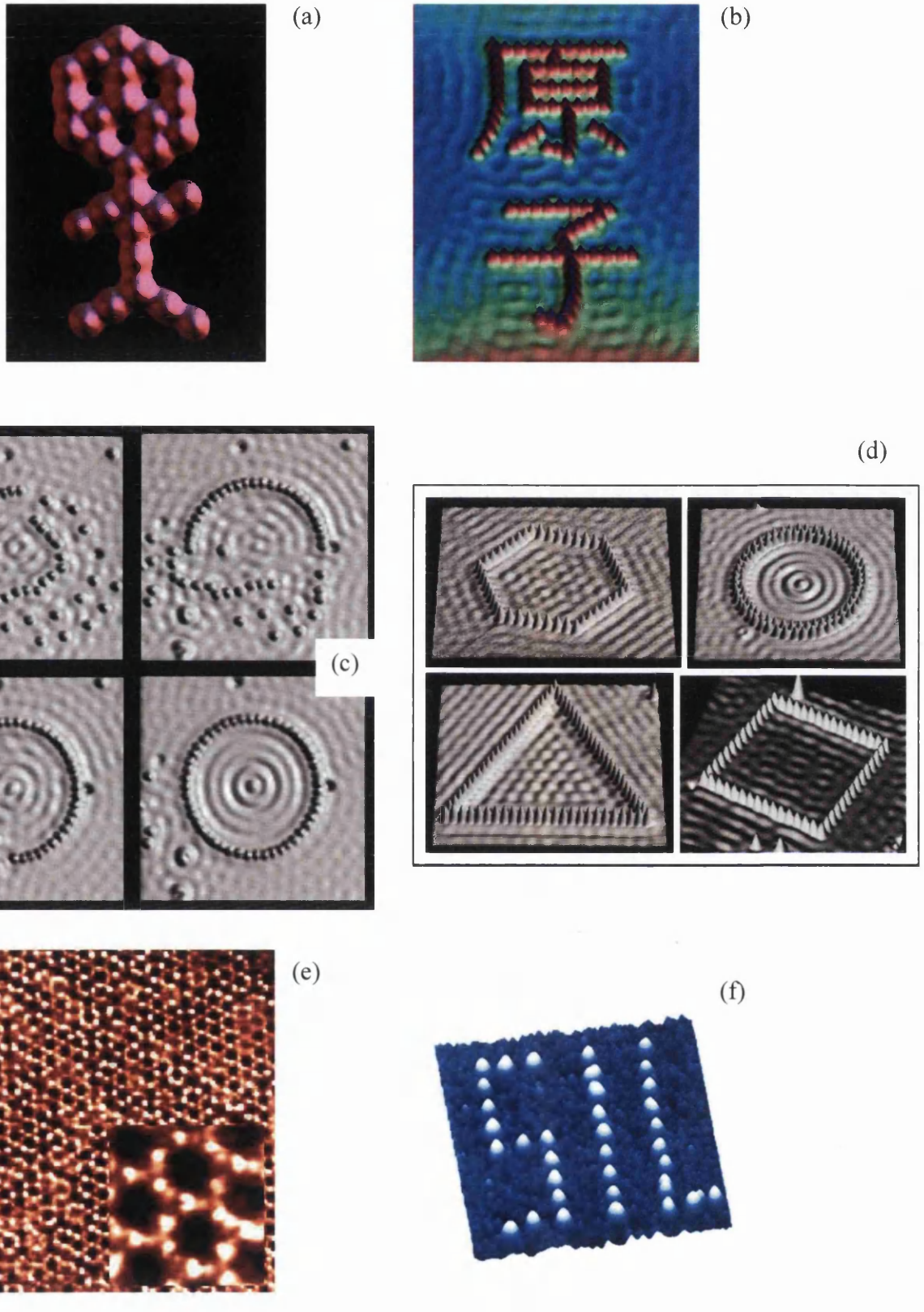

Figure 3-11 (a) Carbon monoxide on Platinum (111) (b) Iron on Copper (111)
(c) Making of Circular Corral with Iron on Copper (d) Corral Collage with Iron on Copper
(e) Gold (111) and oxide with Ethylene Molecules (f) Data Storage by Electron Deposition

The few examples shown above illustrate that STM has more potential than its initial intended function. The exploration of this technique is an endless journey, which will bring more exciting developments to the technology. In this thesis, the STM technique is used for both imaging and patterning on tin dioxide surface; whilst STS and voltage dependent imaging methods provide more insights in to the understanding and analysis of the data acquired through the course of study.

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CHAPTER 4 EXPERIMENTAL TECHNIQUE

The theory of STM and STS had been covered in the previous chapter. The experiments presented in this study were carried out in an ultra-high vacuum (UHV) environment. Under such circumstances, the sample could be examined with little or no contamination. To efficiently apply the surface analysis techniques, it is essential to be aware of the practical aspects of each technique. The purpose of this chapter is to give a brief description on the equipment and procedures used. Such as details of the sample preparation and the equipment used for high temperature experiment and gas exposures.

4.1 SAMPLE PREPARATION

4.1.1 Substrate

To encourage the best results from the STM system, it is important to have a flat (preferably atomically flat) substrate for the sample. Silicon (100) is an ideal choice due to its flatness, as well as the low cost. For the experiments presented in this thesis, 2mm by 9mm Silicon substrates were used.

4.1.2 Tin Dioxide Nanopowder

For all the experiments performed in this research, tin dioxide nanopowder was used. This was made by H. Ferkel[1] *et al* in Germany, using a laser ablation technique. Figure 4-1 shows a schematic diagram of the equipment used to fabricate the nanopowder. To produce the tin dioxide nanopowder, a 1.2kW Nd-YAG laser was aimed on the rotating tin dioxide sample rod in an argon filled chamber, at 1mbar. The size of the grains is related to the pulse width used of the laser.

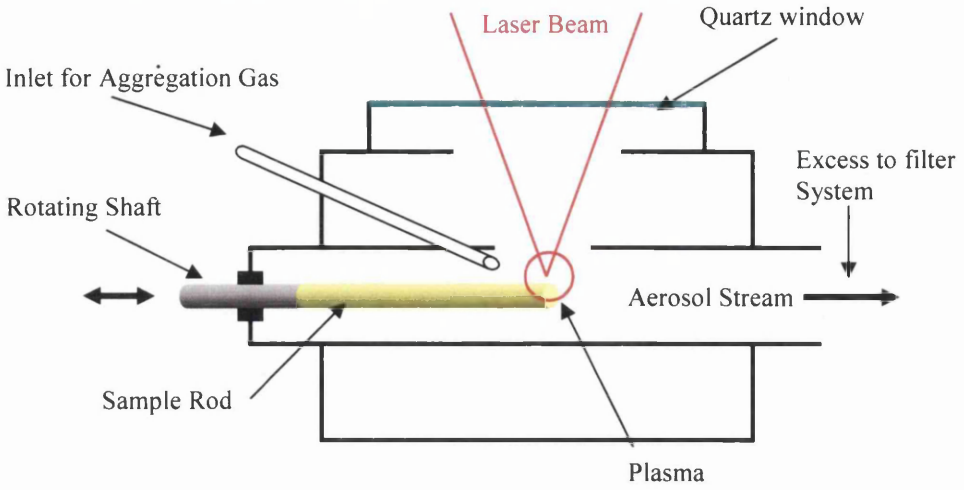


Figure 4-1 Schematic representation of laser evaporation equipment

4.1.3 Tin Dioxide Deposition

At Swansea University, nanocrystalline tin dioxide was initially studied in order to gain a better understanding of its gas sensing mechanism. Primarily this involved the techniques of x-ray photoelectron spectroscopy and STM/STS. Over the course the STM studies the ability to selectively pattern the surface by applying voltage pulses was discovered (refer to chapter 2). There are many sample preparation techniques available for thin film fabrication, especially for gas sensing applications, such as the Sol-Gel technique, radio-frequency (RF) sputtering and dip coating. All samples used this study were made using a variation of the dip coating method, which was developed by T.K.H. Starke at Swansea University[2].

To reduce the possibility of contamination during the sample preparation, all apparatus used in the process were cleaned with Isopropanol. The technique starts with putting a very small scoop of 8nm tin dioxide nanopowder (with a spatula) in a pestle and mortar, which is then lightly ground so as to remove any large agglomerates that might be present. With the aid of needle, a few droplets of α-Terpineol is then added and stirred to form a suspension. This is then left for about ½ hour so that the larger agglomerates of tin dioxide will sink down to the bottom of the mortar, leaving the smaller tin dioxide particles (ideally single grains) on the surface of the suspension.

Using the spatula, contact is made so that the surface tension is just broken then withdrawn. The spatula is not submerged into the solution, and a drop from the suspension is formed on the end of the spatula. This process is aided greatly by the thick viscosity of the α-Terpineol. This droplet is then deposited onto the surface of the substrate, and then placed on a hotplate (shown as Figure 4-3(a)) set to be about 250°C, so as to evaporate the α-Terpineol. This leaves a thin layer of tin dioxide particles on the substrate, and the process is repeated several times to achieve the desired thickness.

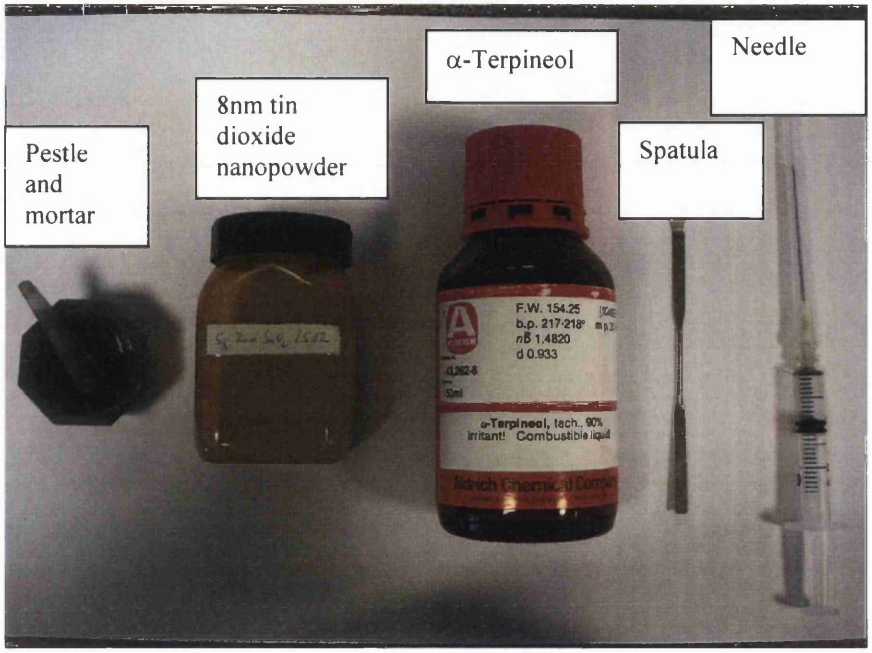


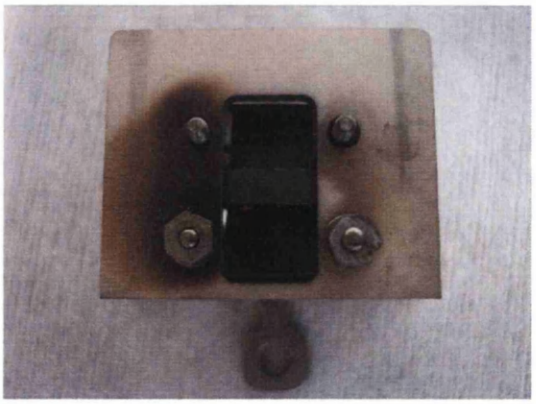
Figure 4-2 Apparatus Used for Sample Preparation

Once suitably coated, the substrate is then placed in a tube furnace (Figure 4-3 (b)). The temperature is then increased at the rate of 18.5°C per minute from room temperature until it reaches 400°C. This temperature is maintained for 20 minutes before being allowed to cool down naturally back to room temperature.

Figure 4-3 (a) HotPlate (b) Furnace

4.1.4 Preparation for Scanning

When using the UHV SEM/STM Omicron system, samples are mounted in a resistive heating sample plate (refer to Figure 4-4 for the positioning of the sample). Sample is held in position by 4 nuts on the top, where only 2 were shown in the figure. While fastening the nuts, a vernier calliper is used to ensure that the gap between the surface ceramic plate and the heating element point (Figure 4-4(b)) is measured as 3.0±0.1mm. This ensures that samples can be safely transfered inside the system, and will fit correctly to the scanning stage.



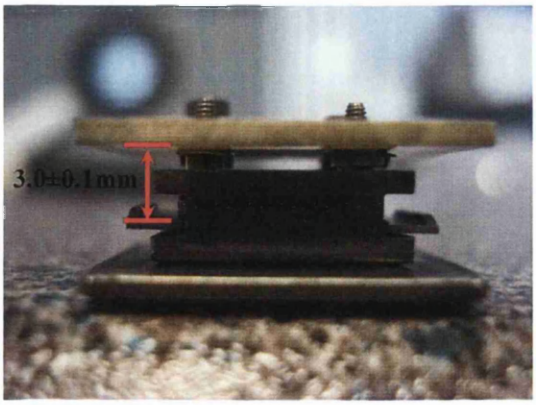


Figure 4-4 (a) Resistive Sample Plate (Top) (b) Resistive Sample Plate (Side)

Once loaded into the system, the sample is degassed in the preparation chamber (Figure 4-7) before scanning. It is placed on the manipulator stage and heated through the heating element in the sample plate. During this procedure, the pressure in the chamber needs to be maintained below $1x10^{-8}$ mbar. The current passing through the heating element was increased gradually, until the power was calculated as 4.5W. The sample is left heated for either 1 hour or until the pressure in the chamber reads below $1x10^{-9}$ mbar.

4.2 TIP ETCHING PROCEDURE

As mentioned in chapter 3, it is important to have an atomically sharp tip, especially if atomic resolution STM images are to be achieved. At present, there are several methods available to fabricate atomically sharp tungsten tips. A method proposed by Fotino[3] involved a two-stage alternating current electrochemical etching process, that is, normal etching and reverse etching, was used in the patterning experiment conducted by A. Houel[4]. Another more simplified method described by Ibe *et al*[5] was used to produce all the tips used in this study. This involves a direct current electrochemical etching method.

Tungsten wire of 0.25mm diameter is immersed about 2mm below the surface of 2 Mol potassium hydroxide (KOH) solution, and forms the anode of the cell. The cathode of the cell is made up by the stainless steel beaker containing the solution (Figure 4-5)

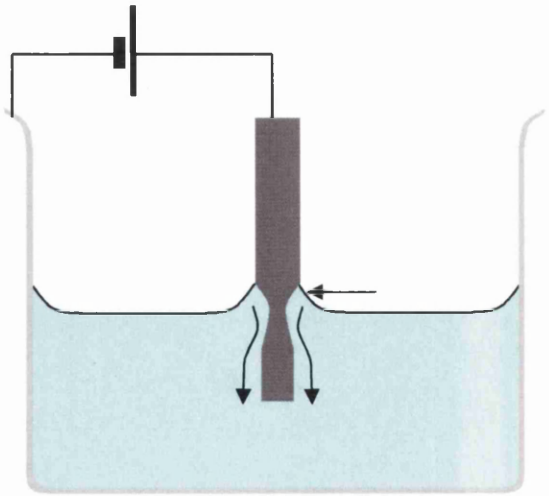


Figure 4-5 Electrochemical Etching Schematic Diagram

By applying a 9V DC across the immersed tungsten wire and the beaker, the cathode (beaker) provides electrons to the solution and reduces KOH to give hydroxide ions (OH^-), which oxidise the tungsten wire, forming a soluble tungstenate (WO_4^{2-}), etching the wire at the air and solution interface. This reactions continues until the weight of the tungsten wire below the solution level exceed the tensile strength of the etched section of the wire and therefore breaks (Figure 4-6), forming a tip[6].

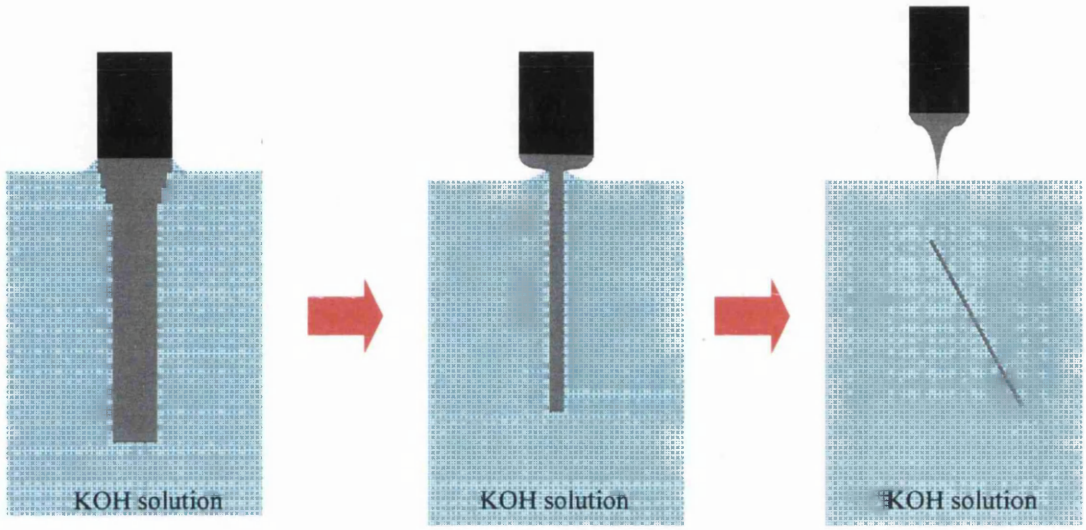


Figure 4-6 Tip Etching Process

It is important to note that during the course of etching process, the solution needs to be left undisturbed as this could result in tips of irregular shape due to the deformation of meniscus at the solution-air interface.

4.3 THE OMICRON STM/SEM HC SYSTEM

All experimental results were acquired using Omicron STM /SEM System (Figure 4-7). The following section provides a general description on the system and details of some important aspects and techniques used during operation.

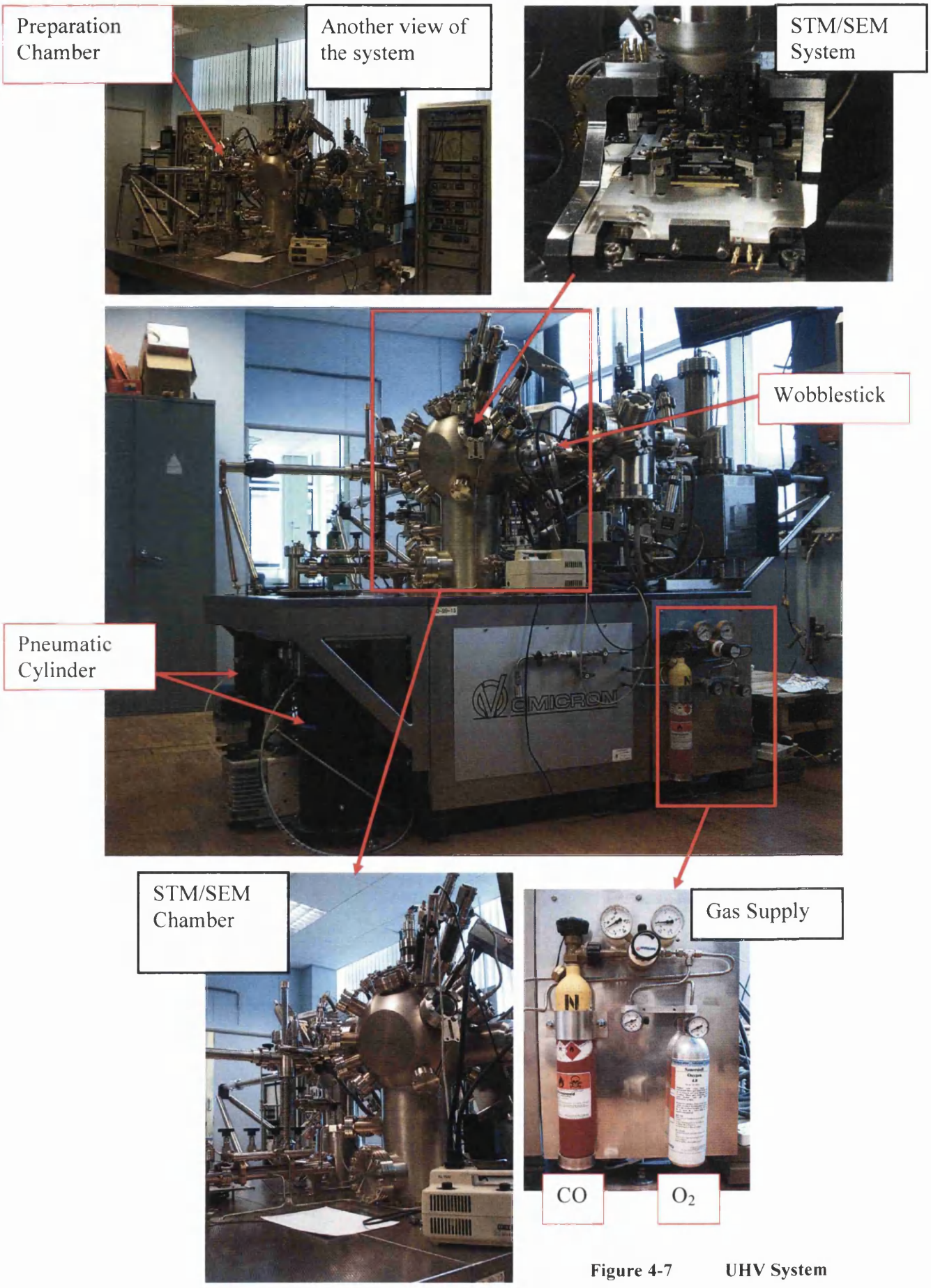


Figure 4-7 UHV System

4.3.1 General Description

In the STM/SEM system (shown as Figure 4-7) the STM stage is mounted to a goniometer via a double damping stage using Viton R rings. This is then mounted horizontally on an 8inch OD flange in a specially designed chamber. The system is mounted on a stainless steel table which is supported by 4 air legs, which provide damping to the system, isolating vibrations that would prove detrimental to scanning. A wobblestick is used for transferring or exchanging the scanner (tip) and samples *in-situ*, which are stored in a 6-way carousel.

4.3.2 Tip Positioner and Tip Scanner

The sample plate was supported by a horseshoe holder on the STM head, with the surface of the sample facing up. This sample stage can be moved in both x and y-axis by piezo inertia drives over a range of 10mm x 10mm.

The exchangeable scanner is guided by 2 pins during transfer and clamped magnetically onto the z-drives of the STM. Similar to the sample stage, the scanner can be independently moved by a 3-axes piezo inertia drive. The movement is limited to 5mm x 12mm on lateral movement and 5mm for Z approach.

Coarse positioning of the tip is performed by the user, with the assistance of a high magnification CCD camera and a television. To bring the tip into the tunnelling range, the STM control unit is switched to an automatic approach mode, which requires a setpoint of desired tunnelling current and gap voltage pre-specified by user. This automatically moves the tip in small steps towards the sample, until the preset conditions are satisfied. The following flowchart (Figure 4-8) explains both tip approaching process.

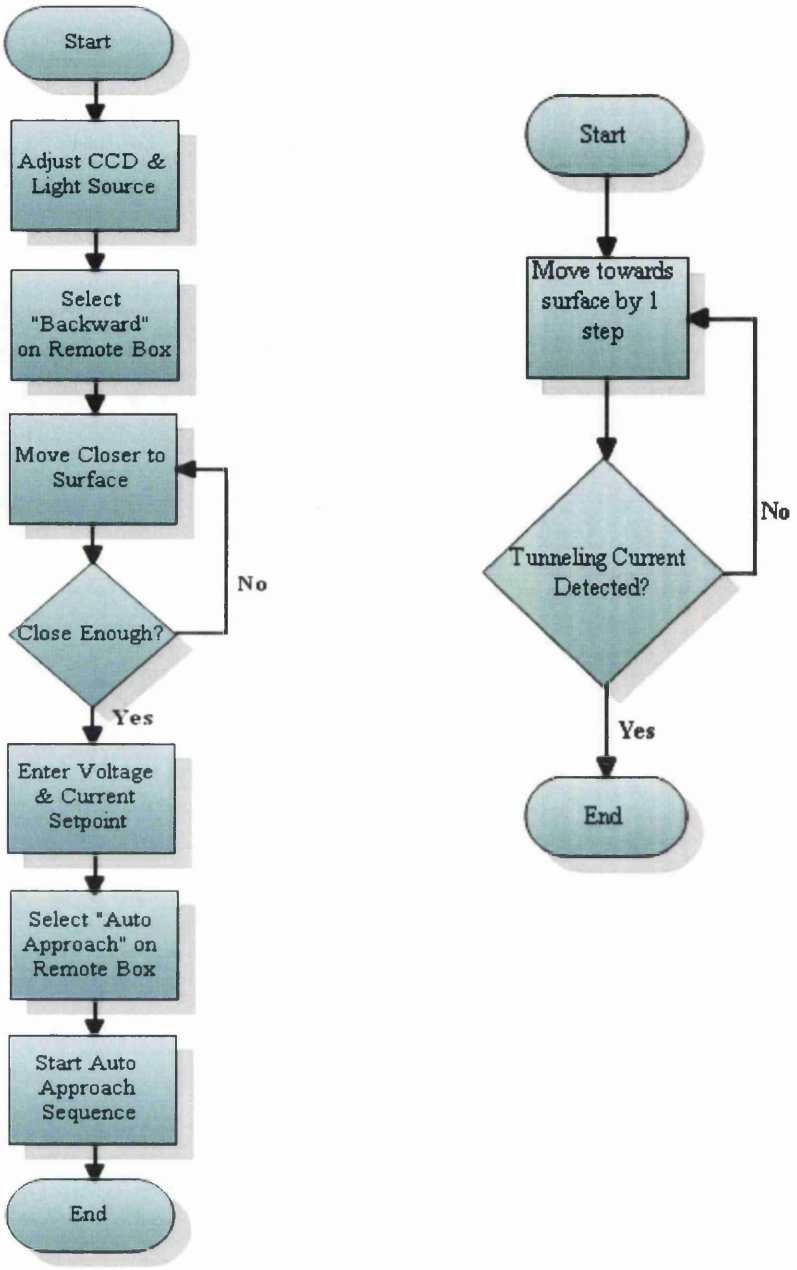


Figure 4-8 **(a) Coarse Approach Sequence** **(b) Fine Auto Approach Sequence**

The probe tip is mounted on a 1/8 inch single tube scanner, which is capable of operating up to maximum scan range of about 8μm x 8μm. This scanner is designed to provide a z-resolution of better than 0.01nm.

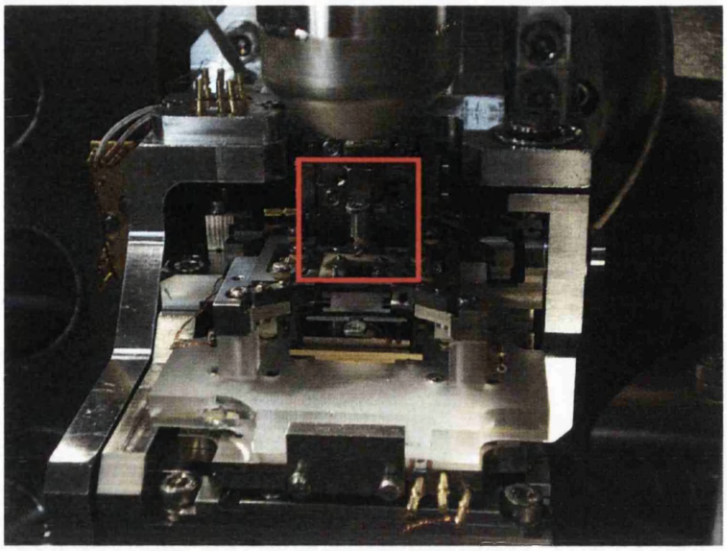


Figure 4-9 Single Tube Scanner

4.3.3 Feedback Control System

When STM is operated under constant current mode, a feedback system is required to control the tip-sample separation by maintain a preset tunnelling current. The feedback system for a typical STM is represented as Figure 4-10.

The process of feedback starts when the tunnelling current is detected by the system on the approach towards the surface. The value of the tunnelling current is amplified with a Pre-Amp to minimise the effect caused by noise and interference. The tunnelling current varies exponentially with the linear variation in the tip-sample distance. A log-amplifier is installed next to linearise the behaviour of the tunnelling current.

The signal after the log-amplifier is compared to the desired tunnelling current value, which was preset by the user. The difference between them is called the error signal, which is used to move the Z-piezo of the scanner, as the output of the feedback system after amplification. The position of the tip would therefore be moved either up or down to compensate the difference on the tunnelling current detected, trying to achieve a constant current whilst scanning. The high voltage amplifier in the system has an effective sensitivity of approximately 100nm/V. Therefore the image obtained with constant current mode will represent the variation of the tip position (Z-voltage on electronics) as a function of surface coordinates (x, y).

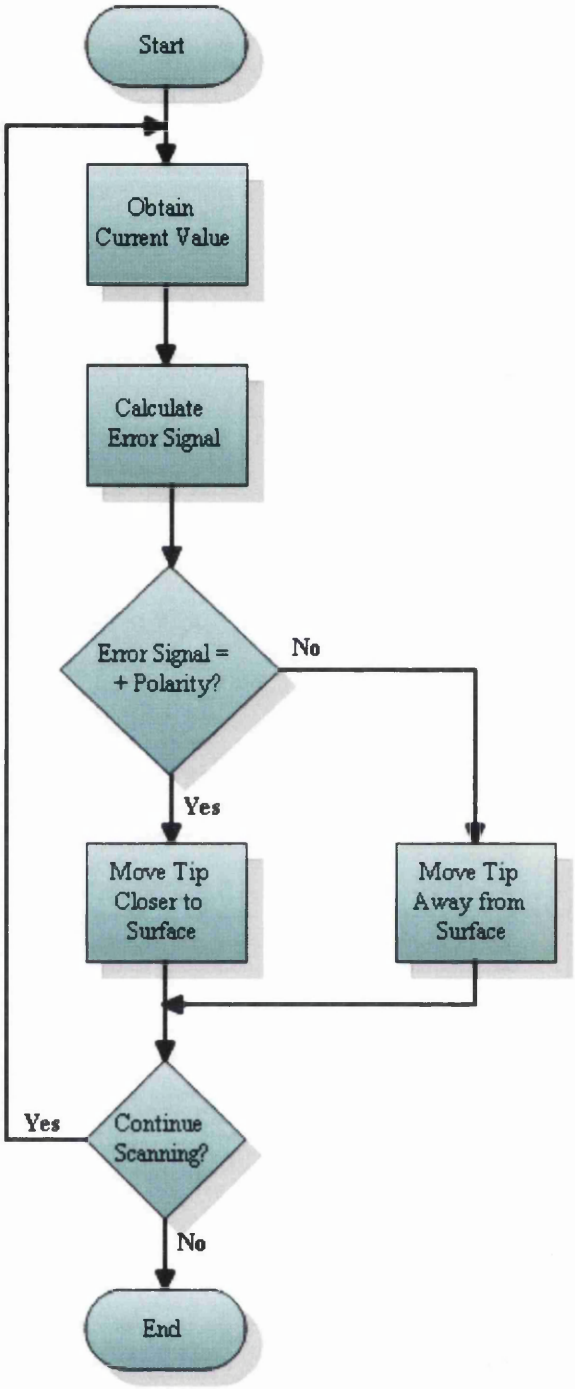


Figure 4-10 STM Feedback Loop

This feedback system is de-activated during the spectroscopic measurement. I-V measurements are then performed giving electronic information from the surface. Similarly, this function was taken off during the nanopatterning procedure, so that the position of the tip is constant throughout the process rather than being adjusted due to the high current flow during patterning.

4.3.4 STM Electronics and Software

In the Omicron system, STM/STS operation is controlled by some basic electronics. This includes a coarse positioning board, regulator board, auto-approach control board, comparator board and a piezo driver board.

The coarse positioning board and auto-approach board work hand in hand to achieve the function of bringing the tip within the tunnelling range without crashing the tip into the sample (refer to section 4.3.2). The regulator board and comparator board are responsible for the operation of feedback loop that was mentioned in the previous section. The piezo driver board would determine the scanning range of STM.

In general, the STM operates in constant current mode when the feedback control is active. Also, the adjustment of the loop gain controls the response of the probe tip during imaging. The STM will operate in constant height mode when the feedback loop is disabled. In this mode, the tip height remains fixed during scan while the variation in tunnelling current is recorded, which represents the surface topography. With the piezo driver control, the user can define the x and y scan size as well as x and y position offset and scan angle.

The electronics boards mentioned earlier are interfaced with a computer through SPM control unit. The SCALA software is responsible for translating the data acquired by electronics boards (STM system) into images and graphs, which would then be used for analysis. Also, all parameters chosen by the user for the varius function in data acquisition are managed by the computer.

The software also provides the ability for nanostructuring, which allows the user to instruct the electronics to perform certain functions via a series of command in a macro. For this study, macros were used to pattern the surface (to be explained in the later section of this chapter).

Furthermore, the software also has the ability to correct drift, which could be thermal or piezo induced. Drift effects can obscure image detail because of the variation in contrasts as well as an unusual greyscale. In the process of drift correction, the tip variation in Z as a function of x and y would be taken into account. Even so, it requires attention when defects such as steps are present on the sample. For further information on Omicron STM electronics and software, the manufacture manual[7,8,9] would be able to explain in greater detail.

4.4 GAS EXPOSURE SETUP

In order to observe the behaviour of the gas sensor under the exposure of certain gases, the UHV STM/SEM system has the ability to introduce gases into the analysis chamber. With this facility, the research in the nanopatterning has been expanded into the realm of molecular docking and nanocatalysis.

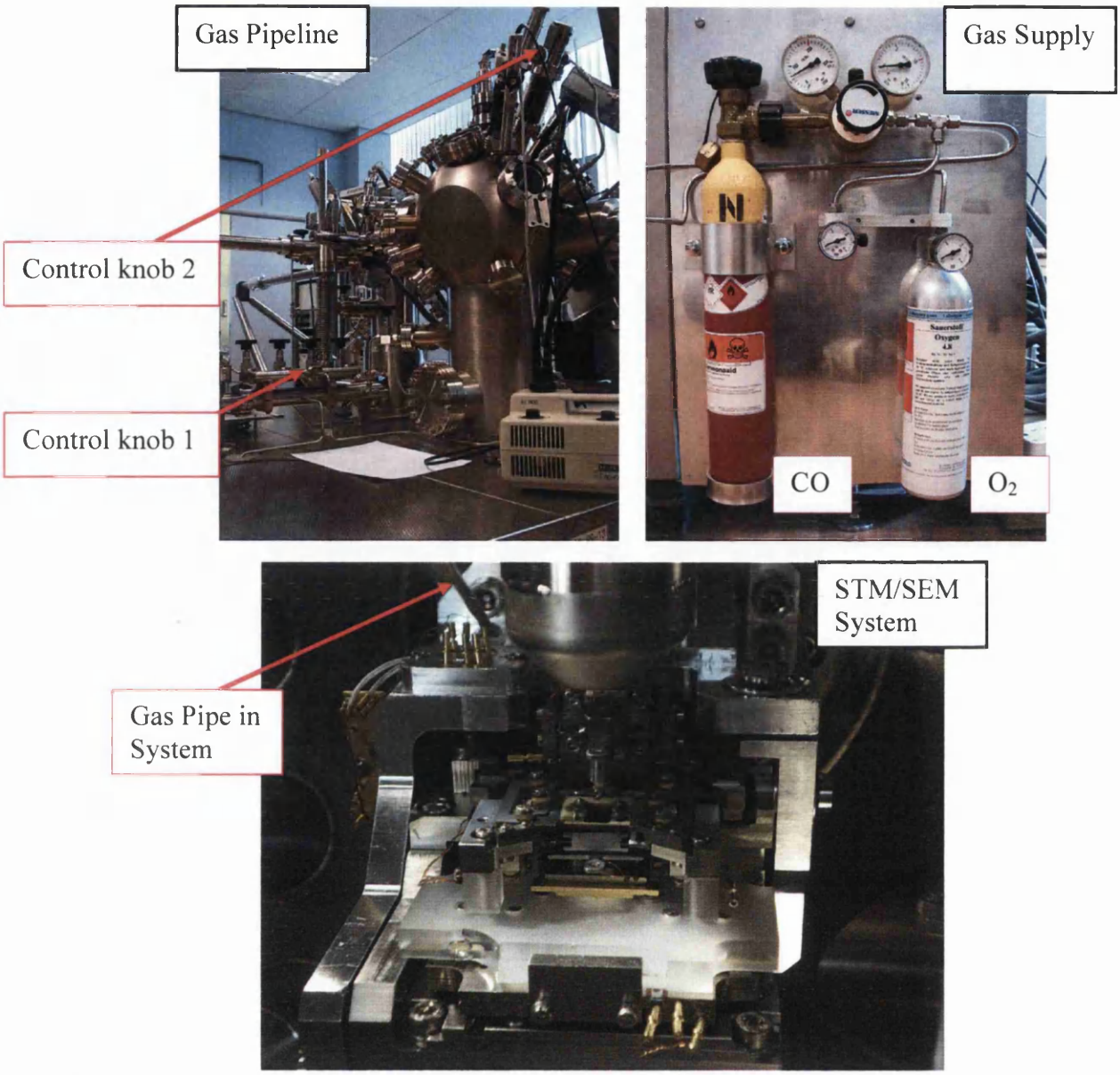


Figure 4-11 Gas Exposure Control (Hardware)

With reference to Figure 4-11, the gas pipeline out of the system was pumped to vacuum for about ½ hour with a rotary pump. The required gas is then allowed to enter the pipeline between gas supply unit and control knob 1. The gas supply is then turned off, while the gas present in the pipeline before control knob 1 is allowed to continue its path till control knob 2. The line is flushed twice in order to minimise the contaminants that are to enter the analysis chamber.

The gas pipe in the analysis chamber (Figure 4-12) is lowered until it is very close to the sample plate. After the gas pipe has been positioned, auto approach procedure can be called for and scanning may begin. Whenever gas is required to be exposed onto the sample surface, open control knob 2 slowly until the desired chamber pressure had been achieved.

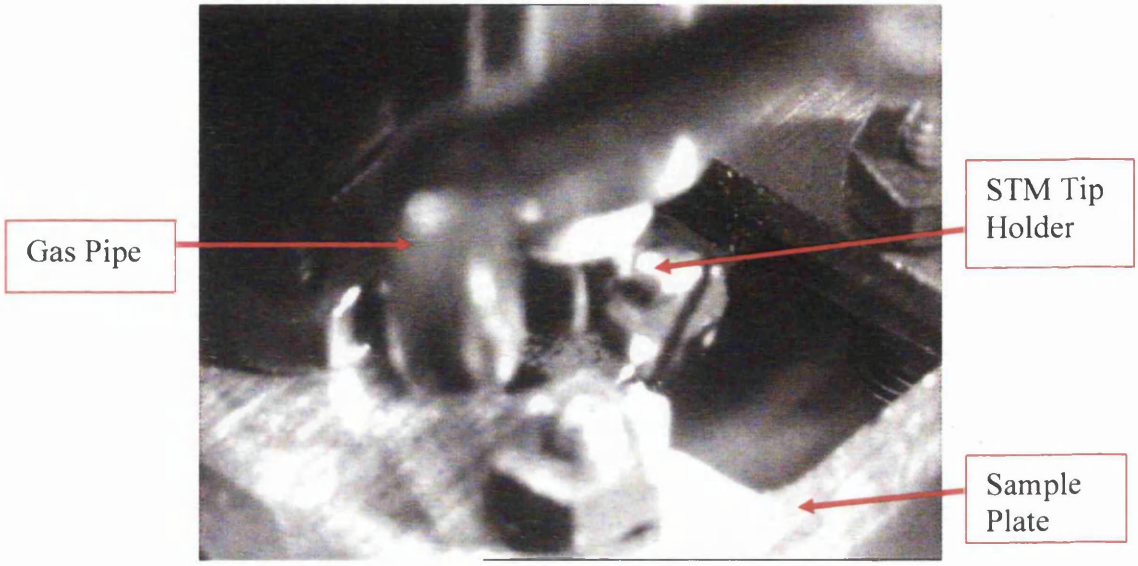


Figure 4-12 Hardware Position During Gas Exposure Experiment

After introduction of the gas required, the amount of the respective gas would slowly reduce in the pipeline. When the amount is too little to sustain the pressure required in the chamber, control knob 1 is slowly opened to replenish the supply.

4.5 TEMPERATURE CONTROL SETUP

Apart from the introduction of gas into the chamber, the system also has the facility to vary the temperature of the sample through a heating element on the stage during scanning. The HC1100 Omicron power supply (Figure 4-13 (a)) and a temperature controller by LakeShore (Figure 4-13 (b)) are used together to change and maintain the required temperature within ±2°C.

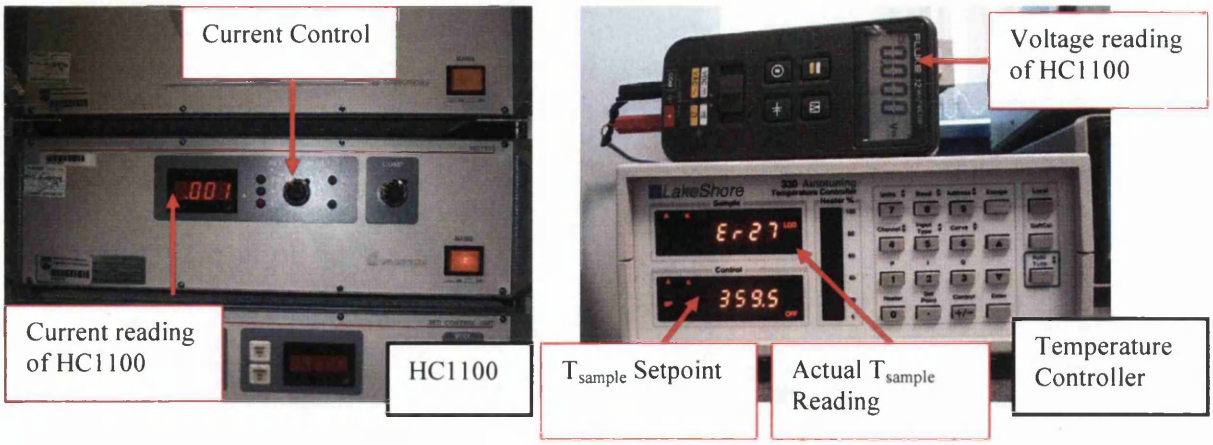


Figure 4-13 **(a) HC1100 Power supply Controller** **(b) LakeShore Temperature**

Using the following calculation, which the formula was obtained by finding the equation that represent the sample-HC1100 temperature relation graph available in user guide by Omicron[9], the temperature representation in HC1100 system was obtained:

$$T_{sample} = 2 \times T_{HC1100} - 296 \qquad \text{(temperature unit = Kelvin)} \qquad (4.1)$$

Therefore, to achieve a sample temperature (T_{sample}) of 150°C, which corresponds to 423K, T_{HC1100} is calculated to be 359.5K. This value will be used as the setpoint of the LakeShore temperature controller. The electrical representation of the sample temperature required is about 3.3W, in accordance to the temperature-power relation graph in the user guide by Omicron[9].

Slowly increase the current control knob on HC1100 (Figure 4-13(a)) until power calculated is 3.3W, which could be obtained by multiplying the current by the voltage reading of HC1100. This is incremented very slow, whilst ensuring the pressure of the analysis chamber is lower than 10^{-9} mbar. The LakeShore temperature controller would activate its feedback loop that would add, or subtract the amount of current flowing in the system to maintain the temperature of 150°C.

More detailed description of the electronics operation aspect of the instruments could be found in the manual from both Omicron[10] and LakeShore.

4.6 NANOPATTERNING PROCEDURE

Through the course of research, dots nanopatterning were done as either single dot event or a 5 by 5 matrix pattern, similar to the approach suggested by J.T. Jones [11].

A single dot patterning event only requires the "single event" function on the Omicron software, which calls for the charge macro file (Figure 4-14) and performs the patterning at the location where the user clicked on the scan.

Figure 4-14 Sequence Program off "Charge File"

The more complex nanopatterning involved the 5 by 5 matrix pattern, which is shown as Figure 4-15. This pattern is formed using Cartesian coordinates, deciding the position of the charging event to be called.

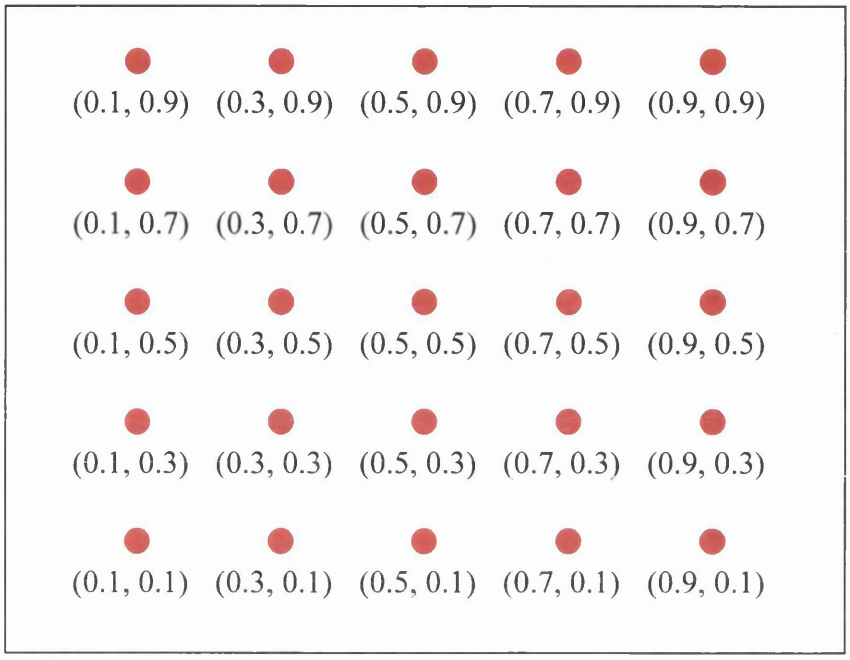


Figure 4-15 5 by 5 Matrix Grid Pattern File

This location file is used in conjuction with the macro file that controls the nanopatterning event. The sequence of flow is shown as Figure 4-16(a). The macro file is programmed in such a way that when it is called to perform nanopatterning, it will start from top left hand of the 5 by 5 pattern, meaning the (0.1, 0.9) coordinate and called the charging macro file (Figure 4-14). Upon completion, the macro will move the tip to the right and repeat the charging function on (0.3, 0.9) location. This keeps going on until the tip reaches (0.9, 0.9) location, where the tip will be moved one step down, then to the extreme left at (0.1, 0.8) position. The tip would be moved down another step to (0.1, 0.7) and started the nanopatterning function cycle again (Figure 4-16(b)). This will only be terminated when the full pattern had been written on the surface of the sample.

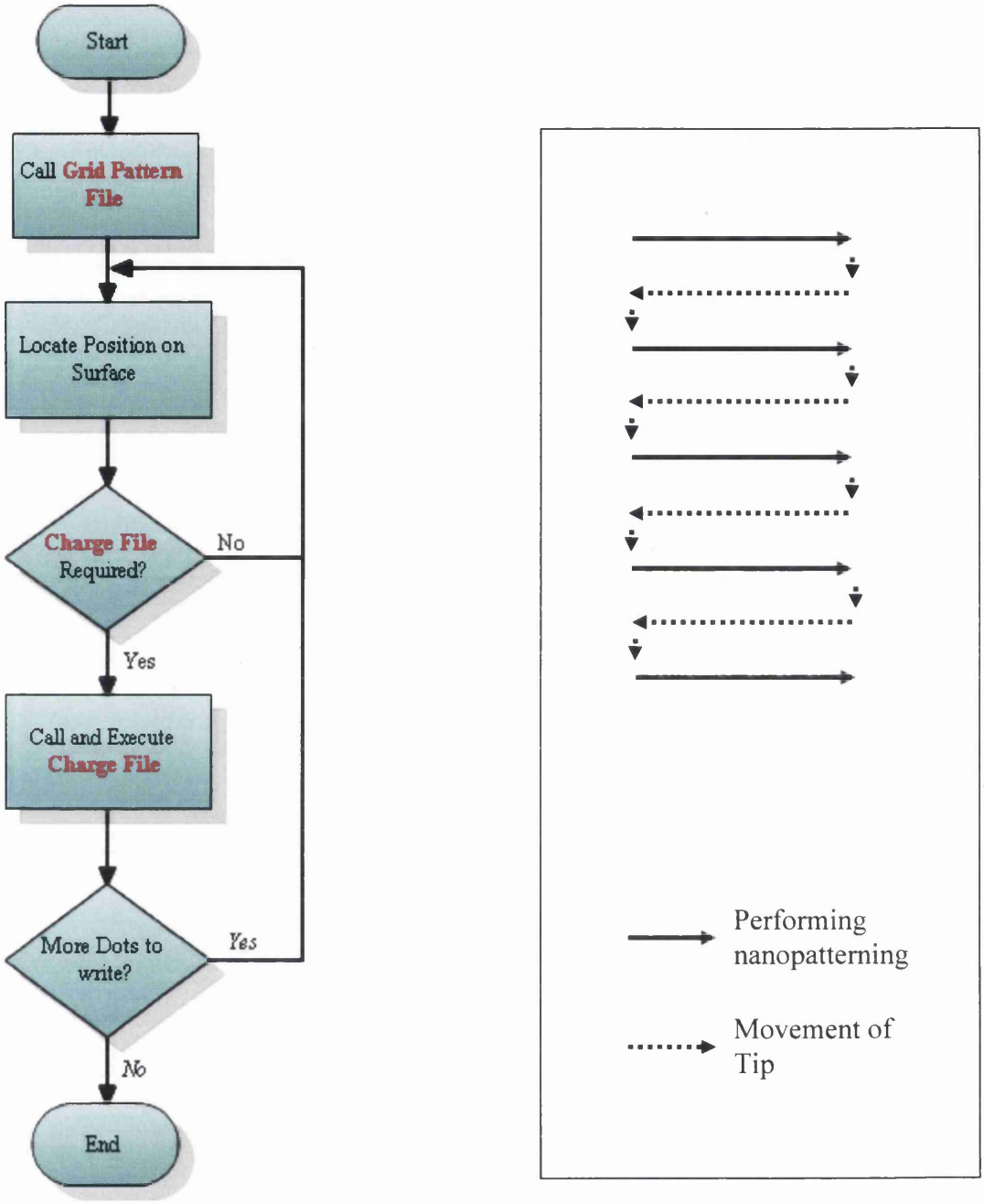


Figure 4-16 (a) Sequence Program of Grid Nanopatterning (b) Direction of Flow of Grid Nanopatterning

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CHAPTER 5 NANOPATTERNING

The hypothesis of the charge writing mechanism[5] developed through the progression of research conducted in Swansea University was explained in chapter 2. To further understand and validate this model, nanopatterning was conducted at 150°C so as to introduce a new factor. In addition, this chapter explores the connection between tip voltage and the nature of the patterned features under normal imaging conditions. In addition, all data in the chapter are acquired at the same temperature as the temperature when nanopatterning was performed.

5.1 Experimental Preparation

5.1.1 STM System

STM and STS measurement were carried out in the Omicron HC STM/SEM system at Swansea University (description of the system is in chapter 4). Tungsten wire was electrochemically etched to provide the atomically sharp STM probe tip, the procedures of the etching technique can also be found in chapter 4.

To ensure the sharpness of the apex of the tip, all etched STM tips were tested by scanning heat cleaned silicon 7x7 surfaces as shown as Figure 5-1, to provide evidence of atomic resolution and ultimate tip quality.

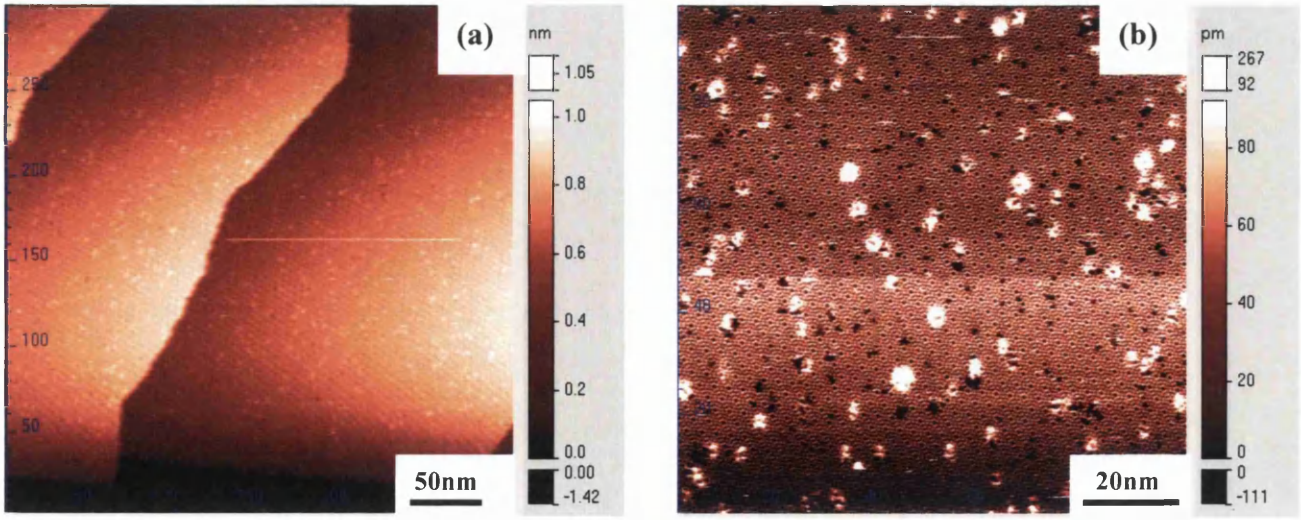


Figure 5-1 **Flashed silicon surface of size (a) 300nm by 300nm showing atomic steps, with a scanning voltage of -1.7V_{tip} at 0.4nA current**

(b) 100nm by 100nm showing a 7x7 surface reconstruction, with a scanning voltage of -1.5V_{tip} at 0.4nA current

5.1.2 Controlling Sample Temperature

In order to achieve the desired sample temperature, the material was heated with the HC1100 system, at power set-point of 3.3W, which correspond to sample temperature of about 150°C. With the "Auto Tuning Temperature" controller unit manufactured by Lake Shore, the temperature could be maintained at 150 ± 3°C (details can be found in chapter 4).

5.2 Nanopatterning Performed at High Temperature

5.2.1 Experimental Preparation

For the case of nanopatterning at 50°C and 150°, the sample temperature was first achieved by the procedure shown in section 5.1.2. When the desired temperature had been obtained, the STM tip was brought close to the surface (procedure shown in chapter 4) and scanned over the material surface so as to select the suitable site for the writing experiments. For all experiments in this section, the dots were attained with tip voltage of -6V with 100μs pulses on the designated location to form a matrix of written dots. The matrix position was designed taking the cue from the suggestion by J.T. Jones[1], together with the macro program that executed the nanopatterning process, which is explained in chapter 4.

5.2.2 Nanopatterning at room temperature, 50°C and 150°C

The resistance of tin dioxide as a function of temperature decreases as a result of more thermally activated carriers being present in the conduction band. To first understand the effect of temperature on tin dioxide during nanopatterning, the same writing parameter setting was used to create a 5x5 matrix pattern at three different sample temperature – room temperature, 50°C and 150°C as shown in Figure 5.2.

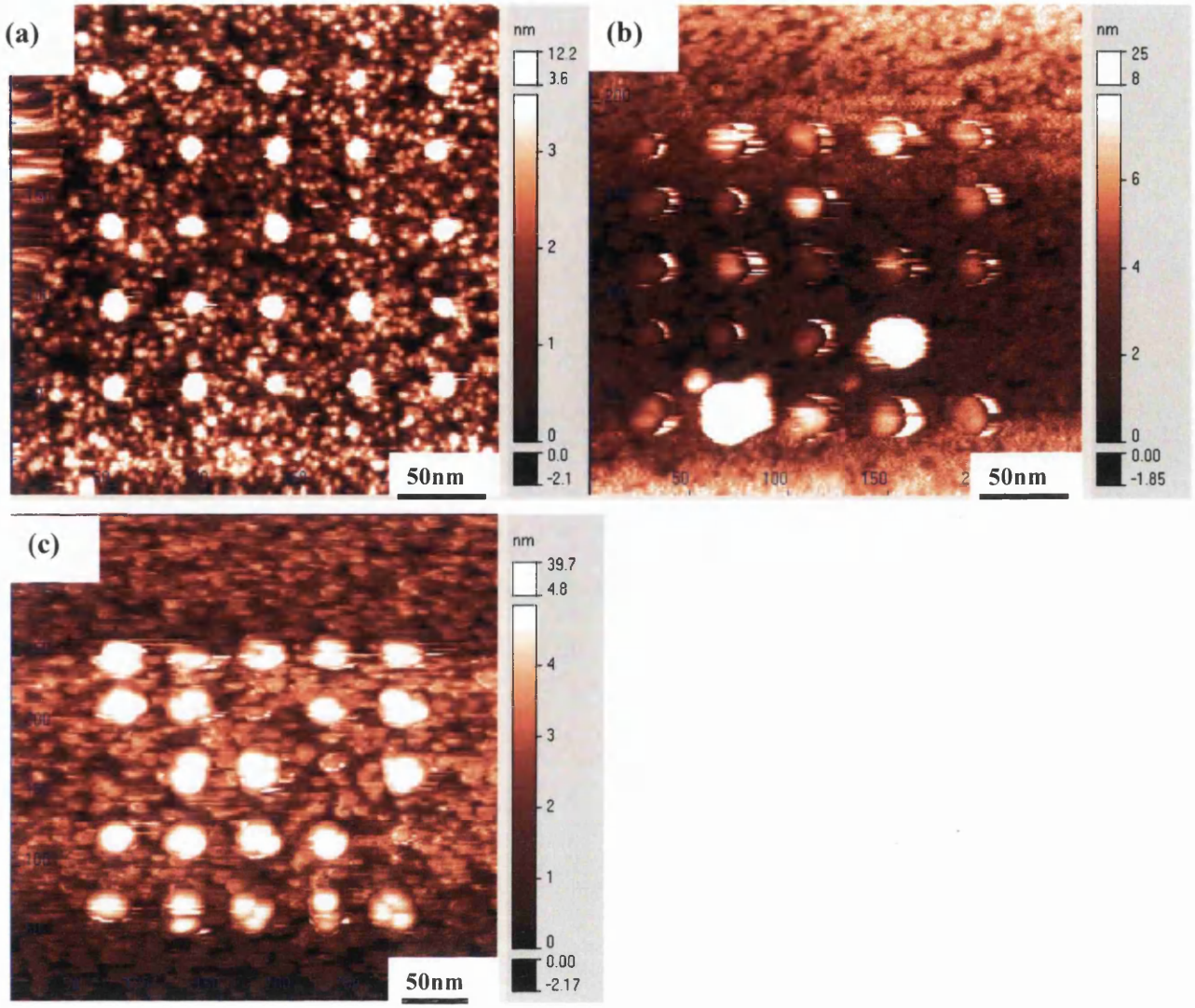


Figure 5-2 **5x5 matrix patterned on surface of (a) 250nm by 250nm at room temperature, (-3.5V_{tip} and 0.58nA current)**

(b) 250nm by 250nm at 50°C, (-3.5V_{tip} and 0.58nA current)

(c) 350nm by 350nm at 150°C, (-3.4V_{tip} and 0.57nA current)

Looking at Figure 5-2, the first impression is that the size of the written dot feature varies as a function of temperature, the smallest size being produced at room temperature. Apart from the physical size, the success rate of nanopatterning seems to be compromised as the temperature increases, where all intended features were successfully patterned for sample at room temperature (a), 92% success rate seen on nanopatterning at 50°C while only 84% of the intended features were successfully written at 150°C. The same writing parameter that provides a 100% success rate in the previous research[2] is no longer valid as the sample temperature increases.

5.2.3 Physical size studies of dots written at Room Temperature, 50°C and 150°C

As mentioned in section 5.2.2, the size of the features seems to vary with respect to the sample temperature. As such, the apparent size of the dots were measured and evaluated using the "line Profile" function available on Omicron software (refer to Figure 5-3 for example) for all of the patterned dot features.

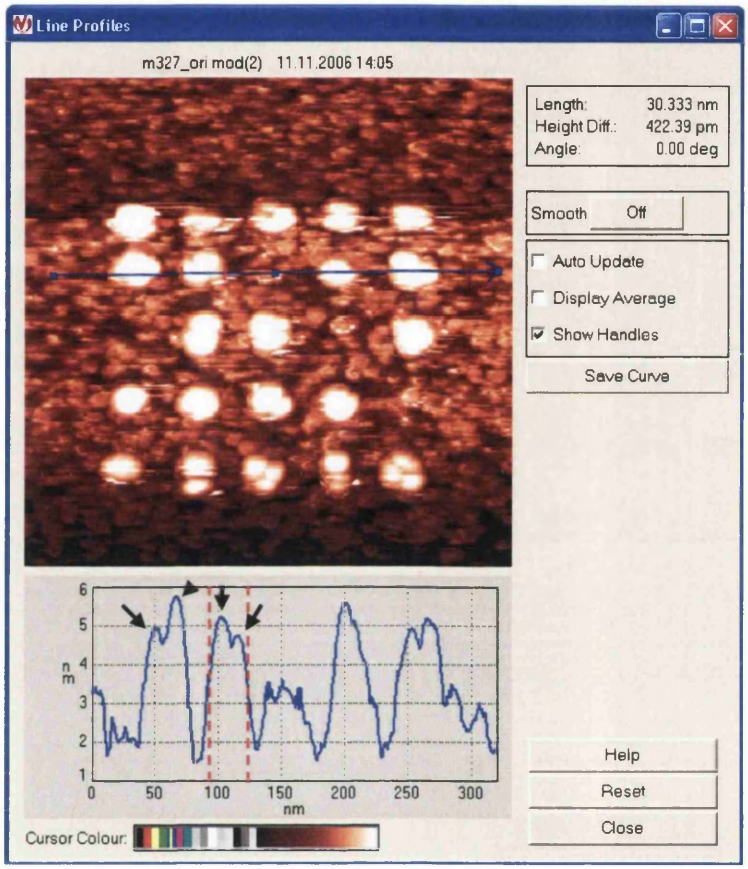


Figure 5-3 **Example of Omicron software window of the "line profile" function that is used for dot size measurement.**

All the sizes measured for the dots are then recorded in the form of matrix, where an example of such a measurement for dots patterned at room temperature is illustrated as Figure 5-4. The readings are presented in form of (x, y) co-ordinates that correspond to (width, height) of the feature. Similar measurements was performed and recorded on the images taken at 50°C and 150°C.

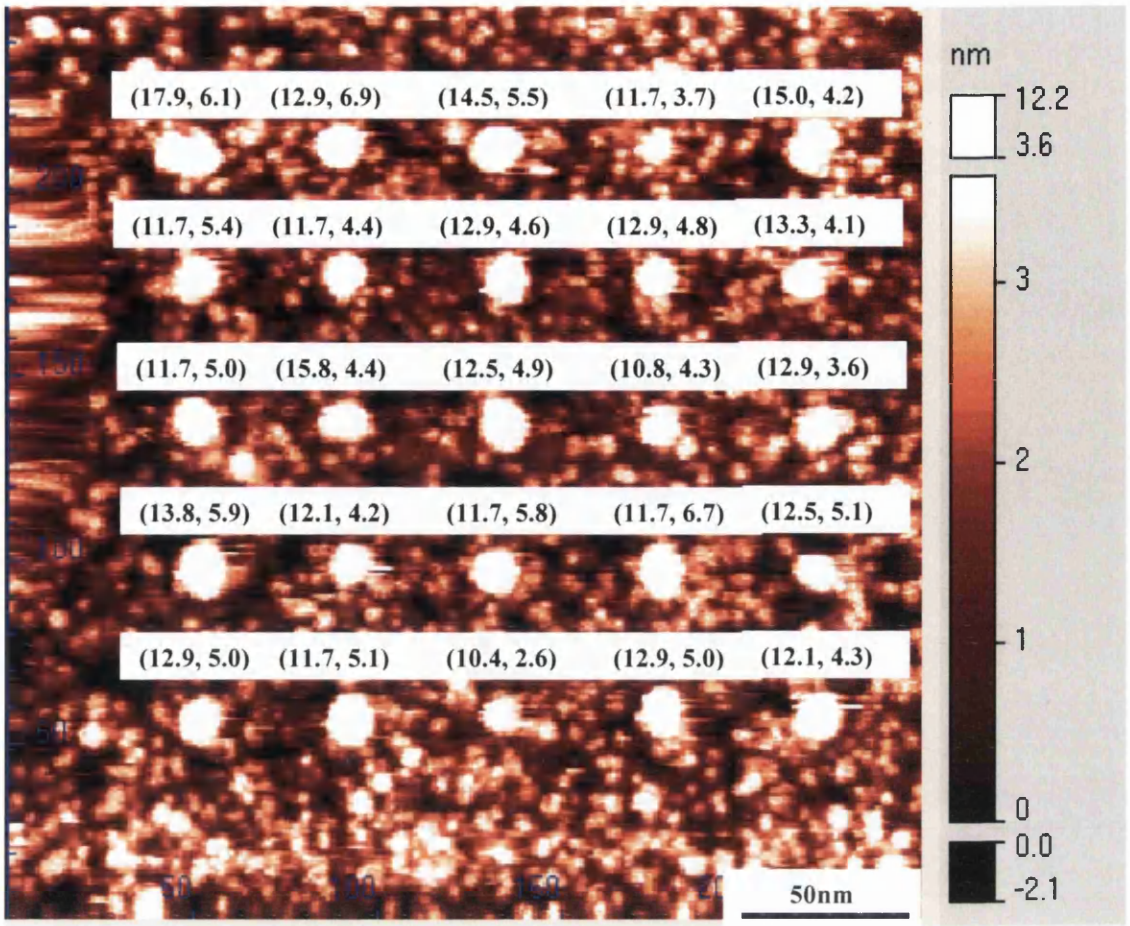


Figure 5-4 **Example on measurement of physical size on the dots presented in accordance to the coordinates, where (x, y) represents (width, height) readings. (Features patterned at room temperature)**

All records of feature size for all patterned dot features in three images were averaged respectively to provide the mean calculation on the length and height (Table 5-1) as a function of temperature.

Mean of Measurement

Temperature	Ave Width (nm)	Ave Height (nm)
Room Temp	12.80	4.86
50°C	17.40	4.84
150°C	25.33	3.45

Table 5-1 **Average of all measurements on the dot features patterned at room temperature, 50°C and 150°C**

With reference to Table 5-1, the width of the written dots during nanopatterning increases with sample temperature. From Figure 5-3, the line profile measurement indicates that 2 peaks are present for most of the dots 150°C (indicated by black arrows), suggesting the possibility that more than one grain was participating in the nanopatterning process, as opposed to a single grain at room temperature. If the measured width of these dots is divided by 2, the average width of the "single" dot at 150°C would be 12.67nm, comparable to the width at room temperature 12.80nm (Table 5-1). This indicates that more grains are taking part in nanopatterning at elevated temperature.

As for the average height presented in Table 5-1, it is interesting to note that it decreases as the sample temperature increases during nanopatterning. The model presented in chapter 2 for the nanopatterning process from Penny *et al* can be used to explain this behaviour. For example, increased current is obtained from patterned grains due to charge storage as shown in Figure 5-5(a) where more higher energy states are available for tunnelling as compared to an uncharged grains. At elevated temperature, the same charge is now shared between two grains and the resultant line profile will be lower in apparent height as the 'depth' of the potential well in the conduction band is not as deep, providing less higher energy states for tunnelling as shown in Figure 5-5(b).

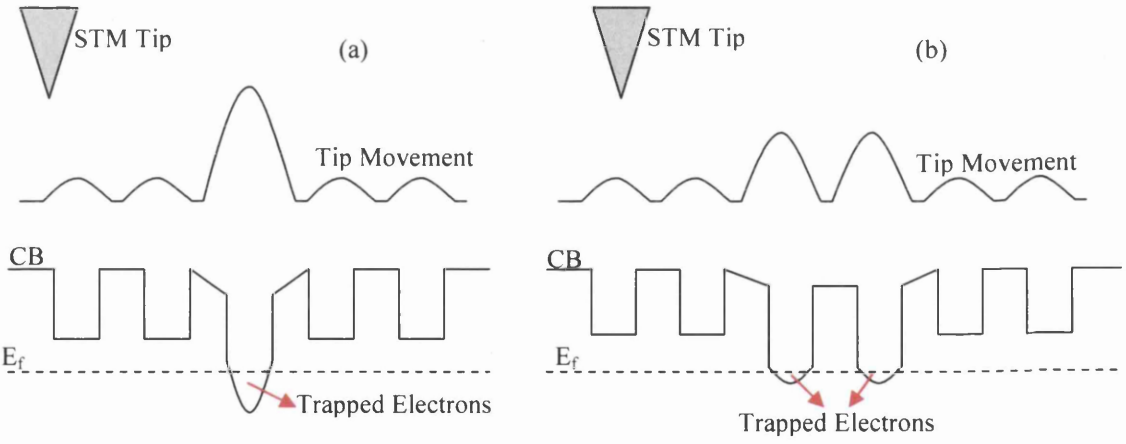


Figure 5-5 **Illustration of the effect of charge spreading on the apparent width and height of the charged features (a) at room temperature and (b) elevated temperature**

5.2.4 STS Studies for dots written at room temperature, 50°C and 150°C

To look further into the understanding of the localised electronic properties of the written dots, Scanning Tunnelling Spectroscopy (STS) Studies were performed on dot features patterned at room temperature, 50°C and 150°C (Figure 5-6). The STS image of dot features patterned at room temperature was provided by Dr. Mark W. Penny.

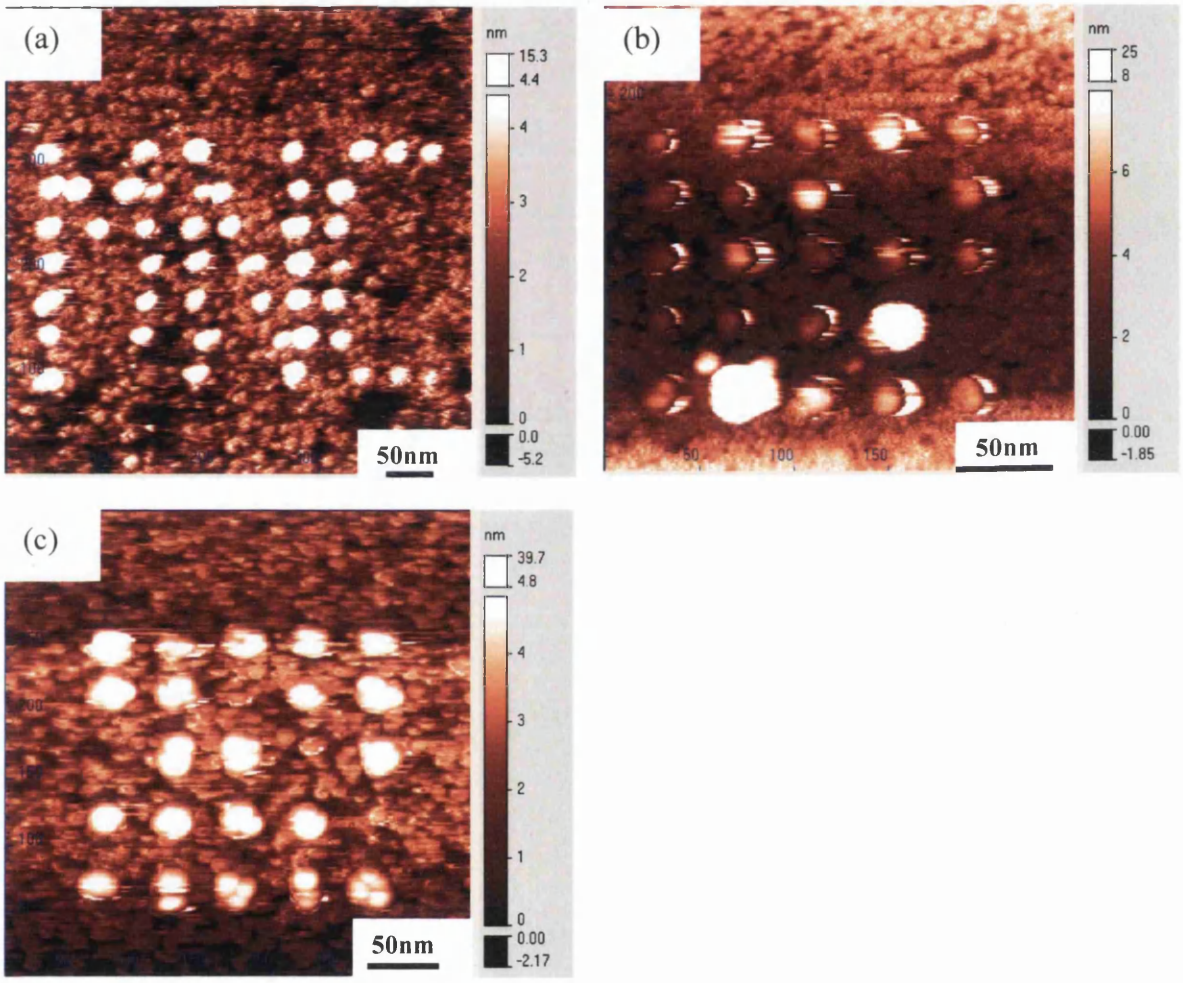


Figure 5-6 **Performing STS from -4V to +4V on (a) 'MNC' pattern written on surface of 450nm by 450nm**

(b) 5x5 matrix patterned on surface of 250nm by 250nm

(c) 5x5 matrix patterned with on surface of 350nm by 350nm with -6V_{tip} for 100μs

The data was extracted by using the "area" option on the "spectroscopy" function available on the Omicron software. When an area is selected, the system will calculate the mean I-V of the area and plot the current as a function of voltage. For a STS image, 10 areas of background and 10 areas of the patterned region (illustration of measurement on STS image for nanopatterning performed at room temperature shown as Figure 5-7) were selected and all current-voltage graphs were recorded (shown at the centre section of Figure 5-7). Similar processing to that conducted in the previous section was carried out.

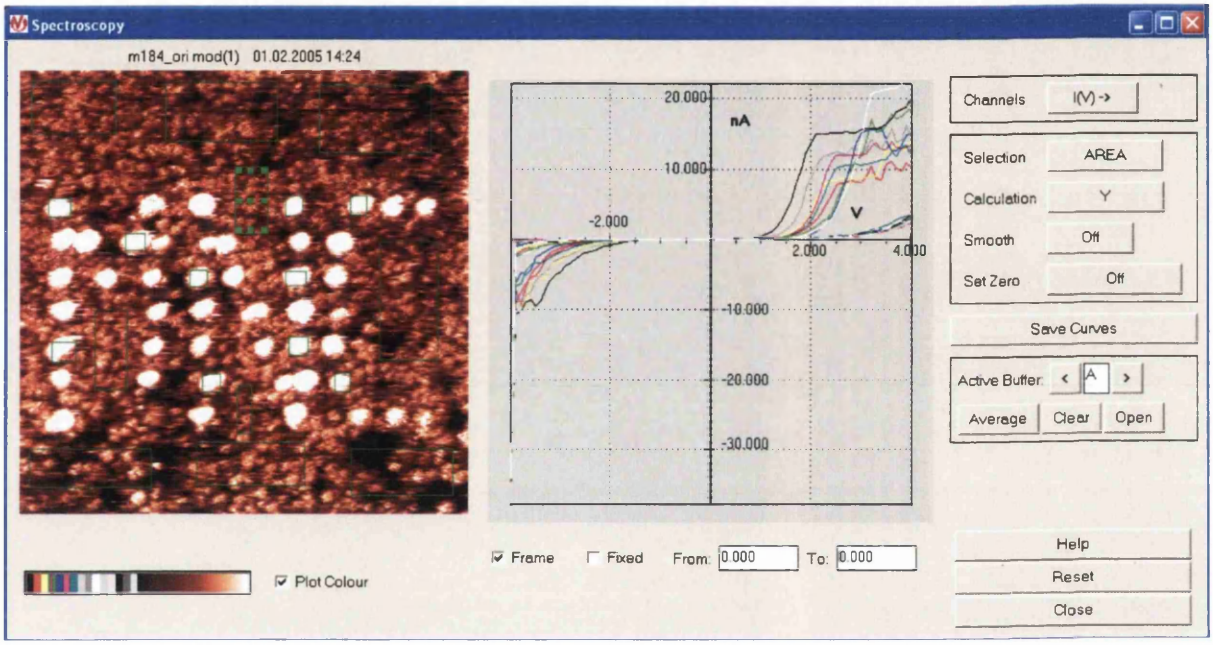


Figure 5-7 **Example of method in extracting STS data from the "MNC" pattern written at room temperature on surface of 450nm by 450nm. Middle section shows the record of the average current-voltage data of the area selected, where the right section shows the setting and selection of "spectroscopy" option.**

To obtain a more representative current-voltage relationship between a patterned region and the background, all data extracted using Omicron software were exported to Excel spreadsheet, where the data for background and patterned region were separated and averaged. The resultant calculation of the current-voltage relationship between the patterned and background region for nanopatterning applied at room temperature, 50°C and 150°C are then plotted in Figure 5-8 respectively.

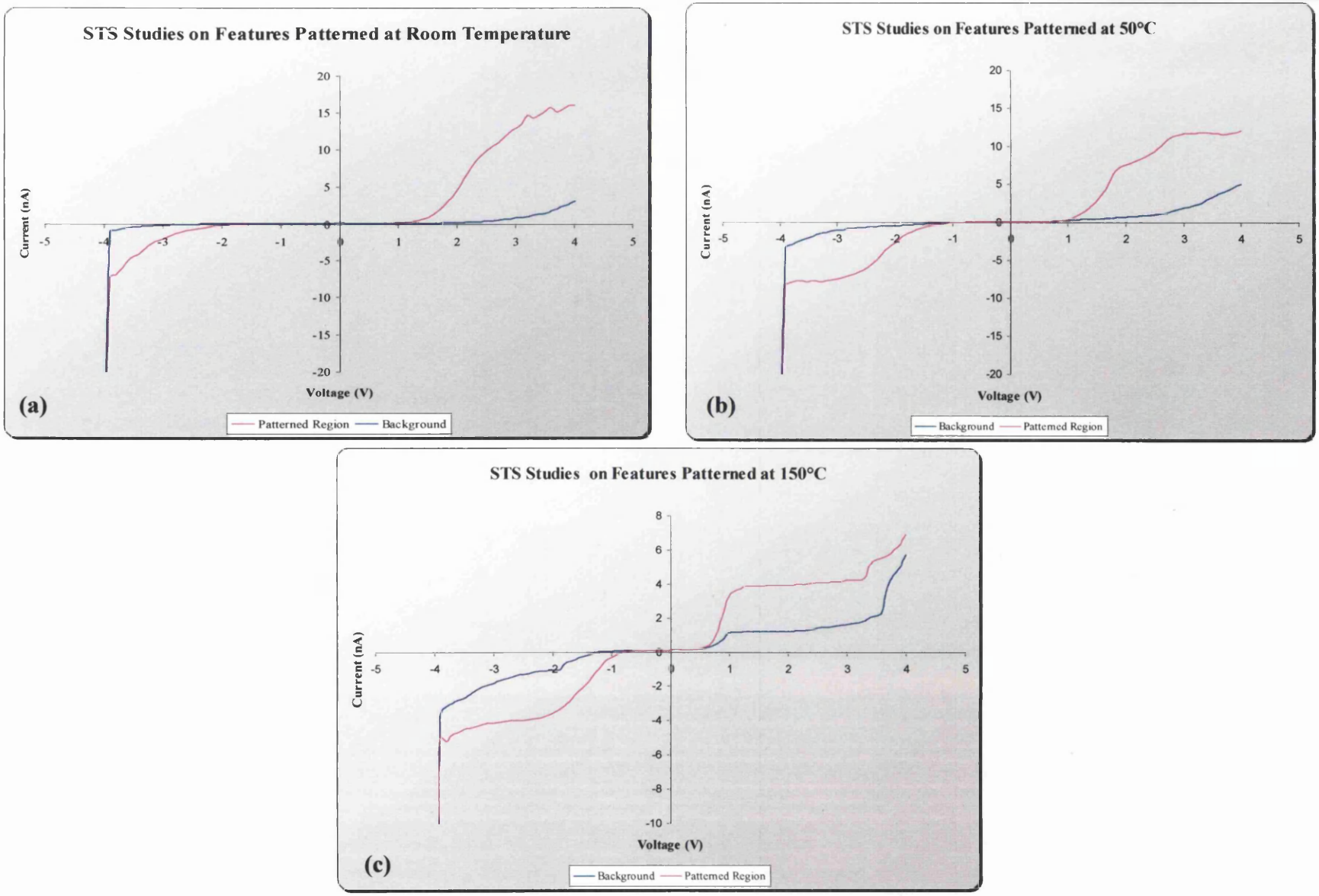


Figure 5-8 **STS Studies by means of 10 readings on background and 10 on written features on (a) 'MNC' pattern written at Room Temperature. (b) 5x5 matrix patterned at 50°C. (c) 5x5 matrix patterned at 150°C.**

With reference to Figure 5-8, there is a similarity between all graphs, where the patterned regions all show a higher amount of current flow as compared to their respective background, regardless of the sample temperature during nanopatterning. This result is consistent with all the experiments performed in the lab previously[2], which support the theory that the nanopatterning process is electronic in origin.

Even though all data are consistent in showing that patterned features have higher conductivity, the current flow on each patterned region reduces as the formation temperature increases. Figure 5-9 shows current-voltage curves for the patterned region as a function of temperature, where increment in integrated current can be observed for every 50°C rise in sample temperature during nanopatterning.

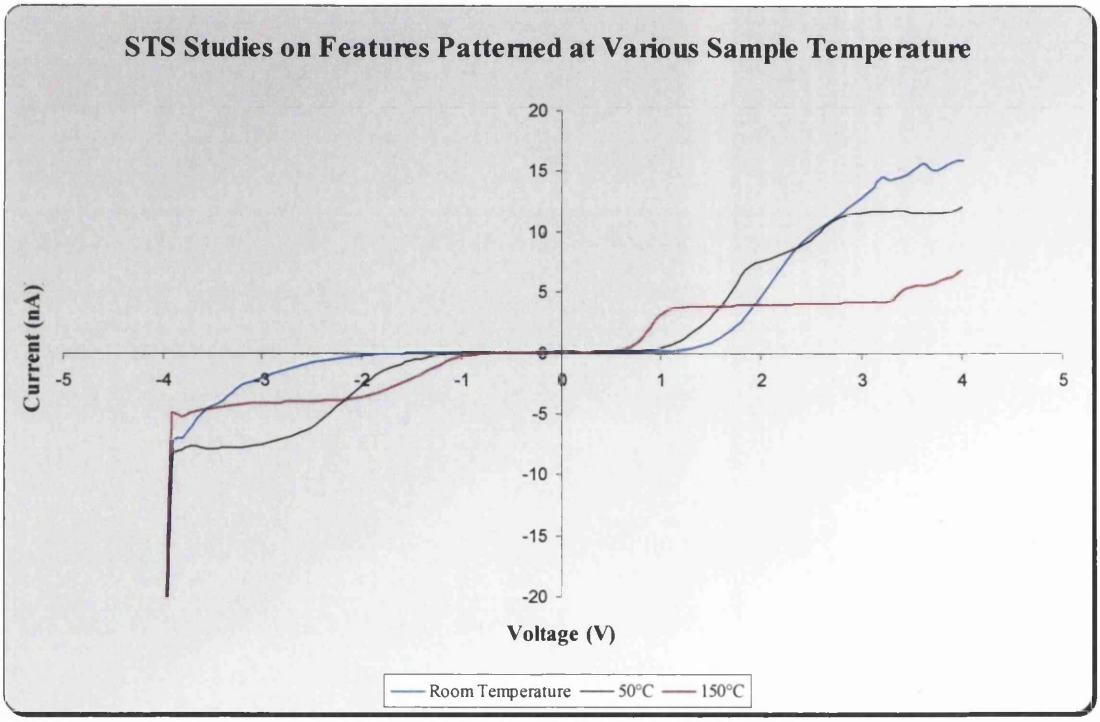


Figure 5-9 **I-V curves taken from the patterned feature at room temperature, 50°C and 150°C respectively.**

It is a known fact that the nature of the STM can vary with sample temperature due to tip sample interactions. As such, to verify the credibility of the analysis, the current-voltage relationship of the non-patterned background during STS was investigated as a function of sample temperature and plotted in Figure 5-10 using the same data extraction approach previously described. Interestingly, the

current flowing through the background for each sample temperature, showed a negligible variations (Figure 5-10). This provides confidence in the reproducibility of the experiments as a function of temperature.

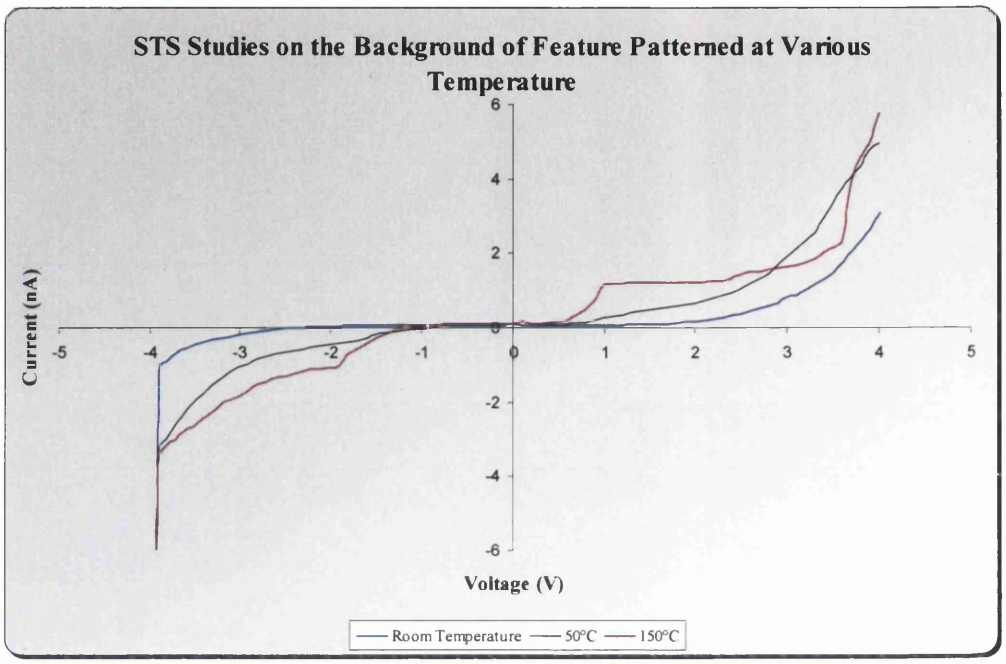


Figure 5-10 **I-V curves taken from the non-patterned area of images at room temperature, 50°C and 150°C**

With that in mind, the comparison between the patterned areas is more evocative as it suggests that the amount of current recorded in the experiment is decreasing as the sample temperature increases during nanopatterning. This supports the claim that lesser electrons are trapped during nanopatterning at a higher sample temperature since they have more thermal energy to tunnel into adjacent grains.

5.2.5 Study of Nanopatterning at 150°C in more detail

The previous work suggest that the nanopatterning process is dependent on the potential difference between the sample and the tip (refer to chapter 2), where the quantum states of the material are being accessed as the tip voltage changes. The electronic information presented in section 5.2.4 suggests that for a fixed tip voltage, the charge storage seems to be smaller as the sample temperature increases during the nanopatterning. In addition, the images reveal that the success rate of nanopatterning decreases as the sample temperature during the writing process increases.

To verify the dependence of the writing on the sample temperature and voltage, a matrix of 5x5 design was used to pattern an area (procedure as in section 5.1.1), with the tip-voltage decreasing for consecutive rows from -3V to -7V. The sample was maintained at 150°C throughout.

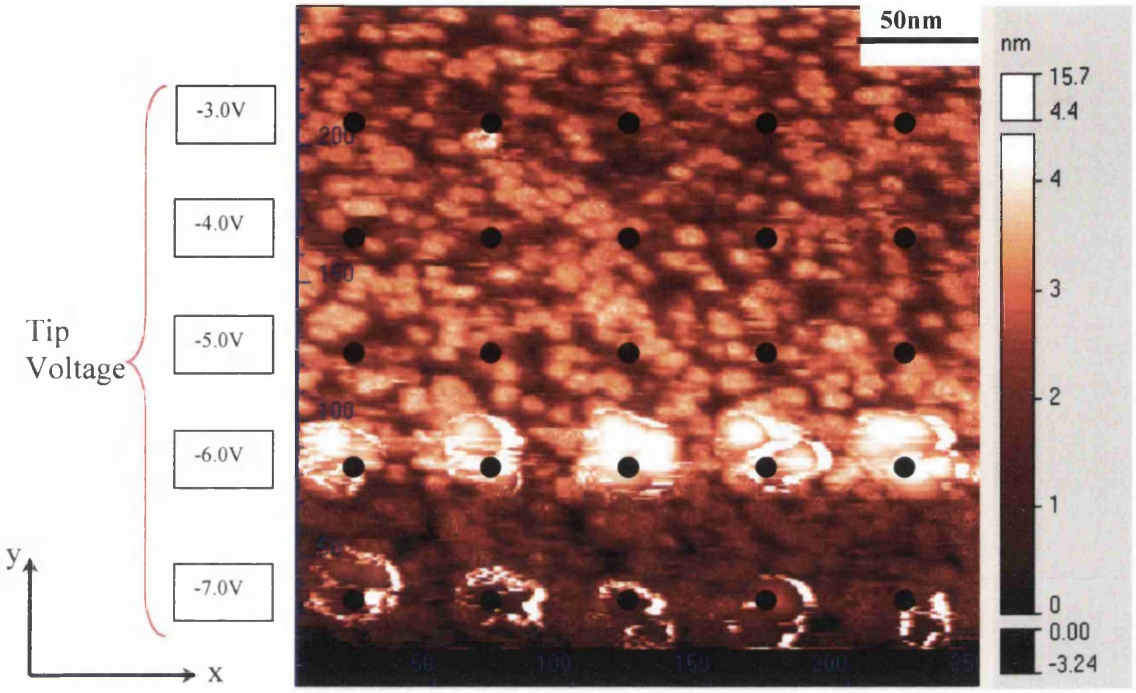


Figure 5-11 **5x5 matrix patterned with x-axis of the same patterning condition and y-axis with variable patterning tip voltage at interval of 1.0V from $-3V_{tip}$ to $-7V_{tip}$ for 100µs**

The first observation on the scanned image was that there was no significant feature visible when writing at -3.0V to -5.0V. As for rows at -6.0V and -7.0V, the dots written show that more than one grain had participated, consistent to the results obtained in section 5.2.1 and 5.2.2.

As the only patterned structures were visible for rows corresponding to -6.0V and -7.0V, to investigate the change in conductivity of the patterned dots as a function of voltage, STS was carried out as in the previous section. The average current-voltage relationship for each tip voltage taken from the pattered regions is shown in Figure 5-12.

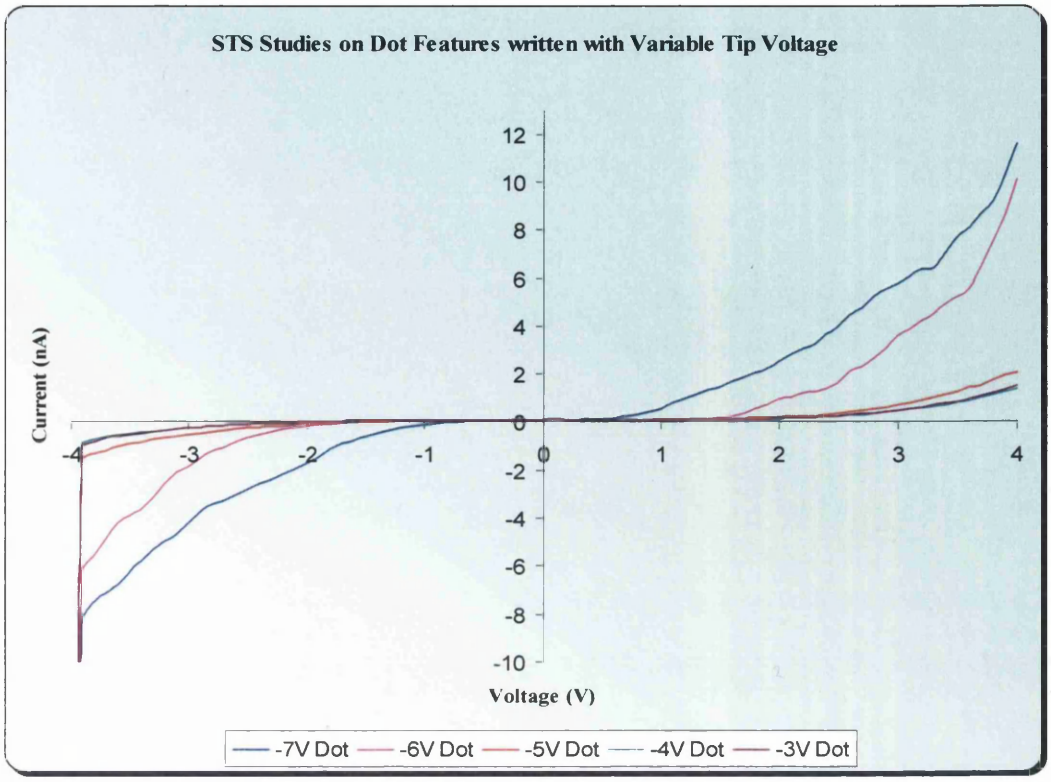


Figure 5-12 Average current of 25 sites, plotted in accordance to the writing tip voltage

The graph shows that at -3.0V and -4.0V, there was no clear distinction in conductivity from that of the background. A noticeable change in current flow begins for dots written with -5.0V tip voltage, showing around a 2nA increase. Dots patterned at -6.0V and -7.0V tip had a more drastic change in conductivity. -7.0V patterned dots showed the highest current flow across the region with ≈10nA, 9nA for those formed at -6V.

Examining the result from previous research[2], where it was proposed that tin dioxide nano-grain became susceptible to nanopatterning when the tip voltage was lower than -5.1V. The success rate was nearly 100% when the tip voltage used is -6.0V, which formed the basis of the nanopatterning research in Swansea University. Interestingly, Figure 5-12 not only supports this theory, it also shows an increment in current flow as the tip voltage changes from -5.0V onwards.

The results presented here show that when performing nanopatterning at 150°C with the typical parameters of $-6V_{tip}$ for 100μs, the number of electrons injected into the tin dioxide grain is lower than when performed at room temperature, and the grain has not yet reached its saturation point. This is shown by the continued increase in current at 150°C when the tip voltage goes from -6V to -7V.

5.2.6 Nanopatterning Hypothesis

The results provide new information regarding the research in nanopatterning on tin dioxide nanoparticle from both a physical and an electronic perspective, which will be shown to be consistent to the model of Penny *et al*[3]. When the temperature of the sample is raised, the thermal excitations increase the number of electrons in the conduction band, meaning that there would be more electrons to participate in any electronic activity, as compared to room temperature. Hence, the energy carried by each electron will be higher and result in the population of higher energy levels. Furthermore, when STM tip scanned over this sample surface, the apex of the tip would experience an increase in temperature, and causes thermal excitation effect on the tip. As such, when nanopatterning is performed, STM tip would inject electrons with higher energy into the grain, and these electrons would also experience a higher excitation state, where the energy might be high enough to tunnel through the potential barrier at the particle boundaries (Figure 5-13) and end up in the neighbouring grain.

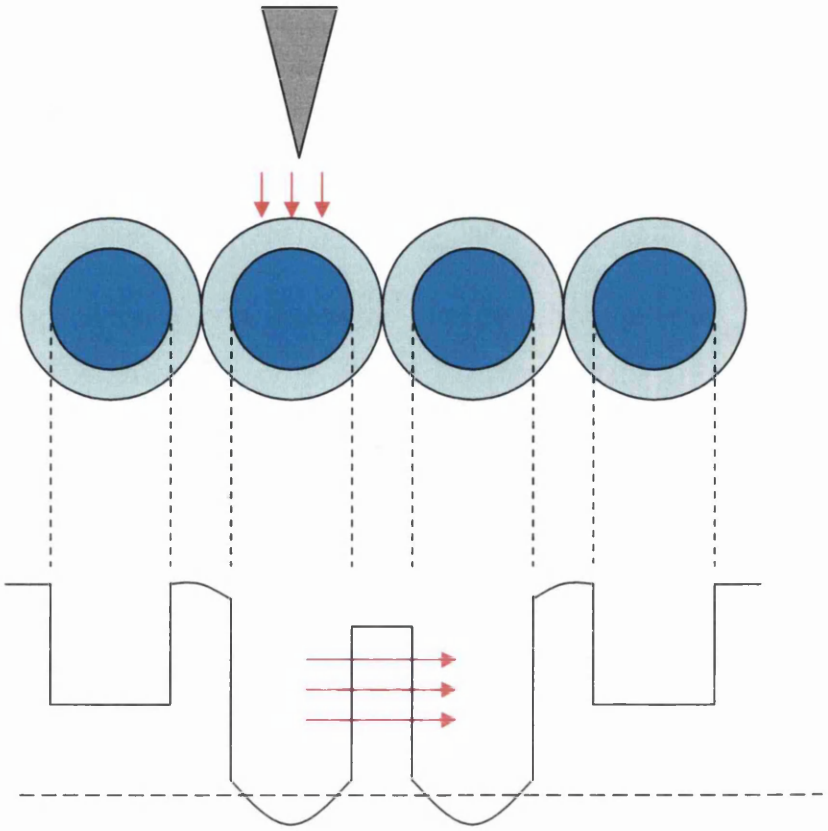


Figure 5-13 **Possibility of electron overcoming the potential barrier between grains through gaining thermal energy.**

In another aspect, as the resistance of the sample decreases at higher sample temperature, the STM tip would experience a higher electron tunnelling current when performing scanning at the same tip-sample separation and voltage, as compared to room temperature. As explained in chapter 3, in order to maintain the pre-set current, the feedback loop of STM system would move the tip away from the surface. Therefore, when the STM tip is scanning the sample surface at 150°C, the STM tip-sample separation would be higher compared to room temperature. Referring to the nanopatterning procedure in chapter 4, the tip-sample separation during normal STM scanning will be maintained when executing the nanowriting process, hence there is also a possibility that at a higher sample temperature, the concentration of electron tunnelling path could be spread over a wider angle (Figure 5-14), resulting in electron entrapment in more than one grain.

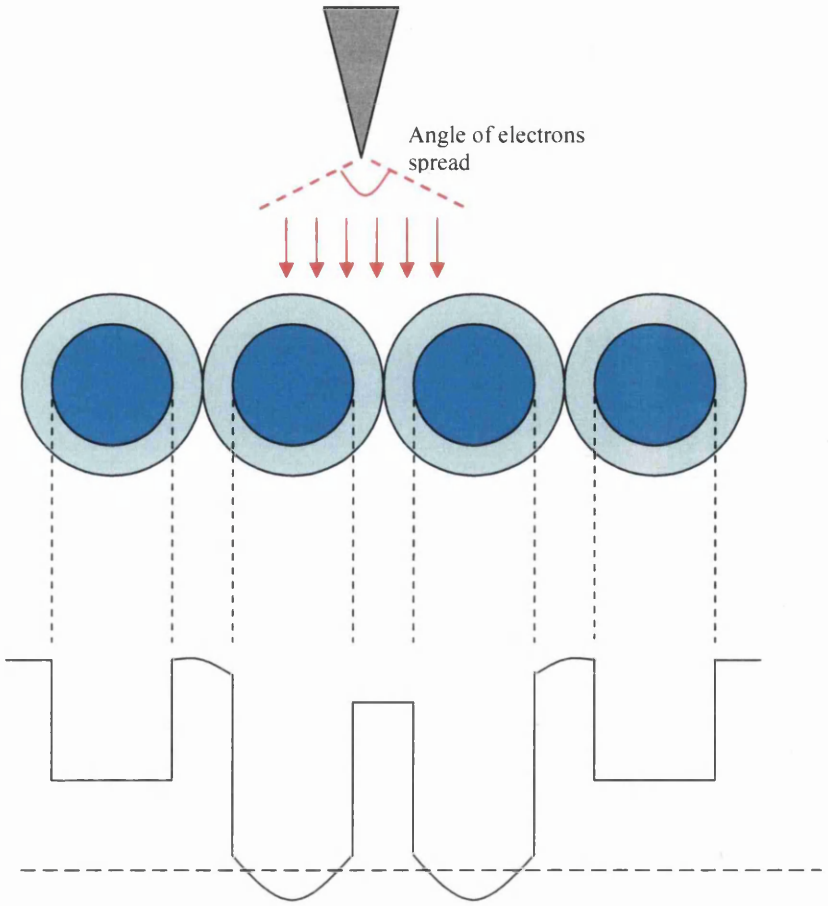


Figure 5-14 **Possibility of spreading the effect of nanopatterning to more than one grain due to the increase in surface conductivity triggered by higher sample temperature**

For either situation introduced above, the number of electron trapped in the grain would be lower as compared to nanopatterning at room temperature, as the size of the written feature would be larger.

5.2.7 Discussion on Nanopatterning Performed at Higher Temperature

With the hypothesis developed in section 5.2.6, both the physical and electronic behaviour of tin dioxide surface when performing nanopatterning at higher sample temperature can be explained.

Physical measurements (section 5.2.3) show that the dots patterned at a higher temperature involve more grains, in the case of 150°C, twice as many than the dots written than at room temperature. At higher sample temperature, the increase in electron density due to thermal excitation would raise the overall conductivity of the material. As explained in section 5.2.6, this provides a suitable condition for electrons to gain sufficient energy to tunnel through the

thin barrier between grains; or a larger tip-sample separation during STM scanning has diluted the focus of the path of electrons from tip to sample that causes an extended number of grains participating in nanopatterning. This result in a wider length measurement on the dot features patterned at higher temperature. The lower apparent height registered during STM scanning of features patterned at higher temperature is also consistent with the above model where the same electron concentration is shared between several grains at high temperature compared to a single grain at room temperature.

Previous work[2] has shown that the region where nanopatterning took place produces a higher current flow when compared to the background of the sample. STS studies in Section 5.2.4 acknowledge the consistency of such responses, but also reveal that the dots patterned at higher temperature have lower current flow as compared to ones at room temperature. Once again this can be explained by the proposed model. A grain with a lower stored electron concentration, due to sharing with neighbouring grains, will have a shallower conduction band profile as shown in Figure 5-5 previously. Less higher energy states, measured relative to the bottom of the conduction band minimum in the grain, will be available for tunnelling for the lower concentration scenario and hence the current will be lower.

Further support is attained with the STS study conducted in section 5.2.5, where 5 rows of dots were patterned with 5 different tip voltages. The result affirms that the tin dioxide grains will only respond to the nanopatterning procedure with a tip voltage of at least -5V, regardless of the sample temperature. This is comparable to the voltage threshold reported previously by Penny[2]. The same work also shows that for tip voltages higher than -6V, there was very little effect on the grain, suggesting that the maximum storage capacity had been reached. However, the STS study presented in this thesis shows that due to the sharing of the electron concentration between adjacent grains, higher voltages can be used to write.

5.3 Effect of Tip Voltage during STM Scanning

From the previous research on nanopatterning research conducted in Swansea University, the tip voltage is one of the main factors that affect the result of nanopatterning. As such, it would be valuable to understand the relationship between potential difference and the effect on the apparent height induced during scanning, below the critical threshold of writing reported by Penny[2].

5.3.1 Experimental Preparation Procedure

The experiments presented in section 5.3 were conducted at sample temperature of 150°C; hence the sample was first heated and sustained to the desired temperature with procedure shown in section 5.1.2, which STM tip would be brought close to the surface (procedure shown in chapter 4) and scanned at -2.5V_{tip} on the material surface so as to select the suitable site for the experiments. When an appropriate site was found, the following procedure (Figure 5-15) was performed to achieve the pattern to be used for the study. The settings in red indicated in Figure 5-15 (a) are as follows:

Preset Tip Voltage	=	-5.0V_{tip}
Required Direction	=	Indicated by yellow arrows
New Preset Tip Voltage	=	Existing Tip Voltage – 1.0V

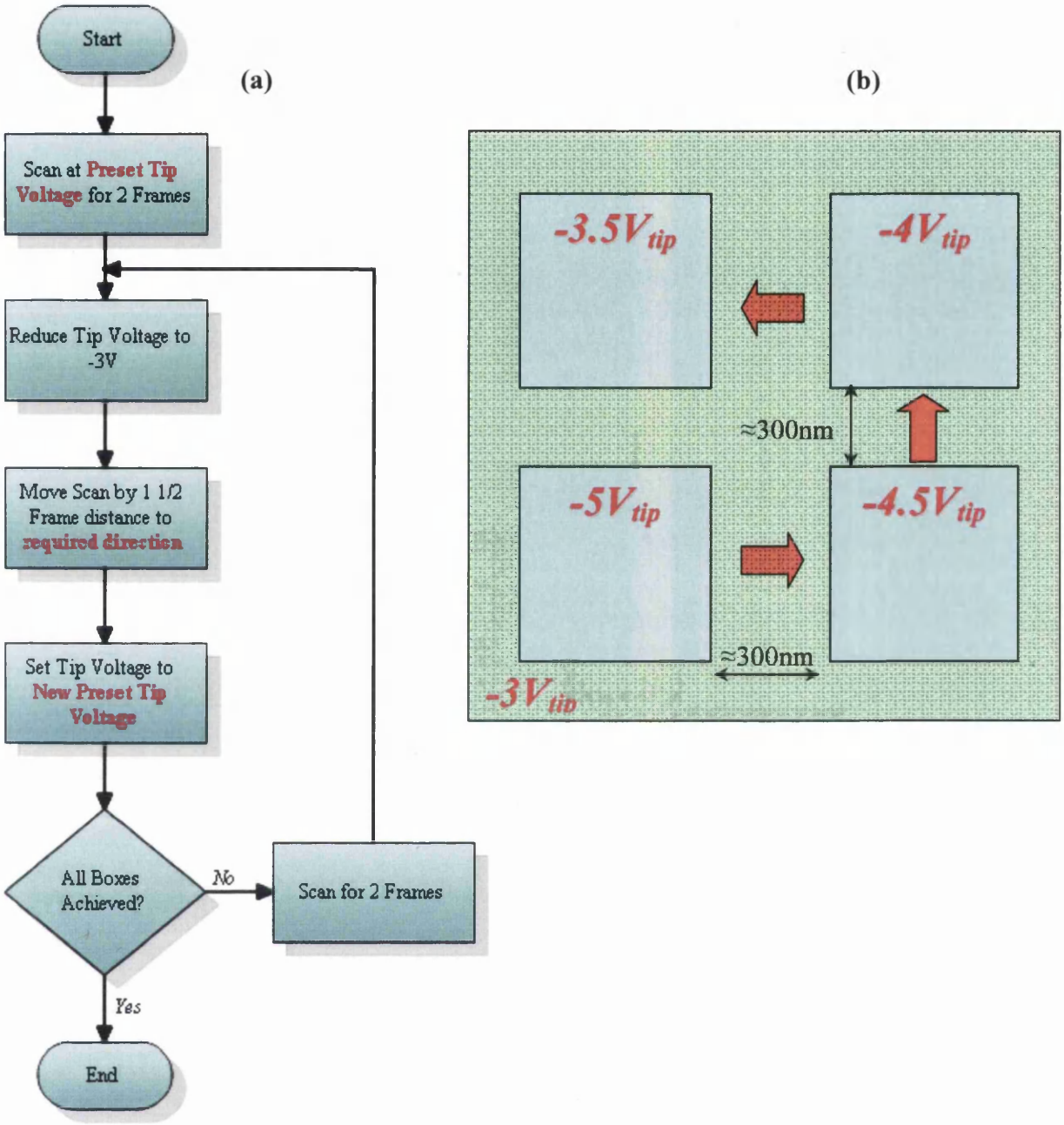


Figure 5-15 **(a) Flow of Sequence in achieving the square features constructed by $-5V_{tip}$, $-4.5V_{tip}$, $-4V_{tip}$ and $-3.5V_{tip}$**

(b) Schematic Diagram to illustrate the path of sequence in building the square features

Tip voltage was first set to -5V and 2 frames performed on an area 200nm by 200nm surface. Upon the completion of the cycle, the tip voltage was reduced to -3V immediately, the scanning region was then moved to the right by 1½ frame (equivalent to ≈300nm). Once all 4 square features were acquired, the scanning range was increased to 800nm by 800nm, so as to obtain the apparent height of

all the square features on the same image, at a tip voltage of -3V. In addition, as the current, scan size and scan speed were kept constant throughout the experiment, the variation factor had been limited to the change in potential difference between the tip and the sample.

5.3.2 Effect of Negative Tip Voltage

Upon the completion of the above procedure, the function of "Y-Average" available on WSxM software[4] was used to extract the average line profile of the square features. The average height of each square scanned at different voltages was extracted from the line profiles, measured relative to the background and plotted in Figure 5-16.

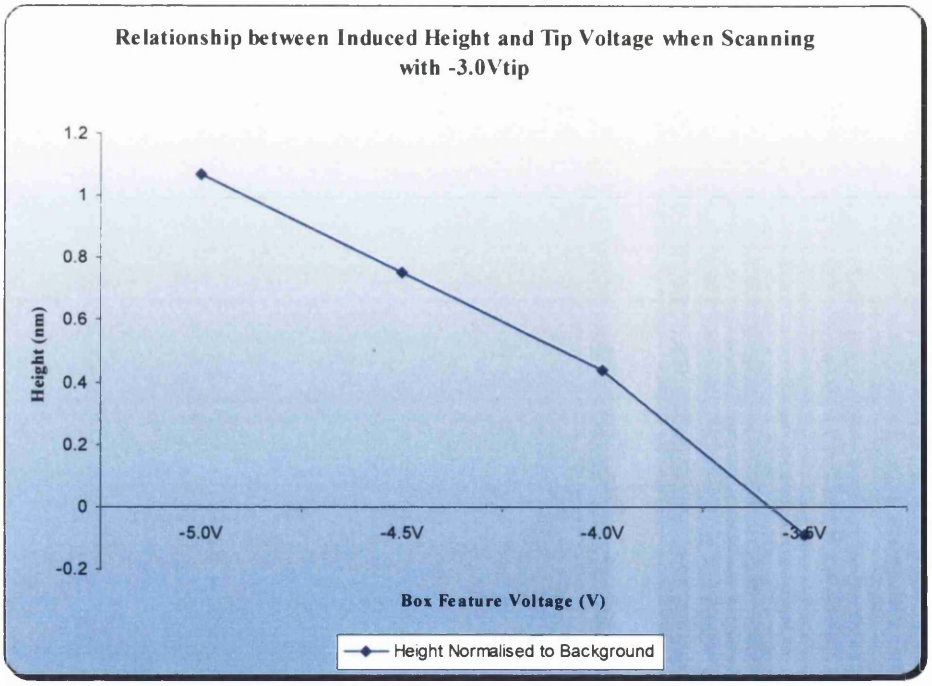


Figure 5-16 **Corrected Apparent height of square features built by -5V_{tip}, -4.5V_{tip}, -4V_{tip} and -3.5V_{tip} with respect to the background scanned at -3V_{tip}**

The first observation is the trend of height induced with respect to the potential difference between the tip and sample, where it reduces in magnitude as the negative tip voltage decreases. The constant pre-set current and scanning speed between all the features signifies that the effect of height change is related to the potential difference across the tip and material surface. This agrees with the behaviour of nanopatterning under the STS studies presented in section 5.2.

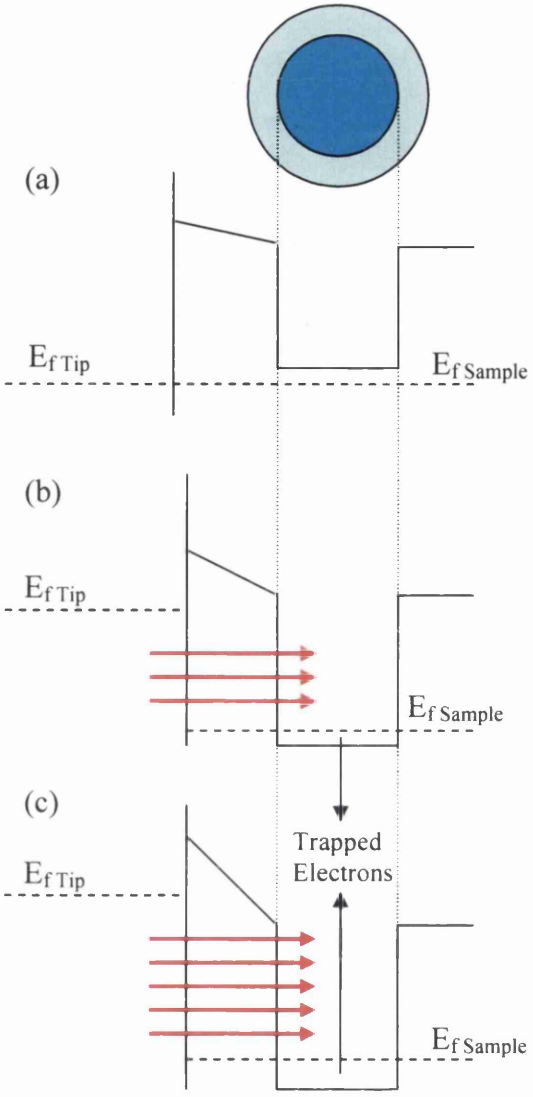


Figure 5-17 **Illustration of effect on Conduction band when Tip Voltage is (a) 0V (b) low negative voltage (c) high negative voltage**

Figure 5-17 demonstrates the effect of changing the tip voltage on the tunnelling process. Figure 5-17 (a) shows the band diagram when no voltage is applied on STM tip. When a low negative tip voltage is applied (b), the wavefunctions between the tungsten tip and the sample overlap, to provide a path for electrons to tunnel from the tip to the sample. If the tip voltage increases (c), the potential difference between tip and sample is higher, hence providing more accessible states for the electron to tunnel into.

The nanopatterning model proposed in chapter 2 shows that electron entrapment occurs when the rate of electron injection exceeds the rate at which electrons tunnel between grains. This results in storage below the Fermi level. If this critical voltage or current is not exceeded then the injected charge can tunnel through to adjacent grains, producing a charged area when scanned with the tip, similar to SEM sample charging. This process is demonstrated in Figure 5-18.

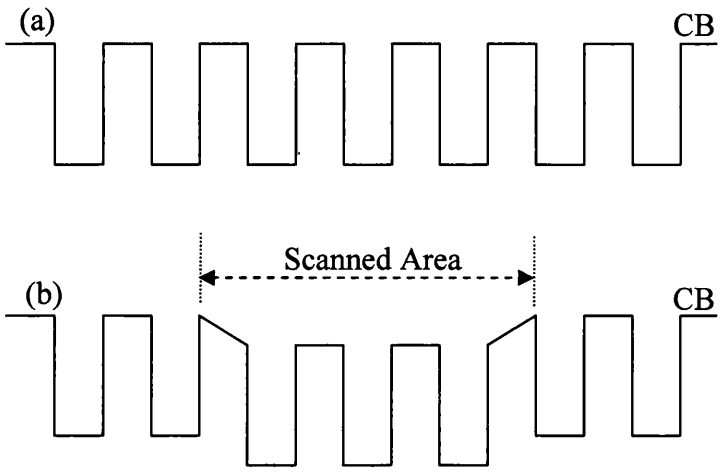


Figure 5-18 (a) Conduction band of tin dioxide grain and (b) conduction band after scanning with negative tip voltage

5.3.3 Difference between patterned dots and voltage scanning

Section 5.3.2 explained the effect of tip voltage on the surface of tin dioxide nanoparticles, at the same time, it pointed out that STM scanning voltage selection is equally crucial in the nanopatterning process.

A similar procedure to that mentioned in section 5.3.1 was carried out, where the 2 dot features were written while the 1st frame of each square box was being scanned. The dot features were achieved by performing "single event" (explained in chapter 4) at $-6.0V_{tip}$ for 100 μs randomly on the surface of the square. The 800nm by 800nm image in Figure 5-19 comprises all 4 square features with the 2 patterned dots.

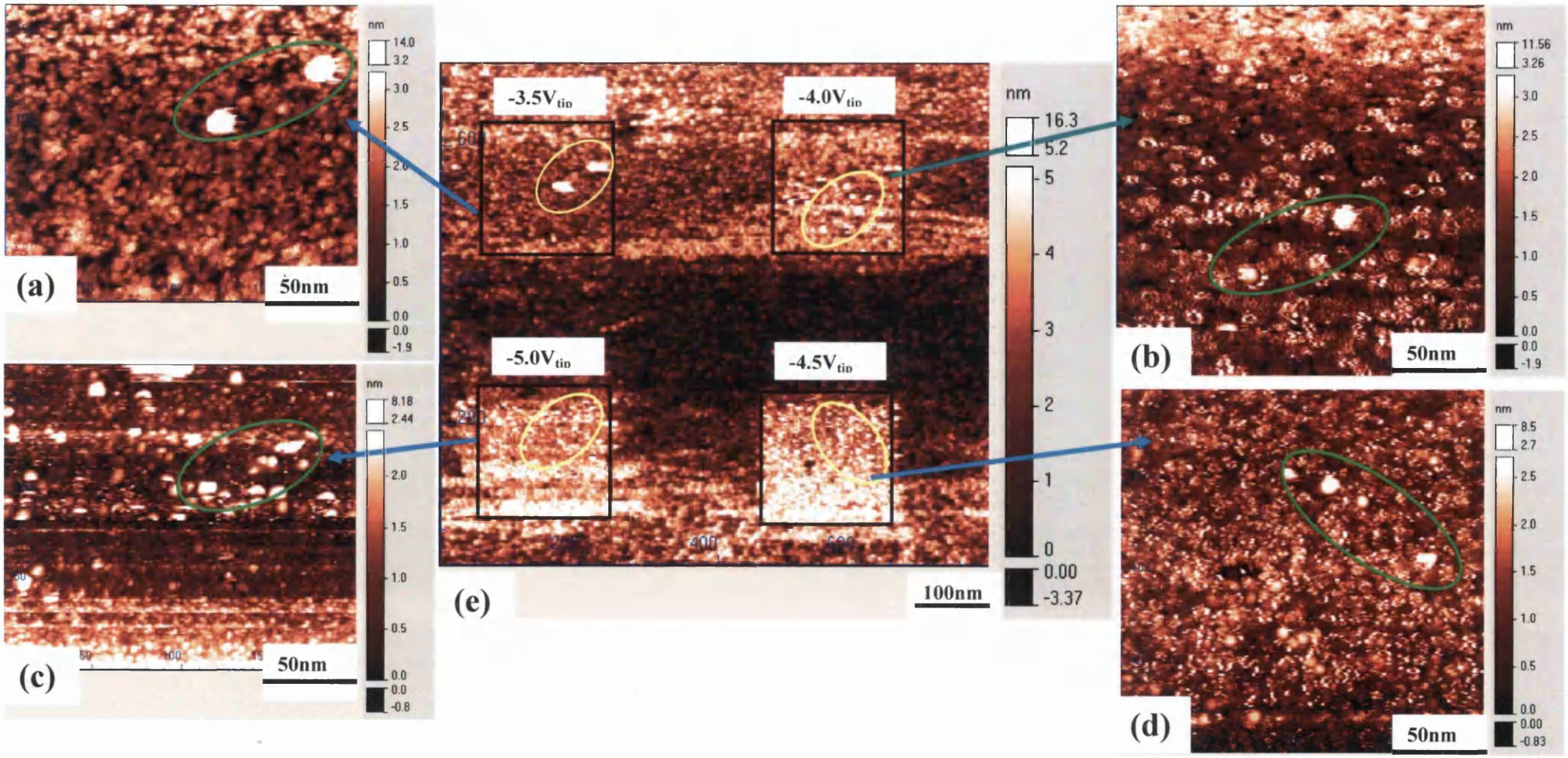


Figure 5-19 2 dot features patterned at $-6V_{tip}$ for 100µs on square feature of 200nm by 200nm scanned with (a) $-3.5V_{tip}$ (b) $-4.0V_{tip}$ (c) $-5.0V_{tip}$ (d) $-4.5V_{tip}$ (e) STM image of 800nm by 800nm with all square features (mark with black box) and the location of the dot features (mark with green circle)

A similar approach to that adopted in section 5.3.2 was used to extract the apparent height data from Figure 5-19 (e). However, as there were 2 dots patterns present on each square feature, the area coverage for the average height measurement in WSxM software is smaller as compared to ones conducted in section 5.3.2. The apparent height of the square feature with 2 dots is plotted on the same axis as the data for the apparent height of the square features in section 5.3.2 for comparison, shown as Figure 5-20.

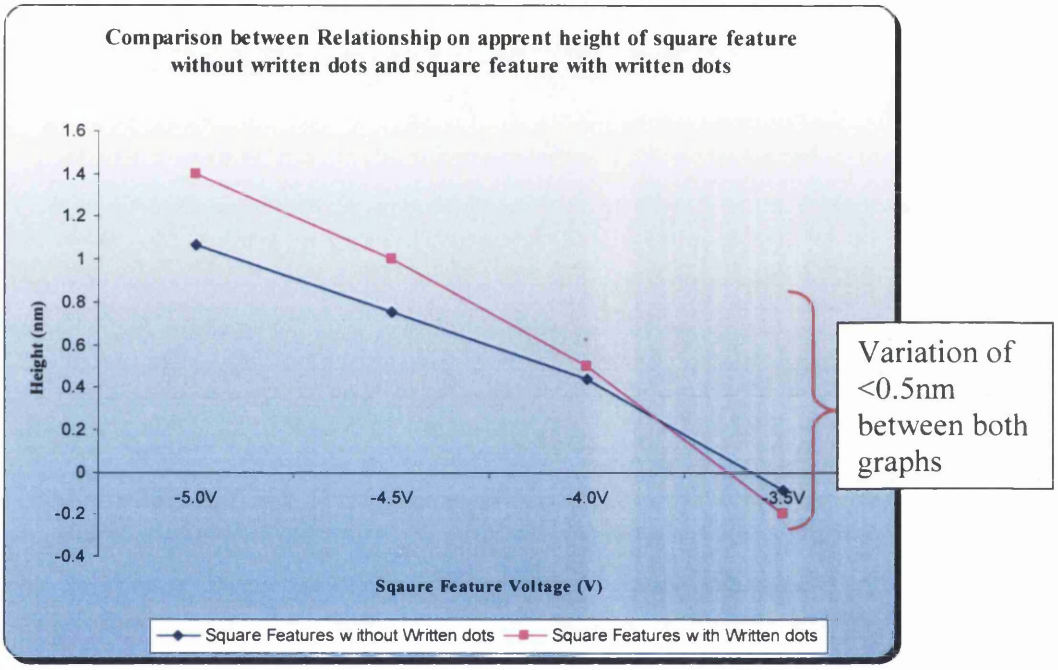


Figure 5-20 **Comparison between apparent height of square features with 2 dots and square features without any form of nanopatterning**

The apparent height of the square features with the 2 dot patterns shows a similar trend, where the apparent height reduces as the tip voltage decreases, and are in agreement within experimental error.

As discussed in section 5.3.2, the higher tip voltage results in more electron entrapment within the grain, hence providing a higher apparent height (or brighter features) on the STM image. As such, when the dot features were patterned on these square features at $-6.0V_{tip}$ for 100μs, the patterned dots is expected to show a different apparent height on the image with respect to the height induced by the tip voltage by imaging. Indeed, when reviewing image Figure 5-19 (e), the dots are more distinctive in the square feature constructed by

-3.5V_{tip} and -4.0V_{tip} (yellow circle). The dot features are not so obvious for square features fabricated by -5.0V_{tip} and -4.5V_{tip}. This is consistent with the fact that scanning appears to produce a general background charging whilst the -6V pulse injects localised charge into the individual grains.

Table 5-2(a) reveals that using a high tip voltage in normal scanning will diminish the full effect of nanopatterning due to unintentional electron entrapment in the background surface. The lower scanning voltage will result in more prominent patterned features.

		-5Vtip	-4.5Vtip	-4Vtip	-3.5Vtip
(a)	**Height (nm)**	3	3.3	3.5	4.5
(b)	**Corrected Height (nm)**	4.4	4.3	4.3	4.3

Table 5-2 **Apparent Height of Dot Pattern (a) with respect to the Square Features produced by -5.0V_{tip}, -4.5V_{tip}, -4.0V_{tip} and -3.5V_{tip} (b) corrected to the apparent height of the square features produced by -5.0V_{tip}, -4.5V_{tip}, -4.0V_{tip} and -3.5V_{tip} with respect to the background scanned at -3.0V_{tip}**

The measurement of the dot features is corrected to the background by adding the apparent height of the respective square features to the background scanned at -3.0V_{tip} (Figure 5-20) to the corresponding apparent height of the dot features measured in Table 5-2(a), recorded as Table 5-2(b). The reading calculated shows a homogeneous 4.3nm height on the dot features when corrected to the background scanned at -3.0V_{tip}, which is comparable to the average height of dot features reported in section 5.2.3 (Figure 5-4). The higher reading in Table 5-2(b) is due to the lower scanning voltage of -3.0V_{tip} as compared to -3.5V_{tip} used in section 5.2.3. The amount of electrons trapped within the grain during nanopatterning appears to be very consistent, but the apparent height registered by STM scanning can be affected by the tip voltage selected, which can facilitate an additional background charge contribution.

5.4 Effect of Accumulative Scanning

5.4.1 Experimental Preparation

The previous section shows the effect of background charging as a consequence of STM scanning at different voltages. This section deals with the effect of cumulative scanning at different voltages.

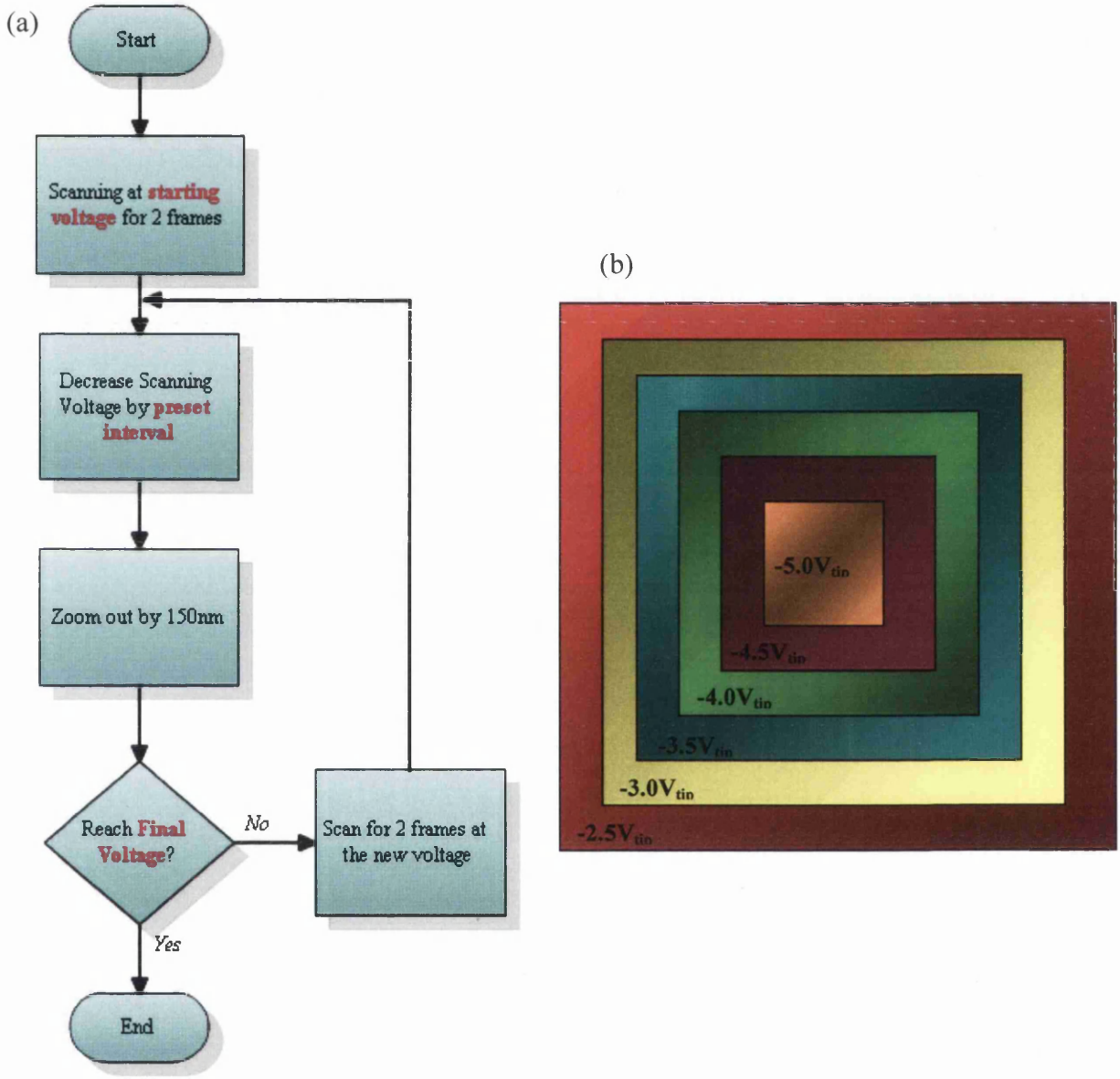


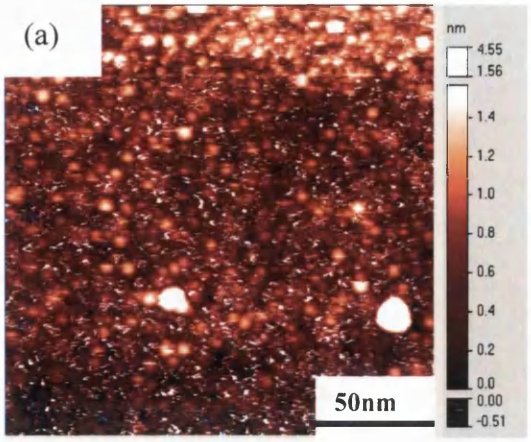
Figure 5-21 **(a) Flow of sequence in achieving the "stacked" square features**

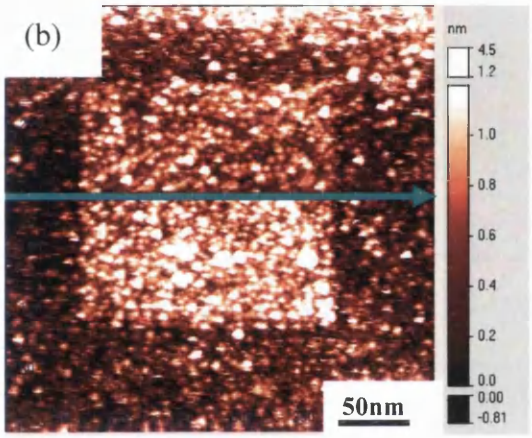
(b) Schematic representing the end product of "stacked" square features created by -5.0V_{tip} (200nm by 200nm), -4.5V_{tip} (350nm x 350nm), -4.0V_{tip} (500nm x 500nm), -3.5V_{tip} (650nm x 650nm), -3.0V_{tip} (800nm x 800nm) and -2.5V_{tip} (1000nm x 1000nm)

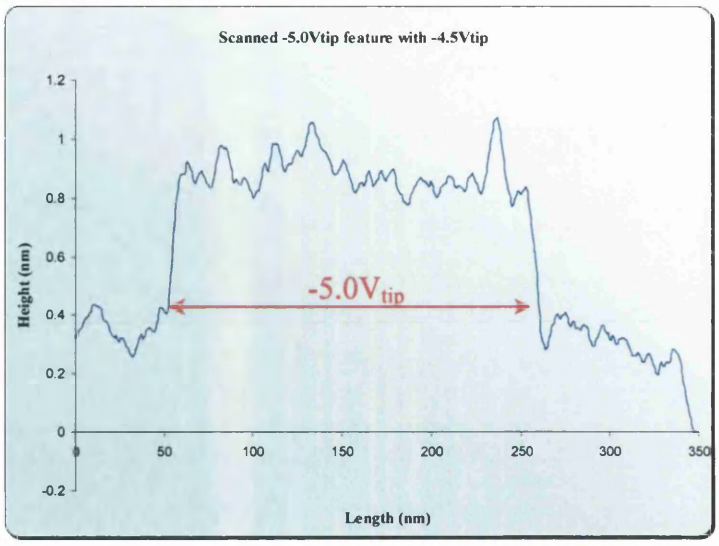
The settings in red indicated in Figure 5-21(a) are as follows:

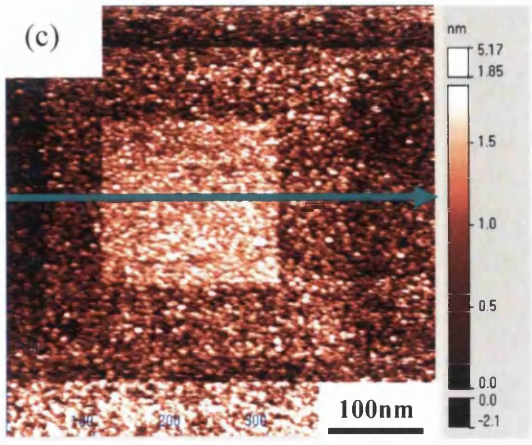
Starting Voltage	= -5.0V_{tip}
Preset Interval	= 0.5V
Final Voltage	= -2.5V_{tip}

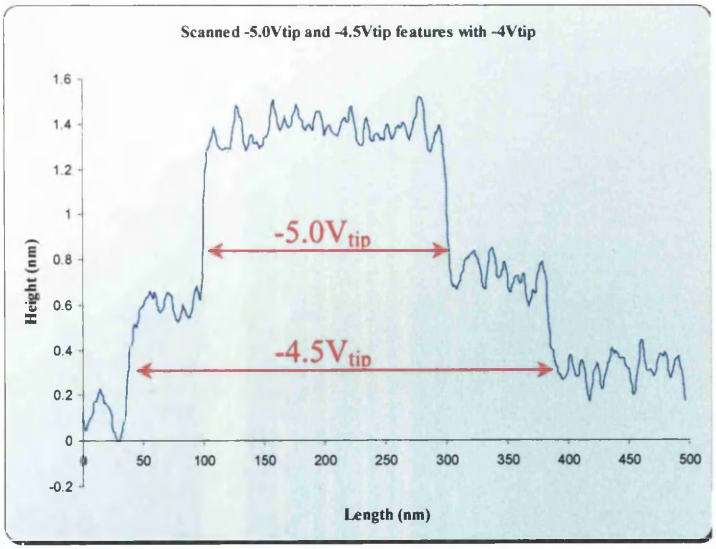
With tip voltage of -5.0V, 2 frames were scanned on 200nm by 200nm area (Figure 5-22(a)). The tip voltage is then reduced to -4.5V before increasing the scan area to 350nm by 350nm (Figure 5-22(b)). Again the STM tip is scanned for 2 frames with the new tip voltage before decreasing the tip voltage by 0.5V and the increasing the scan area by 150nm by 150nm. The cycle was repeated for -4.0V_{tip}, -3.5V_{tip} and -3.0V_{tip}, where the final scan with -2.5V_{tip} was done at 1000nm by 1000nm (Figure 5-22(f)). Throughout the experiment, the current set-point and the ratio of scan size to scan speed was kept constant so as to ensure that the surface involved in the experiment will be exposed to same amount of charge, even with different scan size, making the tip voltage the only variable to affect the outcome of the analysis.

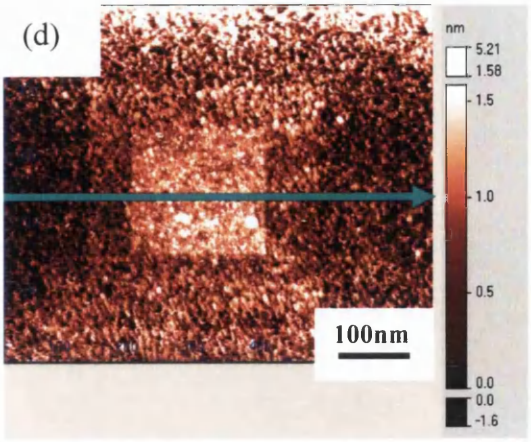

(a)
nm
4.55
1.56
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
0.00
-0.51
50nm

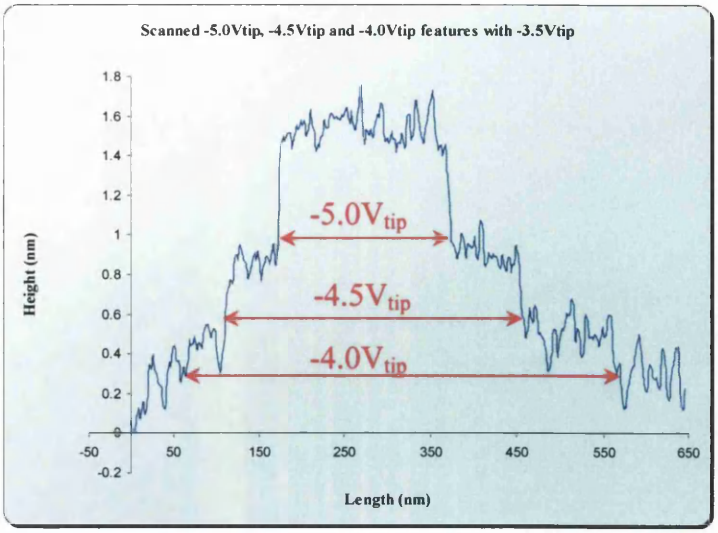

(b)
nm
4.5
1.2
1.0
0.8
0.6
0.4
0.2
0.0
0.00
-0.81
50nm

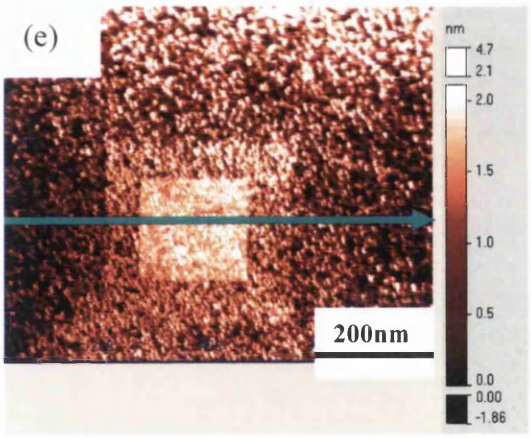

Scanned -5.0Vtip feature with -4.5Vtip
Height (nm)
Length (nm)
-5.0V tip
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
50
100
150
200
250
300
350

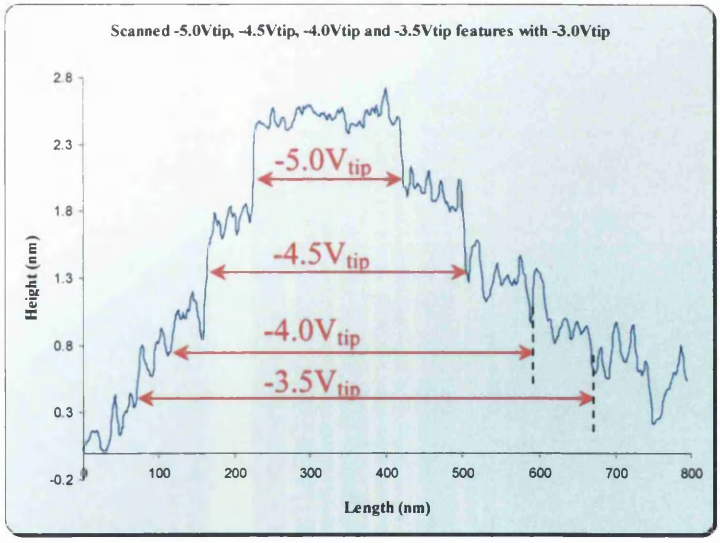

(c)
nm
5.17
1.85
1.5
1.0
0.5
0.0
0.0
-2.1
100nm


Scanned -5.0Vtip and -4.5Vtip features with -4Vtip
Height (nm)
Length (nm)
-5.0V tip
-4.5V tip
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
-0.2
50
100
150
200
250
300
350
400
450
500


(d)
nm
5.21
1.58
1.5
1.0
0.5
0.0
0.0
-1.6
100nm


Scanned -5.0Vtip, -4.5Vtip and -4.0Vtip features with -3.5Vtip
Height (nm)
Length (nm)
-5.0Vtip
-4.5Vtip
-4.0Vtip


(e)
nm
4.7
2.1
2.0
1.5
1.0
0.5
0.0
0.00
-1.86
200nm


Scanned -5.0Vtip, -4.5Vtip, -4.0Vtip and -3.5Vtip features with -3.0Vtip
Height (nm)
Length (nm)
-5.0Vtip
-4.5Vtip
-4.0Vtip
-3.5Vtip

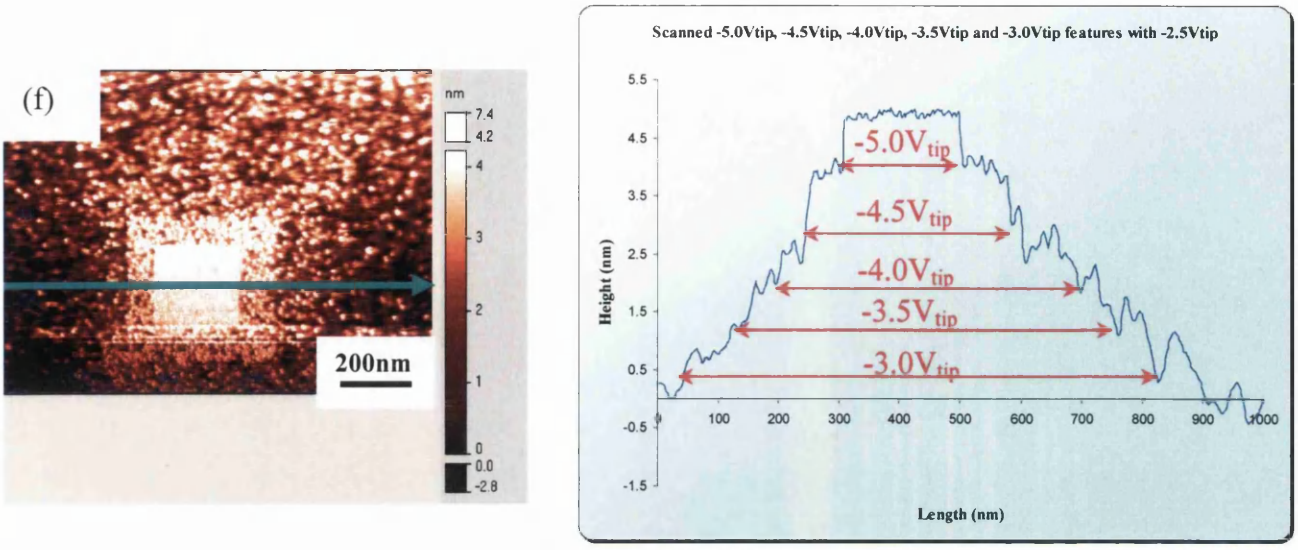


Figure 5-22 **(a) First Square scanned with tip voltage of -5.0V on 200nm by 200nm surface**

(b) Zoom out to 350nm by 350nm and scan the surface with $-4.5V_{tip}$

(c) Zoom out to 500nm by 500nm and scan the surface with $-4.0V_{tip}$

(d) Zoom out to 650nm by 650nm and scan the surface with $-3.5V_{tip}$

(e) Zoom out to 800nm by 800nm and scan the surface with $-3.0V_{tip}$

(f) Final scan with tip voltage of -2.5V on 1000nm by 1000nm surface with line profile across the blue arrow of image, shown on the right of all images

5.4.2 Effect of Cumulative Scanning with Negative Tip Voltage

Using the same approach as mentioned in section 5.3, the line profile presented alongside each image shown in Figure 5-22 was achieved by drawing a box across the image with maximum coverage of the "stacked" feature and calculate the average height measurement using WSxM software[4].

The line profiles in Figure 5-22 show staircase-like patterns on both sides of the graph, indicating clearly the change of height induced by different tip voltages, where a higher tip voltage induced a greater height. In agreement with discussion in section 5.3.2, Table 5-3 shows the tabulation of the apparent height measurement of the square features generated by various tip voltage, corrected to the apparent height of the background in each image. The calculation was achieved by obtaining the difference between the apparent height of the feature and apparent height of the background shown as line profiles in Figure 5-22.

Features	Scanned With				
	-4.5V	-4V	-3.5V	**-3V**	-2.5V
-5.0V Square Feature	0.52	1.08	1.15	**1.63**	4.18
-4.5V Square Feature		0.38	0.55	**1.05**	3.19
-4.0V Square Feature			0.19	**0.52**	2.18
-3.5V Square Feature				**0.19**	1.36
-3.0V Square Feature					0.54

Table 5-3 **Corrected apparent height of square features created by various tip voltage to the scanning tip voltage, data obtained from line profile in Figure 5-22**

However, for this experiment, apart from the variation in tip voltage, some areas were exposed to more electrons (i.e. square feature constructed by $-5.0V_{tip}$ being scanned repeatedly by STM tip over the course of decrement in tip voltage at interval of 0.5V). This could give higher possibility of storing more electrons than the others, and alter the contrast as compared to a single scan at a single voltage. As such, to distinguish between the effect of such accumulative exposure to the STM tip, the result of the "stacked" feature scanned at -3V (The Red column shown in Table 5-3) was compared to the single square features, shown in Figure 5-20, where the square features were generated by the same tip voltage and current set-point of 0.4nA, and scanned for 2 frames each (result shown as Figure 5-23).

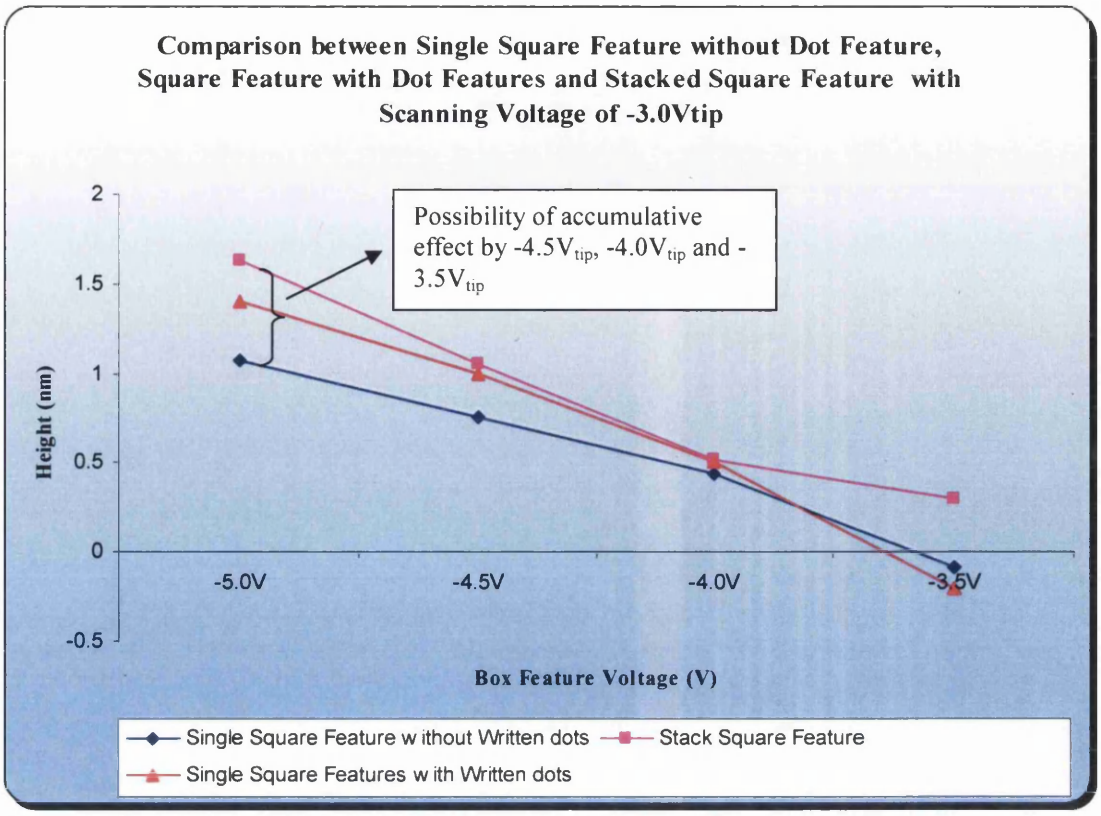


Figure 5-23 **Comparison of apparent height of "stacked" square feature with single square feature without dot feature and single square feature with dot feature, where all square features are generated by the same tip voltage at 0.4nA and 2 frames of STM scan.**

According to Figure 5-23, 2 frames of scanning are insufficient to reach the maximum electron entrapment capacity of tin dioxide grain despite the tip voltage selected. Regardless of the possible variation in experimental error, the effect of cumulative scanning is expected to be the greatest with the square feature achieved by $-5.0V_{tip}$, where it experienced the scanning of $-4.5V_{tip}$, $-4.0V_{tip}$ and $-3.5V_{tip}$ for two frames each during the course of experiment. This is substantiated when the difference of apparent height registered for $-5.0V_{tip}$ square feature between "stacked" and single experimental procedure is observed to be the biggest among all; and the cumulative effect reduces with "stacked" features created by $-4.5V_{tip}$, a lesser effect was recorded for stacked feature initiated by $-4.0V_{tip}$.

The apparent height of the square features created by different tip voltage with the cumulative scanning effect is plotted as Figure 5-24.

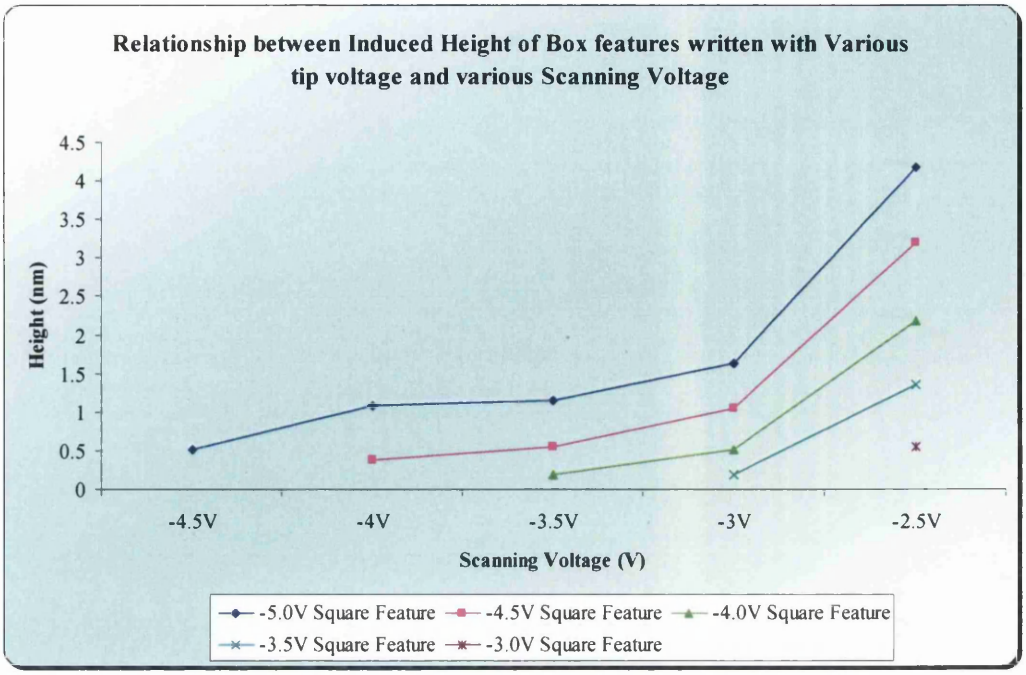


Figure 5-24 **Apparent height of "stacked" square features created by various tip voltage against different scanning tip voltage**

At constant current mode operation on STM technique, the reduction in scanning tip voltage will bring the STM tip towards the sample so as to maintain the tunnelling current set-point, resulting in smaller distance between tip and sample surface. It has been shown by Feenstra[5] and Teng *et al*[6] that the STM tip-sample interaction will be dominated by the electronic properties over mechanical properties when the tip-sample separation is reduced, the lower scanning tip voltage will highlight any electronic features on the sample surface. In-depth illustration (Figure 5-25) in previous research by Dr Mark W. Penny[2] explained that for the STM system, the Tunnelling Transmission Probability (TTP) from tip to sample is higher for the patterned dots as compared to background due to the electron entrapment within the grain, in addition to the enhancement of electronic effect[7] contribution by tip-induced band bending. This effect is observed in Figure 5-24, where there is an abrupt jump on the apparent height of the patterned feature when scanning with $-2.5V_{tip}$.

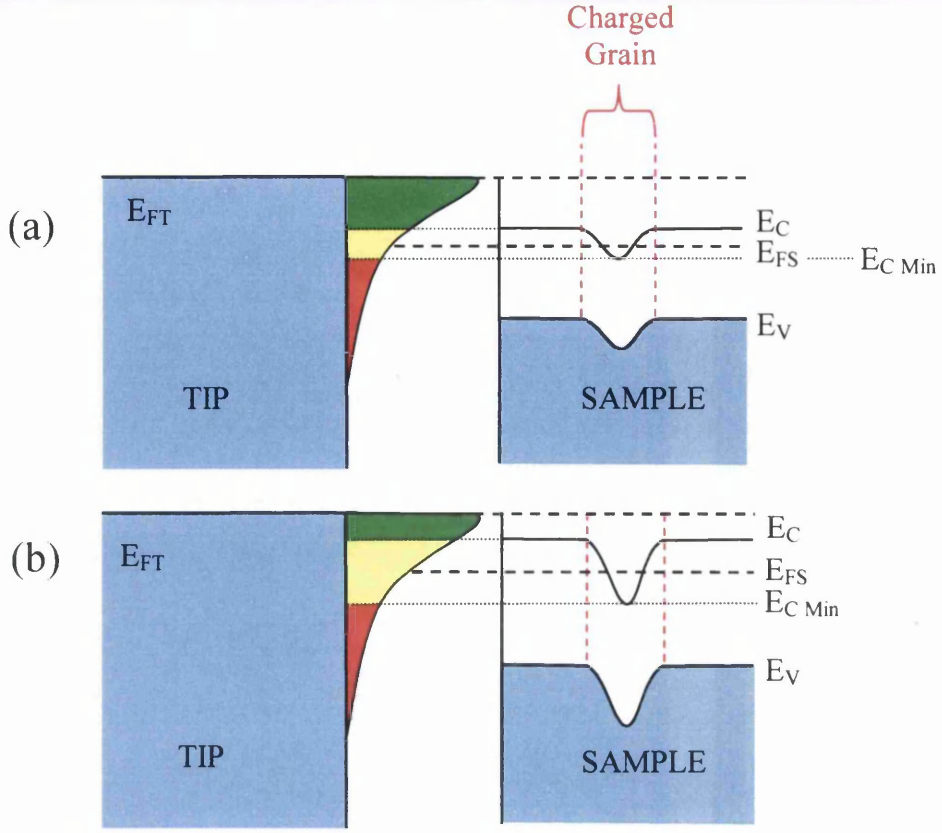


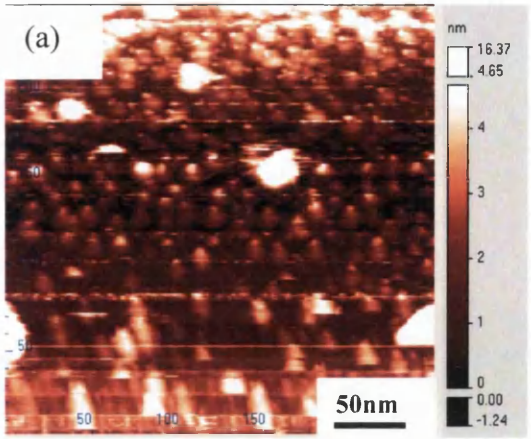
Figure 5-25 **(a) Shows a charged grain on tin dioxide material**
(b) illustrates the enhancement when tip induced band-bending is considered[2]

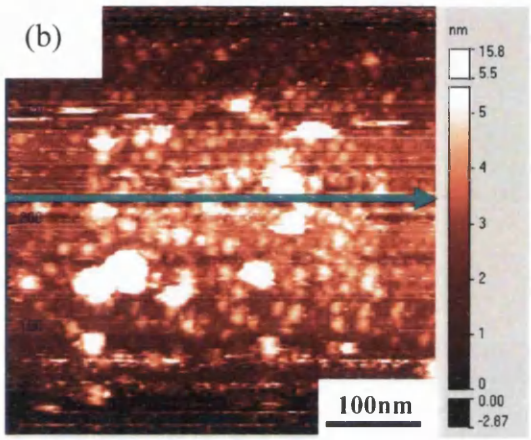
5.4.3 Effect of Cumulative Scanning with Positive Tip Voltage

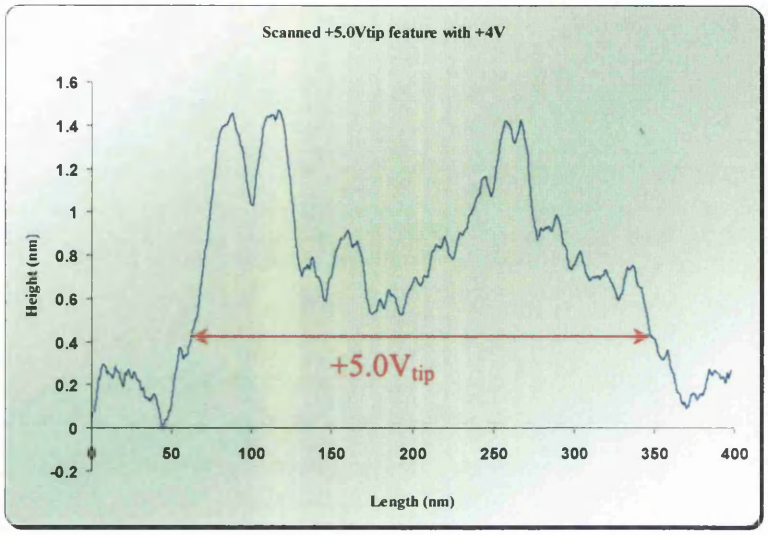
Nanopatterning research in Swansea previously on positive tip voltage has been restricted to the "erasing" process, where the electrons stored in the patterned dots at room temperature are removed by scanning on surface with $+3.2V_{tip}$. To have a glimpse of the effect of positive tip on tin dioxide, the "stacked" square feature experiment presented in section 5.4.2 was repeated with a positive voltage.

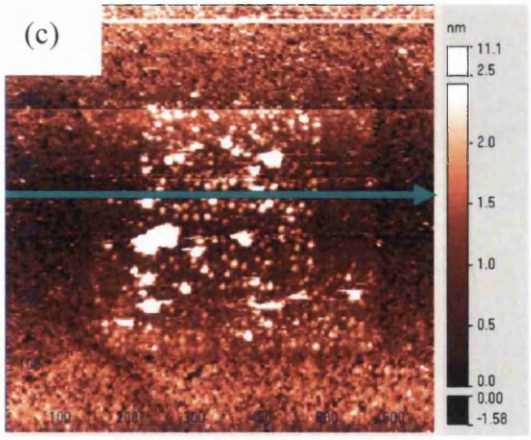
The procedure mentioned in section 5.4.1 is conducted with the new setting for the red indication in Figure 5-21(a), beginning with $+5V_{tip}$ on 250nm by 250nm surface:

Starting Voltage	=	$+5.0V_{tip}$
Preset Interval	=	1V
Final Voltage	=	$+3.0V_{tip}$









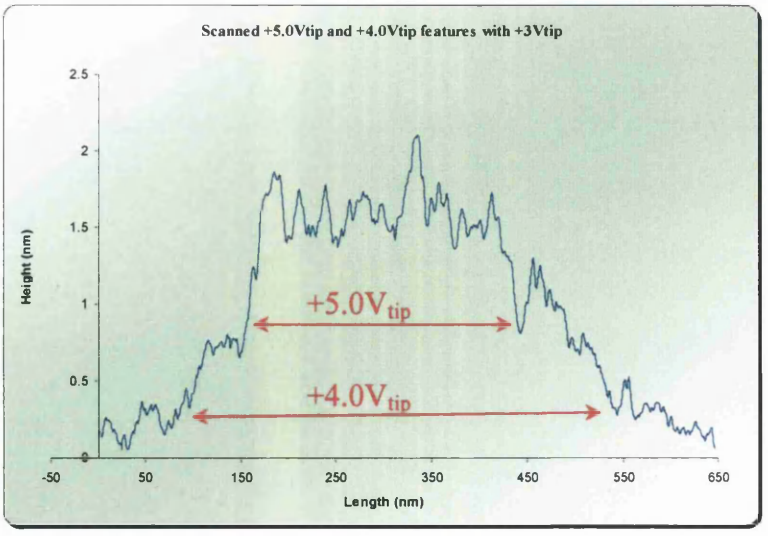


Figure 5-26 **(a) First square feature written with +5.0V_{tip} on 250nm by 250nm surface**

(b) Zoom out to 400nm by 400nm and scan the surface with +4.0V_{tip}

(c) Last scan on 650nm by 650nm with +3.0V_{tip} with line profile across the blue arrow of image, shown on the right of all images

Figure 5-26 shows the STM image and line profile of the patterned feature with respect to the scanning voltage using a similar approach and data acquisition technique used in section 5.4.2.

Observing Figure 5-26(a), the positive tip gave the same effect as $-5.0V_{tip}$, where the tin dioxide grains are distinctive, and continue to stand out for subsequent tip voltages. The similar staircase-like pattern on the line profile in Figure 5-26 indicates change in height induced by different tip voltages. The apparent height measurements for each line profile in Figure 5-26 are tabulated in Table 5-4.

	Scanned with	
Features	**+4V**	**+3V**
+5.0Vtip Square Feature	0.65	1.34
+4.0Vtip Square Feature		0.64

Table 5-4 **Corrected apparent height of square features created by various tip voltage to the scanning tip voltage, data obtained from line profile in Figure 5-26**

The apparent height of the square features is also dependent on the tip scanning voltage. The measurement of the $+5.0V_{tip}$ square feature (Table 5-4) shows an increment in height when scanned with a different tip voltage, suggesting that these features are electronic in nature. Positive tip voltage had only been explored in the "erasing" process of nanopatterning, which is believed to have removed the electrons from the grains. However, this result suggests that scanning at low positive tip voltages can remove background electrons, producing a positive residual surface charge, as illustrated in Figure 5-27.

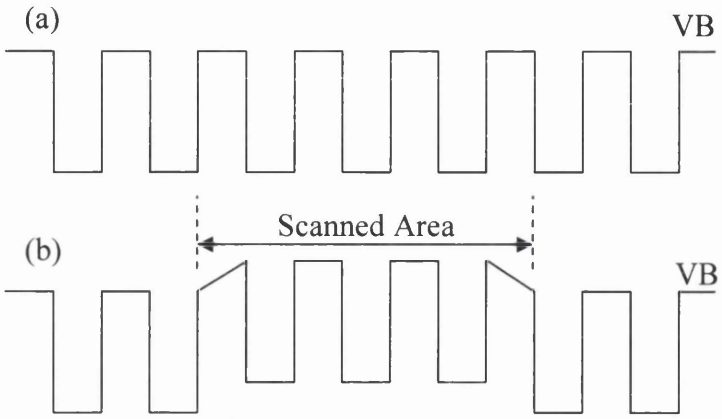


Figure 5-27 **(a) Valence band of tin dioxide grains and (b) valence band after scanning with positive tip voltage**

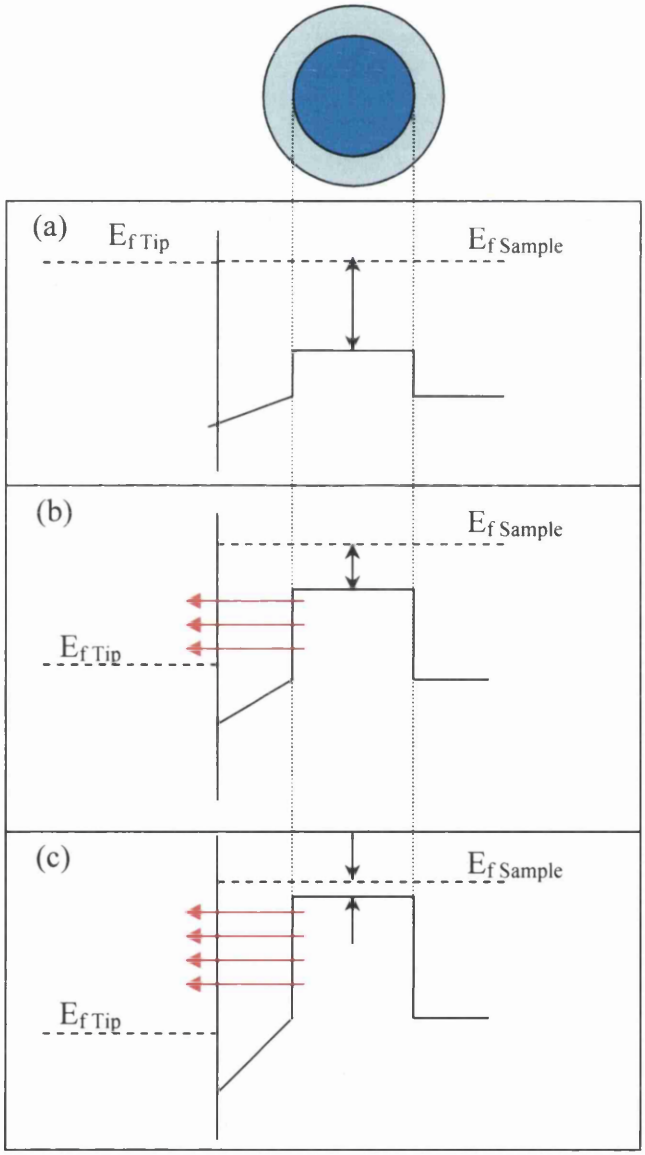


Figure 5-28 **Illustration of effect on Valence band when Tip Voltage is (a) 0V (b) low positive voltage (c) high positive voltage**

Figure 5-28 demonstrates the effect an increment in positive tip voltage during scanning, with (a) showing the band diagram when no voltage is applied on STM tip. At low positive tip voltages (b) the wavefunctions between tungsten tip and the sample will overlap, and create a path for electron to tunnel from sample to tip. Further increment on tip voltage (c), will result in higher number of Local Density of States for electron to tunnel out from the surface material. The effect is similar to function of introducing acceptor to an intrinsic semiconductor, which pushes the Valence band towards the Fermi level of the material, creating a p-type semiconductor.

If the effect of nanopatterning is reversed, where the rate of electrons tunnelling out from the sample is higher than the replenishment from the ground connection of the sample, there is a possibility of a "lack of electron" situation within the grain, resulting in a "reversed" charge writing effect. This set of experiment has provided certain concept of possibility of "reversed charge writing" mechanism, which could potentially explain the phenomena of "erasing" process. Nevertheless, due to limited data available, the concept would require further modelling and experiment before further conclusion can be drawn.

To summarise, this chapter presents a detailed study of the nanopatterning phenomena exhibited by nanocrystalline SnO_2. It expands on previous studies by looking at the effect of temperature on the patterning process. It was found that temperature affects both the size and success rate of the resulting features. As the temperature was increased the size of the resulting features also increased but the success rate declined. From STM images it appeared that at elevated temperature, the patterned features were made up from more than one grain. This was thought to be as a result of the electrons having more energy due to thermal excitation, so they could leak into the surround grains. Another possibility is that the electrons were being injected over a wider angle, as the tip-sample separation also increased with temperature. Due to the effects observed on the patterning process with temperature change, it offers another strong argument for the patterning process being electronic in nature.

The effect of cumulative scanning was also investigated. Although this has been observed before, a detailed study had not been conducted. When voltage pulses are applied to the surface, no features are observed below $-6V_{tip}$. However, when scanning large areas at voltage from $-3V_{tip}$ to $-5V_{tip}$ a distinctive change in the apparent height of the area is observed. In order to achieve distinct, localised patterned features it is thought that the rate at which electrons are injected into the surface must exceed the rate at which electrons can tunnel away into adjacent grains. If this threshold is not exceeded electrons are not trapped below the Fermi level and leak into the surrounding area. This is thought to account for the large scale change of apparent height. This result offers an intriguing insight into the behaviour of the SnO_2 surface, and in doing so corroborates the theory that the patterning process is indeed a result of electron entrapment.

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[5] R. M. Feenstra Physcial B 273-274 (1999) 796-802

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[7] R. M. Feenstra Physical Review B 50(7) (1994) 4561 - 4570

CHAPTER 6 GAS EXPOSURE AND POSSIBILITY OF GRAIN REMOVAL

The main purpose of the research was to develop a deeper understanding of the patterning mechanism. This will allow a plethora of possible applications to be realised, such as nanocatalysis, molecular docking and possibly ultra high density data storage. As mentioned in chapter 1, the use of "self-assembly" in device fabrication could potentially bring forth a new era of device miniaturisation, this could be greatly aided by the use of molecular docking and site specific adsorption. The first part of this chapter presents the results of gas exposure experiments, using oxygen (an oxidising gas) and carbon monoxide (a reducing gas). This was designed to investigate the possibility of molecular docking on the patterned SnO_2 surface; and in doing so provide more information on the nature of the patterned features.

The latter part of the chapter explains a phenomenon that was encountered during the experiment while scanning the patterned features with a positive tip voltage at a higher magnitude than the usual "erasing process" reported in the previous research[1]. This phenomenon can be used to help explain the difficulty in achieving single grain samples for nanopatterning.

All experiments presented in this chapter were carried out at 150°C. The procedure for achieving such conditions is explained in the previous chapter. Similarly to the previous chapter, all data in the chapter are acquired at the same temperature as when nanopatterning was performed.

6.1 GAS EXPOSURE

The experiments presented here show the effect on the patterned surface from exposure to oxygen and carbon monoxide in a UHV environment. Oxygen was chosen as it is an oxidising gas, meaning that it takes electrons to fill in empty states. Conversely, carbon monoxide is a reducing gas, meaning that it would chemisorb onto the oxide layer, hence releasing the electron into the conduction band of tin dioxide particles, in turns increases the conductivity of the material. As such, in theory, oxygen molecules should be attracted to regions that have higher electron

concentration, such as the patterned areas and in doing so remove electrons from the grains; on the other hand, carbon monoxide should do the opposite.

6.1.1 Experimental Preparation

For all the gas exposure experiments, consistency of the experimental setup was maintained visually using the CCD camera. The gas pipe that delivers the gas is moved to the best approximation of distance d, by comparison between the image obtained by the camera and previous still frames, as shown in Figure 6-1.

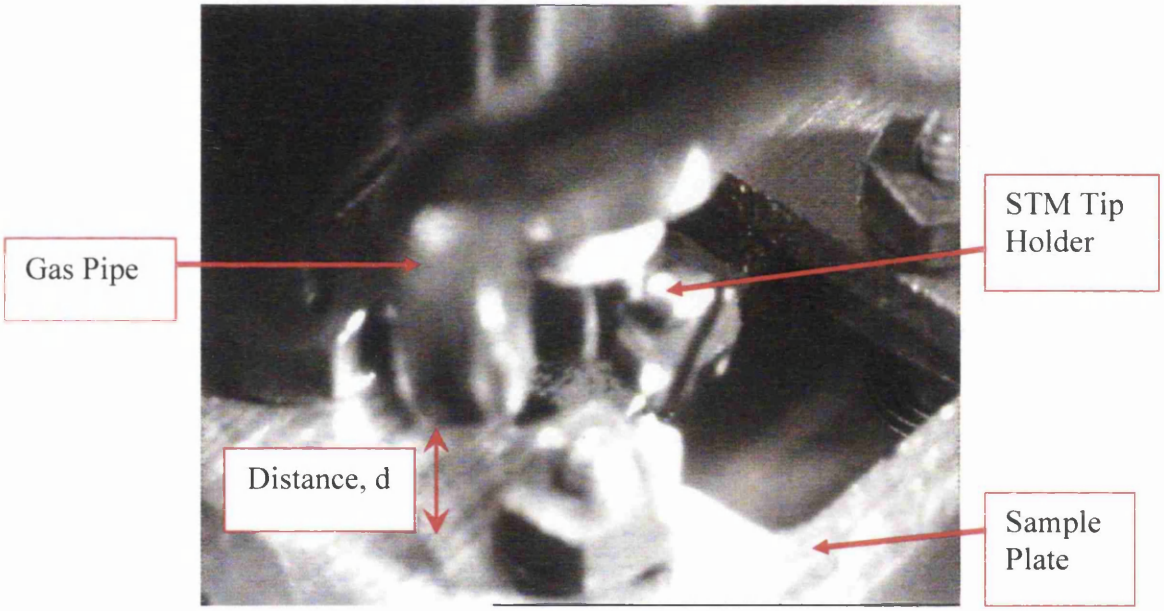

Figure 6-1 Still camera frame taken with the CCD camera

Apart from the position of the gas pipe, the pressure at which gas is inserted into the system is also controlled. Figure 6-2 shows the pressure gauge that is installed in the Omicron system, which measures the pressure in the analysis chamber where STM system is mounted. During all gas exposure experiments, the pressure in the analysis chamber was maintained at 1.6×10^{-9} mbar.

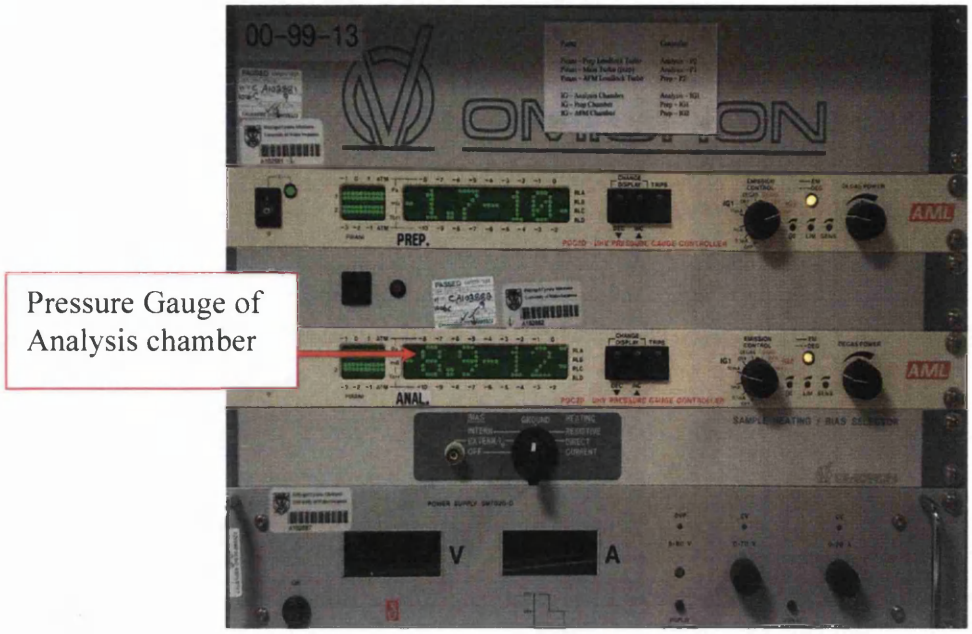

Figure 6-2 **Pressure Gauge of the Analysis Chamber for Omicron System**

6.1.2 Oxygen Exposure at Room Temperature

Previous work in the laboratory revealed that oxygen exposure gradually degraded the written features on the SnO_2 surface over 1 hour[1]. Due to the quantity of patterned dots involved, the response of these dots occupied the majority of the frame, making it difficult to interpret the results of the exposure. As such, the experiment was repeated with fewer features.

The experiment was initially conducted at room temperature. The position of the gas pipe supply was moved towards the sample plate as explained in section 6.1.1. The tip is then approached to the sample surface and three dots were written using the "single event" procedure mentioned in chapter 4 at -6.0V tip voltage for 100μs. After three scanned frames the image stabilised, and when it did, the control valve (refer to chapter 4) was opened until the pressure within the analysis chamber was 1.6×10^{-9} mbar (section 6.1.1). The patterned features were exposed to oxygen for 58 minutes and the following STM images (Figure 6-3) were measured at 15 minute intervals throughout the experiment.

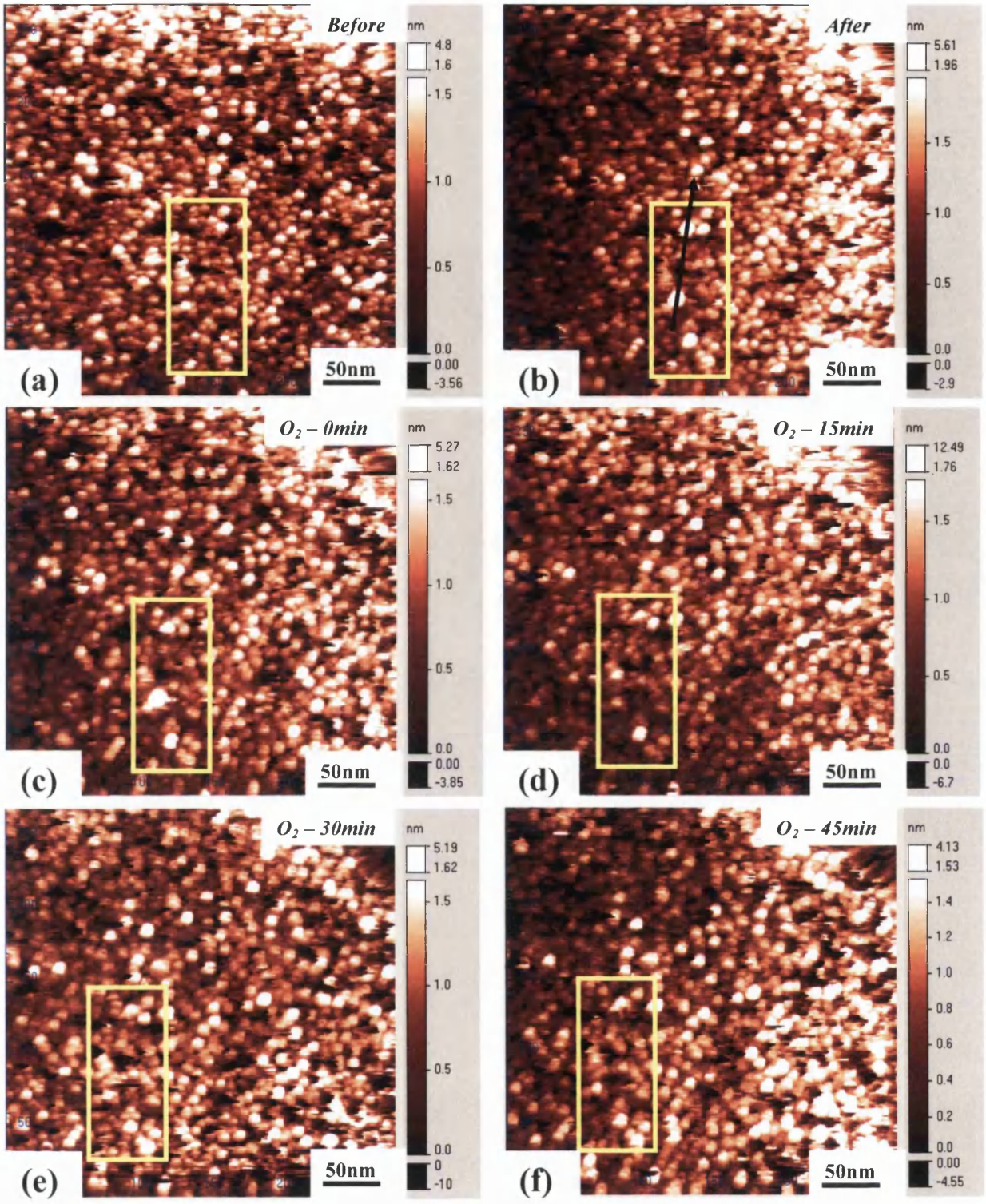

Figure 6-3 Oxygen exposure experiment at room temperature where (a) shows before nanopatterning, (b) shows after nanopatterning, (c) shows time when oxygen is first introduced to the chamber (d) shows the image after 15min of oxygen exposure (e) shows the surface after 30min of oxygen exposure and (f) shows the image before oxygen was cut off from the chamber

The reaction of two of the written dots (shown with the black arrow in Figure 6-3(b)), in terms of height, was measured from frame to frame to the best same location as possible using 'line profile' function of the Omicron software. The data were then recorded and presented in a "stacked" format, by the addition of 3nm between the line profile data obtained from frame to frame, as shown in Figure 6-4.

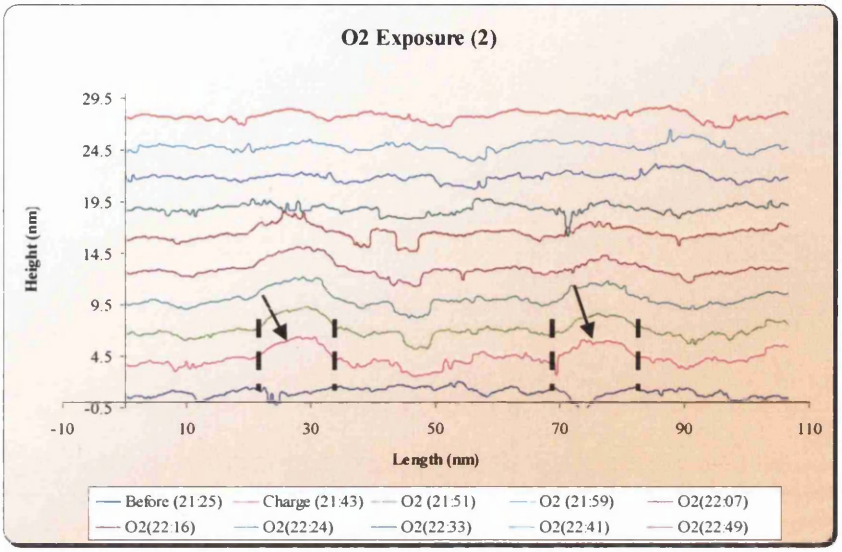

Figure 6-4 **Line profile showing apparent height variation of 2 dots patterned at room temperature being exposed to oxygen gas, which 3nm was added between frame to achieve the stacking effect. Time is given in brackets.**

The stacked data showed 2 peaks (indicated by the arrow in Figure 6-4), which result from the nanopatterning procedure. After the three stabilisation frames and exposure of oxygen, the height of the peak seems to be reducing frame after frame. However, it would be difficult to judge simply by the height, as such, the area under the graph of the same length throughout the different frames were calculated. The results of the change in area for both dots are plotted in Figure 6-5.

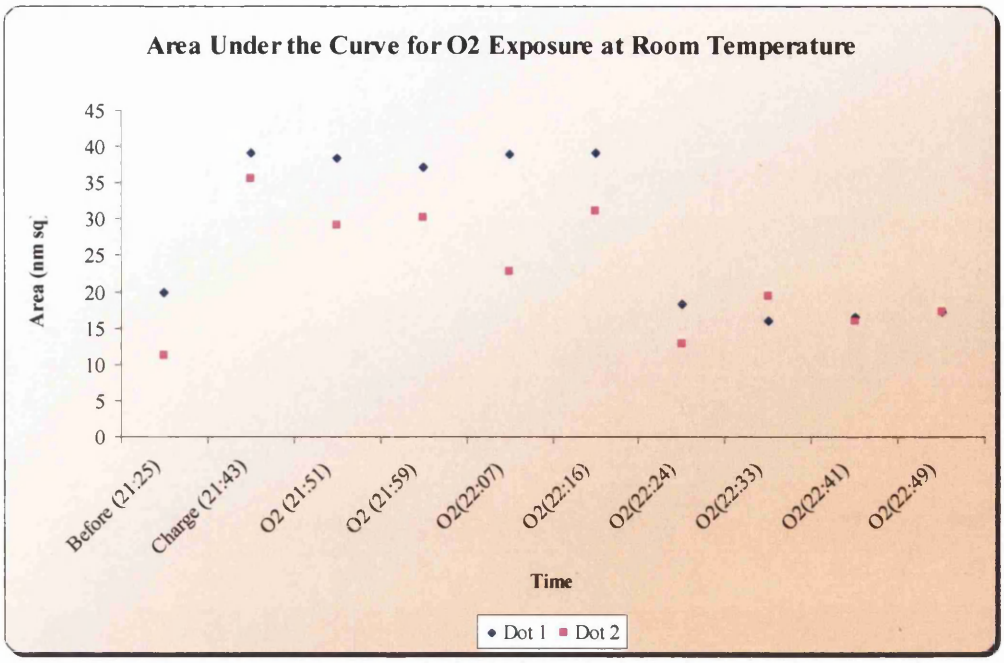

Figure 6-5 **Area under the curve calculation of the "2 peaks" length over all image frames recorded in Figure 6-4**

Looking at the graph, the area of the patterned region increased by >100% after patterning. With the introduction of oxygen to the chamber, the area started to fluctuate but resulted in an overall reduction. It is interesting to note that the area suddenly reduced about 40 minutes after the oxygen exposure.

As presented in chapter 2, tin dioxide is a popular choice for gas sensing applications. The gas sensing mechanism described in the chapter explains that when oxygen species comes into contact with the tin dioxide surface, they will be absorbed onto the material surface. A strong chemical bond will be formed by the electrons in the material surface and the adsorbed oxygen species (known as chemisorption). This forms a depletion region within the tin dioxide grains.

A similar effect occurs in the experiment mentioned above. When oxygen was first introduced to the SnO_2 surface, the oxygen species were attracted to the negatively charged areas, in this instance the patterned features. These are believed to have stored electrons during the patterning procedure. The oxygen species will take away the electrons from the patterned features, which is shown in Figure 6-4 and Figure 6-5, by the reduction of the apparent height and area. With time, more oxygen would come into contact with the

patterned features and result in further electrons being removed from the features, until all the excess electrons from the patterned features are removed. According to Figure 6-5, this happens about 40 minutes after oxygen gas was introduced into the chamber.

Looking at the images in Figure 6-3, it is also interesting to see that there was no sign of "smearing" on the written dots, or sign of charge spreading to neighbouring grains as shown in previous studies. The dots written were very distinctive on the surface, and slowly "merged" to the background. In addition, the grains of the background were clearly resolved throughout the experiment, as though they were completely unaffected by the oxygen exposure. This signifies that in this experiment, the interaction between the oxygen molecules and the tin dioxide material had occurred at the patterned region. This means that the oxygen molecules were preferentially attracted to the patterned region as opposed to the background, supporting the suggestion that the patterned features were electronic in nature.

6.1.3 Oxygen Exposure at 150°C

The previous chapter suggested that nanopatterning conducted at higher sample temperatures could "spread" the electron storage to adjacent grains. Thus experiment presented in section 6.1.2 was repeated at 150°C. This seeks to add validity to the suggestion that similar nanopatterning phenomena had indeed occurred, and the features written are electronic in nature.

Here, three patterned features were written using the "single event" function of the Omicron software after achieving the desired sample temperature. The oxygen gas was then introduced to the chamber for 80 minutes once the scanned area had stabilised. Images shown as Figure 6-6 were chosen at 18 minutes intervals.

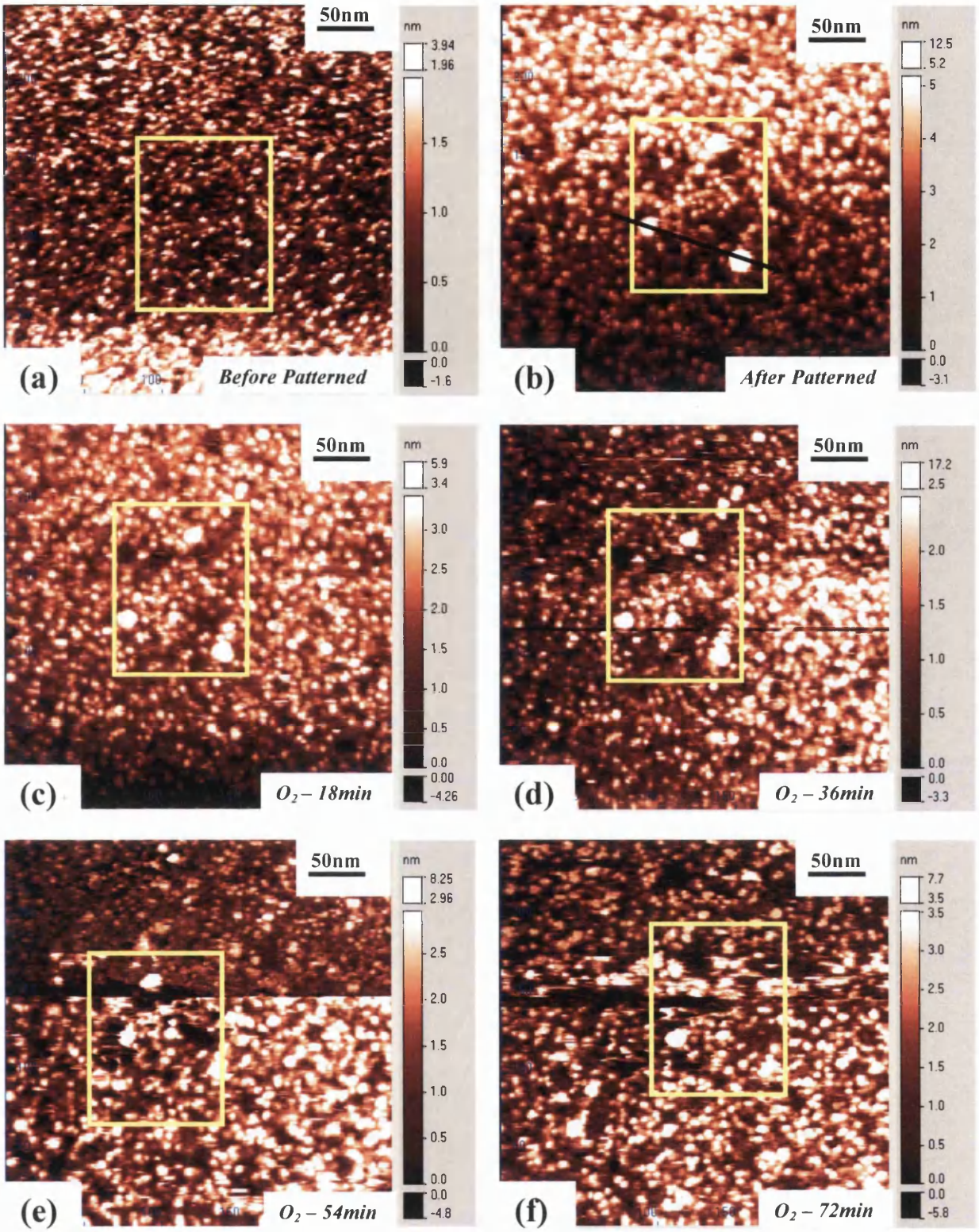

Figure 6-6 Oxygen exposure experiment at 150°C where (a) shows before nanopatterning, (b) shows after nanopatterning, (c) shows image after 18min of oxygen exposure (d) shows the image after 36min of oxygen exposure (e) shows the surface after 54min of oxygen exposure and (f) shows the image before oxygen was cut off from the chamber

Performing the same analysis method as mentioned in section 6.1.2, the variation in height of 2 of the dots (indicated with black arrow in Figure 6-6(b)) was measured using the "line profile" function found on Omicron software and plotted as "stacked" data as shown below in Figure 6-7:

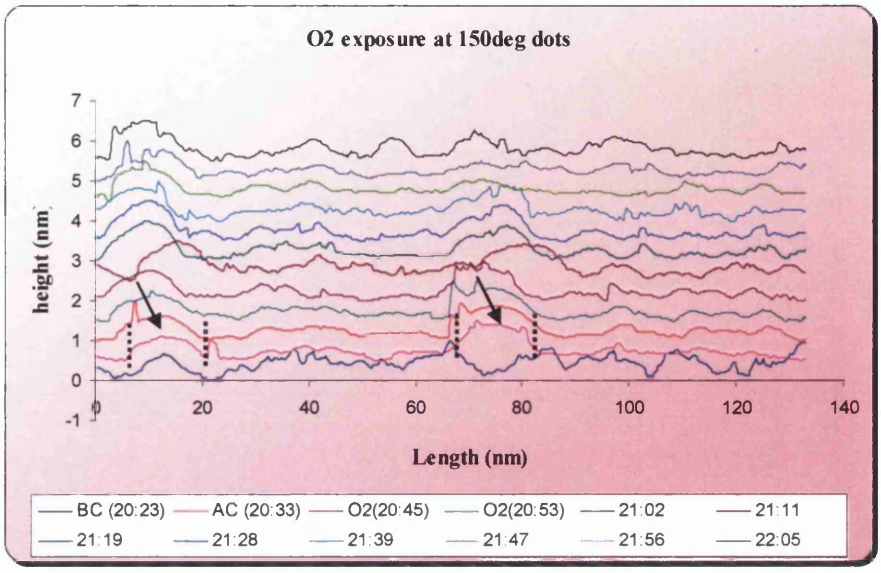

Figure 6-7 **Line Profiles showing apparent height variation of 2 dots patterned at 150°C being exposed to oxygen gas. 0.5nm was added between line scans to achieve the stacking effect.**

Again, the line profiles showed similar results. Peaks appeared after nanopatterning procedure was performed, and gradually reduced as the oxygen gas was introduced into the analysis chamber. However, it seems that the apparent height of the peak is still visible after 1 hour of exposure. Looking more into this, the area of the peaks (indicated by the arrows in Figure 6-7) were measured and calculated, at the same length on each frame, and plotted as Figure 6-8.

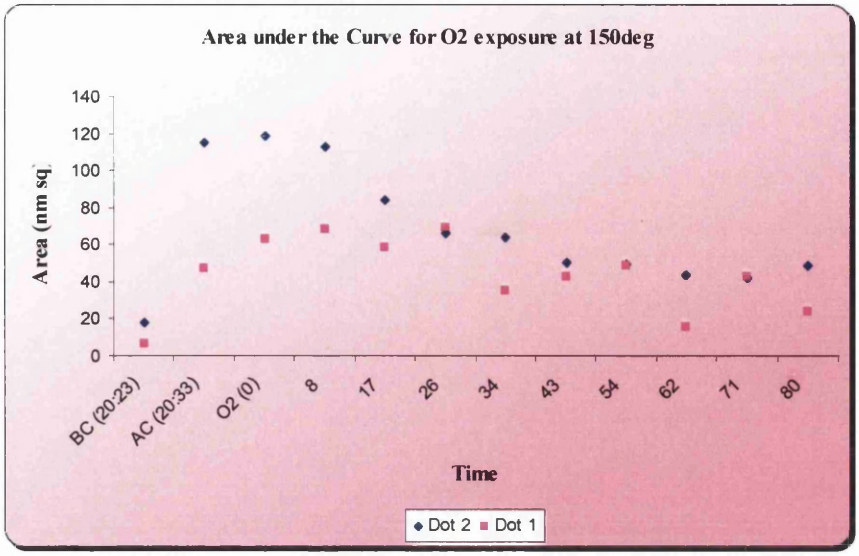

Figure 6-8 **Area under the curve calculation of the "2 peaks" length over all image frames recorded in Figure 6-7**

The area data of both dots showed a similar trend. As expected, the area of the charged region increased after charging. As oxygen was then introduced into the chamber, and throughout the 58 minutes of exposure, the area gradually decreased.

Again it seems that oxygen is preferentially attracted to the patterned regions and extracts the electrons stored within the features. However, due to instabilities whilst scanning, the experiment had to be terminated before the features could be observed to "dissolve" into the background, as expected. Nevertheless, the data acquired indicates that the reaction between oxygen species and the patterned features had occurred, which is shown by the reduction on the apparent height and area (Figure 6-7 and Figure 6-8 respectively) of the patterned features.

6.1.4 Discussion on Oxygen Exposure for Features patterned by Negative Tip

Even though both experiments in section 6.1.2 and section 6.1.3 show the same decreasing trend, which is consistent with the previous research carried out in the laboratory (refer to chapter 2), the rate of change is somewhat different. Refer to graph shown as Figure 6-5, the area of the dots reduces tremendously about 40 minutes after the exposure to oxygen gas, whereas the area of dots written at 150°C (Figure 6-8) shows a gradual reduction in area instead.

Chapter 5 explained the difference between the features written at room temperature and 150°C. The patterned features at 150°C are wider (about a factor of two) but of lower apparent height (average 1.4nm difference) as compared to those written at room temperature. This could be due to the increased temperature causing the "spreading" of the stored electrons to adjacent grains. This results in fewer electrons being trapped within each individual grain. CITS studies show that lower current flow across the features patterned at 150°C in comparison to features written at room temperature, which indicates a lower electron concentration for features created at 150°C.

With the larger dot size, the area calculated for the features patterned at 150°C is expected to be higher than ones written at room temperature. Normally, the wider feature size would indicate a larger area exposed to the oxygen. However, oxygen species are attracted to more negative charged regions, hence the electron concentration would be a more dominant factor than the size of the area to be exposed (Illustration as Figure 6-9(a)). In other words, the lower level of electron stored in features patterned at 150°C is not as attractive to the oxygen when compared to the features written at room temperature. This results in a slower reaction between oxygen species and the features created at 150°C (demonstrated as Figure 6-9(b)), which compares the area reduction rate of the patterned features at room temperature to ones written at 150°C.

Figure 6-9 **Illustration of behaviour of oxygen during gas exposure experiment conducted at (a) Feature patterned at room temperature that has a higher electron entrapment and (b) features written at 150°C that has lower electron stored but of wider size**

The result of the oxygen exposure experiments conducted in section 6.1.2 and 6.1.3 had shown that the interaction efficiency between oxygen molecule and patterned tin dioxide is related to the amount of electrons per unit area. The higher the concentration, the more vigorous the "attack" would be expected by the oxygen species. This could be useful for the application of molecular docking, allowing control over the rate at which molecules are attracted to the patterned surface.

6.1.5 Carbon Monoxide Exposure at Room Temperature

Experiments conducted in section 6.1.2 and 6.1.3 have demonstrated the reaction between the patterned features and reactive gas, which strongly suggested the patterned features are indeed electronic in nature. To further fortify this deduction, patterned features were written at room temperature and exposed to carbon monoxide (reducing gas), which supposedly should have a reverse reaction as the oxygen exposure experiment.

To maintain the consistency of the experiment, 2 dot patterns were written with the "single-event" function, similar to the nanopatterning procedure as in section 6.1.2. Once a stable scan was maintained, carbon monoxide gas was introduced into the chamber. The quantity of the gas was controlled by maintaining the chamber's pressure at 1.0×10^{-9}mbar. This experiment lasted for 126 minutes, where Figure 6-10 below showed the images of the scan throughout the experiment at intervals of 25 minutes.

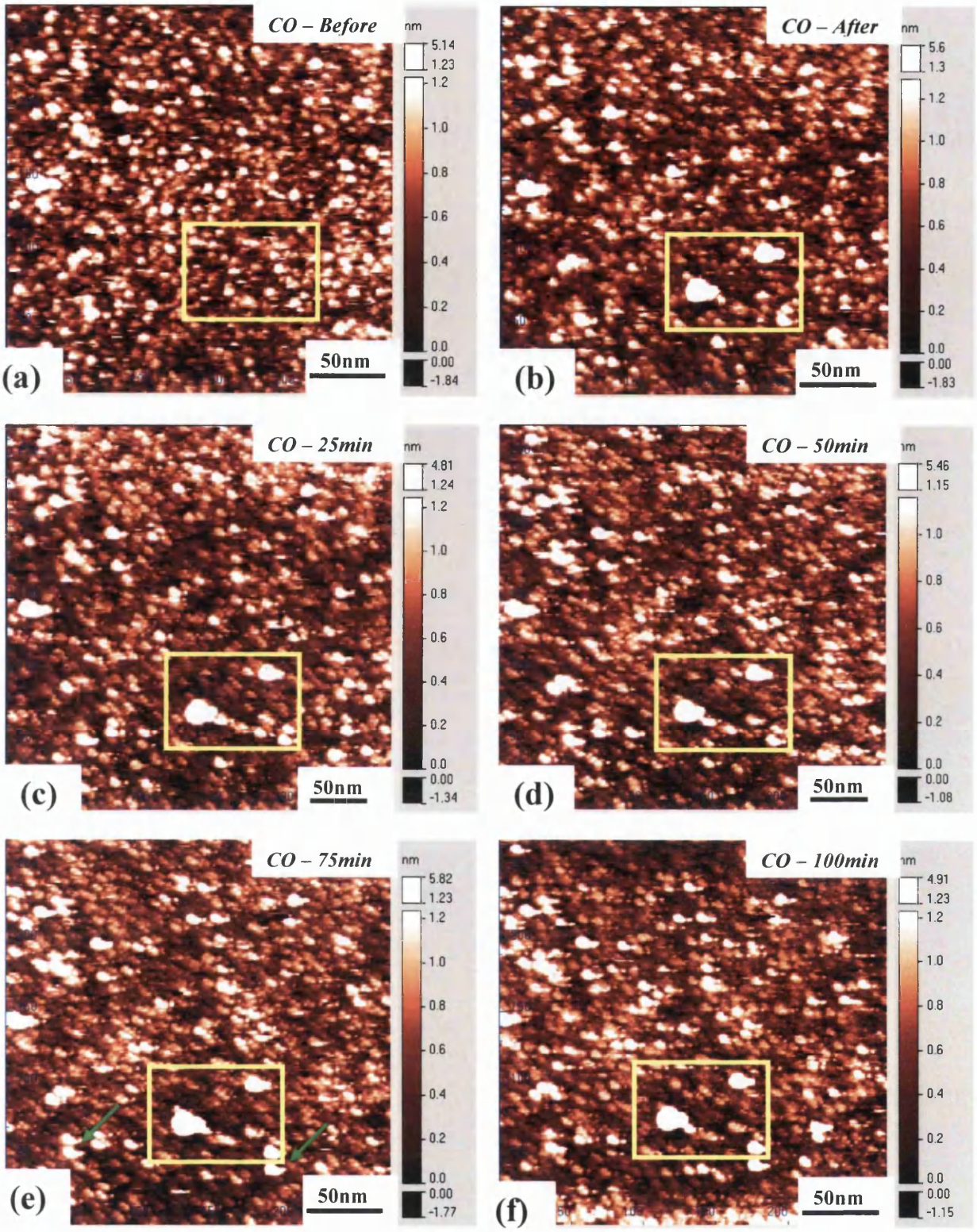

Figure 6-10 Carbon monoxide exposure experiment at room temperature where (a) shows before nanopatterning, (b) shows after nanopatterning, (c) shows image after 25min of carbon monoxide exposure (d) shows the image after 50min of carbon monoxide exposure (e) shows the surface after 75min of carbon monoxide exposure and (f) shows the image before carbon monoxide was cut off from the chamber

By taking line profiles, the apparent height of both dots was measured against the unpatterned background. However, as mentioned above, the reaction between carbon monoxide and the patterned feature is expected to be opposite to the oxygen exposure experiment in section 6.1.2 and 6.1.3, therefore, instead of "stack" analysis technique used before, the results were presented on the same plane (Figure 6-11).

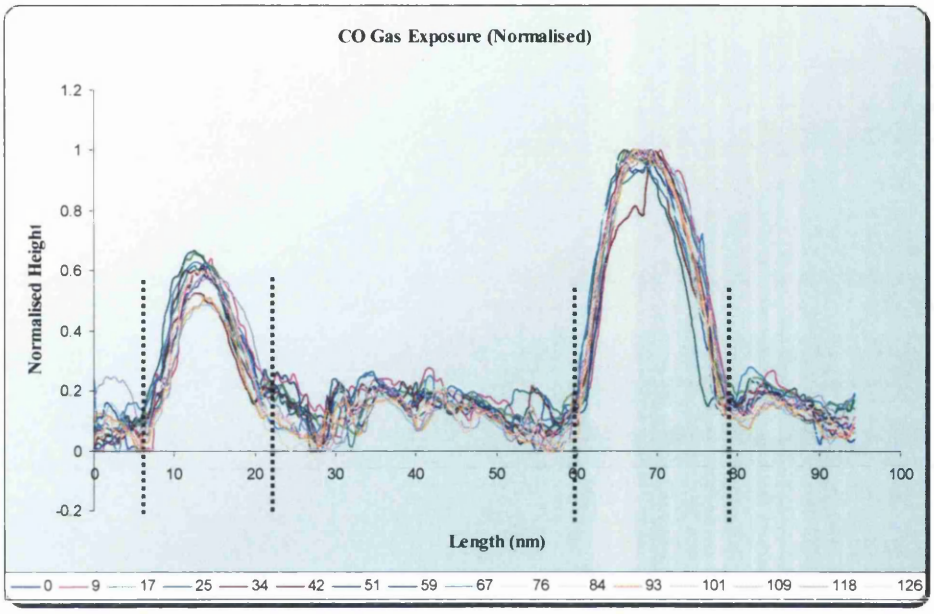

Figure 6-11 **Line Profile showing apparent height variation of 2 dots patterned at room temperature being exposed to carbon monoxide gas.**

Looking at the graph, the variation between apparent heights of both dots are close to negligible, which indicates that the patterned features have very little reaction while in contact with carbon monoxide gas. To investigate the variation in detail, similar area of the dots selected (indicated by lines in Figure 6-11) was calculated for all the frames and plotted as Figure 6-12.

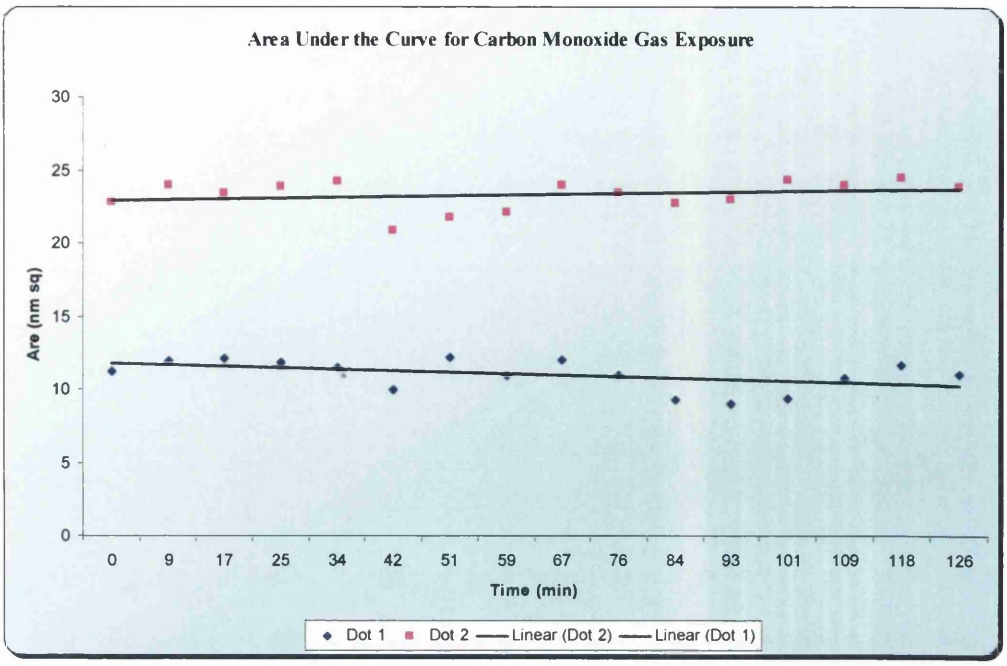

Figure 6-12 **Area under the curve calculation of the "2 peaks" length over all image frames recorded in Figure 6-11**

Graph plotted shows very little fluctuation on the area of both dots exposed to carbon monoxide gas over the time. As such, to facilitate the analysis, the trend line was plotted on Figure 6-12, showing the direction of change in the area of dots over the course of gas exposure. Both trend lines designate that the change in area of both dots is very little to be of significance throughout the 2 hours of the exposure experiment.

As explained in chapter 2, when a reducing gas comes into contact with the tin dioxide surface, it would chemisorb to the oxide layer and thus donate electrons back to the grain[2], hence increasing the conductivity. Previous research on gas sensors at Swansea University[3] shows that the tin dioxide grains reduced the band-gap after exposure to carbon monoxide gas for 90min. This means that the electron concentration in the grain increased and resulted in a higher conductivity of the material surface.

If the patterned features are due to excess electrons stored within the grains, they would be less attractive to carbon monoxide. Indeed, Figure 6-12 shows very little change in the patterned areas over the course of experiment, but some modification was observed in the background. Refer to Figure 6-10(e),

the green arrow pointed out two particular grains that seems to increase in size and more highlighted on the image, despite the patterned region remaining unchanged. This could indicate that the carbon monoxide molecules could prefer the un-patterned background to the written features.

There is a possibility that the electrons injected into a grain during patterning could have reached a saturation point, excluding subsequent electrons. Under such circumstances, even though carbon monoxide took on the oxygen species off tin dioxide surface, there is no room in the grain to accommodate more electrons. Hence the electrons liberated by the oxygen species would flow to ground, rather than become trapped within the grain. This would explain the result from the calculations of area on the patterned features presented in Figure 6-12.

6.2 Possibility of Grain Removal

Throughout the experiments conducted at 150°C, it was noticed that the dots written at elevated temperature tend to have "spike" like features, such as those exhibited in Figure 6-13(a), on the resulting scans. This makes interpretation and measurement difficult with the Omicron software. The following experiment was conducted to study the possibility of stabilising the scanning process. In doing so, observations were made that had not been previously encountered in the research into nanopatterned SnO_2.

Firstly the sample temperature was increased to 150°C, next a 5x5 matrix pattern was written on the surface using nanopatterning procedure explained in chapter 4. This pattern was then put through a series of condition in order to provide a clearer image.

6.2.1 Objective 1: Image Stabilising Attempt with Negative Tip Scanning

From experience, sometimes scanning with STM requires considerable time to condition the tip, before it performs to its best, especially when experiments are conducted at high temperature.

In the first attempt the patterned features were scanned with -3.0V_{tip}, 0.4nA current set-point, for two hours and thirty five minutes. The four images shown in Figure 6-13 are the scans within that time frame, at an interval of about 45 minutes.

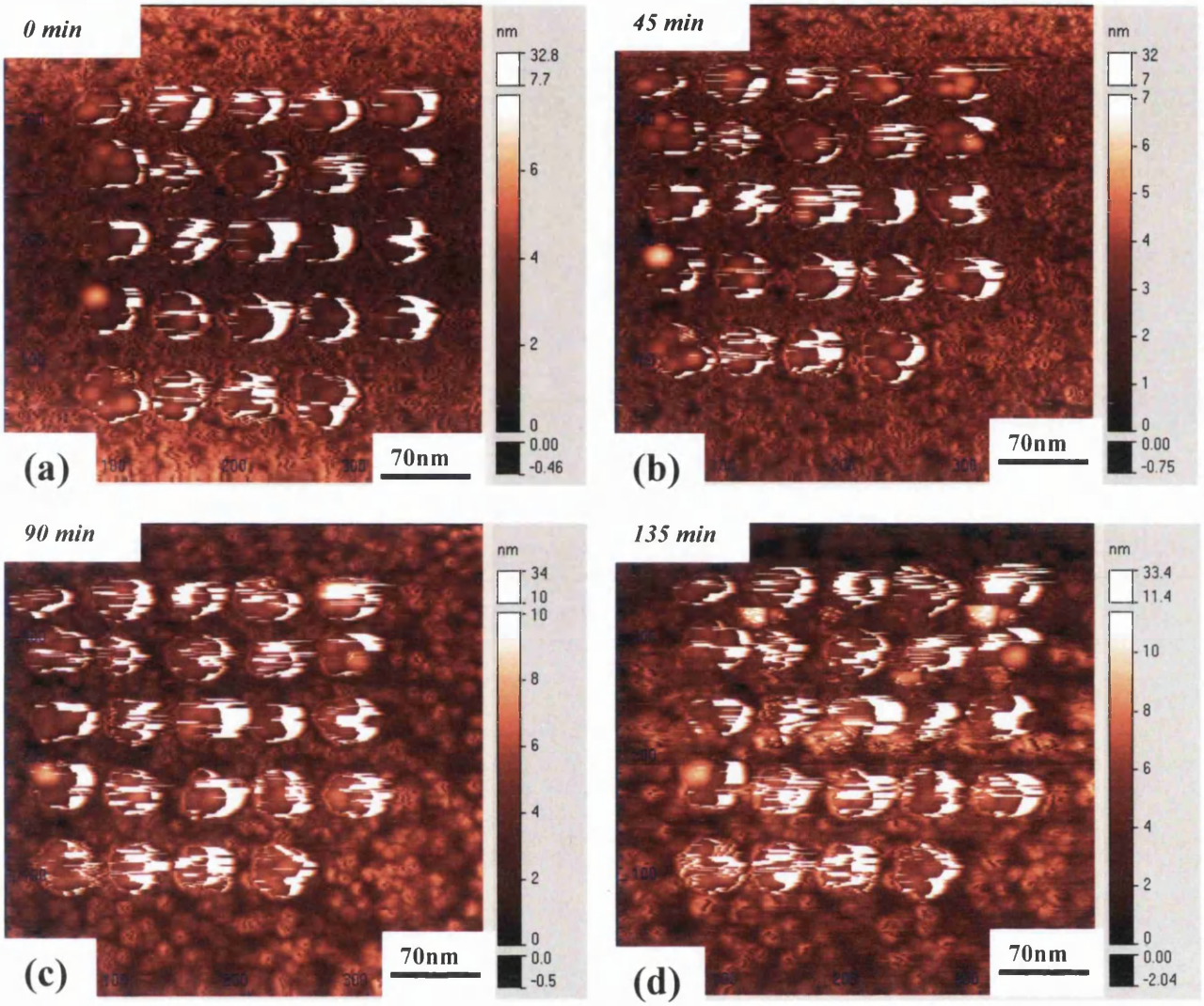

Figure 6-13 **Attempt to obtain clearer image on pattern written at 150°C by scanning with -3V_{tip} where (a) shows after nanopatterning (b) showing the image after 45min (c) showing scan after 90min and (d) showing scan after 135min**

Looking at the images in Figure 6-13, the resolution of the patterned dots did not improve as might be hoped. The background, on the other hand, has shown variations as the experiment progressed. Comparing the four frames shown above, the background became clearer and the grains were more defined as time when on. This indicates that the tip became conditioned throughout the experiment, but this did not help resolve the patterned features, which remained obscured.

6.2.2 Objective 2: : Image Stabilising Attempt with Positive Tip Scanning

Observing that scanning for hours did not improve scanning, the following attempt was made (Figure 6-4). When looking at the line profile measurement, the "spikes" seems to be noise on the original signal. Note that the height of the dots could be measured with the reasonable reading (black arrows), whereas the "spike" add measured heights unrepresentative of the surface (red arrows).

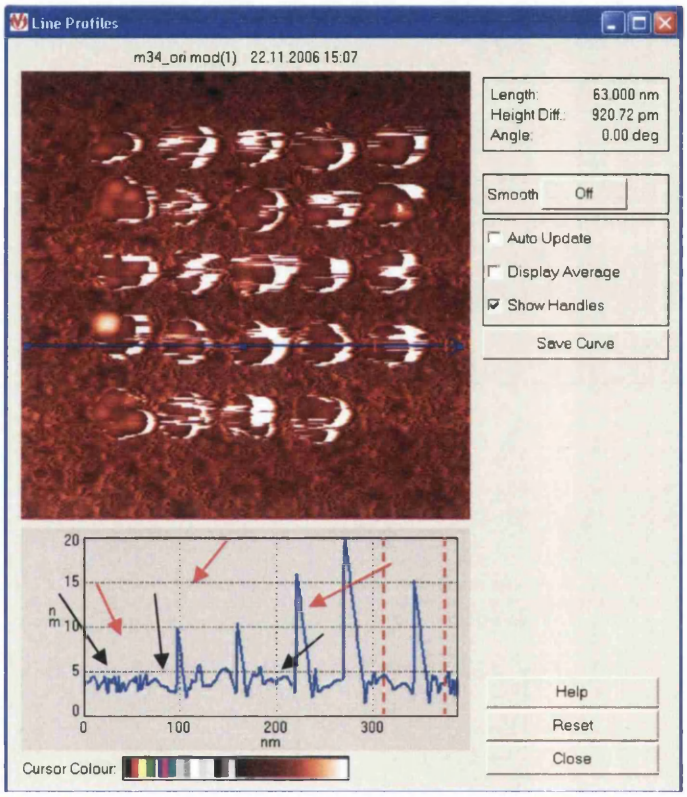

Figure 6-14 Illustration of line profile measurement on "spike" situation

It was mentioned in chapter 4 that the response of the STM tip was dependent on the electron concentration in the area it scans. Looking at the sudden surge of height measured by the system, it might reflect a sudden high concentration of charge at the scanned location. This pushes the STM tip away from the surface abruptly. Scanning with positive tip was introduced (which have been shown to have reduced the size patterned features – the 'erasing process') so as to see if the high concentration of charges could be removed.

To prevent the complete removal of the written features, a $+2.4V_{tip}$ was used which is lower than the normal erasing voltage of $+3.2V_{tip}$. This was selected so as to try and remove just the high concentration of charges, with minimal effect on the patterned region. Scanning was performed for four frames (≈ 30min) and images shown were chosen at interval of two frames during the experiment.

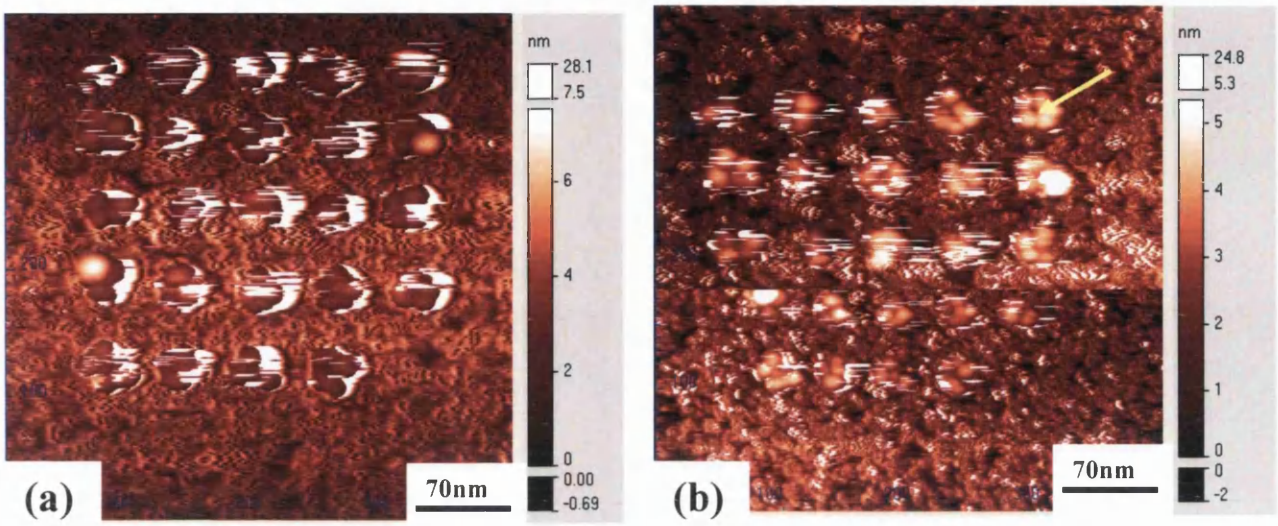

Figure 6-15 **Attempt to obtain clearer image for pattern written at 150°C by scanning with $+2.4V_{tip}$ where (a) shows the beginning of the attempt and (b) showing the images after 30min**

After four scans, the images have noticeably improved, and the shape of the grains seems to be more resolved than before (yellow arrow in Figure 6-15 pointing to patterned region consisting group of grains). When comparing to the experiment where the patterned surface was scanning for 2 ½ hr with a negative tip (refer to section 6.2.1) to the result here, the resulting images have improved dramatically. The same effect occurs to the background of the frame too, where the grains are more apparent. This suggests that positive tip scanning could be the solution to improve particularly spiky images.

As mentioned in chapter 4, the current direction in STM system is determined by the polarity of the tip voltage. In this case, when the images were scanned with positive tip voltage, the electrons would flow out from the sample surface. There is a possibility that when the area is scanned with a positive tip, the excessive electron concentration measured by the STM is removed in

the process and hence stabilises the scanning process producing clearer images.

6.2.3 Objective 3: Image Stabilising Attempt with Higher Positive Tip Scanning

Since scanning with a positive tip improved the situation after just 30 minutes, a higher voltage might result in a bigger and faster reaction. From the previous work done in the laboratory, dots erasing process at positive voltage takes about 1 hour, therefore for this higher voltage experiment, it would be tried for just one frame, to see if the imaging could be improved. The experiment was conducted with $+5.0V_{tip}$.

Unfortunately, the scan went bad, and nothing could be seen on the resulting scans. This occurred during different phases of previous studies, where the tip might need more time to be conditioned before it could perform well. These conditions were maintained for three more frames, but the situation did not improve.

As this experiment was conducted at $+5.0V_{tip}$, which is even higher than the normal 'erasing' voltage used in previous studies, the effect on the pattern was not known, and could prove detrimental. Thus, the experiment was aborted and the tip was cleaned using high voltage pulses, attempting to salvage the possible damaged tip.

Afterwards, scanning was resumed at $-3.0V_{tip}$ and a stable image obtained. However, the previously patterned feature were not visible on the image, therefore the scanned area was increased (600nm by 600nm), so as to review the result of the experiment. After several movements, the following area was found.

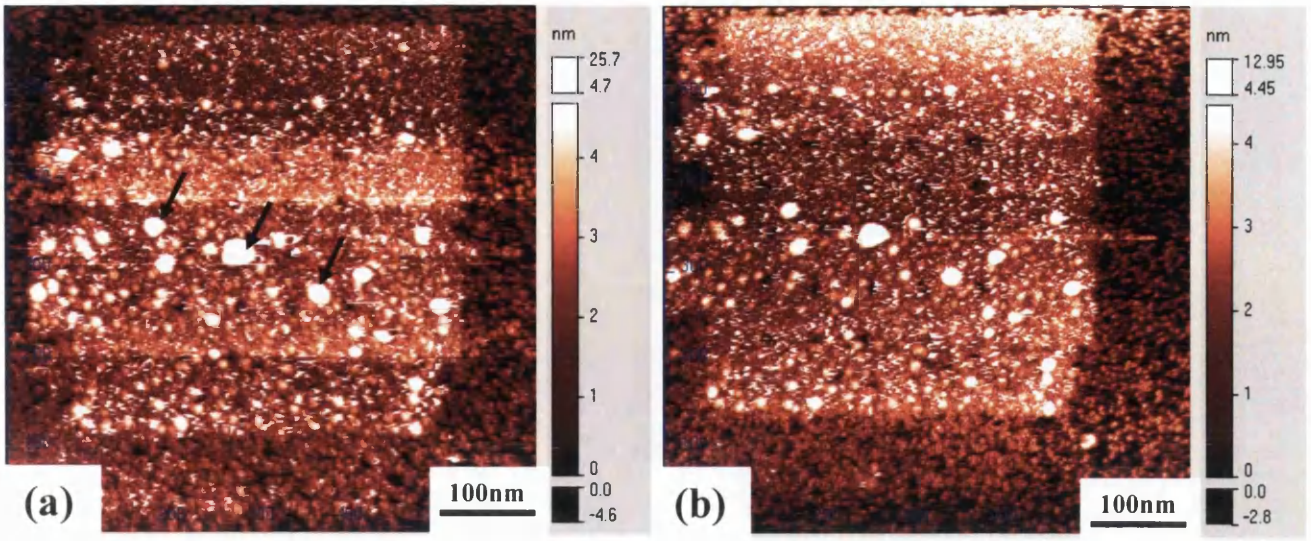

Figure 6-16 **Attempt to locate the patterned region after cleaning the tip where (a) shows the Interesting pattern found using -3.0V_{tip} and (b) showing the same pattern using +2.4V_{tip}**

Image Figure 6-16(a) shows that the area had previously been scanned with a high voltage, especially the middle section of the scan where familiar "stacking" effect presented in chapter 5 could be seen. This indicates that the middle section of the image was scanned with the higher tip voltage as opposed to the previously unscanned regions, which appear lower (darker) on the image.

A pattern can still be vaguely seen on the image, but on closer inspection the image reveals the opposite effect to the normal nanopatterning process which was done in the centre. Here a "dip" is seen rather than the expected "peak", that was visible beforehand. In trying to stabilise the image, another scan with +2.4V_{tip} was conducted, the pattern is even clearer than before (Figure 6-16(b)). Indeed the "dip" pattern can be clearly observed. In addition, there are many features (indicated by black arrows on Figure 6-16) that possess similar characteristics to patterned features that were present around the "dip" pattern.

This is an extremely interesting image, because of the reverse effect observed on the nanopatterned surface. The scan was then zoomed into the area where this unique pattern was found and both $-3.0V_{tip}$ and $+2.4V_{tip}$ were used to acquired an image of each. The results were presented as Figure 6-17 below.

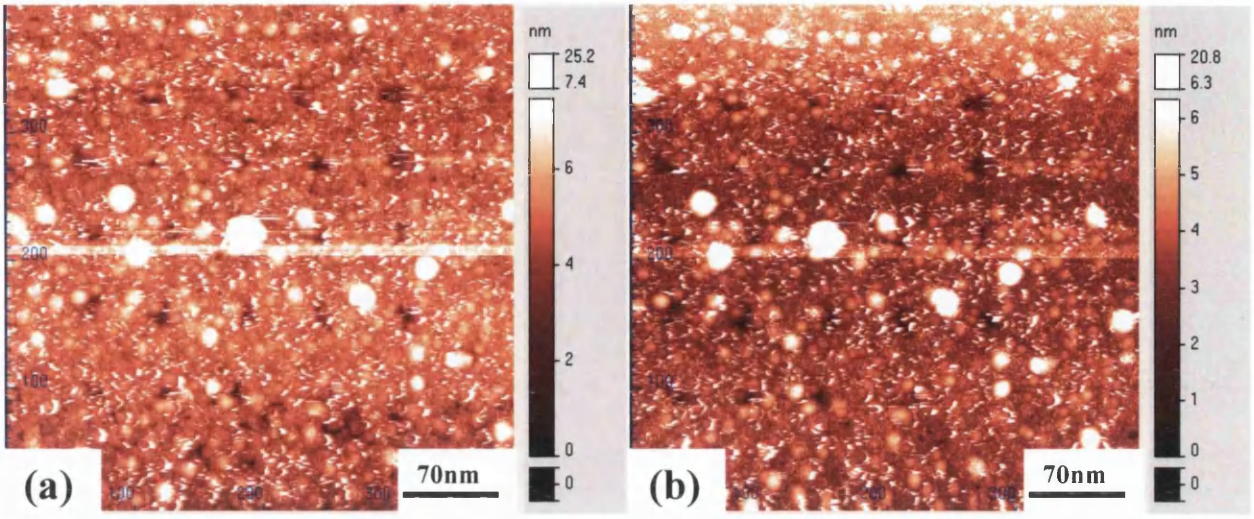

Figure 6-17 **Zooming into the area where the interesting pattern was located where (a) shows the scan with $-3.0V_{tip}$ and (b) shows the image scanned with $+2.4V_{tip}$**

Both scans showed that the image was real, and the "dip" pattern does exist. However, it was shocking that the images shows certain familiarity to an incomplete 5 x 5 matrix grid pattern (refer to chapter 4 for comparison), as though the effect of nanopatterning procedure was reversed. Instead of a brighter image corresponding to a patterned region, the features are darker.

6.2.4 Discussion on Image Stabilising Attempts

Analysing the image obtained in section 6.2.3, it was particularly interesting to see that the incomplete pattern obtained looks like the inverse of the pattern written initially at the beginning of the experiment (see section 6.2). Therefore, a best resolution image scanned at $-3.0V_{tip}$ and $+2.4V_{tip}$ of the area obtained in section 6.2.1 and section 6.2.2 respectively were selected and placed side by side to the images presented in section 6.2.3 for comparison.

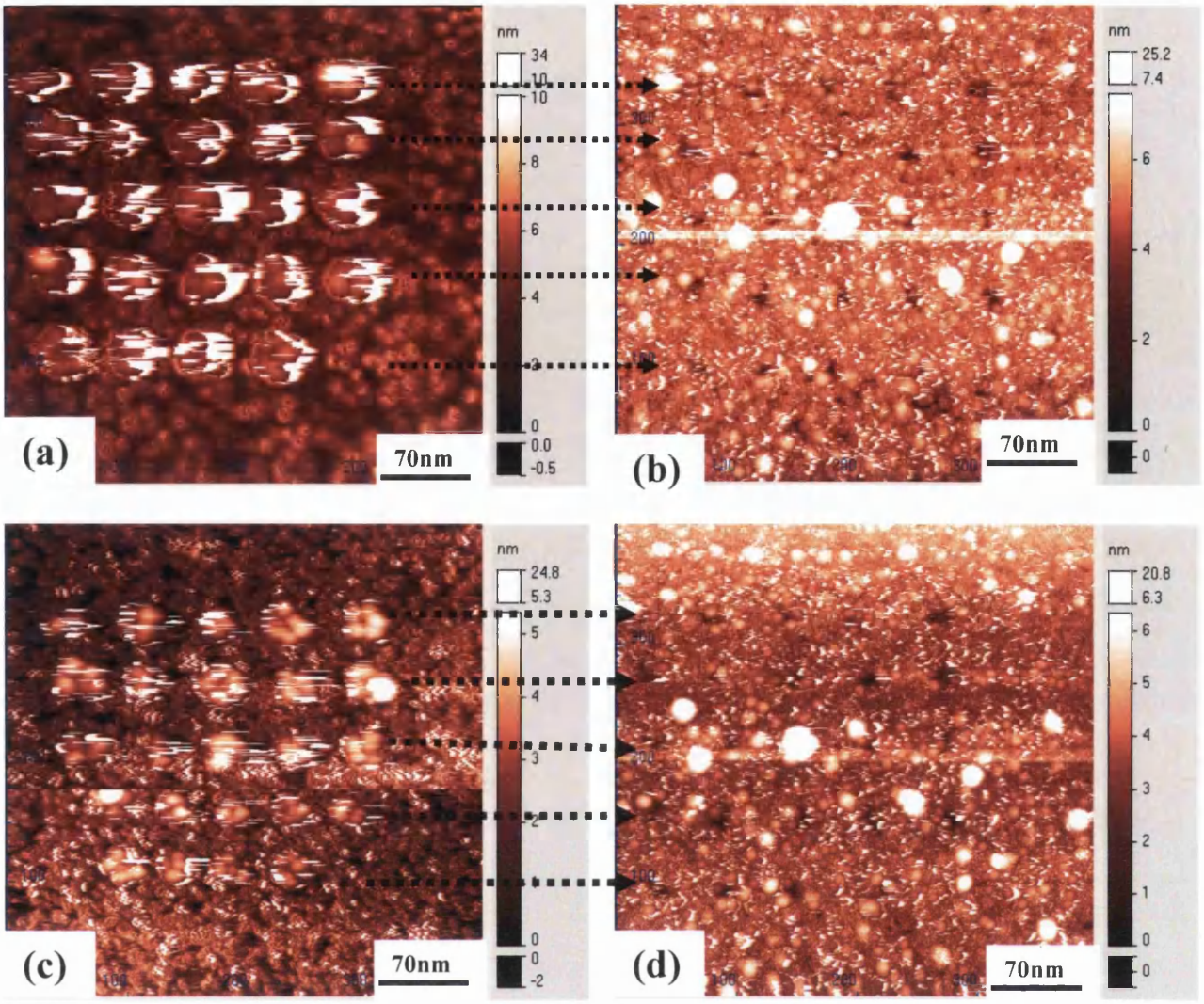

Figure 6-18 **Comparing the images scanned at -3.0V_{tip} between (a) pattern acquired in section 6.2.1 and (b) interesting pattern discovered in section 6.2.3. Similar comparison was done on images scanned at +2.4V_{tip} between (c) pattern in section 6.2.2 and (b) interesting pattern in section 6.2.3**

Referring to the above comparison, the incomplete 5x5 pattern on the left column of the images matches the "dip" pattern on the right. This suggests that extremely likely, they are actually the same area. The process of scanning with a +5.0V_{tip} (section 6.2.3) had triggered a certain mechanism, which results in the situation as they are shown as the right column images above.

When the system was scanned at +5.0V_{tip}, the "erasing process" occurs, where the tip was attempting to remove the electrons stored in the patterned grains. However, due to the higher potential difference between tip and

sample as selected in the experiment, the patterned grains (which contain the excess electrons from charging) experience a greater effect, and were effectively removed from the surface and attracted to the tip leaving behind the hole-like pattern obtained in section 6.2.3.

This helps explain why it was practically impossible to obtain a stable scan during the experiment mentioned in section 6.2.3. As explained in chapter 3, it is advantageous to have an atomically sharp tip, so as to obtain the best resolution of the surface. If the grains were indeed being removed and attracted to the tip, the apex of the tip would be "blunt", due to the attached grain (Figure 6-19(b)). As illustrated as Figure 6-19, the defined features of the nanocrystalline SnO_2 surface will no longer be visible and possibly result in extreme scanning instabilities encountered in section 6.2.3.

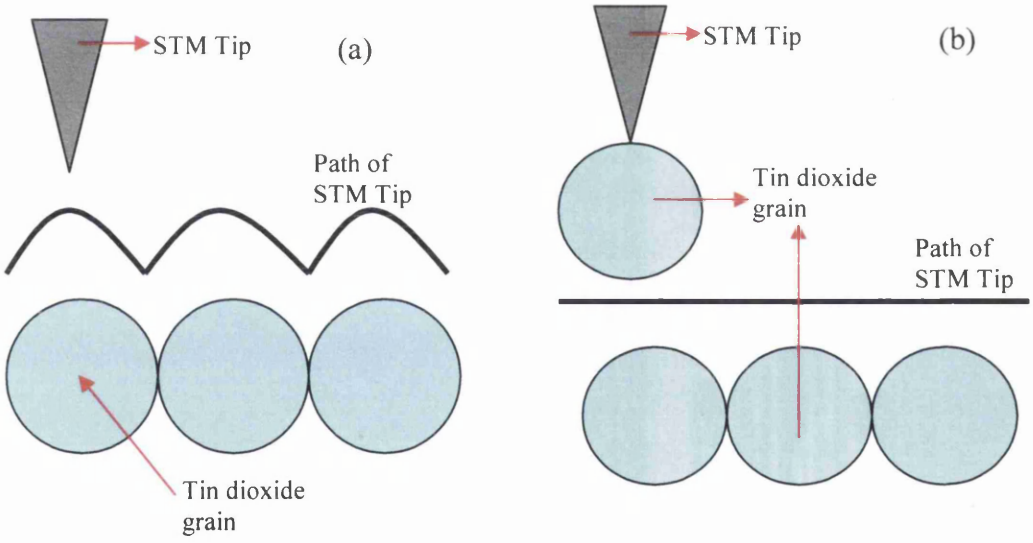

Figure 6-19 **Illustration of STM tip scanning with (a) an atomically sharp tip and (b) a grain stuck at the apex of the tip**

In addition, the familiar "stacking" effect observed in Figure 6-16 was reported in previous studies as described in chapter 5, indicating that the area had been previously scanned with a higher voltage. This higher tip voltage is probably due to +5.0V tip voltage used in section 6.2.3, whereas the other bigger square box feature could be as a result of drift and prolonged scanning at $-3.0V_{tip}$ and $+2.4V_{tip}$, performed in section 6.2.1 and section 6.2.2.

Moreover, the grain-like features spotted around the pattern in Figure 6-18, that was not present previously, could corroborate the possibility of grain removal. It is thought that during the three frames of scanning with a $+5.0V_{tip}$, the charged grained have attached themselves to the STM tip, resulting in the instabilities whilst scanning. The technique of using high voltage pulses in order to re-condition the tip could have deposited these grains on the surface once more, and by clearing the grains off, the sharpness of the tip is restored, apparent by subsequent scans.

To support the idea of grain removal, line profile measurements were taken on the dots. The average height measurement on ten of the dots were ≈5nm on $-3.0V_{tip}$ scanned image (Figure 6-18(b)) and ≈4.5nm on $+2.4V_{tip}$ scanned image (Figure 6-18(d)), and average size of ≈17nm on both $-3.0V_{tip}$ as well as $+2.4V_{tip}$ images. Taking account of the tolerable error on the STM system, the measurements of these materials is very similar to the 8nm tin dioxide nanoparticles used in the study, which is comparable to the size of dots after nanopatterning procedure in the previous research.

REFERENCE:

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[2] Joseph Watson, Kousuke Ihokura and Gary S V Coles, Meas. Sci Technol, 4 (1993) 711-719

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CHAPTER 7 CONCLUSION AND FUTURE WORK

7.1 CONCLUSION

The work presented in this thesis shows the results of investigations into charge writing on nano-crystalline tin dioxide at elevated temperature, using STM/STS. These techniques provide valuable electronic information on how the tin dioxide grains respond to a change in tip voltage, and at elevated temperature. Through the course of the thesis, the interaction of electrons within the grains and the gas exposures to the grains in UHV was explored. These experiments were also used to help explain the "erasing" phenomenon of the written features that was reported in previous studies.

The patterns written on the surface at various temperatures (with similar nanopatterning parameters) suggested that apart from the magnitude of the voltage pulse, the temperature of the material is also a factor to be taken into consideration. The thermal excitation experienced by the material at different temperature alters the resistance of the material. With lower surface resistance at higher temperature, STM and the STS experiments showed that the features written at higher temperature are wider in size but lower in height and have a lower current flow. This suggests that nanopatterning performed at higher temperature will result in fewer electrons stored within the grains due to charge spreading effect into adjacent grains.

To help support and explain the findings of the experiments, a model was developed in Swansea University that approximated the tin dioxide grains as n-type quantum wells. Due to thermal excitation, the high energy electrons injected into the grains have gained sufficient energy to overcome the potential barrier between the adjacent grains, resulting in fewer electrons being trapped within one grain and sharing with the neighbouring grains; another possible theory involves the operation of STM technique, where the higher conductivity of the material surface causes STM tip to scan at a larger distance away from material surface, which provide a wider electron injection angle during nanopatterning procedure. Nevertheless, the STS experiment involving various pulse magnitudes shows the similar nanopatterning threshold of -$5V_{tip}$ as reported in previous studies. This hints that the effect seen on both

topographic and electronic measurements were due to thermal factors but not the properties of the material. This is an important finding that strongly indicates that the features written are indeed electronic in nature.

One of the interesting properties exhibited by the patterned features is the response to the magnitude of the scanning voltage used. The apparent height of the patterned features decreases as the scanning voltage increases, thus the features are far more distinctive at lower scanning voltages. This observation supports the patterns being the result of an electronic change to the surface. However, it is intriguing to note that the scanning voltage will also trigger a charging mechanism at different level, even though the apparent height induced is much lower than nanopatterning settings.

To further verify the nature of the patterned structures, and explore the possibility of molecular docking as an application, the patterned features were exposed to both oxidising and reducing gases whilst in the UHV STM chamber. Oxygen gas experiments provide proof that the oxidising gas is preferentially drawn to the patterned regions on the surface as opposed to the background. However, the rate of electron removal is dependent on the quantity of electrons present within the patterned dot. On the other hand, a reducing gas (carbon monoxide) showed no affiliation to the patterned features but preferred the un-patterned grains of the background. This has further fortified the belief that the patterned features are as a result of electrons being injected into the grains.

The experiments presented in this thesis also gave some insight into the properties of nanocrystalline SnO_2 when images under reversed biased (imaging with a positive tip). The patterned produced by the positive tip show changes in the apparent height of the scanned area with different magnitudes of voltage. However, further experiment would be required to understand the mechanism of nanopatterning using positive tip voltage.

The last section of the result chapter reveals the effect of the magnitude of the tip voltage during erasing of the patterned features on the surface. The result of the experiments demonstrated that a high potential difference between STM tip and the sample surface during the erasing process, would remove the patterned feature from

the surface, leaving behind "holes" that correspond to the position of the previously patterned features. This grain removal hypothesis is substantiated by grain-like features on subsequent scans of the surface, which match the size of tin dioxide grains used to make the sample. In addition, the higher magnitude of tip voltage results in a higher rate of electron extraction, as this only affected the written features, this indicates that the patterned features are electronic in nature, and this could be a result of electrostatic attraction, with the positive tip removing the negatively charged grains.

7.2 FUTURE WORK

Electrostatic Force Microscopy

The results presented in this thesis, as well as the results of previous studies, point towards the patterned features being electronic in nature. Electrostatic Force Microscopy (EFM) is a technique that could give conclusive evidence that the patterned features are indeed the result of stored charge, but unfortunately this could not be carried out satisfactorily. As mentioned in the chapter 2, the UHV system in Swansea University could only perform a "conducing non-contact AFM" technique. The incorporation of a lock-in-amplifier into the Omicron system is currently being explored, which would enable the existing system to perform a "dual pass" EFM technique. The nanopatterning mechanism proposed, suggests that the voltage pulses induced "electron trapping" in the grain of the material, which the EFM technique would be able to verify. Performing EFM after the erasing process should then show that the conductivity of the patterned region has returned to that similar of the background once more.

Studies on Isolated Grains

Single electron tunnelling was one of the avenues explored during the course of this study. However, the sample preparation techniques presently employed are not refined enough to provide a surface with single isolated grains. Figure 7-1 shows a sample prepared with only one coating, and illustrates that the SnO_2 grains clump together in agglomerates that measured over 100nm in width and 60nm in height.

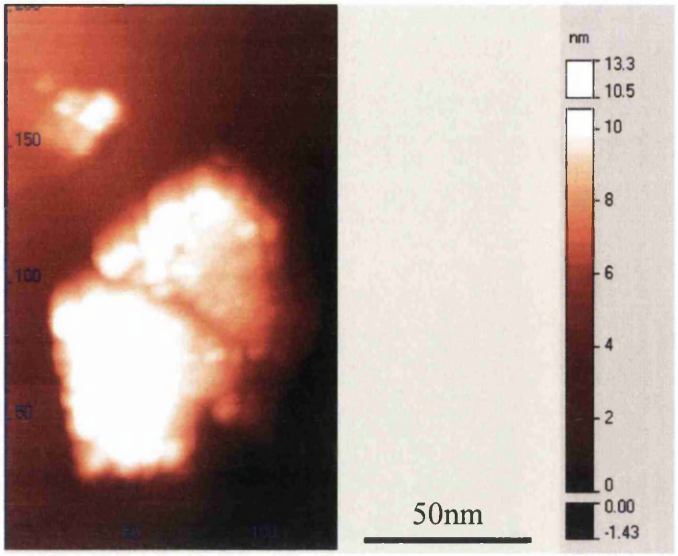

Figure 7-1 AFM image of single coating of Tin dioxide

However, the situation encountered during the 'image stabilising' experiments (refer to chapter 6) has brought forth a possibility of creating a sample with single isolated grains. It was shown that a high positive tip voltage could pick up patterned grains from the surface, leaving a "hole" in their place. The picked up grain could be deposited on the surface by alternating the polarity of the tip. The features that appeared on the surface after the "tip cleaning" process in chapter 6 were measured to be about 17nm in width and 5nm in height, which shows striking similarity to the size of patterned grains measured throughout the study, suggesting that this grain could be an individual charged tin dioxide nanoparticle.

Further experiments could be performed to understand the mechanism for such an occurrence, establishing a controlled grain deposition procedure, as demonstrated below in Figure 7-2.

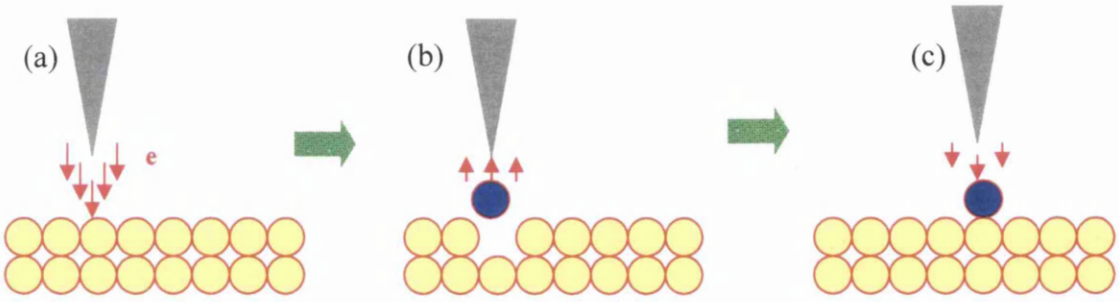

Figure 7-2 Possible Single Grain Deposition Technique

Figure 7-2 illustrates the sequence of events for the procedure, where (a) shows the nanopatterning of a grain on the tin dioxide surface. The bias is then reversed to a high positive tip voltage, to pick up the patterned grain as seen in (b). Lastly, the tip is moved to another surface (possibly another sample altogether) and deposits the picked grain. If this could be accomplished, it would allow the study of single electron tunnelling in nanocrystalline tin dioxide, which could potentially lead to applications such as single electron transistors.

Molecular Docking Experiment

As mentioned in several parts of the thesis, nanopatterning has the potential to be of assistance on the fabrication of nanoscale device by utilizing molecular docking on the surface. However to realise applications such as site specific adsorption, a detailed understanding of the charge writing process is required. In order to verify the conclusions drawn from gas exposure experiments, which suggested the patterned features are electronic nature, further Scanning Tunnelling Spectroscopy (STS) could be conducted. This would involve doing STS on patterned regions while exposing the surface to the selected gas. The change in conductivity on the patterned region would provide the information on electronic activity between the gas introduced and the patterned areas.

Furthermore, it would be valuable to expand research on this area by looking into the possibility of attracting larger molecules to the patterned regions. However, the potential molecule must be carefully selected as the experiment will be conducted in UHV environment. Thus the selected molecules must be able to be removed completely from the system at the end of the experiment through baking, so as to keep contamination to the system to a minimum.