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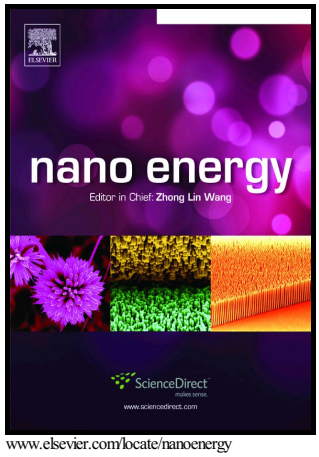

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High Performance Piezotronic Logic Nanodevices Based on GaN/InN/GaN Topological Insulator

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Abstract

Piezotronics and piezo-phototronics have received increasing attention in flexible energy-harvesting devices, self-powered sensor systems utilizing piezoelectric semiconductor materials, such as ZnO, GaN and monolayer MoS_2. Piezoelectric potentials induced by the externally applied strain can effectively control the generation, recombination and transport of the charge carriers for achieving high-performance devices. In this study, we describe the piezotronics effect on the GaN/InN/GaN quantum well, which can induce performances resembling those of topological insulators by a piezoelectric field polarized under the externally applied mechanical strain. The transport properties of bulk and edge states of this quantum well device have been investigated by calculating the electron density distribution

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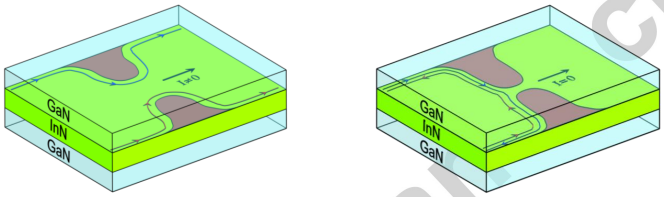
under different widths of the quantum point contact (QPC), which is the origin of more conductance plateaus. In addition, we postulate the mechanical-electronic logic operation mechanisms based on the piezotronics effect adjusting the transport of edge states in the quantum well device. Fundamental logic units such as NOT, NAND and NOR gates have been innovatively designed for performing the logic computation functions from external mechanical stimuli. The logic nanodevices based on the topological insulator have near zero-power consumption and ultrahigh ON/OFF ratio. This work provides a deep insight into the piezotronics effect on the transport of bulk and edge states of the quantum well device, and offers novel solutions to design high-performance low-power mechanical-electronic logic devices.

Graphical Abstract



Logic "1" Logic "0"

Piezotronics effect on topological insulator has been investigated based on GaN/InN/GaN quantum well. High performance piezotronic logic units, such as NOT, NOR and NAND gates can be designed by using GaN/InN/GaN topological insulator.

Keywords: Piezotronics, Topological insulator, Logic nanodevices

1. Introduction

Piezotronics and piezotronics have been important effects existing in the piezoelectric semiconductor materials [1, 2]. Due to the unique coupling characteristics of piezoelectric and semiconductor, carrier transport in these materials can be precisely tuned and controlled by the piezopotential polarized by strain-induced piezoelectric charges[3, 4]. Owing to the high-sensitive characteristics of piezoelectric modulation, various high performance piezotronic

devices have been developed, such as nanogenerators [5-7], strain-gated field effect transistors[8], strain sensors[9] and LEDs[10]. Piezotronics on the quantum devices has attracted extensive interest in conventional piezoelectric materials[11], and the new emerging two-dimensional materials and topological insulators[12]. Enhancing luminescence in monolayer MoS_2 and ZnO has been studied based on the piezotronics effect combined with the quantum effect[13-16].

Topological insulators have become intriguing materials in spintronics and quantum computation regarded as a completely new matter phase recently.[17-19] Topological insulators have the feature of having insulating bulk states and metallic edge states[20, 21], and the electron transport in edge states is immune to the back scattering because of the protection of the time reversal symmetry [20, 22]. Topological spin switch[23-25] and high-performance field effect transistor have been developed based on topological insulators [26, 27]. Furthermore, topological superconductor has been used to find Majorana Fermion, a fundamental particle of physics which can be applied to information storage and quantum computer[19, 28].

Recent studies have shown that the mechanical strain plays an imperative role to induce the topological insulator states in various types of materials, such as GaN/InN/GaN quantum well[29], cubic semiconductor[30], strained bulk HgTe[31] and GaAs film[32]. For the GaN/InN/GaN quantum well, due to the piezoelectric and semiconductor properties of GaN and InN, externally applied strain will induce a polarization field perpendicular to the surface of the InN layer, which will significantly enhance the spin-orbit interaction, giving rise to topological insulator states[29]. Piezotronic effect can change the topological phase of piezoelectric material, and effectively modulate its electron transport leading to promising applications in realizing high performance electronic devices[12]. In this manuscript, we theoretically study the quantum transport of GaN/InN/GaN quantum well to achieve high performance piezotronic devices. A quantum point contact (QPC) is formed as a constriction which can be controlled by strain-induced piezoelectric potential[12]. By comparing electron-density distribution in the quantum well under different QPC widths, the transport behaviors of the bulk and edge states have been illustrated. Strain-induced piezoelectric field can control the QPC width and further modulate the electron transport. Based on the ultrahigh ON/OFF conductance ratio (~ 10^{10}), logic units such as NOT, NAND and NOR gates have been demonstrated according to different connection protocols. Those logic units are stable and robust due to the topologically protected edge states by the time-reversal symmetry[17, 18, 33-35]. HgTe/CdTe topological insulator can be used for designing piezotronic devices, which requires low temperature condition. GaN/InN topological insulator is a suitable candidate that is compatible with the semiconductor technology. By integrating such logic units in circuits, mechanical-electronic logic operations and complex computations can be realized. Such novel strain-gated logic gates have better performances compared with previously reported

piezotronic logic gates[36, 37], such as the ultrahigh ON/OFF ratio and near zero power dissipation. In addition, the conductance sensitivity is also calculated and has the value of approximately 10^5, an advantage in designing highly sensitivity strain sensor.

2. Theoretical Model of GaN/InN/GaN quantum well

A typical quantum point contact (QPC) structure in a small constriction based on the InN quantum well (QW) is illustrated intuitively in Figure 1. A relatively thin strained InN layer is sandwiched between two GaN layers and exhibits inverted bands[29]. A split gate is applied on the side of InN layer. The width of the QPC can be controlled by the voltage applied on the split gate[38]. Figure 1(a) shows a zero-gap band structure in the QPC region in the absence of piezoelectric potential. The gapless edge states are shown by the red line of the band structure and the current can flow across the QPC region without blocking, signaling as the "ON" state. The QPC width decreases with the increase of the applied piezoelectric potential. When the width is narrow enough, the electrons will be blocked and reflected into the opposite boundary owing to the closure of the edge state in QPC region, resulting in the "OFF" state, as shown in Figure 1(b).

The electronic properties in the GaN/InN/GaN quantum well are governed by a six-band Hamiltonian[29]

$$H=\begin{pmatrix} E_0+E_1k_{\|}^2 & A_2k_- & A_1k_+ & 0 & 0 & 0 \\ A_2^*k_- & L_0+L_1k_{\|}^2 & B_1k_+^2 & 0 & 0 & 0 \\ A_1^*k_- & B_1^*k_-^2 & H_0+H_1k_{\|}^2 & 0 & 0 & 0 \\ 0 & 0 & 0 & E_0+E_1k_{\|}^2 & -A_2k_+ & -A_1k_- \\ 0 & 0 & 0 & -A_2^*k_- & L_0+L_1k_{\|}^2 & B_1k_-^2 \\ 0 & 0 & 0 & -A_1^*k_+ & B_1^*k_+^2 & H_0+H_1k_{\|}^2 \end{pmatrix} \quad (1)$$

where $k_{\|}$ denotes the in-plane momentum, $k_{\pm}=k_x\pm ik_y$, $k^2=k_x^2+k_y^2$, and the relevant parameters are $E_0=-46.51$ meV, $E_1=262.71$ meV nm^2, $L_0=3.54$ meV, $L_1=-59.34$ meV nm^2, $H_0=8.4$ meV, $H_1=-29.22$ meV nm^2, $A_1=-32.70$ meV nm, $A_2=-31.68$ meV nm, $B_1=4.62$ meV nm^2 [29].

Various electronic behaviors such as quantum transport and optical absorption, can be obtained via solving the Schrödinger equation with special boundary conditions

$$H\psi=E\psi \quad (2)$$

where ψ is the wave function of the electrons with the energy E. The conductance in InN/GaN quantum well can be given from the Landauer-Büttiker formula [39, 40]

$$G = G_0 \sum_{m,n} |t_{mn}|^2 \tag{3}$$

where $G_0 = 2e^2 / h$ is the conductance unit including the spin degree of freedom, t_{mn} is the transmission coefficient for the electrons scattering from the *m*-th inputting channel to the *n*-th outputting channel. For a uniform strain S applied on the piezoelectric materials, piezoelectric charges are induced and can be calculated from the polarization vector P which is given by[41]

$$(\mathrm{P})_i = (e)_{ijk} (S)_{jk} \tag{4}$$

where e_{ijk} is the piezoelectric tensor. Following the piezoelectric theory, the constituting equations can be written as [42]

$$\begin{cases} \boldsymbol{\sigma} = \mathbf{c}_{\mathbf{E}}\mathbf{S} - \mathbf{e}^T\mathbf{E} \\ \mathbf{D} = e\mathbf{S} + \mathbf{k}\mathbf{E} \end{cases} \tag{5}$$

where $\mathbf{E}$ and $\mathbf{D}$ stand for the electric field and electric displacement vector, $\boldsymbol{\sigma}$ and $\mathbf{c}_{\mathbf{E}}$ stand for the stress and elasticity tensor, and $\mathbf{k}$ stands for the dielectric tensor. Piezoelectric charges can induce piezoelectric field inside the material and produce piezoelectric potential between different surfaces, which can be obtained approximately as

$$V_{\text{piezo}} = \frac{PL_{\text{piezo}}}{\varepsilon_r \varepsilon_0} \tag{6}$$

where P is the polarization vector computed from Eq. (5), L_{piezo} is the length of the piezoelectric material, ε_r and ε_0 are the relative dielectric constant and the vacuum dielectric constant. When the axial strains s_{11}, s_{22}, s_{33} along *x*, *y*, *z* directions are simultaneously applied on the wurtzite structure material, the piezoelectric potential is obtained as

$$V_{\text{piezo}} = \frac{(e_{33}s_{33} + e_{31}s_{11} + e_{31}s_{22})L}{\varepsilon_r \varepsilon_0} \tag{7}$$

where L is the length of the wurtzite structure material.

To compute the transport characteristics of the electrons in InN quantum well, we adopt the free tight-binding package KWANT which is implemented by using the wave function approach[40]. It has been verified that this approach is mathematically equivalent to the commonly used nonequilibrium Green's function (NEGF)[41]. The left and right lead together with a scattering region should be constructed according to the specific geometry of the given system. Concretely, the width of quantum well *W* is set at 60 nm with the lattice constant *a*=1 nm. The scattering region is constructed according to the ref. 23 with the parameters L_x=20

nm and L_{QPC}=40 nm. Before implementing KWANT, the onsite energy for each cubic lattices and hopping energy between its neighbors should be given by discretizing the $k\ p$ Hamiltonian in Eq. (1). The scattering matrix and wave function are the two typical outputs from KWANT for further calculating the conductance and electron density distribution using Landauer-Buttiker formalism[36, 37].

3. Results and discussions

3.1 Transport property of the bulk states

Bulk states are very common in the transport behaviors of nanosystems, including universal conduction bands and valence bands. In this study, the conduction bands of the topological insulator are taken as a typical example to illustrate the transport property of the bulk states.

Figure 2(a) shows the band structures of the InN quantum well in the lead region and its enlargement in the conduction bands. When the Fermi energy is set at 10 meV, there are six bands crossing this energy level, giving rise to the emergence of six bulk states (channels). Because of the width-dependent topological state in the QPC region, the incoming six bulk states from left lead will be strongly scattered by the QPC. Figures 2(b)-(d) show the electron-density distribution in quantum well when those six bulk states are injected from the left lead for the QPC width of 5 nm, 20 nm and 30 nm, respectively. For the narrow QPC width, all the electrons are blocked and the electrical current is nearly zero, as shown in Figure 2(b). When the width increases to 20 nm shown in Figure 2(c), the first four bulk states are opened at the QPC region, thus electrons can travel through the QPC. Further increasing the QPC width, more bulk channels in QPC region are opened. Figure 2(d) shows the presence of the five bulk channels passing through QPC under the width of 30 nm. In fact, the increase of the number of the opening channels results in the presence of conductance plateaus.

3.2 Transport property of the edge states

Owing to the width-dependent electron transport in bulk state, edge states will also be influenced. Figure 3(a) shows the conductance as a function of the QPC width under different Fermi energies of 0 meV, 5 meV and 10 meV. The conductance plateaus are presented clearly at the Fermi energy of 0 meV and 10 meV, corresponding to the transport of the bulk states. For the Fermi energy of 5 meV, there is only one conductance plateau for large QPC widths, corresponding to the electron transport of the edge states. Figures 3(b) – (d) show the electron-density distribution of edge states under the QPC width of 5 nm, 9 nm, 15 nm, respectively. When the width is narrow, the electrons are completely blocked and the

conductance is zero, as shown in Figure 3(b). The electrons can pass through the QPC nearly without blocking under $W_{QPC} = 9$ nm, leading to the conductance G_0. When the QPC width $W_{QPC} = 15$ nm, electrons can partially travel through the system, resulting in the conductance $0 < G < G_0$.

The electron transport shows the evidence of the edge state while Fermi energy is 5 meV. Because the electron transports display the property of the bulk states under the Fermi energy of 0 and 10 meV, these two electron transport properties are similar. The case of Fermi energy 10 meV corresponds to bulk states in the conduction band, as shown in Figure 1(a), and bulk states in the valence band for Fermi energy 0 meV.

3.3 Piezotronics effect on the topological insulator

Previous results suggested that the topological phase of HgTe quantum well, a typical topological insulator, heavily depends on the width of quantum spin Hall bar [23-25]. Generally, tuning QPC is an effective method to control the width of quantum well, which can be controlled by the split gates. By using the molecular beam epitaxy technology, the split gates are able to broaden or shrink the extension of the depletion region depending on the applied voltage[38]. Figure 4(a) shows the schematic of using strain-induced piezoelectric potential to turn the topological property of the quantum well and further modulate the electron transport. Piezoelectric potential produced in wurtzite materials is provided to the left and right split gates aiming at adjusting the QPC width. The applied piezoelectric material is in the form of wurtzite structure such as ZnO, GaN, ZnS and BN, which is synthesized on the substrate of the GaN/InN/GaN quantum well. The piezoelectric coefficient e_{33} and relative dielectric constant ε_r are listed in Table 1.

Figure 4(b) shows the piezoelectric potential as a function of the externally applied strain for various piezoelectric materials. It clearly shows the linear dependence between the piezoelectric potential and strain.

Previous experimental results suggested that the width of QPC can be controlled by split-gate voltage, exhibiting an approximately linear relation [38]. The applied voltage is supplied by the strain-induced piezoelectric potential and thus has the following relationship

$$W_{QPC} = \alpha\left(V_{piezo} + V_0\right) + W_0 \tag{8}$$

where α is the parameter depending on the material, V_0 is the voltage drop between the left and right split gate, W_0 is the initial width of the QPC without applying piezoelectric potential. The relevant parameters used in the calculation are $\alpha = 225\ \text{nm}\cdot\text{V}^{-1}$, $V_0 = 1.93\ \text{V}$, $W_0 = 60$

nm [38].

Figure 4(c) shows the QPC width W_{QPC} varying with strain s_{33} for different materials. A distinctive linear dependence is presented at the narrow strain region. Away from this linear region, the QPC width is unchanged. Figure 4(d) calculates the conductance as a function of strain. In the calculation, the Fermi energy is fixed at 5 meV which corresponds to the edge state, as illustrated in Figure 3(a). There is an abrupt transition between zero conductance and G_0, indicating sharp switch behaviors. The zero conductance is the OFF state and G_0 conductance corresponds to the ON state. The ON/OFF conductance ratio is calculated over 10^{10}. The critical transiting point between ON and OFF state are -0.11%, -0.46%, -1.32% and 0.09% for ZnO, GaN, ZnS and BN, respectively. Because the edge state is immune to the backscattering, the transport of edge state theoretically has no power dissipation, meaning that this type of strain-gated switches consumes very little power. Owing to this excellent performance, piezotronic transistors have been proposed by using HgTe topological insulators[12].

3.4 Piezotronic logic gates based on InN topological insulators

Due to the high-performance and low-power consumption characteristics of strain switches based on InN topological insulators, these novel devices can be used to design logic gate circuits, as shown in Figure 5. The negative strain is compressive strain and positive strain is tensile strain. We define logic "1" when the external strain is larger than 0.46% and logic "0" when the external strain is smaller than the critical value strain. Figure 5(a) exhibits the NOT gate and its truth table. The piezoelectric material is chosen as GaN. When the external strain is smaller than the critical transiting point -0.46%, the input strain is defined as "1", but "0" for the strain larger than -0.46%. The output signal is "1" in the presence of electrical current and "0" in the absence of electrical current. By integrating two strain-gated switches in parallel connection, the logic operation of strain-gated NAND gate can be realized in Figure 5(b). When A and B input terminals have the input strain 0, the output will be 1 due to the NOT operation of single strain-gated switch. The output will be 0 only if the input strain A and B are both 1, as displayed in the truth table. Figure 5(d) shows the logic operation of strain-gated NOR gate by connecting two strain-gated switches in series. If there exists the input strain 1 in A and B terminals, the output will be 0. The output will be 1 when both of the A and B input strains are 0. In comparison with the piezotronic logic gates based on the stain-gated transistor (SGT) where the output is the voltage and a critical value should be assumed due to the poor switch behaviors, logic gates using topological insulators are benefiting from the transport of the edge states, possessing the excellent switch behavior and low-power

consumption characteristics, which is deemed to be a promising candidate for the future flexible electronics.

3.5 Piezotronics strain sensor based on InN topological insulator

Strain sensors can be realized using the InN topological insulators. The conductance sensitivity of the strain sensor can be expressed as follow

$$R = \frac{d\left(G / G_0\right)}{ds_{33}} \tag{9}$$

Figure 6(a) shows the conductance sensitivity R as a function of strain s_{33} for different piezoelectric materials. The Fermi energy is fixed at 10 meV. For each material, there exists a narrow strain sensing region where the sensitivity is very high. Away from this high sensitivity region, the sensitivity is almost zero, corresponding to the switch region. The maximum values of the conductance sensitivity are shown in Figure 6(b). The amplitude of the maximum sensitivity is over 10^4. For ZnS and BN, this maximum value can reach up to 10^5, indicating a ultrahigh sensitivity strain sensor. Ultrahigh sensitivity strain sensors usually show very small sensing ranges [43]. In practical applications, ultrahigh sensitivity piezotronic strain sensors with very small sensing ranges can be used for designing piezotronic analog-to-digital converter devices for strain imaging and analog computing [37].

4. Summary

In this paper, we focus on investigation of the electron transport properties in the GaN/InN/GaN quantum well. This structure can exhibit topological insulating states under the presence of strain-induced piezoelectrically polarized field, named as the piezotronic topological insulator. The transport characteristics of the bulk and edge states can be significantly affected by the QPC width. By calculating the electron-density distribution, the emergence of the more conductance plateaus is attributed to the increase of the number of the opening bulk channels in QPC region. Three typical electron transports for edge states, i.e. full OFF state, full ON state and partial ON state have been studied. Piezotronic logic components such as NOT, NAND and NOR gates are demonstrated by applying the strain-induced piezoelectric potential on the QPC, which can be used to realize logic computing of mechanical signals. Because such logic gates are based on the electron transport of the edge states and have the ultrahigh ON/OFF ratio (over 10^{10}), this novel strain-gated logic devices are featured by high-performance and low-power consumption properties, which presents great advantages over the piezotronic logic devices based on SGTs. Moreover, the

conductance sensitivity has been analyzed for the structure used as a high sensitivity strain sensor.

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Competing interests

The authors declare no competing interests.

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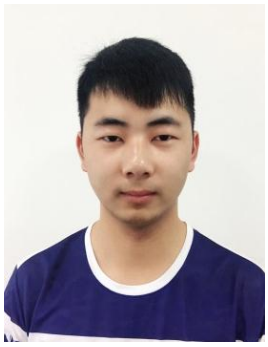

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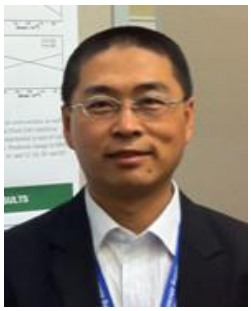

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Figure 1. Schematics of spin-dependent electrons transport and energy bands under different QPC widths in the GaN/InN/GaN quantum well. The spin-up (blue line) and spin-down (red line) electrons travel along boundary. (a) gapless for the wide QPC (the red lines in band structure are edge states) and (b) gap for the narrow QPC.

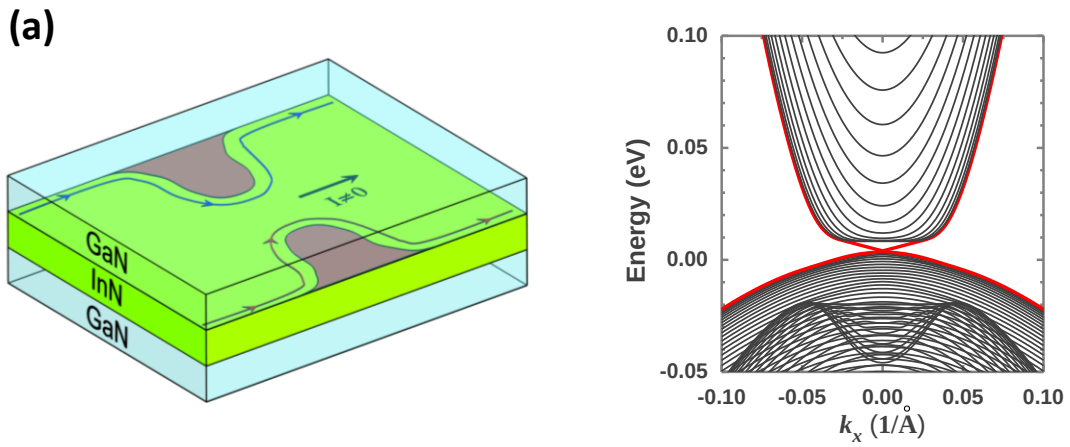
Figure 2. The bulk channels contributing to the more conductance plateaus. (a) Band structure of the lead and its enlargement. When the electron energy is fixed at 10 meV, six bulk channels in the conduction band will be opened. (b), (c) and (d) are the electrons density distribution of six bulk channels at the QPC width W_{QPC}=5 nm, 20 nm and 30 nm, respectively.

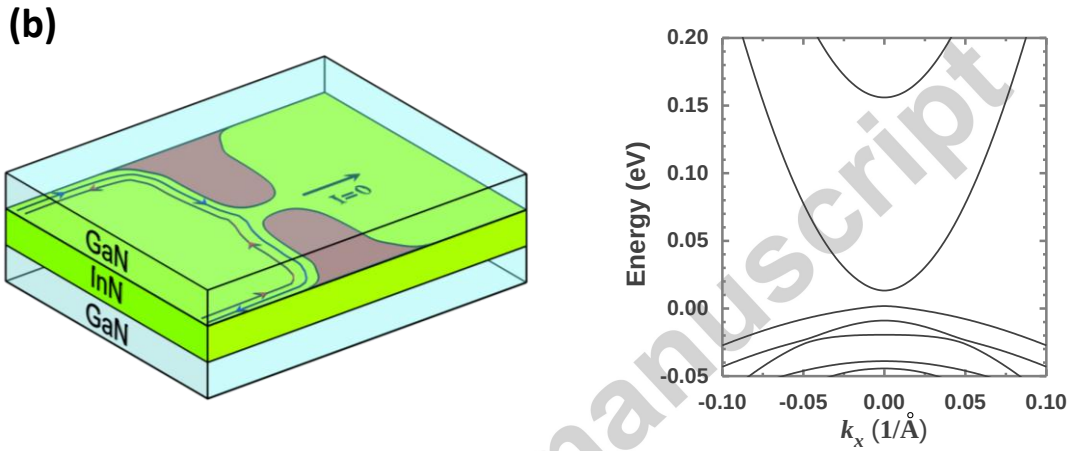
Figure 3. (a) The conductance plateaus varying with the strain under different electrons energy levels. The piezoelectric material is designated as ZnO. Electrons density distribution under different QPC widths. (b) full off state at W_{QPC}= 5 nm, (c) full on state at W_{QPC}= 9 nm and (d) on state with partial reflection at W_{QPC}= 15 nm. The electron energy is fixed at 5 meV.

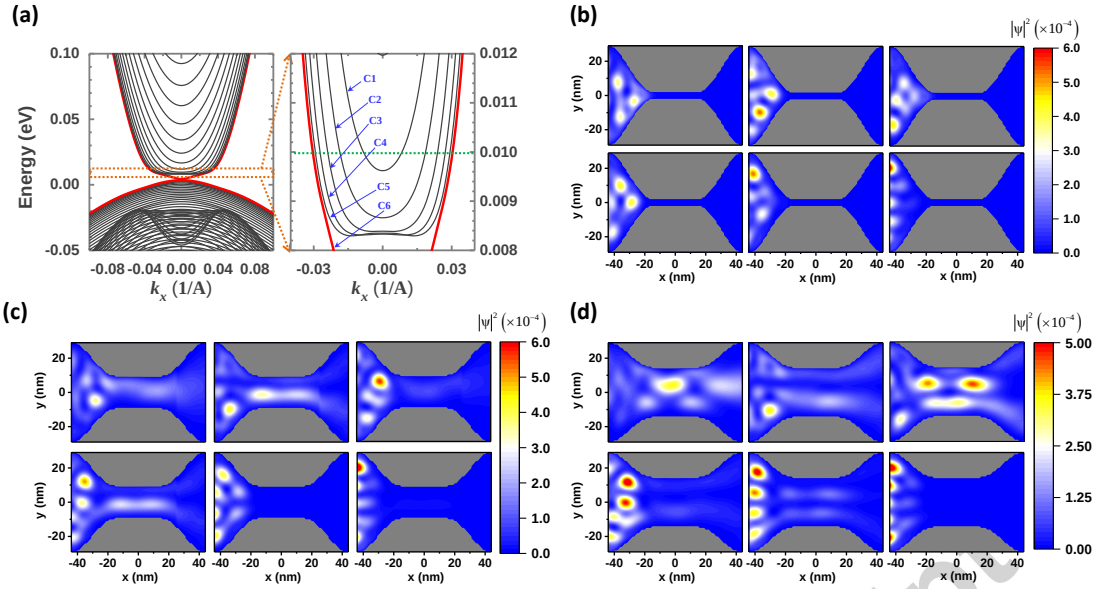
Figure 4. (a) The structure of the piezotronic transistor. The QPC region is formed via two split gates acting on the top GaN layer. (b) Piezoelectric potential against the externally applied strain for different piezoelectric materials. (c) The QPC width as a function of strain. (d) The transporting conductance versus strain.

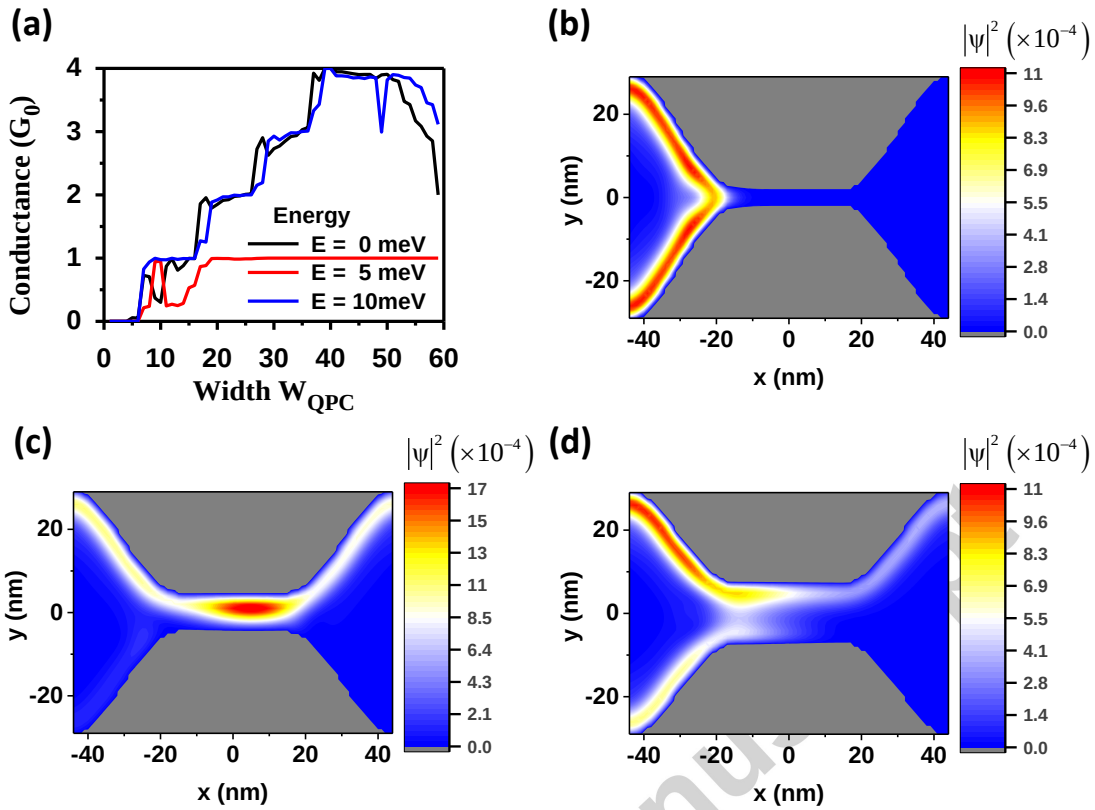
Figure 5. Logic gates and the corresponding truth tables based on the InN topological insulator. (a) NOT gate, (b) NAND gate and (c) NOR gate. The piezoelectric material is GaN and the Fermi energy is fixed at 5 meV. The critical transiting point between zero conductance and G_0 corresponds to the strain -0.46%. The input strain is labeled as 0 for the strain of -0.6% and 1 for the strain of -0.3%.

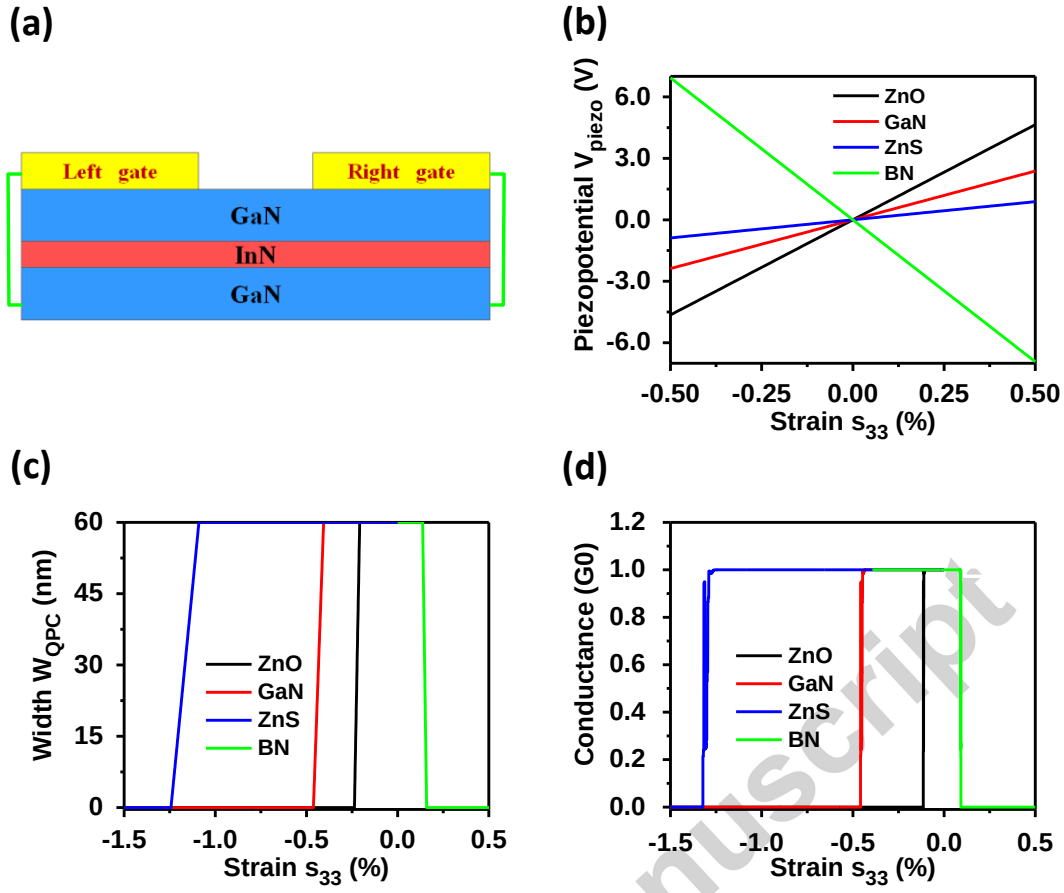
Figure 6. (a) The conductance sensitivity changing with strain under different piezoelectric materials and (b) the maximum value of the sensitivity. The Fermi energy is set at 5 meV.



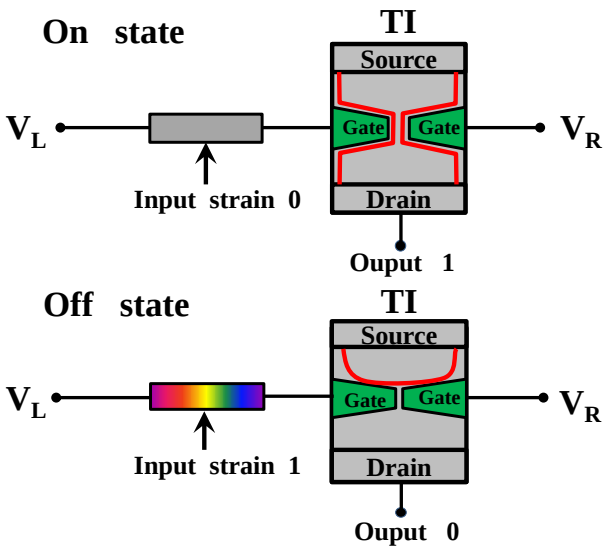






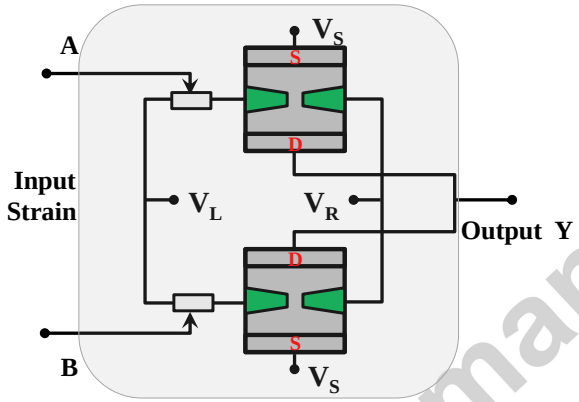


(a)



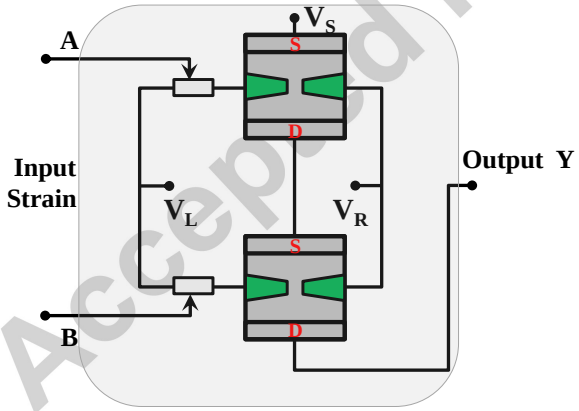
Input Strain	Output
0	1
1	0

(b)



Input Strain		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(c)



Input Strain		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

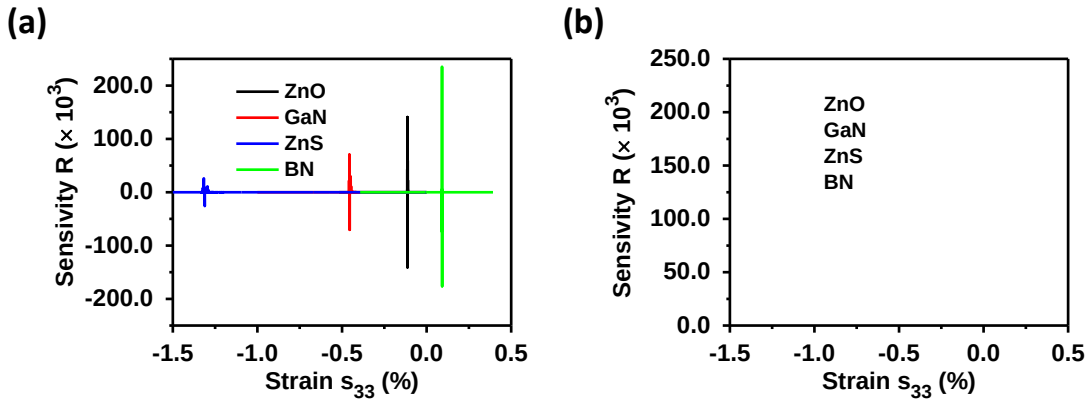


Table 1. Piezoelectric Coefficients and Relative Dielectric Constants for wurtzite structure materials.

material	ZnO[3]	GaN[44]	ZnS[45, 46]	BN[47, 48]
piezoelectric coefficient e_{33} (C/m^2)	1.20	0.65	0.18	-0.85
relative dielectric constant, ε_r	8.9	10.4	6.9	4.16

Highlights:

- Piezotronic logic circuits are designed based on the GaN/InN/GaN topological insulator.
- GaN/InN/GaN topological insulator is a suitable candidate for integrated circuits.
- Topological insulators provide a new way for developing high performance piezotronic transistors.