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FinFET Versus Gate-All-Around Nanowire FET: Performance, Scaling, and Variability

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ABSTRACT Performance, scalability, and resilience to variability of Si SOI FinFETs and gate-all-around (GAA) nanowires (NWs) are studied using in-house-built 3-D simulation tools. Two experimentally based devices, a 25-nm gate length FinFET and a 22-nm GAA NW are modeled and then scaled down to 10.7- and 10-nm gate lengths, respectively. A TiN metal gate work-function granularity (MGG) and line edge roughness (LER) induced variability affecting OFF and ON characteristics are investigated and compared. In the OFF-region, the FinFETs have over an order of magnitude larger OFF-current that those of the equivalent GAA NWs. In the ON-region, the 25/10.7-nm gate length FinFETs deliver 20/58% larger ON-current than the 22/10-nm gate length GAA NWs. The FinFETs are more resilient to the MGG and LER variability in the subthreshold compared to the GAA NWs. However, the MGG ON-current variability is larger for the 10.7-nm FinFET than that for the 10-nm GAA NW. The LER ON-current variability depends largely on the RMS height; whereas a 0.6-nm RMS height yields a similar variability for both FinFETs and GAA NWs. Finally, the industry preferred ⟨110⟩ channel orientation is more resilient to the MGG and LER variability in both architectures.

INDEX TERMS Drift-diffusion (DD), Monte Carlo (MC) simulations, density gradient (DG) quantum corrections, Schrödinger equation based quantum corrections, Si FinFET, gate-all-around (GAA) nanowire (NW) FET, metal grain granularity (MGG), line edge roughness (LER).

I. INTRODUCTION

Fin field-effect transistors (FinFETs) are the preferred device architecture for mass production beyond the 32 nm technology node [1], [2] because they offer superior electrostatic control of the channel over planar metal-oxide semiconductor FETs (MOSFETs) [2], [3]. However, further scaling of the transistors is a cumbersome task requiring novel architectures [4]. Gate-all-around (GAA) nanowire (NW) FETs are promising candidates to replace the FinFETs for future technology nodes due to a better control of the channel transport via fully surrounding gate [5]. Therefore, detailed physical investigation of the available technologies is of great importance for future solutions. Further challenges emerge during fabrication processes in the next technology nodes. The impact of process variations has become a crucial issue to device design [6] that could impair device performance. The main variability sources affecting the device reliability are: random dopants (RD), oxide thickness variation (OTV), interface trap charges (ITC), metal gate work-function granularity (MGG) and line edge roughness (LER) [7]–[13].

Computer-aided-design tools can reduce both the cost and the development time of these novel device architectures [14]. The classical drift-diffusion method assisted by quantum corrections when properly calibrated is a very efficient way of running thousands of simulations and determine

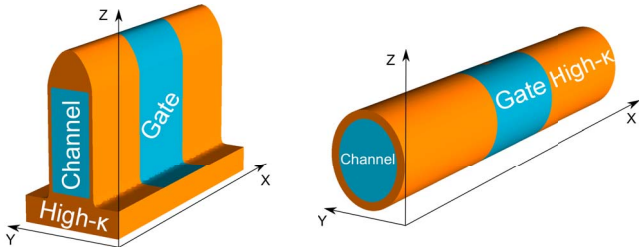

FIGURE 1. Schematics of the simulated (a) FinFETs with a rectangular channel shape and (b) GAA NWs with an elliptical channel shape.

device performance. However, at ON-current conditions the carrier transport at nanoscale becomes i) highly non-equilibrium and ii) strongly affected by quantum-mechanical phenomena. Then a quantum corrected ensemble Monte Carlo technique is a more optimal choice [15], [16]. Additionally, the accurate description of 3D device shapes is of equal importance for accurate device simulations at the nanoscale. That description can be achieved using a finite element (FE) approach [17].

In this paper, we present a comparison of the performance, scaling and variability of realistic silicon based FinFETs and GAA NWs. We start with a FinFET and a GAA NW designed for the 16/14 nm CMOS technology when our simulations of I-V characteristics [15], [18] can be compared with experimental data [19], [20], respectively. We then scale these two architectures to dimensions foreseen for the 5 nm Si CMOS technology [21]. The paper is structured as follows. In Section II, the studied devices and simulation models are described. In Section III, a comparison study of the performance between the FinFET and the GAA NW are presented. Two major variability sources for the FinFET and GAA NW, MGG and LER, are studied in Sections IV and V for the OFF- and ON-regions of the device operation, respectively.

II. DEVICE DESCRIPTION AND SIMULATION APPROACH

The multi-gate device structures used in this paper are created following published experimental data. In Fig. 1, transistor schematics are shown for the 25 nm gate length FinFET (a) from [19] and the 22 nm gate length GAA NW (b) from [20]. After validation of the simulated I-V characteristics against experimental data [15], [18], we have scaled down both devices following the ITRS guidelines [22]. The device dimensions for the experimental and scaled devices are summarised in Table 2. Note that when both devices are scaled the maximum doping concentration in the source/drain regions are kept constant and the Gaussian profile is scaled with the same ratio as the gate length. The complex features of multi-gate transistors, such as the rounded corners seen in Fig. 1, are critical for accurate simulations in the deep nano-regime [23]. An excellent method to achieve a detailed description of the aforementioned device mesh is the 3D finite element (FE) method [17].

Our analysis is carried out using an in-house FE simulator toolbox with capabilities of quantum corrected drift-diffusion (DD) and Monte Carlo (MC) techniques [17]. The DD model is preferred for the simulation of the sub-threshold region due to time efficiency and because the particle based MC method can be noisy at very small currents. The DD simulations are also used to provide an initial solution for the MC to reduce the overall simulation time. In the ON-region of the devices, a non-equilibrium carrier transport dominates, leading to effects like the velocity overshoot, that the DD approach is not able to capture. Therefore, the MC method is used there. The MC engine accounts for all Si related electron scattering mechanisms, acoustic and non–polar optical phonon (intra- and inter-valley) [24], [25], ionised impurity scattering using the third body exclusion by Ridley [26] and de Roer and Widdershoven [27], and interface roughness (IR) scattering using Ando's model [28]. The electron screening in the electron-ionised impurity scattering is using a static screening model [29] obtained using Fermi-Dirac statistic with a self-consistently calculated Fermi energy and electron temperature in a real space of device simulation domain. At the nanoscale regime, quantum mechanics play a significant role that requires the inclusion of some kind of quantum correction model. Consequently, a density-gradient (DG) approach is used with the DD simulations [30]. However, this method requires a calibration against experimental data or quantum mechanical simulations, for example, a Non-Equilibrium Green's function (NEGF) [31] or a Poisson-Schrödinger solver [32]. The DD simulations employ the Caughey and Thomas [33] doping dependent low-field electron mobility model, together with lateral and perpendicular electric field models [34]. We use electron effective masses as calibration parameters in the DG QCs to mimic the source-to-drain tunneling and quantum confinement effects [18]. Table 1 lists the relevant calibration parameters in the DD simulations. Note that the quantum corrected DD simulations are only used for a study of the sub-threshold region. Therefore, Schrödinger equation based quantum corrections were implemented in the 3D FE MC simulation toolbox to allow calibration free simulations. More detailed description of the simulation toolbox is available in [15], [17], and [35].

As aforementioned, devices in a deep nano-scale regime exhibit an increased effect of different variability sources. Therefore, in this paper, we also consider two major sources of device variability, the MGG and LER [8]. For the MGG, randomly generated metal gate profiles are created, which are then mapped onto the gate and fed to the simulation toolbox. To create the profiles, we use the Poisson-Voronoi diagrams approach that mimics the "formation" of metal grains with various shapes and sizes, just like in realistic metal gates [36]. Such method is thought to be more accurate than the square grains approach [37], [38], especially as the size of the gate decreases and the grain size (GS) dimensions become comparable to the gate length. The metal gate material is titanium nitride (TiN) that is considered

TABLE 1. Calibration parameters for the 25/10.7 nm gate length Si FinFET and the 22/10 nm gate length Si GAA NW FETs: saturation velocity (v_{sat}), perpendicular critical electric field (E_{CN}) and the DG electron mass in the transport direction (m_x).

L_G	25 nm		10.7 nm		22 nm		10 nm	
V_D	0.05 V	1.0 V	0.05 V	0.7 V	0.05 V	1.0 V	0.05 V	0.7 V
v_{sat} [cm/s]	$1.0x10^7$	$1.0x10^7$	$1.0x10^9$	$1.0x10^9$	$1.0x10^9$	$1.0x10^9$	$1.0x10^9$	$1.0x10^9$
E_{CN} [cm^2/Vs]	$6.5x10^4$	$6.5x10^4$	$1.0x10^9$	$5.0x10^4$	$4.0x10^6$	$1.3x10^5$	$1.0x10^7$	$2.5x10^5$
m_x [m_0]	0.32	0.32	0.32	0.25	0.4	0.32	0.4	0.25

TABLE 2. Device dimensions and parameters: supply voltage (V_{DD}), physical gate length (L_G), physical source/drain length ($L_{S/D}$), channel width/height (W_{ch}, H_{ch}), effective oxide thickness (EOT), the standard deviation for Gaussian doping in the source/drain (σ_x), doping concentrations for channel (N_{ch}), source/drain ($N_{S/D}$) regions and effective perimeter of the gate for the simulated multi-gate Si transistors.

Symbol	FinFET		GAA NW	
	25 nm	10.7 nm	22 nm	10 nm
$V_{DD,lin}$ [V]	0.05	0.05	0.05	0.05
$V_{DD,sat}$ [V]	1.0	0.7	1.0	0.7
L_G [nm]	25	10.7	22	10
$L_{S/D}$ [nm]	25	10.7	30.8	14
W_{CH} [nm]	12	5.8	11.3	5.7
H_{CH} [nm]	30	15	14.22	7.17
EOT [nm]	1.12	0.62	1.5	0.8
σ_x [nm]	8.07	3.45	7.1	3.23
N_{CH} [cm^{-3}] ($\times 10^{15}$)	1	1	1	1
$N_{S/D}$ [cm^{-3}] ($\times 10^{20}$)	1	1	0.5	0.5
Perimeter [nm]	72	35.8	40.21	20.29

as one of the most promising gate material for multi-gate transistors [39]. The TiN has experimentally observed work functions of 4.6 eV and 4.4 eV with probability of 60% and 40% formation, respectively [40]. These values are used for a random profile generation. More detailed information on the implementation of the MGG profile generation can be found in [36].

In case of the LER variability, we use an uncorrelated profile along the transport direction that introduces variation in the width of the device. In order to achieve this, we have used Fourier synthesis with Gaussian autocorrelation [41] as described in [16] and [42]. The generation of the LER profiles is based on the inverse discrete Fourier transformation and the application of a Gaussian filter over a list of random phases. The characteristics of the LER profiles are based on a correlation length (CL) that is set by the width of Gaussian filter, and a root mean square (RMS) value that is set by the amplitude. Fourier spectra are modelled using the following autocorrelation function:

$$S_G(\mathbf{k}) = \sqrt[2]{\pi}\Delta^2\Lambda e^{(-k^2\Lambda^2/4)} \quad (1)$$

where Λ is the CL, and Δ is the RMS height. The study for the LER is limited to a correlation length of 20 nm, because it was shown that it affects the devices the most [8], [16], with different RMS heights, ranging between 0.6 and 1.0 nm, that were chosen to represent the RMS values observed in experiments [11], [20].

III. PERFORMANCE EVALUATION AND SCALING

Figs. 2 and 3 show simulated I_D-V_G characteristics of the 25 nm gate length FinFET [15] and the 22 nm GAA NW [18] compared with experimental data from [19] and [20], respectively. The normalised drain current (current per unit length) is obtained by dividing the drain current by the channel-covered periphery. For the FinFET the channel-covered periphery is twice the fin height plus the fin width and for the GAA NW is the circumference of the elliptic channel. The results are for both low (0.05 V) and high (1.0 V) drain biases with a channel orientation of ⟨110⟩, because that is the preferred orientation for manufacturing. Note that at a low drain bias of 50 mV and at gate biases greater than 0.4 V the simulated results start to diverge from the experimental data (see Fig. 2). This over-estimation is related to the quantum corrections that mimic the shift of the lowest bound state with respect to the conduction band edge [15]. At low drain bias, the weak quantum confinement caused by the dimensions of the fin results in energy levels that are closely placed together. Nonetheless, as the gate bias increases quantum wells will emerge at the sidewalls of the devices, inducing a strong confinement and a separation of the energy levels. Since the transport happens in the sub-bands our simulator is not able to properly capture this because it only includes the confinement through an effective quantum potential. Note that, for this reason, the results at a low drain bias from the MC simulations are not used for any of the performance comparisons or variability studies. However, at a high drain bias, the 3D MC simulations for both devices were able to accurately reproduce the experimental results without any need for post-processing of access resistance or a change in any of the material bulk parameters [43]. This is because for larger drain biases, the quantum confinement is reduced and the energy of electrons is larger. Therefore, the transport occurs where the sub-bands are energetically closely packed together and becomes quasi-3D. Note also that the 3D DD simulations have an excellent match in the sub-threshold region at both low and high drain biases with the experimental results. Therefore, we are confident that the DD simulations can very well reproduce transport in the sub-threshold region.

Figs. 4 and 5 show I_D-V_G characteristics for the 10.7 nm FinFET and 10 nm GAA NW at both low (0.05 V) and high (0.7 V) drain biases with channel orientations of ⟨100⟩ and ⟨110⟩.

Figure of merits for two multi-gate transistor architectures are summarised in Table 3 where the model refers to the

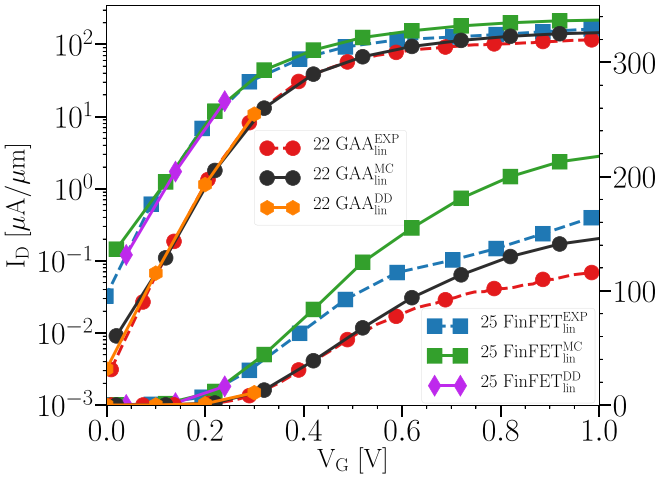

FIGURE 2. Experimental (EXP) I_D-V_G characteristics at a V_D of 0.05 V (lin) for the 25 nm gate length FinFET [19], the 22 nm GAA NW [20], and the related 3D drift-diffusion (DD) and Monte Carlo (MC) simulations. The experimental and MC simulated devices have a channel orientation of ⟨110⟩.

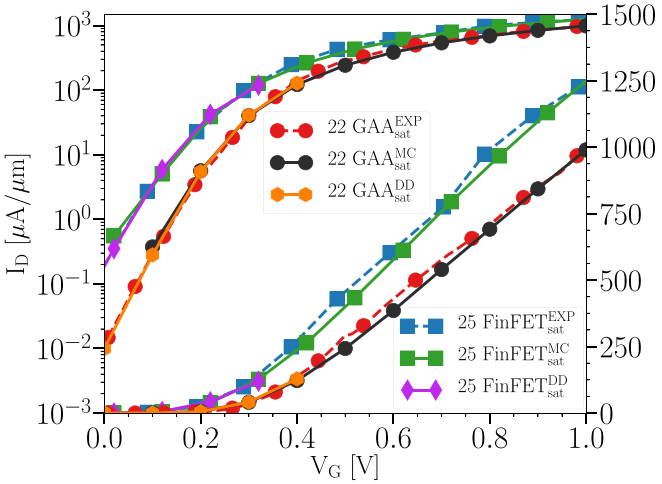

FIGURE 3. Experimental (EXP) I_D-V_G characteristics at a V_D of 1.0 V (sat) for the 25 nm gate length FinFET [19], the 22 nm GAA NW [20], and the related 3D drift-diffusion (DD) and Monte Carlo (MC) simulations. The experimental and MC simulated devices have a channel orientation of ⟨110⟩.

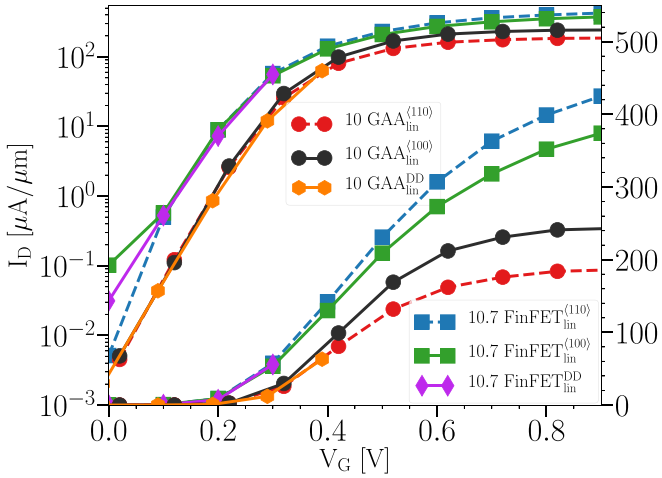

FIGURE 4. Simulated I_D-V_G characteristics for the 10.7 nm gate length FinFET [17] and the 10 nm gate length GAA NW [18] at V_D = 0.05 V (lin) and with channel orientations of ⟨100⟩ and ⟨110⟩.

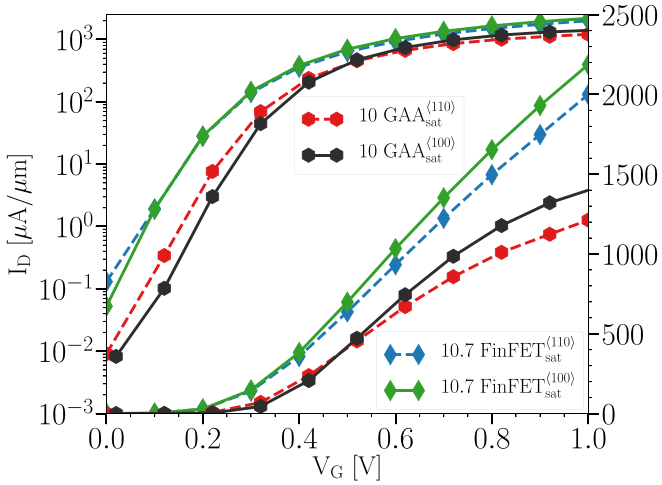

FIGURE 5. Simulated I_D-V_G characteristics for the 10.7 nm gate length FinFET [17] and the 10 nm gate length GAA NW [18] at V_D = 0.7 V (sat) and with channel crystal orientations of ⟨100⟩ and ⟨110⟩.

simulation method. The extraction of the OFF-current (I_{OFF}) is done at a gate bias (V_G) of 0.0 V and the drive current (I_{ON}) at $V_G = V_D + V_T$.

After scaling the 25 nm gate length FinFET to 10.7 nm, we have found that the V_T and sub-threshold slope (SS) experience a minimal change which suggests a good control from the gate, however, the DIBL is increased by 28%. Both the OFF- and ON-currents are improved for the 10.7 nm gate length FinFET. The I_{OFF} is reduced by 21% and the I_{ON} is increased by 9% and 16% for the ⟨100⟩ and ⟨110⟩ channel orientations, respectively. The reduction of the OFF-current also leads to a 45% reduced power consumption for the 10.7 nm FinFET. Finally, the ON/OFF ratio is increased by about 37% and 46% for the ⟨100⟩ and ⟨110⟩ channel orientations, respectively, when the FinFET is scaled down.

Following a similar comparison of the GAA NW, we found that the V_T and SS have also a small change and the DIBL increases by 37% for the 10 nm gate length FET. In case of the I_{OFF}, we observed a 10% reduction of the current which leads to a 37% reduction of the static power for the 10 nm GAA NW. The I_{ON} is decreased by 14% and 12% for the ⟨100⟩ and ⟨110⟩ channel orientations, respectively. Therefore, the comparison of the ON/OFF ratios shows some deterioration for the 10 nm GAA NW when compared to the larger gate length device. The ratio deterioration of the 10 nm GAA NW is caused by the decrease in the ON-current even though the I_{OFF} improves. The saturation of the I_{ON}, seen in Fig. 5, is related to the maximum doping level (see Table 2), thus an increased doping would eliminate the saturation and

TABLE 3. Figure of merits for FinFET and GAA NW architectures: threshold voltage (V_T), sub-threshold slope (SS), drain-induced barrier lowering (DIBL), OFF-current (I_{OFF}), ON-current (I_{ON}), static power (P_{Static}) and the ON/OFF ratio (I_{ON}/I_{OFF}).

Model	FoM	FinFET		GAA NW	
		25 nm	10.7 nm	22 nm	10 nm
MC	V_{Tsat} [V]	0.24	0.24	0.26	0.26
DD	SS_{sat} [mV/dec]	77	76	70	68
DD	DIBL [mV/V]	60	77	57	78
DD	I_{OFFsat} [nA/μm]	188	149	9.9	8.9
MC	$I_{ON}^{\langle 100\rangle}$ [μA/μm]	1860	2030	1590	1360
MC	$I_{ON}^{\langle 110\rangle}$ [μA/μm]	1600	1850	1330	1170
MC/DD	P_{Static} [μW/μm]	188	104	9.9	6.2
MC/DD	$\frac{I_{ON}}{I_{OFF}}(\times 10^4)$ $\langle 100\rangle$	0.99	1.36	16	15.3
MC/DD	$\frac{I_{ON}}{I_{OFF}}(\times 10^4)$ $\langle 110\rangle$	0.85	1.24	13.4	13.1

lead to an increased drive current for the 10 nm gate length GAA NW.

We observed that the 25 and 10.7 nm gate length FinFETs are outperformed by the GAA NWs (22 and 10 nm gate lengths) for the sub-threshold region figures of merit. In case of the SS, the GAA NW has a 9% lower value and more than an order of magnitude smaller OFF-current which also results in over an order of magnitude lower static power. This is achieved due to the better electrostatic control by the surrounding gate of the NW. Finally, notice that the larger V_T of the GAA NW is related to the thicker EOT (see Table 2).

With respect to the ON-region, the FinFET outperforms the GAA NW for both gate lengths. In case of the 25 nm FinFET, the I_{ON} is 20% greater than that of the 22 nm GAA NW for a channel orientation of $\langle 110\rangle$, which increases to 58% for the 10.7/10 nm gate length devices. However, the ON/OFF ratios of the GAA NW for the 10 nm gate length are still more than an order of magnitude larger than those of the 10.7 nm FinFET devices.

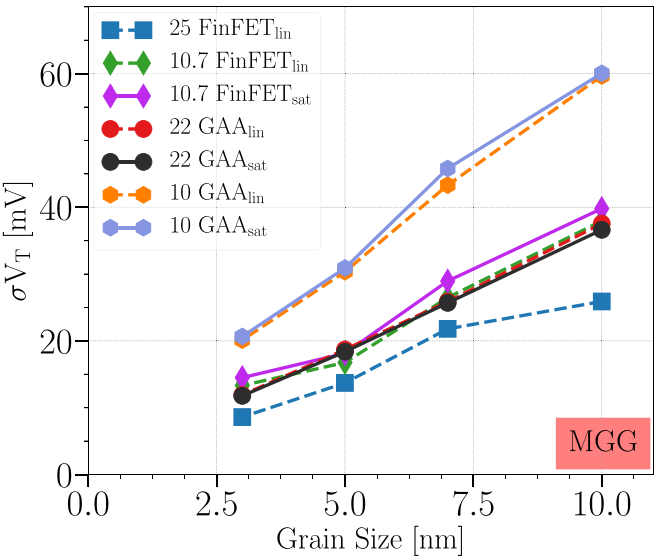

FIGURE 6. Comparison of the standard deviation (σ) of V_T induced by the MGG variability for the 25 nm [42] and 10.7 nm [8] gate length FinFETs, and for the 22 and 10 nm gate length GAA NWs. The respective drain biases are shown in Table 2. The subscript 'lin' refers to a low and 'sat' refers to a high drain bias, respectively.

IV. MGG AND LER VARIABILITY IN THE SUB-THRESHOLD REGION

In this section, we analyse the effect of two major sources of variability, MGG and LER, in the sub-threshold region. To obtain accurate prediction of the variability, we have generated 300 random profiles for each GS and RMS height. Fig. 6 shows the standard deviation (σ) of the threshold voltage (V_T) due to MGG variability for the FinFET and GAA NW. For both architectures, the drain bias has a negligible effect on the σV_T and also, as expected, the variability decreases when the grain size is reduced.

The scaling of the FinFET from the 25 nm to the 10.7 nm gate length increases the MGG variations by 47% for the 10 nm GS. Similarly, σV_T is increased by about 59% at a GS of 10 nm when the GAA NW is scaled down. Note that σV_T is more sensitive to the change of the GS for the 10 nm gate length GAA NW (a slope of 5.6 mV/nm) than for the 22 nm gate length (a slope of 3.7 mV/nm). Generally, the larger the gate, the lower the slope and the magnitude of the MGG variability.

Overall, the linear behaviour that is observed for the σV_T as a function GS is also demonstrated in [9]. However, as the GS becomes comparable to the gate area, this linear trend is likely to change. Moreover, the FinFET is more resilient to the MGG variability in the sub-threshold region than the GAA NW, at both gate lengths. This is due to the fact that the FinFET, unlike the GAA NW, is controlled by the sidewall gates, which leads to less variability of the V_T, that was demonstrated in [44]. The 10 nm FinFET has a 36% smaller V_T variability with a GS of 10 nm than the NW at a low drain bias.

Fig. 7 shows the V_T variability due to the LER. The 25 nm FinFET has a three times lower σV_T than the scaled 10.7 nm FinFET (for the 25 nm FinFET, the only available

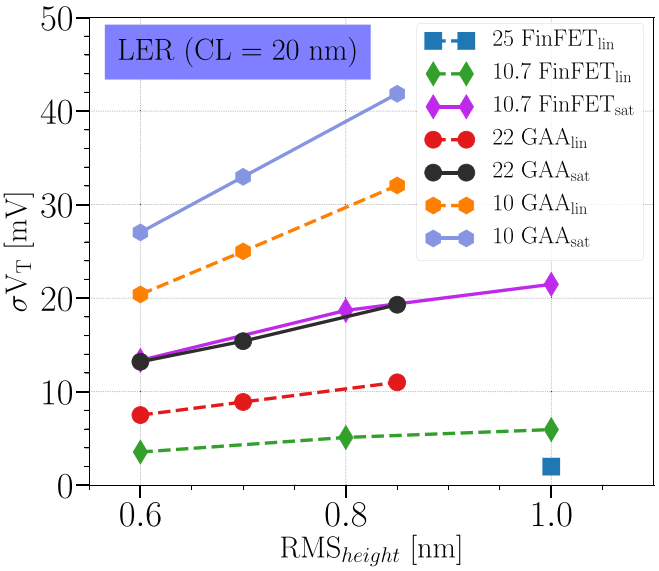

FIGURE 7. Compares the standard deviation (σ) of the V_T induced by the LER variability, for the 25 nm [42] and 10.7 nm [8] gate length FinFETs, and the 22 and 10 nm [18] gate length GAA NWs.

data for comparison is at an RMS of 1 nm). Increasing the drain bias leads to an increasing V_T variability unlike in case of the MGG. The scaling of the GAA NW from the 22 nm gate length to the 10 nm device leads to a ~ 2.2 times greater σV_T for all the analysed RMS heights. When comparing both architectures, the 10.7 nm gate length FinFET ($V_D = 0.7$ V) has a two times lower σV_T than the GAA NW (0.6 nm RMS height). Note that in case of both FETs the electron density, which exhibits complete volume inversion, is quantum-mechanically confined into the middle of the channel. However in case of the GAA NW the confinement is much stronger than in the FinFET because of its smaller channel height. Therefore the device with a greater confinement will be more strongly affected by imperfections (induced by the LER) in the confining potential. Note that the slope for the nanowire transistor (59.3 mV/nm) is steeper than for the FinFET (20.3 mV/nm). This suggests that control of the LER parameters during fabrication processes is more crucial for the GAA NW than for the FinFET, which has been also shown (see Fig. 6) for the MGG. The V_T variability is dominated by the MGG for both device structures and gate lengths. However, at the smallest studied GS and RMS height, the MGG and LER have a comparable effect.

Table 4 compares how much the MGG and LER variability sources affect the multi-gate devices (limited to a high drain bias, sat) with respect to the nominal values. These relative values (in %) are calculated as:

$$\frac{\sigma V_T}{(\text{nominal } V_T/100)}, \tag{2}$$

where the corresponding nominal values are taken from Table 3. Table 4 shows that the MGG affects both the FinFET and GAA NW variability more than the LER. Moreover, the FinFET is more resilient to the MGG and LER variability sources than the GAA NW.

TABLE 4. Comparison of the standard deviation against the nominal values of the 10.7 nm gate length FinFET and the 10 nm GAA NW FET.

	MGG (GS [nm])		LER (RMS$_{height}$ [nm])	
	5	10	0.6	0.8
OFF-region				
10.7 FinFET$_{sat}$	7.5%	16.6%	5.5%	9%
10 GAA$_{sat}$	11.9%	23.1%	10.4%	15%
ON-region				
10.7 FinFET ⟨110⟩	3.3%	6.2%	2.2%	3.4%
10.7 FinFET ⟨100⟩	3.4%	6.1%	2.5%	4.6%
10 GAA ⟨110⟩	3.6%	5.7%	4.6%	9.1%
10 GAA ⟨100⟩	3.5%	5.6%	4.3%	8%

V. MGG AND LER VARIABILITY IN THE ON-REGION

In this section, we investigate the ON-region variability of the devices affected by MGG and LER. The MC approach described in Section II was used for these simulations. Due to the time requirement of this method we have limited the number of simulations to a 100 for each GS and RMS height.

Fig. 8 shows the MGG ON-current variability (σI_{ON}) at a high drain bias, for the 20 nm gate length FinFET from [45], the 10.7 nm gate length FinFET, and the 22/10 nm gate length GAA NWs. Note that the on current variability study in [45] was carried out using DD simulations with DG quantum corrections. Here, we present these results because there are no known study, to our best knowledge, on similar devices in the ON-region using ensemble MC simulations which has a predictive power.

Analysing the results for the ⟨100⟩ channel orientation, the scaling of the 20 nm gate length FinFET to 10.7 nm resulted in twice as large σI_{ON}, for all grain sizes. The scaling of the 22 nm gate length GAA NW to 10 nm gate length led to around 1.3 times higher σI_{ON} for all grain sizes. When comparing both architectures, the σI_{ON} for the 10 nm gate length FinFET is 64/44% higher than that of the equivalent GAA NW at a GS of 10/5 nm. This trend is opposite to the observations in the sub-threshold region where the MGG resulted in a larger variability for the GAA NW. Note that the GAA NW has a smaller channel cross-section than the FinFET which results in a larger confinement in the NW channel, thus the electrons are on average closer to the interface in the FinFET. Therefore, the MGG has a greater effect on the σI_{ON} for the FinFET architecture. With respect to the channel orientation, the industry preferred ⟨110⟩ channel orientation is less affected by the MGG than the ⟨100⟩.

In Fig. 9, we show the I_{ON} variability due to LER for the 10.7 nm FinFET and 10 nm GAA NW architectures. The study is limited to the scaled devices because there are no published data in the on-region for the larger gate length

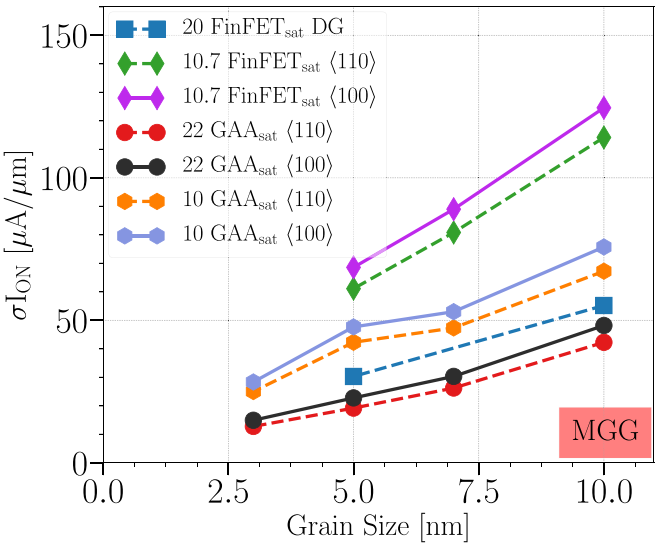

FIGURE 8. The standard deviation (σ) of I_{ON} induced by the MGG variability, for the 20 nm [45] and the 10.7 nm [8] gate length FinFETs, and for the 22 and 10 nm gate length GAA NW FETs.

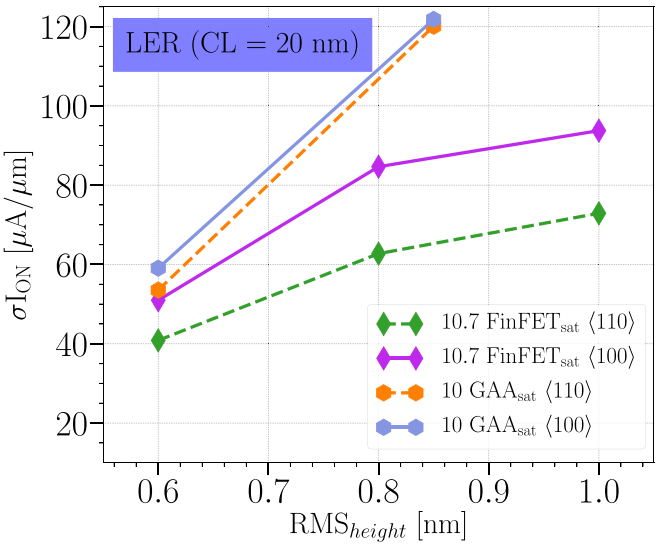

FIGURE 9. The standard deviation (σ) of I_{ON} induced by the LER variability, for the 10.7 nm [8] gate length FinFET, and the 10 nm gate length GAA NW FET.

devices affected by LER. Comparing both architectures for the ⟨100⟩/⟨110⟩ channel orientations, the FinFET resulted in a 23/39.3% lower σI_{ON} than the GAA NW at an RMS height of 0.8 nm. Reduction of the RMS height to 0.6 nm results in a comparable ON-current variability between the FinFET and the GAA NW for the ⟨100⟩ channel orientation. However, in case of the ⟨110⟩, at an RMS height of 0.6 nm, the GAA NW has a σI_{ON} 31% larger than the FinFET device. The stronger LER effect for the GAA NW is related to the smaller channel height which causes a stronger confinement than in case of the FinFET. As aforementioned for the sub-threshold region variability, devices with a greater confinement will be more strongly affected by LER deformations. The high degradation observed in the ON-current due to the LER could be a limiting factor for the scaling of the deep nano-scaled GAA NW transistors if the parameters (e.g., RMS height) are not optimised.

Comparing the MGG and LER influence for the ON-region, we found that the FinFET is affected more by the MGG variability source that is shown in Table 4. However, the LER in the GAA NW has a stronger effect on the device than the MGG, which is related to the cross-section variation of the channel due to the LER.

VI. CONCLUSION

A combined 3D quantum-corrected FE DD and MC simulation study of the performance, scalability and variability (MGG and LER) is performed for 25/10.7 nm gate length Si FinFETs and 22/10 nm gate length Si GAA NW FETs. The main conclusions can be summarised as follows.

Performance:

- In the OFF-region, the FinFET devices have 9% larger SS values and over an order of magnitude larger OFF-currents that those of the equivalent GAA NW FETs.
- In the ON-region, the 25/10.7 nm gate length FinFETs deliver 20/58% larger ON-currents than the equivalent 22/10 nm gate length GAA NW.
- The ON/OFF ratio of the FinFETs (1×10^4 when L_G = 10.7 nm) are more than an order of magnitude lower than those of the GAA NWs (13×10^4 when L_G = 10 nm).

Scalability:

- When the FinFET gate length is scaled from 25 to 10.7 nm: i) the OFF-current is reduced by 21%, ii) the ON-current is increased by 9/16% for the ⟨100⟩/⟨110⟩ channel orientations and iii) the ON/OFF ratio is increased by 37/46% for the ⟨100⟩/⟨110⟩ channel orientations.
- When the GAA NW gate length is scaled from 22 to 10 nm: i) the OFF-current is reduced by 10%, ii) the ON-current is also reduced by 14/12% for the ⟨100⟩/⟨110⟩ channel orientations and iii) the ON/OFF ratio is slightly deteriorated.

Variability:

- The FinFETs are more resilient to the MGG and LER variability in the sub-threshold region than the GAA NW FETs.
- The control of the LER parameters (CL and RMS) during the fabrication process is more crucial for GAA NWs than for FinFETs.
- The FinFETs are more affected by the MGG variability in the ON-region than the GAA NWs. σI_{ON} for the 10 nm gate length FinFET is 64/44% higher than that of the equivalent GAA NW at a GS of 10/5 nm.
- The FinFETs are more resistant to the LER variability in the ON-region than the GAA NWs.
- The industry preferred ⟨110⟩ channel orientation is more resilient to the MGG and LER variability sources in

the FinFET and GAA NW FETs than in the ⟨100⟩ orientation transistors.

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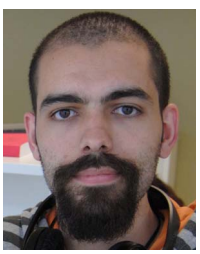

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