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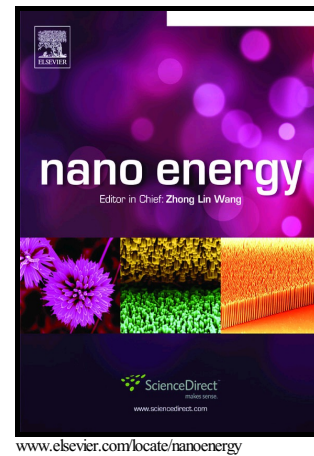
nano energy

Editor in Chief: Zhong Lin Wang

ScienceDirect

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Cite this article as: Jiaheng Nie, Gongwei Hu, Lijie Li and Yan Zhang, Piezotronic Analog-To-Digital Converters Based on Strain-gated Transistors, *Nano Energy,* https://doi.org/10.1016/j.nanoen.2018.02.034

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Piezotronic Analog-To-Digital Converters Based on Strain-gated Transistors

Jiaheng Nie[1], Gongwei Hu[1], Lijie Li[2], Yan Zhang[1,3,4,*]

[1]*School of Physics, School of Physical Electronics, University of Electronic Science and Technology of China, Chengdu 610054, China*

[2]*Multidisciplinary Nanotechnology Centre, College of Engineering, Swansea University, Swansea, SA1 8EN, UK*

[3]*Beijing Institute of Nanoenergy and Nanosystems, Chinese Academy of Sciences, Beijing 100083, China*

[4]*College of Nanoscience and Technology, University of Chinese Academy of Sciences, Beijing 100049, China*

[*] To whom correspondence should be addressed; zhangyan@uestc.edu.cn

Abstract

We report a novel approach to achieve piezotronic analog-to-digital converters (ADCs) based on strain gated transistors (SGTs). A single SGT can act as voltage converter, comparator, and amplifier. The new piezotronic ADC devices benefit from high sensitivity of the piezotronic SGT responding to the external strains. This design can significantly reduce the power consumption and the size of these devices, which are considered as crucial factors in self-powered systems. The fundamental concept of the device design has been demonstrated by three piezotronic ADC architectures formed by various networks comprised of SGTs and resistors. Analog-to-digital conversion and logic operations of these piezotronic ADCs blocks are analyzed and logic truth tables for all those configurations are presented. This design has immense potential for enormous applications in future human-machine interfaces, internet of things, and sensor networks.

Keywords: piezotronics; strain-gated transistor; piezotronic Analog-To-Digital Converter; piezotronic logic device; strain mapping

1. Introduction

Piezotronics and piezophototronics [1, 2] have attracted tremendous interests in the self-powered technology, [3] pervasive computing, [4, 5] and sensors [6]. Carrier transport characteristics of nanodevices can be controlled by strain-induced piezoelectric charges [7]. Recently, a series of novel devices have been obtained based on piezoelectric semiconductor materials in multifunction logic computing, [8] biomedical sensors, [9] ultra-high sensitivity strain sensors, [10] piezoelectric field effect transistor, [11] piezophototronic LEDs, [12, 13] and solar cell [14]. Piezotronic and piezo-phototronic array strain mapping devices have obtained significant attention for the applications in the new emerging field of flexible electronics and parallel optical signal processing [15, 16].

Piezotronic logic elements have become very promising for future applications in direct detecting, processing, and control of the external environmental stimuli. Based on the high-sensitivity strain-gated transistors, piezotronic logic devices can be fabricated by using ZnO nanowires (NWs) for the basic logical operations such as NAND, NOR, and XOR [4]. Piezo-phototronic binary computation has also been reported by using wurtzite structure ZnO and CdS [8]. Coupling of piezoelectric, semiconductivity and optical characteristics plays a key role to convert the mechanical or optical stimuli to ON or OFF output signals in piezoelectric logical devices.

Strain mapping and digital processing need the conversion from a continuous-time and continuous-amplitude analog signal to a discrete-time and discrete-amplitude digital signal. Piezotronic transistors act not only as strain sensors, but also as signal comparators and amplifiers. These properties offer novel piezotronic analog-to-digital converters (ADCs). Due to the high-sensitivity and low-power consumption properties, the strain-gated transistors (SGTs) are promising candidates for flexible and low-power piezotronic ADCs. The strain sensitivity (gauge factor) of SGTs can reach up to 1250, which is higher than Si-doped and carbon nanotubes strain sensor [6]. Furthermore, the energy consumption of the nanowire devices is in the order of pW, which can be regarded as zero power consumption [17]. SGTs can also exhibit ultra-fast response time because the device size is in the nanoscale. Therefore, the piezoelectric logic device based on SGTs can be a fundamental component of electronic circuits, with prominent characteristics of high-sensitivity, ultra-low power consumption and fast response time.

In this manuscript, the basic principle of piezotronic analog-to-digital converter based on SGTs has been demonstrated. Three design approaches are proposed by using the piezotronic effect. First type is structured by using various SGTs with different current-voltage characteristics, which can be obtained by various piezoelectric materials or with energy band engineering. To simplify the device fabrication, second type is using various resistors and SGTs with the same

current-voltage characteristics. These two types of piezotronic ADCs can realize ultra-low power consumption with reduced number of components. The third type is the assembly of piezotronic transistor-based strain sensors and conventional ADCs for the purpose of comparison with above two new designs. Take the first type as an example, the schematic diagram is illustrated in Figure 1. Piezotronic ADC devices are inserted into the flexible substrate, forming large-scale piezotronic ADCs arrays for detecting the external strain, as shown in Figure 1(a). Figure 1(b) shows the enlarged image of four piezotronic ADCs, and the basic structure of a single piezotronic ADC device consists of four branched SGTs that can achieve 2-bit output of strain signals. Figure 1(c) shows the circuit symbol and equivalent circuit of each branch based on SGT series circuit. Figure 1(d) shows the circuit diagram, which has N SGT branches. Piezotronic ADCs have enormous potential applications for strain imaging, man-machine interface, artificial intelligence and analog computing.

2. Basic Principle of Piezotronic Analog-to-Digital Converter

The basic block unit of a piezotronic ADC is the SGT acting as the strain-voltage converter, the comparator and amplifier. When the electrical current exceeds a certain threshold, the SGT will change from OFF state to ON state, corresponding to digital output signals 0 and 1, respectively. The strain threshold can be different by choosing SGTs with different current-voltage characteristics. Various SGTs with diverse I-V characteristics produced by various routines can form ADC devices responding to different external strains. Thus, the strains with different amplitude intervals can be encoded to different digital output signals. Therefore, the ADC devices fabricated from SGTs of N breaches will convert a tensile or compressible strain signal to digital information.

For a single SGT with a fixed bias voltage V_D, the current density can be given by [7]

$$J = J_0 \cdot \exp\left(\frac{q e_{33} s_{33} W_{piezo}}{2\varepsilon_s kT} \right)\left[\exp\left(\frac{q\ V_D - V_{out}}{kT} \right) - 1 \right] \tag{1}$$

where J_0 is the saturation current density, q is the absolute value of an electron charge, e_{33} is the piezoelectric coefficient, s_{33} is the applied strain along the grown direction, W_{piezo} is the width of piezoelectric charge distribution, ε_s is dielectric constant, k is Boltzmann constant and T is the temperature, V_{out} denotes the output voltage.

The voltage on a resistor can be obtained from a piezoelectric transistor and resistor series

circuit. Figure 2 shows the output voltage V_{out} and voltage sensitivity dV_{out}/ds_g as a function of

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strain s_g varying from 0 to 10%. Figure 2(a) and (d) show that the output voltage V_{out} increases with the increasing strain s_g for a fixed resistor R = 1 kΩ and drain voltage V_D ranges from 1 V to 7 V. The sensitivity of SGT dV_{out}/ds_g is approximatively constant at small strains, for example, less than 3% of strain at V_D =1 V, and it increases with the drain voltage V_D. Figure 2(b) and (e) also exhibit output voltage V_{out} and sensitivity dV_{out}/ds_g with strain s_g at the fixed drain voltage V_D =2 V, while resistor R varies from 10 kΩ to 150 kΩ. Output voltage V_{out} increases with the strain and reaches up to 2.0 V. The sensitivity can be higher when R is smaller. The sensitivity deceases from 1.8 to 0 with increasing strain. Furthermore, the output properties of piezotronic transistor significantly depend on the piezoelectric materials as shown in Figure 2(c) and (f). The output voltage and sensitivity of the piezotronic transistors based on ZnO, GaN and InN are plotted as a function of strain for fixed R = 1 MΩ and drain voltage V_D = 2 V. ZnO piezotronic transistor has higher output voltage and sensitivity compared to GaN and InN for strain ranging from 0 to 4.5%. In our calculations, piezoelectric constants e_{33} for ZnO, [18] GaN, InN are 1.22, 0.73, and 0.97 C/m^2 respectively. [19] Dielectric constants ε_s are 8.91, [18] 10.4, and 14.6 respectively. [19] Although we use the ideal piezotronic junction model to demonstrate the general principle of piezotronic ADCs, the V_{out} variation can significantly increase by controlling the sensitivity of the SGT. In practice, the V_{out} can change from 0 V to 0.975 V at drain-source voltage of 1.0 V in previous experiments. [4]

For a K-bits piezotronic ADC, strain resolution (Res) is an important factor and can be obtained by uniformly dividing the strain region, which is given by [20]

$$Res = \frac{s_0}{s_m} = \frac{s_0}{2^K s_0} = \frac{1}{2^K} \tag{2}$$

where $N = 2^K$, s_0 is strain interval, s_m is maximum value of strain and equals to $2^K s_0$. Res is expressed by K instead of $1/2^K$.

The conversion error coefficient from strain signal to digital signal should satisfy the relation [20]

$$\delta \leq \frac{1}{2} LSB \tag{3}$$

where *LSB* equals to s_0.

$e\left(t\right)$ is noise signal with T, sampling interval, equaling $1/f_{sample}$. [20]

$$e\left(t\right) = Q\left(\frac{t}{T} - \frac{1}{2}\right) \tag{4}$$

where *Q* is the size of the elementary quantization step, which is equivalent to *LSB*.

Mean value of noise power spectrum within a certain *T* was derived by [20]

$$NP_0\left(rms\right) = \sqrt{\frac{1}{T}\int_0^T \left[e\left(t\right)\right]^2 dt} = \sqrt{\frac{1}{T}\int_0^T \left[Q\left(\frac{t}{T} - \frac{1}{2}\right)\right]^2 dt} = \frac{Q}{\sqrt{12}} \tag{5}$$

To summarize, signal to noise ratio, SNR (in dB) is given by the equation (6) in piezotronic ADCs. s_m are all values included in the upper and lower bounds, which demonstrates the full-scale strain range [20].

$$SNR\left(dB\right) = 20 \cdot \log_{10}\left(\frac{s_m\left(rms\right)}{NP_0\left(rms\right)}\right) \tag{6}$$

The ideal sinusoidal input analog signal is used in this paper to further characterize piezotronic ADC's SNR property. In this condition, SNR is linear in the resolution *K* [20].

$$SNR\left(dB\right) = 20 \cdot \log_{10}\left(\frac{s_m}{2\sqrt{2}} \cdot \frac{1}{\frac{s_m}{2^K \sqrt{12}}}\right) = 6.02 \cdot K + 1.76 \tag{7}$$

3. Piezotronic Analog-To-Digital Converters Based on strain-gated transistors

Take piezotronic ADCs based on four SGTs as example, three piezotronic ADC architectures can be designed using the basic principle. The first two piezotronic ADCs have few electronic elements, which are beneficial to reduce power consumption. The functions of all three types of piezotronic ADCs are identical. The minimum interval s_0 of three piezotronic ADC is 0.25%, and strain resolution (Res) is $s_0/s_m = 1/2^K$. *SNR* (=13.8 dB) is employed to achieve a better interpretation of ADC performance limits, where we choose ideal sine signal and noise from sampling error without influence of materials characteristics and external noise.

3.1 Piezotronic ADCs based on strain-gated transistors and fixed resistors

Piezotronic transistors based on various materials or techniques can result in different output

responses to externally applied strains. Figure 3(a) shows the schematic diagram of piezotronic ADCs by using four strain-gated transistors connected with four fixed resistors parallelly to obtain digital signal of the strain value. Each SGT has different current-strain characteristics as shown in Figure 3(b). Branch SGT #4 has highest sensitivity and thus will be firstly switched to ON state for small strain of 0.25% with the threshold current of 0.1 mA. When the strain increases, the branch SGT #3, #2 and #1 can be switched on at strains of 0.5%, 0.75% and 1.00%. There are four basic signal output states for the strain varying from 0 to 1.00%. The logic signal of the ADCs outputs "00" for strain less than 0.25%. While strain is within the region 1 (0.25% ~ 0.5%), only branch SGT #4 is switched on and the output signal is "01". Signal state "10" is output for the strain in region 2 (0.5% ~ 0.75%) for which branch SGT #4 and #3 are in ON state and branch SGT #2 and #1 are in OFF state. While the branch SGT #4, #3 and #2 are simultaneously switched on and branch SGT #1 is switched off for the strain in region 3, "11" signal occurs. In this design, branch SGT #1 is used for overflow test. While the strain is higher than 1.00%, the branch SGT #1 has the output "1", thus, all of branch are switched on. This is overflow state, which indicates the strain reach the upper limit of measurement of this piezotronic ADC. The generated four logic units "00", "01", "10" and "11" can be used for the further encoder.

Piezotronic ADCs based on four parallel SGTs exhibit excellent performance compared to conventional ADCs. For instance, the comparator and the amplifier can be realized by a single piezotronic ADC. This principle can be also used in integrated resistance network by parallelly connecting different SGT circuits, giving rise to multifunctionality of assembled units. Piezotronic ADCs offer a unique method for strain-to-digital conversion by eliminating the comparator network, which can be used to reduce the number of elements and simplify conversion steps. Thus, this design leads to very low power consumption.

3.2 Piezotronic ADCs based on strain-gated transistors and various resistors

Figure 4(a) shows the schematic of second type piezotronic ADC based on the same SGT and various resistors. This design principle can simplify the device fabrication. With applied strain, drain voltage of each SGT is different, resulting in different current outputs. The source-drain voltage can be fixed at a constant value for each SGT by properly adjusting the resistor value. Figure 4(b) shows the output current as a function of the strain for fixed source-drain voltages of V_{DS} = 1 V, 0.75 V, 0.5 V, and 0.25 V, respectively. Four logic states, "00", "01", "10" and "11" are generated while the strain changes from 0% to 1.00%. When the threshold current is set at 0.5 mA, the logic value is "00" state for the strain 0% - 0.25% at the threshold current of

0.5 mA. All SGTs are in OFF states at this condition, as shown in Figure 4(c). The first SGT being at ON state corresponds to the maximum source-drain voltage V_{DS} = 1 V for the strain varying in 0.25% - 0.5%, leading to "01" logic state. With the strain increases to 0.5% - 0.75, the second SGT is also at ON state and the logic state is "10". The third SGT starts to open and logic state "11" is generated for the strain range of 0.75% - 1.00%.

3.3 Piezotronic ADCs based on single strain-gated transistors

For comparison, SGT acts as a strain sensor, which can be directly connected with conventional ADCs based on silicon chip. The design schematic is shown in Figure 5. When a bias voltage is added on piezoelectric transistor, the strain-induced piezoelectric potential will change the output voltage V_i. There is a comparator circuit of rated voltage for four resistors divider, resulting in reference voltages with various levels. Logic value "1" is generated when V_i is higher than the threshold level of the comparator. Logic value "0" is generated when V_i is less than the threshold level of the comparator. The output logic value from the comparator is transferred to the registers and used for next logic computations. The output terminal of the register connected to the gate logic circuit for the truth table of the strain signal, as shown in Figure 5(c).

4. Summary

Piezotronic ADCs can be used to convert external strain value to logic bit by using various circuit architectures with strain-gated transistors. There are three proposals to design piezotronic ADCs: the first two are using strain-gated transistors but with fixed resistors and with various resistors. The third one is based on single strain-gated transistors. The logic states can be obtained by comparing the output current with a threshold value under the external strain. The logic truth table is presented as a key parameter relating the strain signal to the logic bit. Based on the logic operation principle, piezotronic ADC can be further employed into high-sensitivity devices to achieve identification and measurement of external information synchronously. This study not only provides a theoretical insight into the design of novel ADCs, but also has wider potential applications for human–electronics interfacing and nanoelectromechanical systems.

Thousand Talents program for a pioneer researcher and his innovation team, China.

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Jiaheng Nie received his B.E. in communication engineering from North China University of Water Resources and Electric Power in 2014. He is now pursuing his M.S. degree under the guidance of Professor Yan Zhang in School of Physical Electronics in UESTC. He is interested in the fields of piezotronics and piezo-phototronics.

Gongwei Hu received his B.S. degree (2014) from China Three Gorges University and M.S. degree in Theoretical Physics (2017) from Lanzhou University. He is currently pursuing the Ph.D degree under the guidance of Professor Yan Zhang in School of Physics in UESTC. His research focuses on the field of functional nanostructures and their physics.
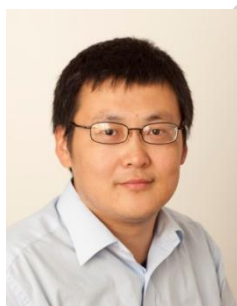

Lijie Li is an associate professor at Swansea University, UK. His research interests are design, modeling, fabrication, and characterization of MEMS, NEMS, sensors and actuators. He is Fellow of IET, and senior member of IEEE.
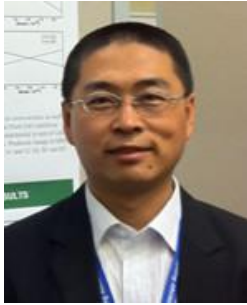
Yan Zhang is a professor at University of Electronic Science and Technology of China. He received his B. S. degree (1995) and Ph.D degree in Theoretical Physics (2004) from Lanzhou University. Then, he worked as associate Professor (2007) and Professor (2013) of Institute of Theoretical Physics in Lanzhou University. In 2009 he worked as research scientist in the group of Professor Zhong Lin Wang at Georgia Institute of Technology. His research interests include self-powered nano/micro system, piezotronic and modeling of nonlinear dynamics of NEMS.

Graphical Abstract
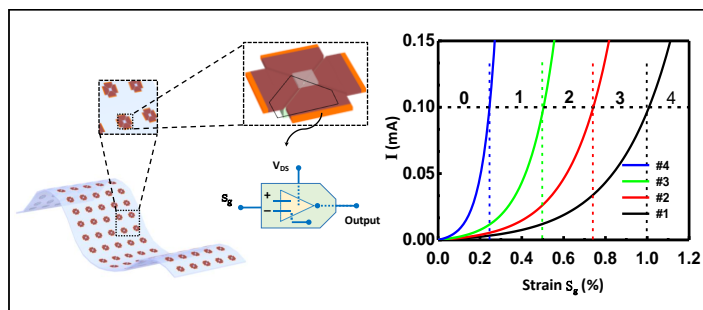
Piezotronic Analog-To-Digital Converter based on strain-gated transistor can be used for sensors and piezotronic logic. The new device design has potential application in strain mapping because the piezotronic transistors provide excellent properties of high sensitivity and lower power consumption.

Figure 1, (a) Schematic diagram of the piezotronics SGTs embedded into a flexible substrate. (b) enlarged graph of four piezotronic ADCs. (c) Circuit symbol and equivalent circuit of a single piezotronic ADC. (d) Circuit diagram of N SGT branches.

Figure 2, Calculated strain sensitivities under a set of external strains for proposed SGT devices with different drain voltage V_D (a) and (d), different resistors in series connection (b) and (e), and various piezoelectric materials such as ZnO, GaN, and InN (c) and (f).

Figure 3, ADC consisting of SGTs and fixed resistors. (a) schematic circuit. (b) simulated I-S_g curve. (c) logic truth table.

Figure 4, ADC consisting of SGTs and various resistors. (a) schematic circuit. (b) simulated I-S_g curve. (c) logic truth table.

Figure 5. ADC configured by using a single piezotronic SGT. (a) schematic diagram. (b) equivalent circuit. (c) simulated logic truth table.

(a)

(b)

(c) V$_{DS}$

S$_g$

+

−

Output

V$_{DS}$

Vout

R

(d) S$_g$ ↓

N

1	2	3	N
Piezopotential	**Piezopotential**	**Piezopotential**	**Piezopotential**
Comparator	**Comparator**	**Comparator**	**Comparator**
Amplifier	**Amplifier**	**Amplifier**	**Amplifier**

•••

Output 1 **Output 2** **Output 3** **Output N**

Figure 1

Figure 2

(a)

(b)

(c)

Strain (%)	#1	#2	#3	#4	Output States
0.00 - 0.25	0	0	0	0	"00"
0.25 - 0.50	0	0	0	1	"01"
0.50 - 0.75	0	0	1	1	"10"
0.75 - 1.00	0	1	1	1	"11"
>1.00	1	1	1	1	NA

Figure 3

(a)

V_D

R R R R

Output 1 Output 2 Output 3 Output 4

R R R R R

(b)

Strain (%)	#1	#2	#3	#4	Output States
(c) 0.00 - 0.25	0	0	0	0	"00"
0.25 - 0.50	0	0	0	1	"01"
0.50 - 0.75	0	0	1	1	"10"
0.75 - 1.00	0	1	1	1	"11"
>1.00	1	1	1	1	NA

Figure 4

(a)

(b)

(c)

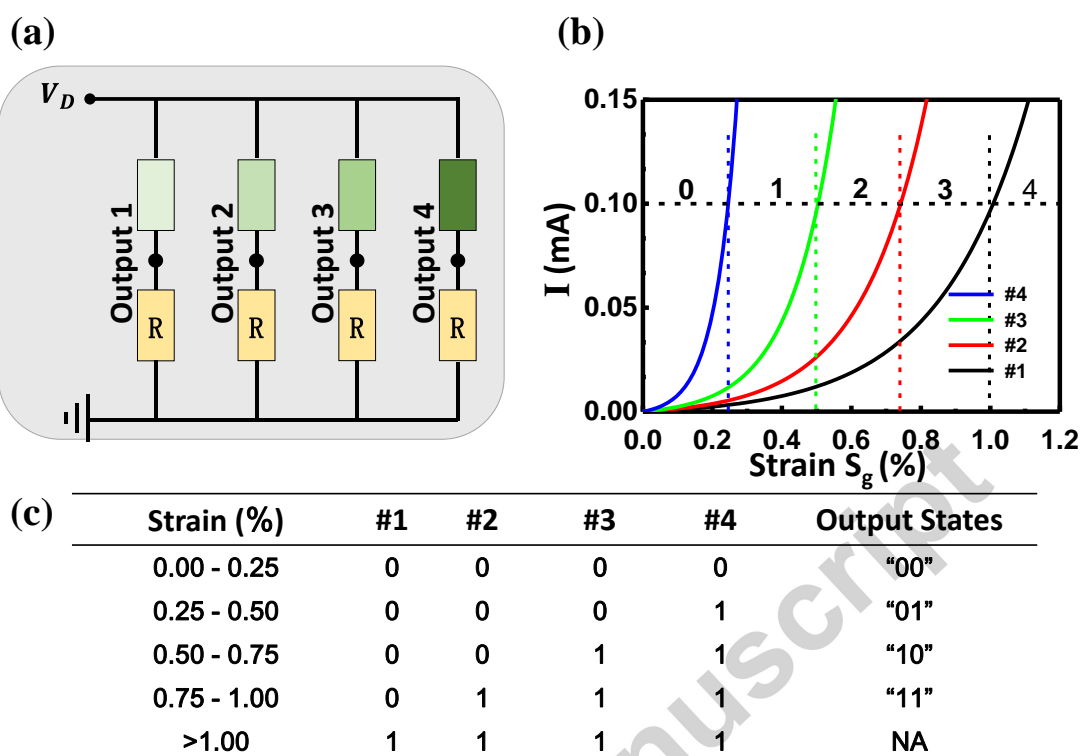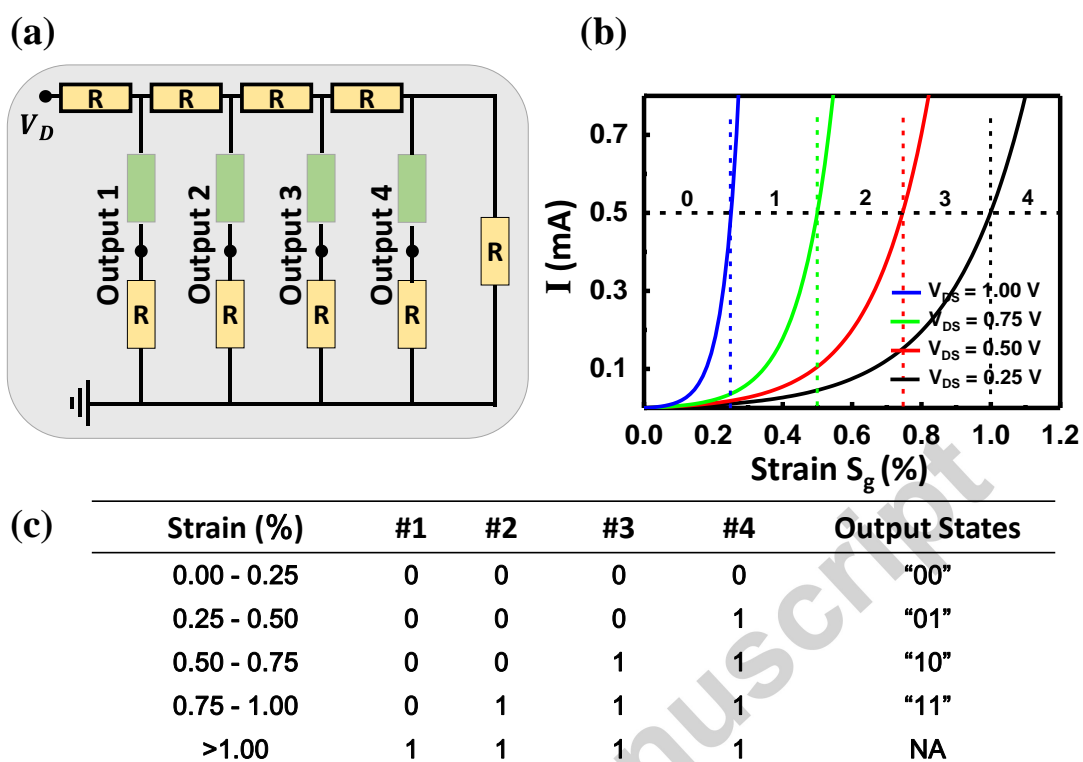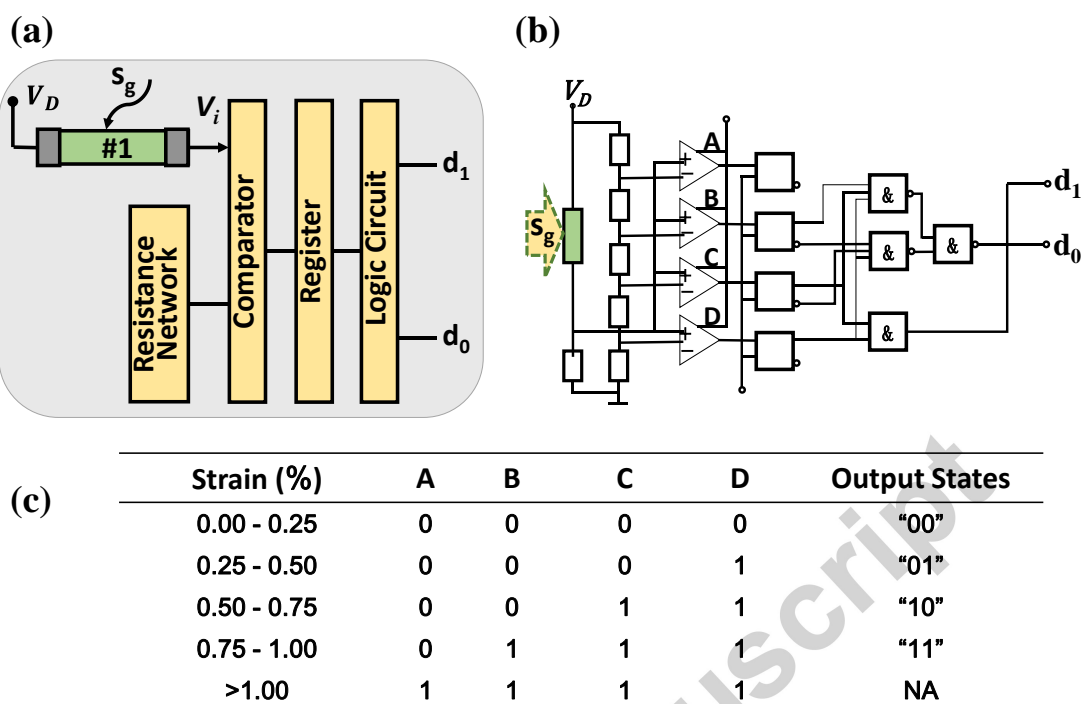| Strain (%)	A	B	C	D	Output States
0.00 - 0.25	0	0	0	0	"00"
0.25 - 0.50	0	0	0	1	"01"
0.50 - 0.75	0	0	1	1	"10"
0.75 - 1.00	0	1	1	1	"11"
>1.00	1	1	1	1	NA

Figure 5

Highlights:

1. SGTs exhibit multiple functions in the single piezotronic transistor, such as voltage converter, comparator, and amplifier.

    2. Three piezotronic ADC architectures are investigated based on piezotronic SGTs.