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Impact of cross-section shape on 10 nm gate length InGaAs FinFET performance and variability

Natalia Seoane, Guillermo Indalecio, Daniel Nagy, Karol Kalna and Antonio J. García-Loureiro

***Abstract*—Three cross–sections (rectangular, bullet–like and triangular), resulting from fabrication process, of nanoscale $In_{0.53}Ga_{0.47}$As-on-insulator FinFETs with a gate length of 10.4 nm are modelled using in–house 3D finite–element density–gradient quantum–corrected drift–diffusion and Monte Carlo simulations. We investigate the impact of the shape on I–V characteristics and on the variability induced by Metal Grain Granularity (MGG), Line-Edge Roughness (LER) and Random Dopants (RDs) and compared to their combined effect. The more triangular the cross–section, the lower the off–current, the drain–induced–barrier–lowering and the sub–threshold slope. The I_{ON}/ I_{OFF} ratio is 3 times higher for the triangular–shaped FinFET than for the rectangular–shape one. Independently of the cross-section, the MGG variations are the pre–eminent fluctuations affecting the FinFETs, with 4-to-2 times larger σV_T than that from the LER and the RDs, respectively. However, the variability induced threshold voltage (V_T) shift is minimal for the MGG (around 2.0 mV), but V_T shift increases 4-fold and 15-fold for the LER and the RDs, respectively. The cross–section shape has a very small influence in V_T and off-current of the MGG, LER and RD variabilities, both separated and in combination, with standard deviation differences of only 4% among the different device shapes. Finally, the statistical sum of the three sources of variability can predict simulated combined variability with only a minor overestimation.**

***Index Terms*—Density gradient (DG) quantum corrections; Drift–diffusion (DD); FinFET; Metal grain granularity (MGG); Line–edge Roughness (LER), Random dopants (RDs).**

I. Introduction

MULTI-GATE devices, such as FinFETs, have become one of the best substitutes in the scaling of the conventional planar CMOS technology for future technology nodes, because of their ability to reduce short–channel effects. Moreover, III–V materials are being exhaustively investigated to replace Si in the n–channel multi–gate CMOS [1], because of their larger carrier mobility and saturation velocity [2]. As the dimensions of the semiconductor devices progressively shrink, the impact of random intrinsic sources of variability on their performance is becoming more bothersome [3]. Metal grain granularity (MGG) [4], line–edge roughness (LER) [5] and random dopant (RD) [7] fluctuations are examples of major contributors to the device variability.

The FinFET performance is largely dictated by the fin geometry [8]–[10] with a cross–section shape affecting transistor leakage [11] and the AC performance [12]. Therefore, in this paper, we study three possible cross-section shapes of a 10.4 nm gate length $In_{0.53}Ga_{0.47}$As FinFET on insulator which can occur in fabrication [13], [14]. We analyse the impact of these shapes on the performance and variability of the device. In addition, the variability induced by the MGG, LER and RD is studied both independently and combined to assess non-Gaussian properties of overall variability at nanoscale [6]. The III-V channel multi-gate transistor is selected over the Si channel because the stronger quantum-mechanical confinement of the carrier transport in the channel. The investigation is carried out with 3D density–gradient (DG) quantum–corrected [15] drift–diffusion (DD) and ensemble Monte Carlo simulations. These simulators use finite elements to create the simulation domain accurately describing 3D geometry of the shapes of cross-sections in FinFETs including rounded corners [16].

The structure of the paper is as follows. Section II describes the structure and main characteristics of the FinFET devices, the simulation method and the implementation of the different sources of variability. Section III discusses the performance and variability results for the three cross–section devices and, Section IV summarises the main conclusions of this work.

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II. Methodology

A. Device Structure

We have analysed three 10.4 nm gate length $In_{0.53}Ga_{0.47}$As FinFETs that have the same fin width (6.1 nm), EOT (0.59), cross–sectional area (92 nm^2) and length of the source/drain (S/D) regions (10.4 nm). Moreover, all the device structures have identical Gaussian n–type doping in the S/D (a peak value 5x10^{19} cm^{-3} and a lateral straggle σ=1.85 nm) and an uniform p–type doping (10^{17} cm^{-3}) in the channel. However, their fin heights (H_{fin}) are different (see values in Table I) to allow for a constant cross–section area criterion. Both the rectangular shaped (REC), shown in Fig. 1(a) [13], and the bullet–like shaped (BUL), shown in Fig. 1(b) [14], FinFETs are designed following experimental devices that are properly scaled down [17] following the ITRS [18] guidance for high performance logic III–V multi–gate devices. The third considered device, the triangular shaped (TRI), presented in Fig. 1(c), has been included for comparison purposes as an extreme cross–section shape architecture.

B. Simulation Method

To accurately model the cross–sectional shapes with rounded corners of these devices, the use of finite elements (FE) is essential. For that reason, our study has been carried

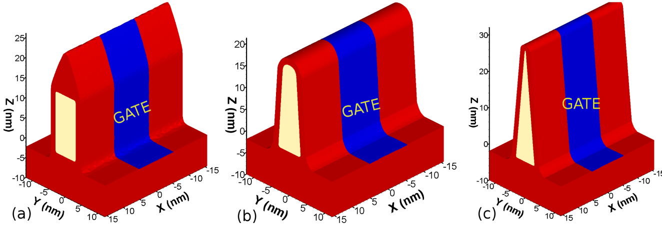

Figure 1. Scheme of the 10.4 nm gate length $In_{0.53}Ga_{0.47}As$ FinFET on insulator for the three analysed cross-sections: (a) rectangular (REC), (b) bullet-shaped (BUL) and (c) triangular (TRI).

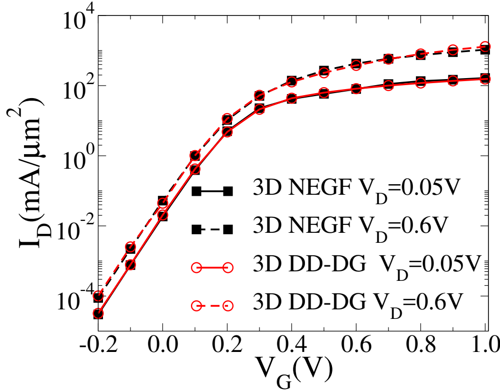

Figure 2. I_D–V_G characteristics comparing ballistic Non–Equilibrium Green's Function data (NEGF) [22] against 3D density–gradient quantum–corrected simulations (3D DD-DG) for the 10.4 nm gate length $In_{0.53}Ga_{0.47}As$ FinFET with a rectangular cross–section.

out with in–house built 3D FE DG quantum–corrected (QC) DD and Monte Carlo (MC) device simulators [2], [15]. Both simulation tools are coupled in such a way, that QC-DD simulations are used in the sub–threshold and QC-MC are utilised in the on–region, with both simulation techniques matching at the threshold. These simulators have been extensively used for variability studies affecting different types of semiconductor devices, such as HEMTs [19], MOSFETs [20], FinFETs [4] or nanowires [21]. Initially, the 3D DD–DG simulations are calibrated for the rectangular cross–section device in the sub–threshold at both low and high drain voltages against ballistic Non–Equilibrium Green's Function (NEGF) simulations [22]. The calibration includes adjusting parameters in a high-field mobility model [15] and electron effective masses serving as parameters in the DG approach. The DG quantum corrections can mimic the source-to-drain tunnelling and model quantum confinement effects on carrier density [4]. Fig. 2 shows the calibration of the I_D–V_G characteristics obtained from the 3D DD–DG against 3D NEGF for all the simulated gate biases. Note that the drain current has been normalised by the cross–section area. For an accurate study of the on–region performance, 3D finite–element DG-QC Monte Carlo (MC) simulations were employed. The MC toolbox uses an analytic non-parabolic anisotropic model for energy dispersion in valleys, includes phonon scatterings (acoustic, non-polar optical intra-valley and inter-valley, polar optical), interface roughness, ionized impurities, piezoelectric, and alloy scattering [2], [17].

MGG, LER and RD are principal sources of variability which will make each FinFET microscopically different. In the study of the MGG, we use Poisson Voronoi Diagrams (PVD) to generate patterns of gate metal grains. This methodology, described in detail in [24], is able to capture the shape of the domains that grow from randomly located nucleation points as seen in real fabrication [25]. The metal used in the gate is TiN with two possible grain orientations having work–function (WF) values of 4.86 and 4.66 eV and probabilities of occurrence of 60% and 40%, respectively. Note that the WF of the device with a uniform gate is 4.78 eV. The LER is implemented in the devices following the Fourier synthesis method, as explained in [20]. There are two parameters that characterise the line–edge roughness: i) the correlation length, that describes the deformation along the x–direction of the device and ii) the root mean square height, that represents the deformation in the y–direction. The RD variations are considered as random discrete dopants in the S/D regions of the device that have been placed in the nodes of the discretisation mesh via a rejection technique from the device with the continuous doping [26]. In the rest of the simulation domain the doping charge remains unchanged. For each cross–section and fluctuation source, we have generated an ensemble of 300 devices, each with a different MGG, LER, RD or MGG/LER/RD (the three sources combined) distribution at both low and high drain biases, which amounts to a total of 7200 simulated configurations (300 different device configurations $*$ 4 sets of variability $*$ 2 values of drain bias $*$ 3 device shapes).

Table I
FIN HEIGHT, OFF–CURRENT, THRESHOLD VOLTAGE, SUB–THRESHOLD SLOPE, DRAIN–INDUCED–BARRIER–LOWERING, ON–CURRENT AND ON/OFF RATIO FOR THE THREE CROSS–SECTION SHAPES OF THE 10.4 NM GATE LENGTH FINFET. THE DRAIN BIAS IS 0.6 V. THE ON–CURRENT IS SELECTED AS THE DRAIN CURRENT WHEN V_G=V_D+V_T.

	REC	BUL	TRI
H_{fin} (nm)	15.2	19.9	30.3
I_{OFF} ($\mu A/\mu m^2$)	55.8	36.3	20.1
V_T (V)	0.186	0.199	0.216
SS (mV/dec)	79.1	78.1	61.3
DIBL (mV/V)	75.5	67.2	67.3
I_{ON} ($mA/\mu m^2$)	821	878	945
I_{ON}/ I_{OFF}	1.47×10^4	2.42×10^4	4.70×10^4

III. Cross-Section Impact on Variability

Initially, I_D–V_G characteristics for the 10.4 nm gate length $In_{0.53}Ga_{0.47}As$ FinFET with either a REC, BUL or TRI cross-section are compared at low and high drain biases in the sub–threshold (Fig. 3) and in the on–region (Fig. 4). For the three device shapes, we have extracted all the figures of merit (FoM) affecting both the sub–threshold: off–current (I_{OFF}), sub–threshold slope (SS), threshold voltage (V_T), drain–induced–barrier-lowering (DIBL), and the on–region (I_{ON}). Results are

presented in Table I at a high drain bias including a comparison of on–off ratios (I_{ON}/ I_{OFF}). The threshold voltage is calculated via a constant current criterion (I_T=7.5×10^{-7} A). The same criterion is used for all the cross–section devices and for studies at both low and high drain voltages. The on–current is selected as the drain current when V_G=V_{Dsat}+V_{Tsat} and the off–current is extracted at V_G=0.0 V. The triangular cross–section transistor exhibits the best FoM in majority of the components. It has a reduced I_{OFF} and DIBL, and a nearly ideal SS of 61 mV/dec indicating a better gate control due to the stronger quantum-mechanical confinement. Moreover, its I_{ON}/ I_{OFF} ratio is 1.9 and 3.2 times larger than those of the bullet and the rectangular cross–section devices, respectively. All these attributes make the triangular cross–section device more suitable for digital applications. However, its larger fin height might be more challenging for fabrication. Moreover, non–rectangular fin structures may suffer from current crowding, which can deteriorate the device performance [23].

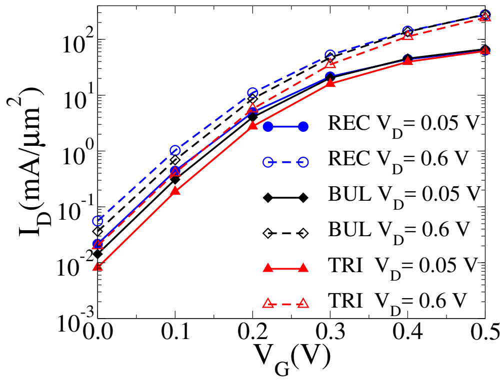

Figure 3. Sub–threshold region I_D–V_G characteristics for the 10.4 nm gate length $In_{0.53}Ga_{0.47}As$ FinFET with either a rectangular (REC), a bullet-shaped (BUL) or a triangular (TRI) cross-section.

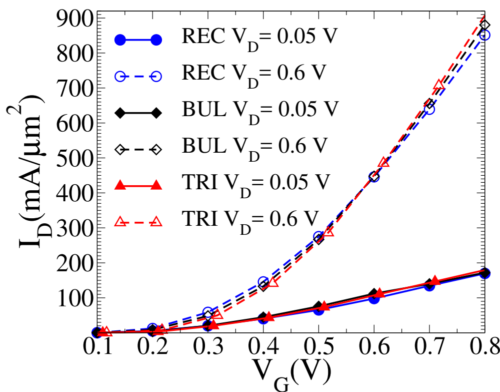

Figure 4. On–region I_D–V_G characteristics for the 10.4 nm gate length $In_{0.53}Ga_{0.47}As$ FinFET with either a rectangular (REC), a bullet-shaped (BUL) or a triangular (TRI) cross-section.

A. Metal Grain Granularity

Once the ideal devices (not affected by any source of fluctuation) have been characterised, we evaluate the effect that different sources of variability have on their performance. With respect to the MGG, we have limited the study to devices with an average grain size (GS) of 7 nm. An in–depth study of the influence of the grain size can be found in [27]. An example of a metal gate profile from the grain size of 7 nm is shown in Fig. 5(a). 2D cuts of the electron concentration at the centre of the gate (X=0 nm) for the three shapes are shown in Fig. 5(b)–(d), for this particular MGG profile. The electron density is spread along the whole channel for the REC and BUL shaped–devices, even though the largest concentration is localized at the top of the cross–section. Note that a large part of the gate profile's right–hand side has a WF value of 4.86 V (area of interest shown in a green rectangle in Fig. 5(a)), which pushes the electron density away from that side of the device (shown in Fig. 5(b)–(d)). The threshold voltage is lower for the BUL shape than for the REC one, which is opposite to the behaviour seen in the ideal devices presented in Table I. This can be explained by the larger control at the top of the gate for the BUL device in this profile. On the other hand, the electron density accumulates towards the bottom of the TRI cross–section device, and it is significantly reduced at the narrow top due to the strong quantum confinement.

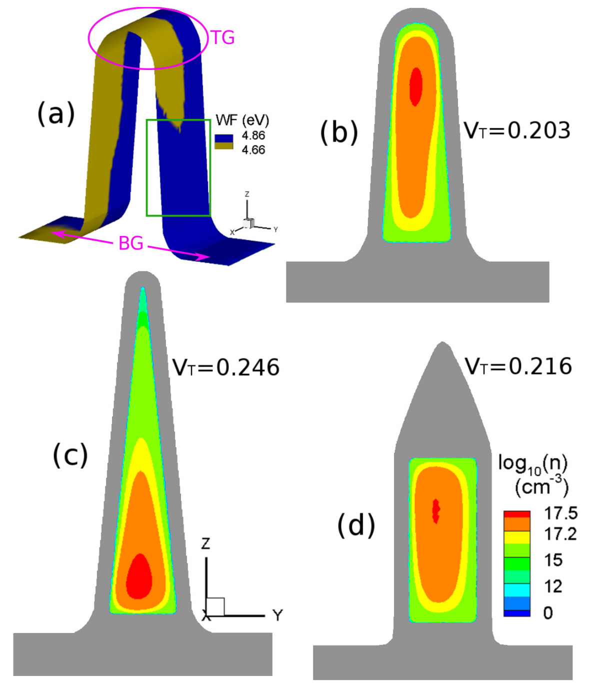

Figure 5. (a) Example of a TiN metal gate profile under the influence of MGG with a 7 nm grain size. Electron density cross–section in the middle of the gate of the FinFET (X=0 nm) affected by the MGG profile for the (b) bullet, (c) triangular or (d) rectangular shapes at V_G=V_T and V_D=0.6 V. V_T values for each shape are also shown.

The question of what physically occurs under the influence of the MGG, is answered by generating fluctuation sensitivity maps (FSM) for all the three cross–section devices. These maps, first introduced and described in [28], graphically assess how sensitive a certain FoM is to the WF value present on different parts of the gate. Fig. 6 shows the 2D I_{OFF} FSM for the REC, BUL and TRI FinFETs at a low drain bias of 0.05 V. Note that, the lighter/darker the colour, the more/less sensitive

a region of the gate is to the MGG variability. The top (TG) and bottom (BG) of the gate are indicated both in this figure and in Fig. 5(a). The source/gate (SG) end (X=−5.2 nm), the middle of the gate (MG) (X=0 nm) and the drain/gate (DG) end (X=5.2 nm) are also shown.

In the rectangular–shaped FinFET, the grains located in the side–walls of the gate are the most influential, whereas those placed on the TG have a much lower sensitivity due to the 11 nm thick layer of oxide over the channel (as seen in the scheme of the device in Fig. 1(a)) that is also present in the fabricated device [13]. In the BUL and TRI shaped devices, the thickness of the oxide layer in top of the channel is scaled down to 1.48 nm (the EOT is 0.59 nm). This explains why for the bullet–shaped FinFET, the TG and its proximity are the most sensitive regions to variations in the MGG. In the TRI device, the metal grains occupying both the BG and the side–walls of the gate are dominant contributors to the I_{OFF} variations, due to the larger quantum confinement at the top. Finally, note that, independently of the cross–section, there is not a perfect symmetry in the sensitivity seen from the TG to both BGs (as one would have expected), due to the random nature of the Voronoi generated metal grains [28]. However, the conventional variability figures (as for instance the standard deviation) are not able to capture these behavioural differences between the cross–section shapes. The off–current variability for the triangular device (σlog($I_{OFF}(A)$)=0.420 at high drain bias) is only 1% and 5% larger than those of the BUL and REC devices, respectively. Fig. 7 shows a comparison of the V_T standard deviation due to the three analysed sources of variability as a function of the drain bias and the cross–section shape. For the MGG, σV_T (around 32 mV) is practically independent of the cross–section and the drain bias, exhibiting differences of only 4% between the different shapes.

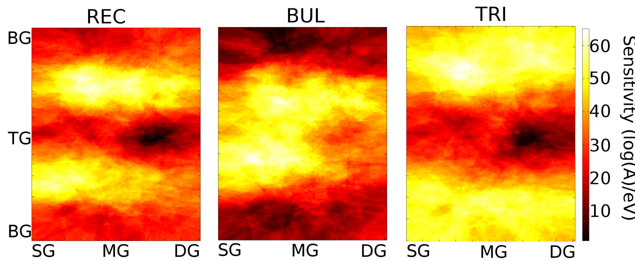

Figure 6. 2D off–current fluctuation sensitivity maps (FSM) due to MGG variability for the three cross–sectional shapes corresponding to the metal gate profiles in Fig.5 (b), (c), and (d) at a low drain bias.

B. Line Edge Roughness

When studying the influence of the LER, we have limited the analysis to devices with a correlation length (CL) of 10 nm and a root mean square (RMS) height of 0.8 nm, considering uncorrelated fin edge roughness variations. These values were chosen to represent the ones observed in experimental devices [27]. Fig. 8(a) and (b) show the current density in the transport direction for two bullet–shaped FinFETs that produce the maximum and minimum threshold voltage, respectively. Note that in both extreme cases the main deformations occur

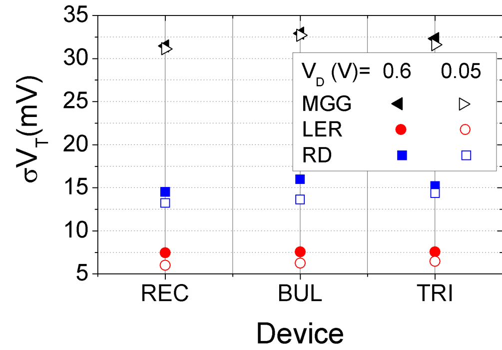

Figure 7. Comparison of the V_T variability due to MGG, LER or RDs for the three studied cross–sectional shapes of the FinFET.

in the gate region, where they are most influential, either via a widening of the device channel (as seen in the device that shows the minimum V_T) or via a transversal displacement (as displayed for the minimum V_T device) that will reduce the electron concentration in that region. The off–current and threshold voltage variabilities due to LER are around 4 times smaller than those due to the MGG and completely unaffected by the cross–section shape (σlog($I_{OFF}(A)$)=0.106 and σV_T=7.56 mV at a high drain bias for the TRI device). On the other hand, the V_T variability due to LER increases with the drain bias as seen in Fig. 7, the increments ranging between 17% for the TRI device to 24% for the REC one.

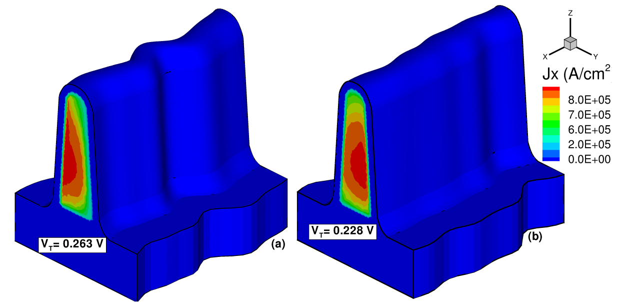

Figure 8. Current density along the x–direction inside the body of the semiconductor at V_G=V_T and V_D=0.05 V for two extreme LER profiles that lead to either (a) the maximum or (b) the minimum V_T value.

C. Random Dopants

With respect to the RD variability, Fig. 9 shows an example of the potential profile generated by a specific distribution of the RDs inside the channel of the rectangular cross–section device at the threshold when the applied drain voltage is 0.6 V and V_G=V_T. Fig. 10 shows the off–current on a logarithmic scale versus the number of RDs for the three cross–section shapes. The insets plot the distribution of the I_{OFF} (top left corner of the figure) and the RDs number distribution (bottom right corner of the figure). The actual number of dopants in a particular simulated device is randomly chosen from a Poisson distribution that will have a mean value product of the n–type doping concentration by the channel area of the simulated FinFET (a mean doping concentration is created by around

50 dopants). Unlike for LER and MGG, the off–current RD variability weakly depends on the cross–section shape, with a σlog(I_{OFF}) for the TRI shape FinFET (0.267 at a high drain bias) by 5% and 12% larger than those of the BUL and REC devices, respectively. The RD threshold voltage fluctuations are around 2.1 times smaller than those of the MGG, as seen in Fig. 7. For the REC device, σV_T is marginally lower than those of the other two cross–sections.

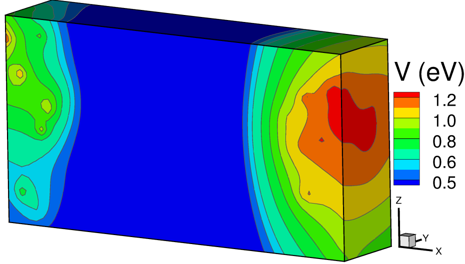

Figure 9. Electrostatic potential in the channel of the rectangular–shaped FinFET for a pattern of RDs at V_G=V_T and V_D=0.6 V.

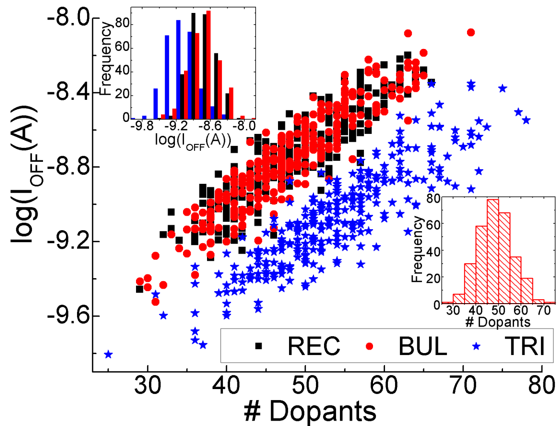

Figure 10. Off–current versus the number of dopants for the three cross-section devices at 0.6 V drain bias. The histograms in the insets show the (top left) distributions of off–current and (bottom right) number of dopants.

D. Combined variability

Once the impact of the three sources of variability has been separately evaluated, their combined effect was again studied via an ensemble of 300 different devices. Fig. 11 shows (from top to bottom) the distribution of V_T due to variability induced by MGG, LER, RDs and their combination (COMB) for the rectangular device at a low drain bias. The standard deviation of the distribution and the threshold voltage shift (ΔV_T) are also presented in this figure. ΔV_T has been calculated as the difference between the mean of the statistical sample ($< V_T >$) and the value of the magnitude for an ideal device ($V_{T-ideal}$). Results show that while the threshold voltage shift is very small for the MGG variability (2 mV), it substantially increases for the other sources of variability, being 4 and 15 times larger for the LER and the RDs, respectively. The

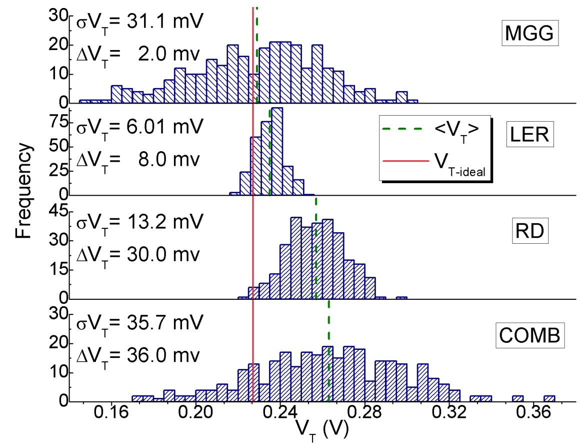

Figure 11. V_T distribution due to three different variability sources (MGG, LER and RDs) and their combined effect (COMB) in the REC FinFET at V_D=0.05 V. The standard deviation (σV_T), the mean value ($< V_T >$), the V_T of the device not affected by any variability source ($V_{T-ideal}$), and the threshold voltage shift ΔV_T=$< V_T >$–$V_{T-ideal}$ are shown.

Table II

I_{OFF}, SS AND V_T STANDARD DEVIATIONS DUE TO THE COMBINED EFFECT OF MGG, LER AND RDS AT V_D=0.05 V. THE STATISTICAL SUM OF THE THREE SOURCES OF FLUCTUATIONS (σV_T EQ.(1)) HAS BEEN INCLUDED FOR COMPARATIVE PURPOSES TOGETHER WITH THE V_T DISTRIBUTION RANGE (V_T RANGE).

	σI_{OFF} (log(A))	σSS (mV/dec)	σV_T (mV)	σV_T Eq.(1) (mV)	V_T range (mV)
REC	0.502	2.67	35.7	34.3	197
BUL	0.504	2.48	35.7	35.9	203
TRI	0.522	2.34	36.0	35.5	219

statistical sum of the three sources of variability has the following V_T standard deviation:

$$\sigma V_T = \sqrt{(V_{T-MGG})^2 + (V_{T-LER})^2 + (V_{T-RD})^2} \quad (1)$$

and a cumulative threshold voltage shift given by:

$$\Delta V_T = \Delta V_{T-MGG} + \Delta V_{T-LER} + \Delta V_{T-RD} \quad (2)$$

The full simulations of the three sources of variability combined give $\Delta V_T = 36$ mV, a value 10% lower than the one predicted by Eq. (2). However, Eq. (1) can anticipate the standard deviation of the combined variability with an overestimation of only 4%. This is also valid for the other two cross–section devices as shown in Table II (see the column σV_T obtained from Eq. (1)). The table demonstrates the immunity of I_{OFF} and V_T combined variability to cross–section shape (as seen before in the independent study of the three variability sources). Note that the more triangular the cross–section, the larger the V_T distribution range (difference between the highest and lowest distribution values), as seen in Table II. Finally, there is an impact of the shape on the SS variability. The TRI device is more resilient with a σSS 12% lower than that of the REC cross–section.

IV. CONCLUSION

We have analysed the impact that the cross–section shape has on the performance and variability affecting the 10.4 nm gate length $In_{0.53}Ga_{0.47}As$ FinFET. The TiN metal grain granularity, the line–edge roughness and the random dopant variations have been assessed for three cross–section shapes (rectangular, bullet–like and triangular) in the sub–threshold region. Both the rectangular (REC) and the bullet–like (BUL) devices were created following the appropriate scaling (via the ITRS) of experimental devices, and the triangular device (TRI) was chosen as an extreme case. We have demonstrated that the TRI cross–section device has a better gate control, presenting a reduced I_{OFF}, DIBL and SS (nearly ideal) and a significant larger I_{ON}/ I_{OFF} ratio than that of the other device shapes. Therefore, the triangular cross–section FinFET is more suitable for digital applications although, it is worth mentioning that its larger fin height will be more challenging for process fabrication. There is an immunity of the MGG, LER and RD variability affecting FinFETs to the cross–section shape, with changes in the V_T and I_{OFF} standard deviations of only 4% between the different device shapes, although both the electron distribution and the sensitivity (FSM) inside the device were quite different. This resilience to the variability is essential for the future development of sub–10 nm technology nodes because it will allow for larger deviations in cross-section shapes during the fabrication process.

The MGG variations (7 nm grain size) are the dominant source affecting FinFETs with the three analysed cross-sections, with a V_T standard deviation 4 times and 2 times higher than that of the LER (CL=10 nm and RMS=0.8 nm) and the RDs, respectively. However, the variability induced V_T shift is much smaller for MGG (2 mV) than for the LER (8 mV) and the RDs (30 mV). Finally, we have shown that the statistical sum of the three sources of variability is still an accurate method to foresee their combined, more realistic variability (combined σV_T is $\sim$ 36 mV independently of the cross–section shape) despite the deep nanoscale dimensions of transistors which increases variability coupling effects, giving only a 4% overestimation.

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REFERENCES

[1] N. Waldron, C. Merckling, W. Guo, P. Ong, L. Teugels, S. Ansar, D. Tsvetanova, F. Sebaai, D. H. van Dorp, A. Milenin, D. Lin, L. Nyns, J. Mitard, A. Pourghaderi, B. Douhard, O. Richard, H. Bender, G. Boccardi, M. Caymax, M. Heyns, W. Vandervorst, K. Barla, N. Collaert and A. Thean, "An InGaAs/InP quantum well FinFET using the replacement fin process integrated in an RMG flow on 300 mm Si substrates", *Symp. VLSI Technol. Dig. Tech. Pap.*, pp. 1–2, 2014. DOI:10.1109/VLSIT.2014.6894349

[2] N. Seoane, M. Aldegunde, D. Nagy, M. A. Elmessary, G. Indalecio, A.J. García-Loureiro and K. Kalna, "Simulation study of scaled $In_{0.53}Ga_{0.47}As$ and Si FinFETs for sub–16 nm technology nodes", *Semiconductor Science and Technology*, vol. 31, no. 7, pp. 075005(7pp), June 2016. DOI:10.1088/0268-1242/31/7/075005

[3] X. Wang, A. R. Brown, B. Cheng and A. Asenov, "Statistical variability and reliability in nanoscale FinFETs", *IEDM Tech. Dig.*, pp. 103–106, 2011. DOI:10.1109/IEDM.2011.6131494

[4] N. Seoane, G. Indalecio, E. Comesana, M. Aldegunde, A. J. García-Loureiro, and K. Kalna, "Random dopant, line-edge roughness, and gate workfunction variability in a nano InGaAs FinFET", *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 466–472, 2014. DOI:10.1109/TED.2013.2294213

[5] G. Leung and C. O. Chui, "Variability of inversion-mode and junctionless FinFETs due to line edge roughness", *IEEE Electron Device Lett.*, vol. 32, no. 11, pp. 1489–1491, 2011. DOI:10.1109/LED.2011.2164233

[6] X. Wang, A. R. Brown, N. Idris, S. Markov, G. Roy, and A. Asenov, "Statistical Threshold-Voltage Variability in Scaled Decananometer Bulk HKMG MOSFETs: A Full-Scale 3-D Simulation Scaling Study", *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2293–2301, August 2011. DOI:10.1109/TED.2011.2149531

[7] S. Markov, B. Cheng and A. Asenov, "Statistical variability in fully depleted SOI MOSFETs due to random dopant fluctuations in the source and drain extensions", *IEEE Electron Device Lett.*, vol. 33, no. 3, pp. 315–317, March 2012. DOI:10.1109/LED.2011.2179114

[8] S. Dubey and P. N. Kondekar, "Fin shape dependent variability for strained SOI FinFETs", *Microelectronic Engineering*, vol. 162, pp. 63–68, 2016. DOI:10.1016/j.mee.2016.04.015

[9] F. A. M. Rezali, N. A. F. Othman, M. Mazhar, S. W. M. Hatta and N. Soin, "Performance and Device Design Based on Geometry and Process Considerations for 14/16-nm Strained FinFETs", *IEEE Trans. Electron Devices*, vol. 63, no. 3, pp. 974–981, Mar. 2016. DOI:10.1109/TED.2016.2520583

[10] W-T Huang and Y. Li, "Electrical characteristic fluctuation of 16-nm-gate trapezoidal bulk FinFET devices with fixed top–fin width induced by random discrete dopants", *Nanoscale Research Letters*, vol. 10, p. 116 (8pp), 2015. DOI:10.1186/s11671-015-0739-0

[11] B. D. Gaynor, and K. S. Hassoun, "Fin shape impact on FinFET leakage with application to multithreshold and ultralow–leakage FinFET design", *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 1561–1567, Aug. 2014. DOI:10.1109/TED.2014.2331190

[12] K. P. Pradhan, S. K. Saha, P. K. Sahu and Priyanka, "Impact of fin height and fin angle variation on the performance matrix of Hybrid FinFETs", *IEEE Trans. Electron Devices*, vol. 64, no. 1, pp. 2738–2744, Jan. 2017. DOI:10.1109/TED.2016.2631301

[13] V. S. Basker, T. Standaert, H. Kawasaki, C.-C. Yeh, K. Maitra, T. Yamashita, J. Faltermeier, H. Adhikari, H. Jagannathan, J. Wang, H. Sunamura, S. Kanakasabapathy, S. Schmitz, J. Cummings, A. Inada, C. -H. Lin, P. Kulkarni, Y. Zhu, J. Kuss, T. Yamamoto, A. Kumar, J. Wahl, A. Yagishita, L. F. Edge, R. H. Kim, E. Mclellan, S. J. Holmes, R. C. Johnson, T. Levin, J. Demarest, M. Hane , M. Takayanagi, M. Colburn, V. K. Paruchuri, R. J. Miller, H. Bu, B. Doris, D. McHerron, E. Leobandung and J. ONeill, "A 0.063 μm^2 FinFET SRAM cell demonstration with conventional lithography using a novel integration scheme with aggressively scaled fin and gate pitch", *Symposium on VLSI Technology*, pp. 1–2, 2010. DOI:10.1109/VLSIT.2010.5556135

[14] G. Patton, "Evolution and expansion of SOI in VLSI technologies: Planar to 3D, *IEEE International SOI Conference*, pp. 1–40, 2012. DOI:10.1109/SOI.2012.6404357

[15] A. J. García-Loureiro, N. Seoane, M. Aldegunde, R. Valin, A. Asenov, A. Martinez and K. Kalna, "Implementation of the density gradient quantum corrections for 3D simulations of multigate nanoscaled transistors", *IEEE Trans. Comput-Aided Des. Integr. Circuits Syst.*, vol. 30, no. 6, pp. 841–851, 2011. DOI:10.1109/TCAD.2011.2107990

[16] P. A. Markowich, "The Stationary Semiconductor Device Equations", Springer-Verlag, ISBN: 978-3-211-99937-0, 1986. DOI:10.1137/1029145

[17] M. Aldegunde, A. J. García-Loureiro, and K. Kalna, "3D finite element Monte Carlo simulations of multigate nanoscale transistors", *IEEE Trans. Electron Devices*, vol. 60, no. 5, pp. 1561–1567, 2013. DOI:10.1109/TED.2013.2253465

[18] International Technology Roadmap for Semiconductors (ITRS), 2013 Edition, https://www.dropbox.com/sh/qz9gg6uu4kl04vj/AADD7ykFdJ2ZpCR1LAB2XEjIa?dl=0

[19] N. Seoane, A. J. García-Loureiro, K. Kalna and A. Asenov "Impact of intrinsic parameter fluctuations on the performance of HEMTs studied with a 3D parallel drift-diffusion simulator", *Solid-State Electronics*, vol. 51, no. 3, pp. 481–488, March 2007. DOI:10.1016/j.sse.2007.01.030

[20] G. Indalecio, M. Aldegunde, N. Seoane, K. Kalna and A. J. García-Loureiro, “Statistical study of the influence of LER and MGG in SOI MOSFET”, *Semicond. Sci. Technol.*, vol.29, pp. 045005 (7pp), 2014. DOI:10.1088/0268-1242/29/4/045005

[21] M. A. Elmessary, D. Nagy, M. Aldegunde, N. Seoane, G. Indalecio, J. Lindberg, W. Dettmer, D. Peric, A. J. García-Loureiro and K. Kalna “Scaling/LER study of Si GAA nanowire FET using 3D finite element Monte Carlo simulations”, *Solid-State Electronics*, vol. 128, pp. 17–24, Feb. 2017. DOI:10.1109/ULIS.2016.7440050

[22] ATLAS Users Manual, Silvaco Inc., pp. 13–1–24, 2012.

[23] Y. Li and C.-H. Hwang, “Effect of Fin Angle on Electrical Characteristics of Nanoscale Round-Top-Gate Bulk FinFETs”, *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3426–3429, Dec. 2007. DOI:10.1109/TED.2007.908908

[24] G. Indalecio, A. J. García-Loureiro, M. Aldegunde, and K. Kalna, “3D simulation study of work-function variability in a 25 nm metal-gate FinFET with curved geometry using Voronoi grains”, in *Proc. 17th Int. Conf. Simul. Semicond. Proc. Devices (SISPAD)*, pp. 149–152, 2012.

[25] G. Indalecio, A. J. Garcia–Loureiro, N. Seoane and K. Kalna, “Study of metal–gate work–function variation using Voronoi cells: comparison of Rayleigh and Gamma distributions”, *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2625–2628, 2016. DOI:10.1109/TED.2016.2556749

[26] N. Seoane, M. Aldegunde, A. J. García-Loureiro, R. Valin, and K. Kalna, “3D ‘atomistic’ simulations of dopant induced variability in nanoscale implant free $In_{0.75}Ga_{0.25}As$ MOSFETs”, *Solid-St. Electron.*, vol. 69, pp. 43–49, 2012. DOI:10.1016/j.sse.2011.11.031

[27] N. Seoane, G. Indalecio, M. Aldegunde, D. Nagy, M. A. Elmesssary, A. J. García-Loureiro and K. Kalna, “Comparison of fin–edge roughness and metal grain work function variability in InGaAs and Si FinFETs”, *IEEE Trans. Electron Devices*, vol. 63, no. 3, pp. 1209–1216, Mar. 2016. DOI:10.1109/TED.2016.2516921

[28] G. Indalecio, N. Seoane, K. Kalna and A. J. Garcia–Loureiro “Fluctuation sensitivity map: a novel technique to characterise and predict device behaviour under metal grain work–function variability effects”, *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1695–1701, 2017. DOI:10.1109/TED.2017.2670060