Study of Local Power Dissipation in Ultrascaled Silicon Nanowire FETs

Antonio Martinez, John R. Barker, Manuel Aldegunde, and Raul Valin

***Abstract*— The local electron power dissipation has been calculated in a field-effect nanowire transistor using a quantum transport formalism. Two different channel cross sections and optical and acoustic phonon mechanisms were considered. The phonon models used reproduce the phonon limited mobility in the cross sections studied. The power dissipation for different combinations of source, channel, and drain dimensions have been calculated. Due to the lack of complete electron energy relaxation inside the device, the Joule heat dissipation over-estimates the power dissipated in small nanotransistors. This over-estimation is larger for large cross sections due to the weaker phonon scattering. On the other hand, in narrow wires, the power dissipation inside the device can be large, therefore, mitigating against fabrication of very narrow nanowire transistors. We have also investigated the cooling of the device source region due to the mismatch of the Peltier coefficients between the source and the channel.**

***Index Terms*— Nanowire transistors, NEGF simulations, power dissipation, energy transport.**

I. Introduction

NANOWIRE field effect transistors are strong candidates for future CMOS technology due to superior electrostatic integrity [1], [2]. Power dissipation is one of the effects limiting aggressive transistor scaling. Previous studies on dissipation in nanostructures have been carried out using a Non-Equilibrium Green's Function Formalism (NEGF) for 1D devices such as resonant tunnelling devices [3] as well as with Monte Carlo simulations for various nanoscale devices [4]. However, the study of power dissipation in extremely scaled nanowire transistors has not been investigated using the NEGF formalism. As the cross section of the transistor becomes small, the effective electron-phonon coupling increases and as a consequence the power dissipation increases [5]. In this letter, we have used a NEGF formalism to study the relaxation of hot electrons for a gate-all-around Si nanowire transistor at high drain bias. Two different cross-sections have been considered. We compute the spatially resolved power dissipated by electrons inside devices with different combinations of source, channel and drain lengths.

Manuscript received October 7, 2014; accepted November 1, 2014. Date of publication November 6, 2014; date of current version December 22, 2014. This work was supported by EPSRC under a Career Acceleration Fellowship Grant EP/I004084/2: Quantum simulations of future solid state transistors of A. Martinez. The review of this letter was arranged by Editor E. A. Gutiérrez-D.

A. Martinez, M. Aldegunde, and R. Valin are with the College of Engineering, Swansea University, Swansea SA2 8PP, U.K. (e-mail: a.e.martinez@swansea.ac.uk).

J. R. Barker is with the School of Engineering, University of Glasgow, Glasgow G12 8LT, U.K.

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2014.2368357

II. Physical Models

The NEGF equations are solved in the effective mass approximation [6] using masses extracted from Tight Binding calculations [7]. A mode space representation for the cross section is used [6]. The electron-phonon interaction was included via the self-consistent Born approximation with the parameters and self-energy models described in [6]. Throughout this letter the phonon system is in equilibrium, therefore phonon transport is not considered. Previous work [6] shows that our electron-phonon and electron Hamiltonian models produce similar phonon limited mobility and drain current reduction when compared to full band and semi-classical models. The local power transfer by the electron to the lattice is given by [3] and [8]:

$$P(r) = -\nabla \cdot J_K(r) + E(r) \cdot J(r) \tag{1}$$

The last term in the RHS of Eqn. (1) is the local Joule power. The first term in the RHS is the change in the "kinetic energy" current of the electron ensemble. If the kinetic energy current is constant then the electron system follows the bending of the potential and therefore does not increase the electron mean energy relative to the conduction band minima, i.e., there are no hot electron phenomena. A large change in kinetic current implies the heating or cooling of the electron system. Eqn. (1) is used in this letter to estimate the local power dissipated by the electrons inside the transistor. When calculating the power dissipation, solving the NEGF equations to a higher degree of accuracy is required than when just calculating the drain current, as many more Born iterations are required to change the energy of electrons travelling from drain to source by 400meV (typical optical phonon energies in Si are between 16–60 meV). The source/drain transistor contacts are assumed to be Ohmic, or in the NEGF context, perfectly absorbing boundaries. The electron distribution in the source/drain is the (equilibrium) Fermi-Dirac distribution. When the source and drain extension regions included in the simulation domain are shorter than the energy relaxation mean free path and also shorter than the real fabricated extension regions, the electrons in the simulation are artificially forced to be in equilibrium in these open boundaries. As a consequence, if the length of the source is too short, low energy electrons coming from the source contact will not have sufficient space to absorb energy from the phonons and therefore no cooling of the source will

TABLE I
POWER DISSIPATION AND DRAIN CURRENT REDUCTION IN DIFFERENT LENGTH AND CROSS SECTION NANOWIRE TRANSISTORS

S/ Ch / D (nm)	Cross-section (nm^2)	$100\frac{Total\ power}{Joule\ power}$	Current reduction (%)
10/6/24	2.2x2.2	54	50
10/6/24	3.6x3.6	18	34
24/6/10	2.2x2.2	26	57
24/6/10	3.6x3.6	11	33
10/6/64	2.2x2.2	92	54
10/6/64	3.6x3.6	56	40
10/40/30	2.2x2.2	73	82
10/40/30	3.6x3.6	36	63

be observed. Similarly, the heating of the drain will not occur in a short simulated drain region.

III. RESULTS

Gate-all-around n-type Si nanowire transistors with undoped channel and donor concentration of 10^{20} cm^{-3} in the source and drain have been investigated. Two different cross-sections (2.2×2.2 nm^2) and (3.6×3.6 nm^2) have been considered. The power dissipated has been calculated for four different combinations of source/channel/drain lengths: (i) 10/6/24, (ii) 24/6/10, (iii) 10/6/64 and (iv) 10/40/30 nm. This allowed us to study the role of the source, drain and channel regions in the energy dissipation of the entire device. The drain bias used is 0.4 V. For all the devices, the corresponding percentage of Joule power dissipated inside the device and the current reduction are presented in table I for $V_G = 0.9$ V. The current reduction due to phonon scattering is given by: $|(1 - I_{scatt}/I_{bal}) \times 100$ where $I_{scatt}(I_{bal})$ is the current with(without) including phonon scattering processes. The current reduction is mostly dependent on the channel length. For the small cross section nanowire the reduction is 50% (80%) for 6nm (40 nm) channel length. This reduction is not proportional to the length of the channel. For the large cross section, the current reduction is still strongly dependent on the channel length but there is some dependence on the drain length as can be seen by comparing the 10/6/24 with the 10/6/64. This dependence is attributed to the poorer electrostatic control in the large cross section device. It will be shown that for the 6nm channel length device the channel is so short that much of the potential drop is concentrated in the channel/drain region where a substantial part of the power dissipation occurs but it is not as localized as predicted by the Joule power alone (see lower left panel of Fig. 1). The power dissipation is mostly related with the length of the drain. However, comparing the power dissipated in devices with dimension 10/6/24 with those with 10/40/30 shows that a substantial part of the power is dissipated in the channel as those devices have approximately the same drain length. By comparing the power dissipated in the 10/6/64 devices with that in the 10/40/30 devices shows that the drain is just 20% more efficient in dissipating power than the channel. The effect

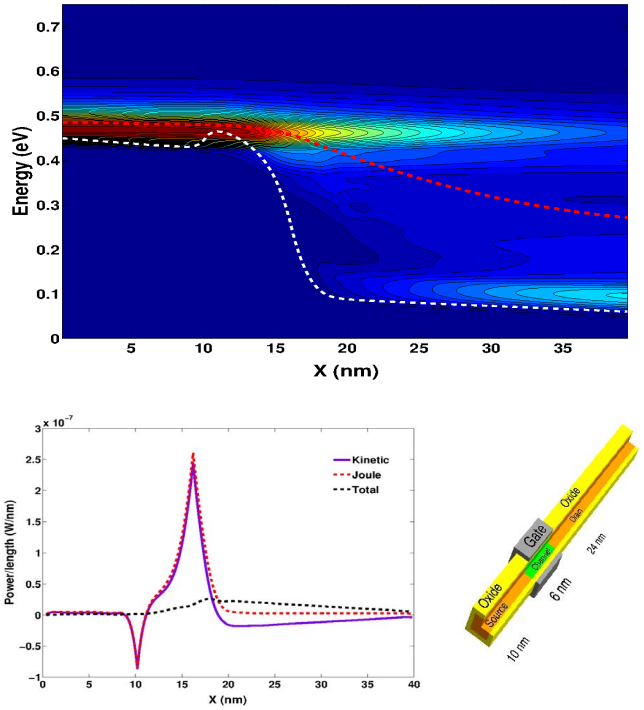

Fig. 1. Upper panel: Current spectra for the 10/6/24 silicon nanowire transistor with 2.2×2.2 nm^2 cross-section at $V_G = 0.9$ V. The first sub-band (white dotted line) and the average current energy (red dotted line) are also presented. Lower left panel: Spatial distribution of the power per unit length for the same device. The power is normalized to unit length along the wire (axial) direction. The Joule power (red dashed) and the divergence of the kinetic energy (blue) are also shown. Lower right panel: gate-all-around architecture of the 10/6/24 device.

of scattering is more severe in the smallest cross section devices as reflected in a higher percentage of Joule power dissipated inside these devices. The current spectra along the axis of the 2.2×2.2 nm^2 cross-section nanowire, at $V_G = 0.9$ V, is shown in Fig. 1. The average current energy [3] and the first sub-band are also shown. The average current energy decreases with the distance within the drain due to the energy relaxation of the hot electrons as they move through the drain. However, even after travelling 24 nm into the drain, the electrons injected from the source have not reached equilibrium. At the drain end, the current mean energy has only dropped by half (200meV) of the total energy drop. The right lower panel shows the device architecture and dimensions of the long drain device. The lower left panel of Fig. 1 shows the density of the total power, the Joule power and the divergence of the kinetic energy current along the nanowire transistor at $V_G = 0.9$ V. The Joule power essentially follows the derivative of the conduction band energy and its maximum is at x = 16.2 nm with a value of 2.61×10^{-7} W/nm. However, the maximum of the total power dissipated is a little bit farther (x = 18 nm) and its value is 2.58×10^{-8} W/nm, ten times smaller than the Joule value. We stress that the local power dissipation not only depends on the electron-phonon coupling strength but also crucially on the local density of states. The latter is strongly dependent on dimension, geometry and bias for sub 10 nm dimensions. The real space NEGF formalism captures this dependency unlike other methodologies such as Monte Carlo and Drift-Diffusion.

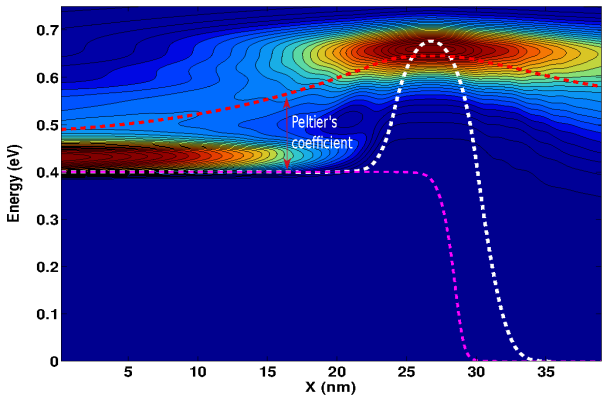

Fig. 2. Current spectra for the 24/6/10 transistor with 2.2×2.2 nm^2 cross-section at $V_G = 0.5$ V. The first sub-band (white dotted line) and the average current energy (red dotted line) are also presented. The quasi-Fermi level is shown in magenta. Note that the difference between the average current energy and the Fermi level is equal to Peltier's coefficient.

The integrated total and Joule power through the whole device are 4.25×10^{-7} W and 7.78×10^{-7} W. For the same device length (10/6/24 nm) but with a larger cross-section, the power dissipation is smaller as expected [5]. The corresponding maximum values of the total and Joule power density are 3.02×10^{-8} W/nm and 1.34×10^{-6} W/nm: two orders of magnitude different. The corresponding integrated total and Joule power through the whole device are 6.91×10^{-7} W and 3.80×10^{-6} W respectively. It is important to highlight that even for a relatively long drain region, 64 nm, hot electrons in the 3.6×3.6 nm^2 device leave the drain without relaxation (i.e. the total power dissipation is 56% of the Joule power).

For the small cross section device in which longitudinal dimensions are (source/channel/drain) 10/40/30 nm, the corresponding local power dissipated is 73% of the Joule power at $V_G = 0.9$V. This device has the same total length (80 nm) as the long drain device analysed but the channel is longer (40 nm vs. 6 nm). Since the dissipation in the channel region is lower compared to the drain region, the power dissipated is 19% less than the power dissipated in the long drain device, indicating the higher efficiency of the drain dissipating power.

All these results indicate that using the Joule law for nanoscale transistors is inaccurate.

Finally, we have studied longer source devices with 24/6/10 nm long source/channel/drain regions and 2.2×2.2 nm^2 and 3.6×3.6 nm^2 cross-sections. Fig.2 shows the current spectra ($V_G = 0.5$ V) for the small cross-section device. In this case the gate barrier energy is around 250 meV; source electrons surmounting the barrier through phonon absorption cool the source of the transistor. The average current energy in the drain is larger than in the source, indicating a net cooling of the lattice. The Peltier coefficient, given by the difference between the average current energy and the quasi-Fermi level, is also shown in the figure. Since it is larger in the channel than in the source, a heating of the electron system and cooling of the lattice occurs in the source/channel interface [3], [4]. The integrated power inside the simulated region is negative, as the power dissipated in the drain is unable to compensate the cooling of the source. The Joule power and integrated power are 9.94×10^{-11} W and -2.17×10^{-11} W, but the total power integrated, including the device and its surrounding equilibrium regions, is positive and equals the Joule power as expected. This negative local power occurs at very low gate bias. At high gate bias, the source cooling is very small as compared to the power dissipated in the drain, even for short drain extensions. At $V_G = 0.9$ V, the Joule and total powers are 6.76×10^{-7} W and 1.79×10^{-7} W, which results in only 26% of the Joule power dissipated inside the device.

IV. Conclusions

The NEGF formalism coupled to 3D electrostatics has been used to calculate the local power dissipated inside silicon gate-all-around nanowires. Devices with two different cross-sections have been considered. Scattering is more severe in the smallest cross section devices, which leads to stronger power dissipation inside the device for the 2.2×2.2 nm^2 nanowires. At high gate bias, the power dissipated inside the transistor is approximately 50% (30%) of the Joule power for the device with 2.2×2.2 (3.6×3.6) nm^2 cross-section and source/channel/drain of 10/6/24 nm. For the smallest cross-section device with 64 nm drain almost all the power is dissipated inside the transistor. Thus very narrow nanowire transistors are not recommended: since the oxide coating has low thermal conductivity the only way to remove the thermal energy is via the silicon core. Furthermore, the thermal conductivity in the silicon core decreases as the cross section decreases making the situation worse. The power dissipated is approximately 50% of the Joule power for a wider device with the same drain length but 3.6×3.6 nm^2 cross-section. Finally, the cooling of the transistor has been demonstrated for small drain extension (10 nm) when the barrier is substantial ($\sim$250 mV). This effect occurs due to the strong difference in Peltier coefficients between the source and gate of the transistor.

References

[1] H. Yan *et al.*, "Programmable nanowire circuits for nanoprocessors," *Nature*, vol. 470, no. 7333, pp. 240–244, 2011.
[2] S. D. Suk *et al.*, "Investigation of nanowire size dependency on TSNWFET," in *Proc. IEEE IEDM*, Dec. 2007, pp. 891–894.
[3] R. Lake and S. Datta, "Energy balance and heat exchange in mesoscopic systems," *Phys. Rev. B*, vol. 46, no. 8, pp. 4757–4763, 1992.
[4] E. Pop, "Energy dissipation and transport in nanoscale devices," *Nano Res.*, vol. 3, no. 3, pp. 147–169, 2010.
[5] R. Kotlyar *et al.*, "Assessment of room-temperature phonon-limited mobility in gated silicon nanowires," *Appl. Phys. Lett.*, vol. 84, no. 25, p. 5270, 2004.
[6] M. Aldegunde, A. Martinez, and A. Asenov, "Non-equilibrium Green's function analysis of cross section and channel length dependence of phonon scattering and its impact on the performance of Si nanowire field effect transistors," *J. Appl. Phys.*, vol. 110, no. 9, p. 094518, 2011.
[7] K. Nehari *et al.*, "Influence of band structure on electron ballistic transport in silicon nanowire MOSFET's: An atomistic study," *Solid-State Electron.*, vol. 50, no. 4, pp. 716–721, 2006.
[8] A. C. Smith, J. F. Janak, and R. B. Adler, *Electronic Conduction in Solids*. New York, NY, USA: McGraw-Hill, 1967.